Dynamic Electrothermal Macromodeling Techniques for Thermal-Aware Design of Circuits and Systems

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***Abstract*—The applicability of classical macromodeling techniques to dynamic electrothermal analysis is reviewed, with emphasis on specific aspects of the Fourier heat conduction problem. Modeling based on the characterization of thermal multiports is considered, and the identification of corresponding thermal impedances in frequency and time domain is discussed, along with the synthesis of electrical equivalents well suited for standard circuit simulators like SPICE. The presented approach is illustrated through relevant case-studies, namely, two basic analog electronics circuits in state-of-the-art bipolar technologies.**

Keywords—compact thermal modeling; electrical macromodeling; silicon germanium (SiGe); silicon on glass (SOG); thermal feedback; thermal impedance

I. INTRODUCTION

The thermally-induced reduction in performance and reliability in state-of-the-art electronic devices, circuits, and systems is a critical issue [1], [2] to be faced at early design stage by self-consistently solving the electrical and thermal problems. A technique allowing effective electrothermal (ET) analyses in the environments of standard circuit simulators involves the adoption of (electrical) equivalent dynamic thermal compact models (DTCM) to describe the heat propagation, where the temperature rises correspond to voltages and the dissipated powers to currents. Electrical equivalents can be determined at various granularity levels (e.g., device portion, whole device, chip, package, PCB) through different approaches, namely, (i) from the discretization of the Fourier heat equation, e.g., with finite differences or finite elements methods [3], or (ii) by matching the step response of the equivalent circuit to the measured or simulated temperature step response in some regions of interest, which can be achieved through identification procedures based on residues/poles or time constants. Despite the large body of available research, still quite demanding challenges are unsolved, and an effort in classification and standardization of the proposed approaches – ranging from the use of simple pre-defined topologies to general model order reduction techniques [4] – is useful.

In this paper, we focus on DTCM identification through standard electrical macromodeling techniques [5], [6] by exploiting the intrinsic properties of the heat conduction problem. In particular, we show that the identification can be effectively tackled in frequency domain (FD) with the formulation introduced in [7], [8] and applied to dynamic ET simulation [9]-[11], and that similar considerations can be made for the time domain (TD) [12]. As a demonstration and validation of the above approaches, ET effects are investigated in two basic analog electronics circuits in state-of-the-art high-frequency bipolar technologies, i.e., a silicon germanium (SiGe) common-emitter (CE) amplifier and a silicon-on-glass (SOG) differential pair (Fig. 1).

II. THERMAL EQUIVALENT NETWORKS

The thermal conduction problem in a bounded region is ruled by the heat equation, which relates the generated power density g [W/m^3] and the temperature T [K]

$$\rho(\mathbf{r})c(\mathbf{r})\frac{\partial T(\mathbf{r},t)}{\partial t} = \nabla\cdot\left(k(\mathbf{r})\cdot\nabla T(\mathbf{r},t)\right) + g(\mathbf{r},t) \quad (1)$$

where ρ is the mass density [kg/m^3], c is the specific heat [J/(kgK)] and k is the thermal conductivity [W/mK] of the medium. Using separation of variables, the temperature field in (1) subject to uniform initial condition, and to Dirichlet, Neumann or mixed boundary conditions, can be found as a solution of an eigenvalue problem [13].

The heat dissipation in an electronic system takes place only in some regions (heat sources), and the temperature field is to be modeled only in assigned positions (each corresponding to a heat source) that are relevant from an electrical viewpoint.

For the sake of simplicity, let us first consider the case of a single heat source so as to provide some basic theory. The transient thermal behavior of a power-dissipating device/chip is fully described by the (*self-heating*) *thermal impedance*, defined as the normalized temperature step response [14]

$$Z_{TH}(t) = \frac{T(t) - T_{AMB}}{P_D} = \frac{\Delta T(t)}{P_D} \quad (2)$$

where T and T_{AMB} are the device/chip and ambient temperatures, respectively, and P_D is the amplitude of the applied power step. If the thermal impedance is known, the temperature rise above ambient due to the application of an arbitrary power profile $P_D(t)$ can be expressed as the following convolution:

$$T(t) - T_{AMB} = \left[\frac{d}{dt}Z_{TH}(t)\right] * P_D(t) = Z_{TH,impulse}(t) * P_D(t) \quad (3)$$

where $Z_{TH,impulse}$ is the normalized temperature impulse response, given by [15]

$$Z_{TH,impulse}(t) = \sum_{k=1}^{\infty}\Gamma_k e^{-\lambda_k t} \quad (4)$$

being λ_k real positive eigenvalues constituting a monotonically increasing sequence, and Γ_k positive shape factors for the

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considered physical domain. It is worth noting that, due to properties of (4), the thermal impedance is monotonic. Taking the Laplace transform of (3), we get

$$\Delta T(s) = Z_{TH,impulse}(s) P_D(s) \quad (5)$$

where

$$Z_{TH,impulse}(s) = \sum_{k=1}^{\infty} \frac{\Gamma_k}{s+\lambda_k} \quad (6)$$

$Z_{TH,impulse}(s)$ being passive and positive real [15]. It is apparent that (6) can be interpreted as a single-port electrical equivalent of the thermal impedance, since it is the electrical impedance of a canonical Foster representation (form I) of a generalized (distributed) passive lumped RC network, with proper positive values for the parallel pairs of resistors R and capacitors C, i.e.,

$$Z_{TH,impulse}(s) = \sum_{k=1}^{\infty} \frac{R_k}{1+sR_kC_k} \quad (7)$$

$$R_k = \Gamma_k / \lambda_k \qquad C_k = 1/\Gamma_k \quad (8)$$

Any DTCM approach allows truncating series (7), thus leading to a lumped approximation of $Z_{TH,impulse}$.

The single-port network can only be used to describe self-heating, i.e., the heating on a device/chip due to the power dissipated by the device/chip itself. If the electronic system under analysis includes M power-dissipating regions (M heat sources), the thermal interactions are taken into account through the *mutual* (*coupling*) *thermal impedance* $Z_{THij}(t)$, which – in analogy to (2) – is defined as

$$Z_{THij}(t) = \frac{\Delta T_i(t)}{P_{Dj}} = \frac{\Delta T_j(t)}{P_{Di}} \quad (9)$$

that is, it represents the temperature rise over ambient of a heat source due to the activation of the other, normalized to the power dissipated by the latter. Self and mutual thermal impedances are the elements of the M×M *thermal impedance matrix*, which is symmetric due to the reciprocity. In this case, the electrical equivalent is given by a multiport (distributed) network relating the temperature $T_i(t)$ and power $P_{Dj}(t)$ defined at the *i*-th and *j*-th ports, respectively. The structure and properties described for the single-port can be easily generalized to the M-port by introducing the concept of RC multiport networks [16].

III. Techniques for DTCM Identification

Standard electrical macromodeling techniques can be adapted for the identification of thermal impedances in FD and TD, so as to (i) take advantage of well-established methods and (ii) preserve all the fundamental properties of the thermal impedance (e.g., passivity, reciprocity, monotonic step response) in the identified model.

For a system with M heat sources, the thermal impedance data in the FD can be represented as an M-port network in terms of a Foster matrix expansion

$$Z_{TH,impulse}(s) = \sum_{n=1}^{N_p} \frac{R_n}{s-p_n} \quad (10)$$

where N_p is the identified number of real poles (in our experience in the order of 10) and the corresponding M×M residue matrices R_n are positive semi-definite. The identification can be obtained through Vector Fitting (VF) [5] followed by a passivity enforcement step. A convex optimization approach [7] providing optimal residue matrices at fixed poles has been found to be well suited for thermal identifications, as reported in [9]-[11].

If thermal impedances are available in the form of time samples (logarithmically-spaced due to the large range of time constants), the TD identification is in principle to be preferred. This can be performed for single-port elements with many techniques, such as the peeling method [17], and for multiports with the Time Domain Vector Fitting (TDVF) [6], with careful evaluation of the convolution integrals accounting for the logarithmic spacing of the input data, as demonstrated in [12].

Regardless of the identification procedure, the synthesis of the equivalent Foster multiport is achieved as outlined in [8].

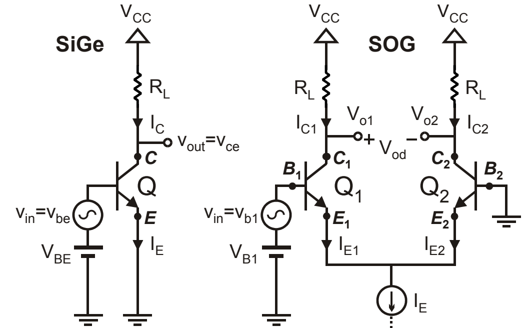

Fig. 1. Sketches of the SiGe CE amplifier (left) and of the SOG differential pair (right) analyzed in this work.

IV. Case-Studies

A. SiGe CE amplifier

The SiGe heterojunction bipolar transistor (HBT) employed in the CE amplifier was fabricated by Infineon Technologies within the framework of the European Project DOTFIVE [18]; the key features are: maximum cut-off and oscillation frequencies f_T/f_{max}=190/250 GHz, and open-emitter breakdown voltage BV_{CBO}=6.8 V. The emitter area is given by $W_E \times L_E$=0.2×2.67 μm^2, W_E and L_E being the effective emitter width and length, respectively. The intrinsic transistor region is surrounded by shallow and deep trenches filled with electrically – and thermally – insulating materials in order to boost the RF performance [19].

The thermal resistance R_{TH} (i.e., the steady-state Z_{TH} value) of the device was determined by a twofold approach, namely,

- *Numerically*, through a merely thermal 3-D simulation performed with a commercial software package relying on the finite-element method (FEM). Great care was taken in representing all the details (including the slot contacts and the metallization pattern) of the geometrically complex structure, as well as in selectively re-meshing the regions where high temperature gradients are expected. The thermal conductivities of the materials were initially set to accepted literature values.
- *Experimentally*, by invoking an improved common-base variant [20], [21] of a classical approach based on simple DC measurements [22].

Unfortunately, a great discrepancy (~42%) arose between the numerical (3250 K/W) and experimental (5600 K/W) R_{TH} values, consistently with the results recently obtained for STMicroelectronics transistors [20]. An effort is currently

being made to understand the physical reason leading to the numerical underestimation. The only procedure to retrieve the experimental value by a 3-D simulation involves the reduction of the thermal conductivities k of the materials that mainly affect the base-emitter junction temperature. In particular, k was adjusted to 68 W/mK (instead of 140-150 W/mK) for the silicon region enclosed by the shallow trench. After this pre-processing calibration step, the transient thermal impedance Z_{TH} was simulated, and the corresponding Foster network was identified by resorting to the theoretical approach described in [17]. The comparison between FEM data and results obtained with the identified circuit is shown in Fig. 2. Also reported are: (i) the Z_{TH} calculated via the traditional semi-analytical method presented in [23], in which the thermal problem is represented by considering a rectangular heat source embedded in a homogeneous silicon domain with k=140 W/mK superiorly limited by an adiabatic surface, and (ii) the data determined with the corresponding identified network. The figure reveals that the FEM Z_{TH} is much higher than that evaluated through the simplified model in [23], although the *cooling* emitter contact (accounted for in the first) was replaced by a zero heat flux condition (in the latter). This is to be attributed to the prevailing twofold *heating* action of (i) the reduced thermal conductivity of the silicon, and (ii) the shallow/deep trenches, which inhibit the heat spreading.

The CE amplifier was then simulated with the popular PSPICE program [24] by resorting to the following strategy:

- The SiGe HBT was represented by a subcircuit that (i) includes a conventional bipolar transistor as main element, and linear and nonlinear controlled sources to account for the variation of the temperature-sensitive parameters during the simulation run, (ii) is provided with an input temperature node and an output power node in addition to the standard electrodes. All the parameters of the model described by the subcircuit were calibrated through an extensive experimental campaign.
- The identified Foster network was connected to the temperature and power nodes of the above subcircuit.
- V_{CC}, V_{BE} (=V_B) and R_L were chosen equal to 2 V, 0.9 V, and 50 Ω, respectively.
- A small AC signal v_{be} (=v_b) with a 2 mV semi-amplitude and assigned frequency was applied.

The AC gain and the semi-amplitude of the temperature oscillation as a function of frequency are shown in Fig. 3 by accounting for the Foster networks corresponding to the FEM and the simplified Z_{TH}; also illustrated is the AC gain obtained by deactivating the ET feedback (T=300 K). The results can be summarized as follows:

- The DC biasing points are characterized by (I_C=4.15 mA, ΔT_j=42 K) and (I_C=2.61 mA, ΔT_j=5.8 K) for the FEM and simplified networks, respectively, ΔT_j being the temperature rise over ambient of the base-emitter junction, while I_C=2.38 mA for the isothermal (at T=300 K) case.
- The ET AC gains are higher than the T=300 K one (~2.4) over the whole frequency range; this is ascribable to (i) the larger excursion of the output characteristics under ET conditions, and (ii) the higher biasing current.
- The contribution (i) dominates at lower frequencies, where the temperature can follow the (slow) oscillation of the electrical signals, but lowers beyond 100 kHz, thus leading to a decrease in AC gain. The temperature fluctuations eventually extinguish for frequencies higher than 5 GHz, and the gain reduces to that corresponding to *isothermal* conditions at T=342 K (FEM) or T=305.8 K (simplified model), which in both cases is still higher than the T=300 K counterpart due to contribution (ii).

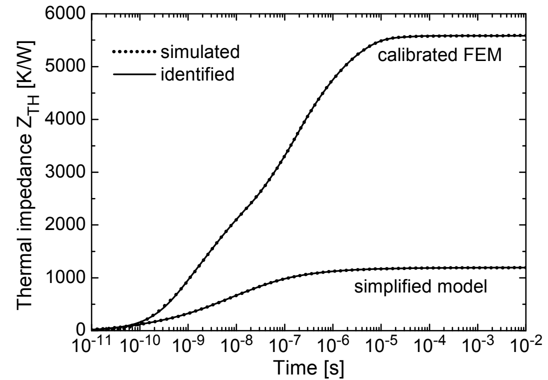

Fig. 2. Comparison between simulated (dotted lines) and identified (solid) thermal impedances corresponding to the 3-D FEM simulation and the simplified model proposed in [23].

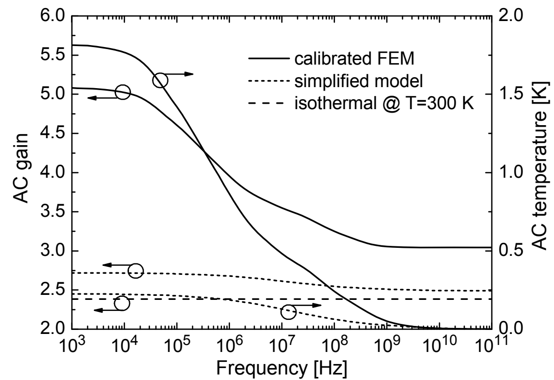

Fig. 3. AC gain (left) and temperature (right) of the CE SiGe amplifier by considering the thermal feedback networks corresponding to the 3-D FEM simulation (solid lines) and the simplified model proposed in [23] (short-dashed); also shown is the AC gain corresponding to T=300 K (dashed line).

B. SOG differential pair

In SOG technology, the RF performance is improved by replacing the conventional silicon substrate with a high-resistivity glass one, and embedding the active transistor region in a (small) silicon island entirely surrounded by electrically – and thermally – insulating materials [25]. Thermal issues arising in SOG bipolar differential pairs have been analyzed from the experimental and theoretical viewpoints in [26]; it was found that severe self-heating of individual devices might yield a radical distortion in the steady-state circuit behavior. In particular, it was shown that the standard linear operating region of the voltage-transfer characteristic (VTC) where the pair behaves as an amplifier can be replaced by a positive differential resistance branch (under current-driven mode) or a hysteresis phenomenon (under voltage-driven mode). This turns into the occurrence of two additional (stable) operating points for V_{IN}=0 V, in which one transistor hogs the whole DC current I_E and the other becomes dry ($I_{C1}\approx I_E$, $I_{C2}\approx 0$), ($I_{C1}\approx 0$, $I_{C2}\approx I_E$), while the expected symmetric behavior ($I_{C1}=I_{C2}\approx I_E/2$)

becomes unstable. Here the analysis is extended to the dynamic case by considering two trench-isolated transistors with $W_E \times L_E = 1 \times 20$ μm^2, BV_{CBO}=16.7 V, and edge-to-edge spacing amounting to 62.5 μm. The self-heating and mutual thermal resistances were determined to be R_{TH}=19000 K/W and R_M=1200 K/W, respectively [26]. The resistances R_L were chosen equal to 250 Ω.

The following procedure was adopted:

- Similarly to the SiGe case, each individual device was described by a PSPICE subcircuit [10].
- The transient evolutions of the self-heating (Z_{TH}) and mutual (Z_M) thermal impedances were determined by carrying out calibrated 3-D thermal-only FEM simulations of the whole pair structure.
- The 2×2 matrix of thermal impedances was identified in the FD and the corresponding equivalent network was synthesized according to the approach discussed in Section III [10]. The network was then automatically included in a thermal feedback block (TFB) compatible with PSPICE thanks to an *in-house* tool.
- Subsequently, a dynamic ET representation of the pair was generated in PSPICE by connecting the TFB to the subcircuits associated to Q_1 and Q_2.
- All simulations were performed by considering I_E=1.6 mA and V_{CC}=4 V as DC bias.

A first AC analysis was carried out for V_{IN}=0 V by applying the DC bias at t=0 and an AC signal v_{in} with amplitude equal to 5 mV and frequency f=10 kHz at t=10 ms. Isothermal (at T=300 K) simulations conducted by deactivating the thermal feedback revealed that

- In the DC bias point the current I_E is identically partitioned between transistors Q_1 and Q_2.
- The circuit provides a differential-mode gain v_{od}/v_{in} of about -6.73.

ET effects were subsequently restored by connecting the pair to the TFB; in this case, the pair is driven to one of the stable hogging conditions when the AC signal is applied, and the circuit does not behave as an amplifier any longer due to the VTC flattening.

Another AC analysis was conducted by applying both the DC bias and AC signal at t=0, and varying the v_{in} frequency. The evolution of the collector currents is depicted in Fig. 4. It is shown that the differential pair moves to the asymmetric mode in shorter times than in the case without AC signal applied. In particular, the Q_1 side is destined to bear all the DC current since the first half-wave of v_{in} is positive. It can be also observed that the time instant at which the current hogging condition is reached is almost independent of the v_{in} frequency.

V. CONCLUSIONS

The applicability of the DTCM approach to the dynamic ET simulation of electronic systems has been discussed from the perspective of standard electrical macromodeling strategies. Techniques like VF, TDVF, and convex passive identification of equivalent impedances have been reviewed in view of the specific properties of thermal multiports. The approach is exploited for the ET analysis of basic analog electronics circuits in state-of-the-art high-frequency bipolar technologies.

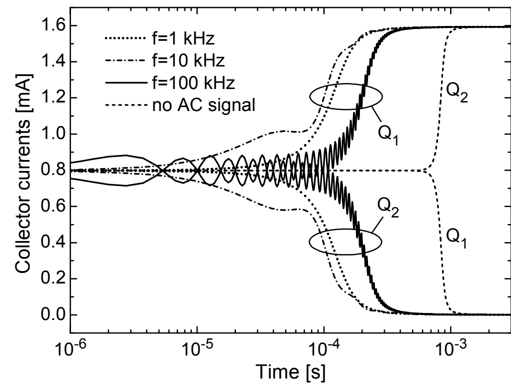

Fig. 4. Collector currents against time for various frequencies of the AC signal v_{in}, namely, 1 (dotted lines), 10 (dot-dashed), and 100 (solid) kHz. V_{CC}, I_E, and v_{in} were all applied at t=0. Also shown are the currents in the absence of AC signal (dashed lines).

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