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2013 J. Phys.: Conf. Ser. 439 012008

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Growth of vertically aligned multiwall carbon nanotubes columns

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Abstract. Capability of patterning carbon nanotubes (CNTs) growth is of tantamount importance for a number of applications ranging from thermal to electronic. This article reports on the columnar growth of vertically aligned multiwall carbon nanotubes (VA-MWCNTs) on patterned Silicon (Si) surface. We have developed procedures based on negative as well as positive masking approaches which allows the growth of predetermined MWCNTs patterns. We describe in detail the process steps leading to Si surface patterning. As quoted above, patterns are exploited to grow VA-MWCNTs. We have focused in particular on the growth of CNT pillars by chemical vapor despoition (CVD) technique at 850°C with camphor and ferrocene as carbon precursors and catalyst respectively. Field emission scanning electron microscopy (FESEM) is employed at low magnification to verify the correct patterning, and at high magnification to examine the surface morphology of CNTs pillars. The pillars are up to 2 mm high, their height being tailored through the deposition time. The diameter of each MWCNT is in the range 30-70 nm and the length is up to few hundred micrometers. The small CNT pillars produced, have several electrical and thermal applications. For instance they can be very useful for heat transfer systems as the lower thermal conductivity of fluids can be improved by the inclusion of nanotubes thanks to their peculiar 1-dimensional heat transfer characteristics.

1. Introduction

Nowadays Carbon based nanomaterials are among the most interesting materials. Following Ijima report [1], these materials have stimulated quite a lot of activity in different areas of science and engineering because of their extraordinary physical and chemical properties. Due to their high thermal and electrical conductivity, rigidity, strength, ... [2], CNTs are ideal for a wide variety of applications. CNTs can be produced by various processes [3] including arc discharge, laser ablation and chemical vapor deposition (CVD). The most promising of these techniques for large scale production is CVD as it opens opportunities of controlled massive [4] as well as precise growth on patterned substrates [5]. The vertically aligned carbon nanotubes (VACNTs) uniformly grown by CVD on a patterned surface feature interesting unique mechanical, electrical and thermal properties which led to propose a variety



of potential application such as heat dissipation systems [5], biosensors [6], field emission sources [7], conductive electrodes and micro mechanical devices [8].

An efficient and economical method of patterning by soft lithography, which enables to produce highly dense VA-MWCNTs columns, is described in the present work. Exploiting such patterning we have grown a number of CNTs structures using precursors that allow fast growth and good CNT quality.

2. Surface patterning of silicon substrate

We have developed a procedure to pattern silicon wafer by soft photolithography technique in both positive and image reversal mode that ensure the growth of well defined structures of CNTs. The protocol we have used for the patterning of silicon surfaces involves the following steps;

2.1. Realization of the mask

The first important step for this patterning is to design the mask on a Mylar sheet. There are two types of photomasks: positive and negative photomasks (figure 1). Black colored parts represent the areas which stop the UV radiation while these radiation can transmit through the white parts of the mask.

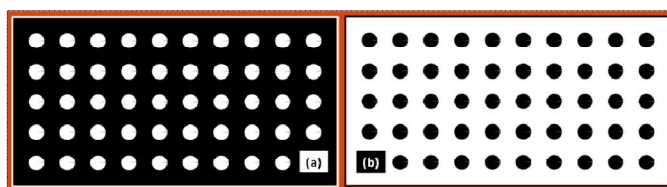


Figure 1. Soft Mylar photomasks a). Positive mask b). Negative mask

2.2. Mask transfer to the substrate

After the realization of photomasks, the substrates are prepared for the application of photoresist. The steps required to transfer the mask to the substrate are;

2.2.1. Wafer Cleaning. Silicon (100) substrates were cleaned with an acetone ultrasonic bath for 10 minutes followed by soaking in 2-Propanol for a few minutes to get rid of contaminations, debris and particulates. Furthermore, the wafers were washed in Piranha solution 3:1 ($H_2SO_4:H_2O_2$) for 5 minutes to enhance the hydrophilic behavior [9] as well as to remove organic residues from the surface. At the end of this procedure wafers were extensively rinsed in de-ionized water, dried under nitrogen flux and subsequently heated at $120^\circ C$ for a few seconds to obtain moisture free cleaned Si substrates (figure 2-a).

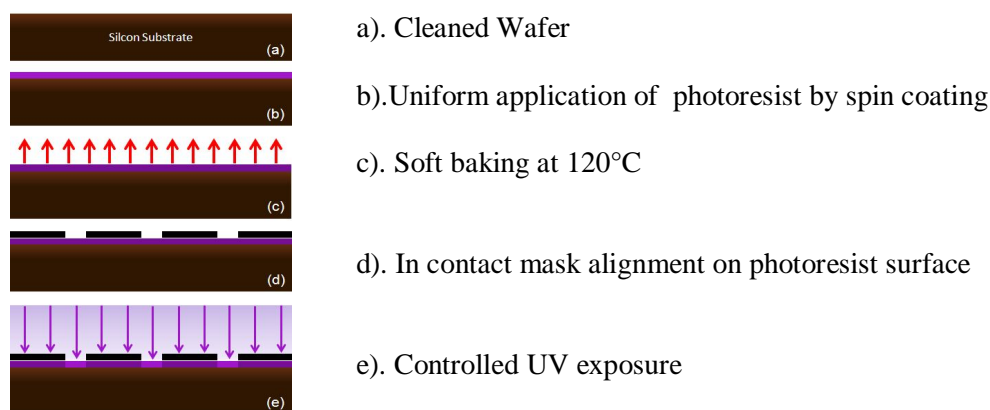


Figure 2. Steps involved in the transferring of mask to the substrate

2.2.2. Photoresist Application. Commercially available photoresist AZ5214E from MicroChemicals has a capability to work for both positive and negative masks. The cleaned wafers were held on spinner's stage by creating a vacuum between substrate and sample holder. After dispensing enough quantity of photoresist on silicon wafer, a uniform layer of photoresist (figure 2-b) was obtained using a spinner programmed at 600 rpm for 5 seconds and at 4000 rpm for the subsequent 40 seconds.

2.2.3. Soft Bake. After the uniform application of the photoresist layer, the silicon substrate was soft baked at 120°C for 2 minutes (figure 2-c). The temperature and duration of soft baking are critical parameters in photo-imaging as it transfers the photoresist coatings to imageable layer. Soft baking for a too long time or at high temperatures can degrade the sensitivity of photoresist by destroying the sensitizer or reducing its solubility in the developer. It may also produce cracks in the photoresist film which ultimately leads to poor resolution. Shorter than needed baking may tend to affect the adhesion and exposure to the photoresist layer as both exposed and unexposed areas would be attacked by the developer. It could make the photoresist layer non uniform and patchy, resulting in the poor precision of photolithographic process [10].

2.2.4. UV Exposure. Before the UV exposure, the mask was aligned with the wafer, so that the pattern could be transferred onto the wafer surface precisely. It is important to remove any kind of particles, trapped between the resist and the mask, which may damage the mask and lead to defects in the pattern. The photoresist-coated silicon wafer was brought into physical contact with the photomask and held in vacuum to avoid the diffraction effect and to attain high resolution (figure 2-d). Once the mask and wafer were accurately aligned, the photoresist was exposed through the pattern with a high intensity ultraviolet light with UV light power density of 3mW/cm² (figure 2-e). The exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer.

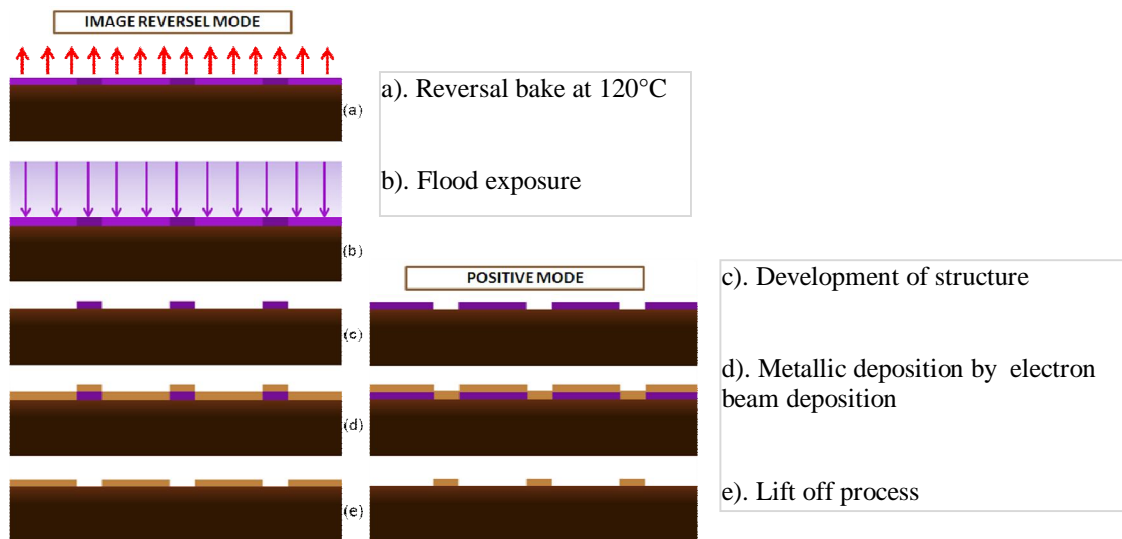


Figure 3. Fabrication of patterned structures in Positive and Image Reversal Mode

2.2.5. Development of photomask.

a) Development of positive mask. The next step was to dissolve soluble areas of photoresist by basic developer and to get visible patterns on wafer. The wafer with positive mask was directly developed in 1:1 solution of commercially available AZ 351 developer (from MicroChemicals) in de-ionized water.

The areas that were exposed to UV light were removed after developing, leaving windows exposing the underlying material. In other words, the mask, contains an exact copy of the pattern which will remain on the wafer (figure 3-c).

b) Development of negative mask. For the negative photomask (image reversal mode), few extra steps were involved after the UV exposure. After such step, the system is baked at 120°C for 2 minutes (figure 3-a) and a flood exposure in UV light without mask for 70 seconds (figure 3-b) is applied. These steps lead to an inversion in the chemistry of the photoresist that was not exposed to UV light at step 2.2.4. This resist become polymerized and more difficult to dissolve in 1:1 AZ Developer: de-ionized water solution. Hence it remains on the surface and the developer solution removed only the remaining resist portions (figure 3-c).

2.3. *Fabrication of Patterned Structure:*

After the successful imaging of the photomasks on the substrate the next step is to coat with a metal layer the areas where we don't want carbon nanotubes growth to occur. The following steps are required to such purpose.

2.3.1. Metallic Deposition by Electron beam Evaporation. CNTs can be grown on silicon substrate using an appropriate carbon source and a catalytically active metal. On the other end, non catalytic metals can be used to inhibit CNT growth. Hence, we used copper to cover the substrate where we don't wanted carbon nanotubes growth [11]. Metallic deposition was performed by electron beam evaporation technique in a vacuum chamber at 10^{-7} torr pressure. First a 20 nm thick titanium (Ti) layer was deposited and then a 200 nm thick copper (Cu) one added on top of it (figure 3-d). Ti is used as a buffer layer to overcome the poor adhesion of copper to silicon improving copper adhesion and stability.

2.3.2. Lift off Process. After deposition of metallic layers on the silicon substrate, a lift off process was performed in an ultrasonic bath at 60°C in acetone or normal methyl pirrolydinone (NMP) for 10-15 minutes (figure 3-e). During the lift off process the polymerized layer of photoresist under the metallic layer was detached from the silicon surface, leaving behind the required structures on the silicon substrate.

3. Growth of CNTs Columns by Thermal Chemical Vapor Deposition

The growth of vertical columns of multiwall carbon nanotubes on patterned silicon wafer was achieved by catalytic chemical vapor deposition of a reagent containing both the carbon and the catalyst sources. Ferrocene was used as catalytic source as it is a fine precursor to obtain iron nanoparticles, which leads to the formation of carbon nanotubes [12]. Commercially available camphor was used as carbon precursor as it is inexpensive and non-toxic. Furthermore, the arrangement of pentagonal and hexagonal carbon rings in camphor atoms makes it a good source to produce nanotubes [13].

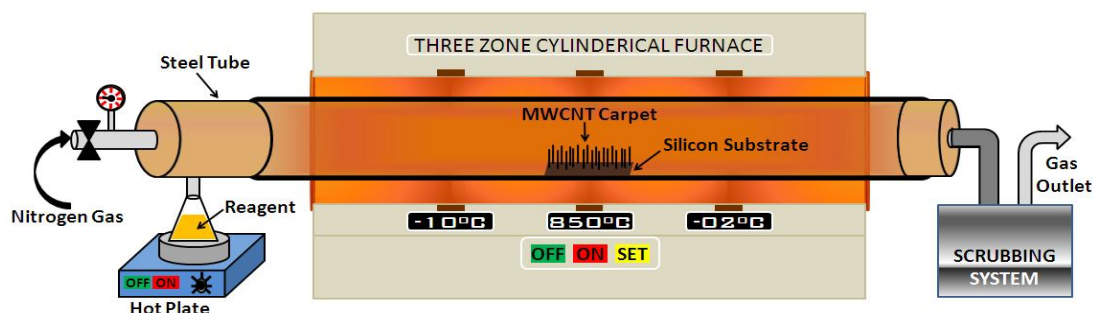


Figure 4. Thermal Chemical Vapor Deposition Growth System

The CVD unit used for CNTs growth is shown in Figure 4. A 100 cm long horizontal steel tube was placed in a 3-Zone furnace which has the ability to maintain a uniform temperature up to 1200°C throughout its length i.e. 60cm. The silicon substrates were placed in the central region of the furnace and inert atmosphere was maintained by nitrogen gas flux (420 ml/min). The pressure of the gas was kept slightly higher than the atmospheric pressure to avoid inward air leakages ensure. A pyrex conical flask containing the reagent mixture of camphor and ferrocene (20:1) was connected to the steel tube by a T joint between the furnace and nitrogen inlet. The pyrex flask assembly was rested on the hot plate.

The furnace temperature was maintained at 850°C and the pyrex flask was heated up to the vaporization of the reagent which starts above 200°C. The vaporized reagent was carried into the furnace by the nitrogen gas flux. The uniformity of the vapors flow was maintained by the temperature of the flask.

Because of the pyrolysis of the gases, the iron particles and carbon species were carried through the high temperature furnace. The iron particles works as catalyst and the deposition of carbon species on Si substrate resulted in the growth of carbon nanotubes. After a suitable time i.e.60 to 90 minutes, depending upon the required thickness of the CNTs carpet, the furnace was turned off. The similar method is described in further details by Musso et. al [4].

2. Surface Morphology

After the growth step is carried out, the produced structures were examined by FESEM. A ZEISS SUPRA-40 FESEM was used to study the structure, orientation, size and dimensions of nanotubes. In figure 5 (a,b), the circular patterning of different sizes on silicon substrate is shown. The vertical columns of carbon nanotubes grown by CVD shows that the length of circular columns is up to 1.5 mm. The diameters of the cylindrical columns are 250 μm (figure 5-c) and 500 μm (figure 5-d) and correspond to the mask features. The length of the columns, can be tailored by tuning the growth time in the range from a few micrometers to few millimetres.

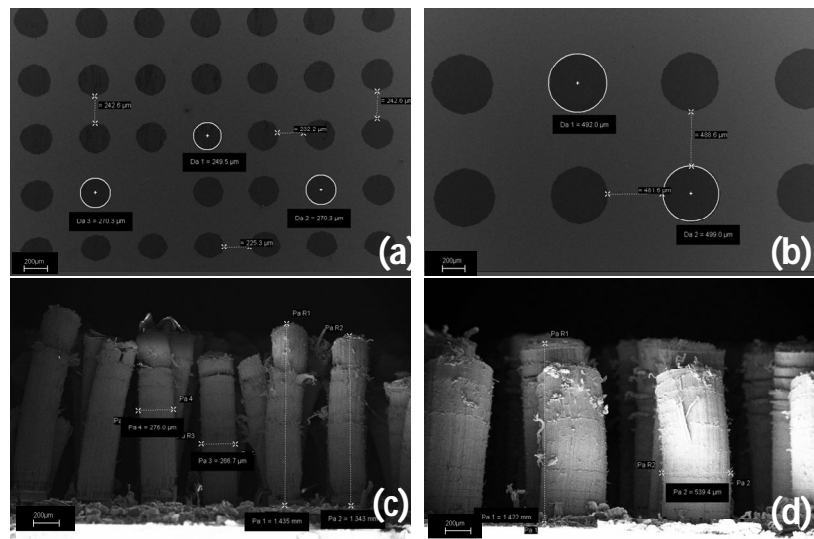


Figure 5. Patterned silicon substrates (a) & (b) and CNT columns (c) & (d)

Figure 6 shows some variety of structures based on MWCNTs varying in dimension and spacing as well as in structures type grown in our CVD system.

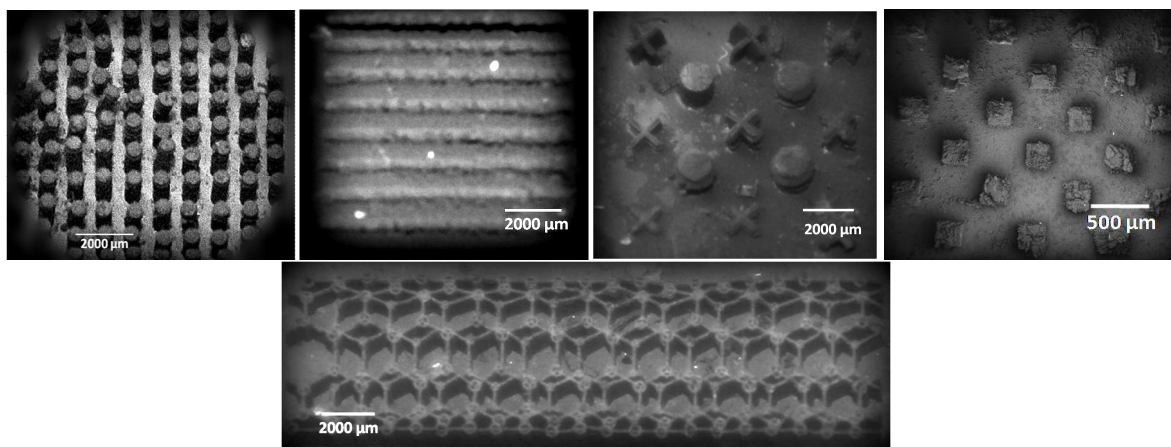


Figure 6. CNT based structures grown by CVD Technique

Figure 7 shows the structure, orientation, and dimension of carbon nanotubes inside the specific macroscopic structure. The diameter of a MWCNT is in the range of 30nm-70nm, only a few having diameter under 20 nm. The length of carbon nanotubes is up to few hundreds of micrometers. Most of the carbon nanotubes are well vertically aligned. Micrographs shown in figures 5 (a, b and c) are from the middle part of a column and micrographs in figure 5 (d, e and f) are from the top edge.

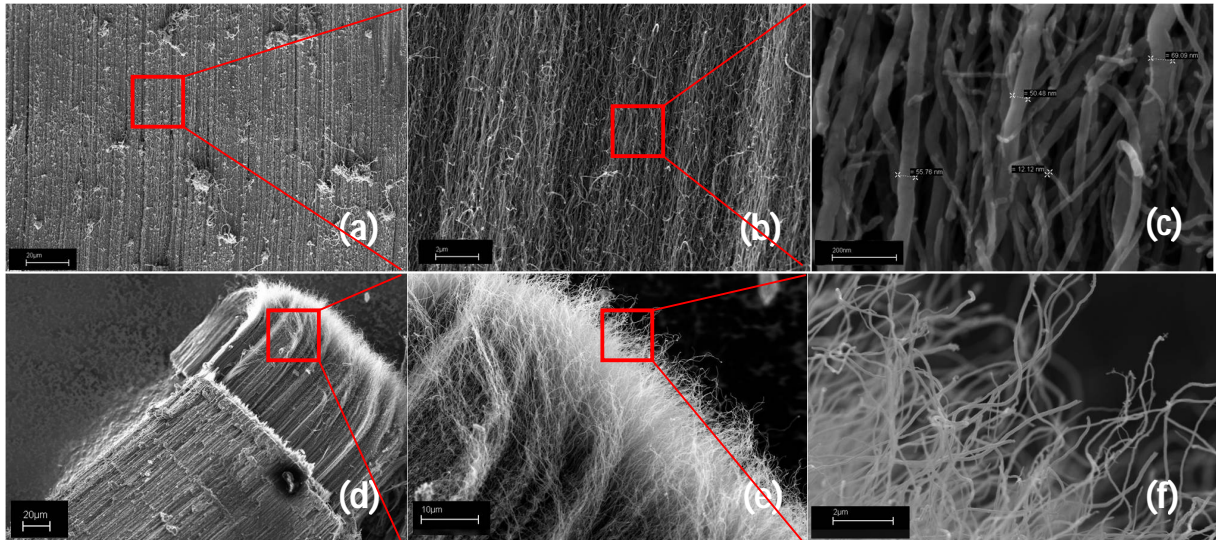


Figure 7. SEM micrographs of carbon nanotubes based structures

3. Structural Characterization

CNTs have been characterized by Raman spectroscopy to gain information about their structure. The Raman spectra of CNTs contains rich information about the electronic states and the phonon dispersion as it involves strong resonances of the incoming and outgoing photons and the vibrational states with the electronic energy levels of a tube [14].

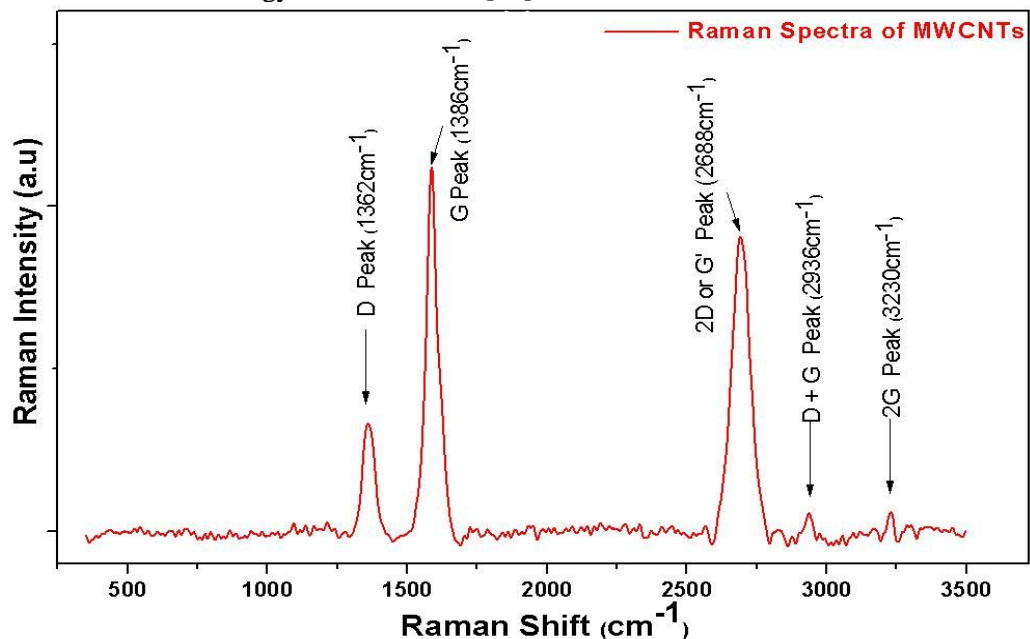


Figure 8. Raman Spectra of CNT based column

The D mode (breathing mode, A_{1g} band) is peaked in the 1300-1400 cm^{-1} range when excited with a visible laser. It is a typical disorder band observed in MWCNTs. The shorter intensity of D peak indicates the fineness of graphite layers. The G mode (Tangential Mode, E_{2g} band) is peaked in the 1550-1615 cm^{-1} range and corresponds to the stretching mode of sp_2 bonds in the graphite plane. A second-order-mode, often called G' mode is observed between 2620 and 2775 cm^{-1} [15, 16] which is

based on double resonance mechanism. Its intensity increases with the decrease in the lattice disorder [17].

4. Conclusion and Future Viewpoints

An efficient protocol has been developed for the patterning of silicon substrate for different shapes and dimensions of carbon nanotubes columns. The patterning do not hinder the growth of CNTs as demonstrated by the results reported. The obtained vertically aligned multiwall carbon nanotubes based columns can be used for different applications including thermal dissipation system, microelectrodes etc.

Acknowledgment

The authors are thankful to Dr. Micaela Castellino, Dr. Salvatore Guastella, Diego Pugliese and Vijay Deep for useful discussion and assistance during experimentation and characterization. PA acknowledges the support of the Italian Ministry of Research (FIRB grant RBFR10VZUG).

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