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TCO optimization in Si heterojunction solar cells on p-type wafers with n-SiO_x emitter

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Abstract

Silicon heterojunction solar cells have largely demonstrated their suitability to reach high efficiencies. We have here focused on p-type c-Si wafers as absorber, considering that they share more than 90% of the solar cell market. To overcome some of the issues encountered in the conventional (n)a-Si:H/(p)c-Si configuration, we have implemented a mixed phase n-type silicon oxide (n-SiO_x) emitter in order to gain from the wider bandgap and lower activation energy of this material with respect to (n)a-Si:H. The workfunction of the transparent conductive oxide layer (W_{TCO}) plays also a key role, as it may induce an unfavourable band bending at the interface with the emitter. We have here focused on AZO, a promising alternative to ITO. Different layers with varying W_{TCO} were prepared, by changing relevant deposition parameters, and were tested into solar cells. The experimental results have been explained with the aid of numerical simulations. Finally, for the n-SiO_x/(p)c-Si heterojunction with optimized W_{TCO} a potential conversion efficiency well over 23% has been estimated.
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1. Introduction

Amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction (HJ) solar cells have largely demonstrated their suitability to reach high efficiencies [1]. During the last years, to overcome some of the issues of the conventional design (mostly the parasitic optical losses at low wavelengths due to light absorption in the emitter layer) different

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materials with higher bandgap than a-Si:H have been studied and tested as replacing emitter to obtain a short circuit current density (J_{sc}) gain [2]-[4].

Despite the fact that the highest efficiency reached with the HJ technology has been obtained using n-type crystalline silicon absorber [5],[6], the p-type c-Si holds more than 90% of the world PV market. It seems thus particularly important to improve the device performance using p-type wafers. In this work we have applied mixed-phase phosphorus-doped SiO_x (n-SiO_x) as advanced n-type emitter on p-type c-Si wafers. The n-SiO_x layer is advantageous as it shows larger energy gap and enhanced conductivity with respect to amorphous silicon films. The complete device structure is n-SiO_x/(i)a-Si:H/(p)c-Si/(i)a-Si:H/(p)a-Si with Al on the back side and a transparent conductive oxide layer (TCO) plus metal grid as front electrode.

The primary requirements for TCO are high electrical conductivity and good visible transparency. Al doped Zinc Oxide (AZO) and Indium Thin Oxide (ITO) are among the most common transparent conductive oxides used as contact layer. ITO is generally preferred, mostly because of its good optical and electrical properties (resistivity ~ 10^{-4} ohm cm). On the other hand, although its resistivity is ~ 10^{-3} ohm cm, AZO is cheaper, more abundant and environmentally friendly than ITO. In addition, band alignment is an important aspect when selecting the TCO, as the misalignment of its workfunction (W_{TCO}) to the bands of the emitter may lead to the presence of a barrier against the extraction of the charge carriers. Depending on the solar cell configuration, AZO may have a more suitable workfunction with respect to ITO. Optimization of the workfunction can be also attempted by varying the deposition conditions. In the present work we focus on the use of AZO as front TCO and explore the variation of workfunction and conductivity when changing relevant deposition parameters, such as sputtering power and temperature. The effect on HJ solar cells is investigated experimentally and by means of numerical simulations.

2. Experimental

Silicon HJ solar cells were prepared starting from the RCA cleaning step on 250 µm thick, <100> FZ, 1 Ω cm resistivity, p-type c-Si wafers. A 5 nm (i)a-Si:H layer was used for surface passivation purposes on both sides of the wafer. Subsequently a 10 nm emitter layer was deposited while a 20 nm (p^+) a-Si:H layer was applied on the back side.

n-type doped SiO_x was here applied as advanced emitter. The layer was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) at 13.56 MHz, using a gas mixture of hydrogen (H_2), silane (SiH_4), carbon dioxide (CO_2), and phosphine (PH_3). The plasma power density, the pressure, the temperature and the $PH_3/(PH_3+SiH_4)$ doping ratio were fixed at 40 mW/cm^2, 2.5 Torr, 150°C and 2% respectively. The gas flow ratio $R = CO_2 / SiH_4 = 1$ was chosen based on previous work [7].

The cell front side was completed with an 80 nm thick AZO layer, deposited by DC pulsed magnetron sputtering at variable power in the range 200 – 400 mW, while the deposition temperature was varied from 25°C to 450°C; the final deposition temperature for the devices was settled under 300° C to prevent the degradation of amorphous layers. The metallization was formed by evaporating a 2 µm Al layer onto the back side and promoting local point contact by means of laser firing [9]. Finally, a grid shaped metal contact was applied on the front side by low sintering temperature (< 300 °C) with a screen printable Ag paste.

The Si heterojunction solar cells were characterized by measuring the Quantum Efficiency, both External (EQE) and Internal (IQE), and the current density versus voltage (J-V) under a class A solar simulator at AM1.5 condition. Prior to the metallization step, QSS-PCD was used to evaluate possible damages affecting the wafer passivation due to the TCO sputtering process.

Capacitance-voltage (C-V) measurements were performed to extract the W_{TCO} value. In this case a pad of ITO was grown on top of a p-type c-Si wafer, and a eutectic InGa electrode was deposited on the rear surface after removal of the native oxide. The amplitude and frequency of the AC probe during the C-V measurement were set to 50 mV and 100 kHz, respectively.

As an aid to the interpretation of the experimental results we additionally carried out numerical simulations on the TCO/n-SiO_x/c-Si(p) structure, by using a numerical model already developed for stacked thin films devices [10].

3. Results and Discussion.

In this work we have focused on sputtered AZO as front TCO. Different deposition conditions have been explored. In Table 1 we show the results of W_{TCO} and sheet resistance (R_sheet) measurements for selected samples deposited at different sputtering power and/or deposition temperature. The W_{TCO} value spans over the range 4.17 - 4.49 eV, with larger values in case of higher sputtering power. The sheet resistance varies between 18 and 45 Ω/square, which, considering the sample thicknesses, correspond to a resistivity between 2.4 $x10^{-4}$ and $1.1x10^{-3}$ Ω cm.

Table 1. W_{TCO} and R_sheet of selected AZO films for different sputtering power and deposition temperature values.

Sample	R_sheet Ohm/sq	thickness nm	Power Watt	T dep °C	W_{TCO} eV
TCO39	40	80	250	220	**4.17**
TCO90	45	240	300	270	**4.22**
TCO89	38	140	300	270	**4.26**
TCO38	30	80	350	220	**4.30**
TCO32	18	190	500	270	**4.49**

To highlight the role played by W_{TCO} in the HJ solar cell performance, a simulation study has been carried out considering the TCO/n-SiO_x/a-Si:H/(p)c-Si structure. For the novel n-SiO_x emitter, measured values of activation energy, mobility, and bandgap energy have been used as input parameters (E_{act} = 0.12 eV evaluated for 10 nm thick layers; μ= 2.5 cm^2/Vs; E_g = 2.2 eV, based on the E_{04} value). Details on the material characterization have been reported elsewhere [11]. Electron affinity and defect density within the forbidden gap have been assumed similar to a-Si:H. In all the simulations, the electron affinity was thus fixed at 4.05 eV for c-Si and 3.9 eV for both n-SiO_x and buffer layers. Figure 1 shows the simulated J-V curves under illumination for W_{TCO} varying in the range 4.1 eV - 4.6 eV. When W_{TCO} increases, the performance of the solar cell degrades until an undesired “S” shape appears in the J-V curve. This analysis clearly shows that AZO is more appropriate than ITO (with W_{TCO} ~ 4.6 - 4.9 eV) for the present solar cell configuration.

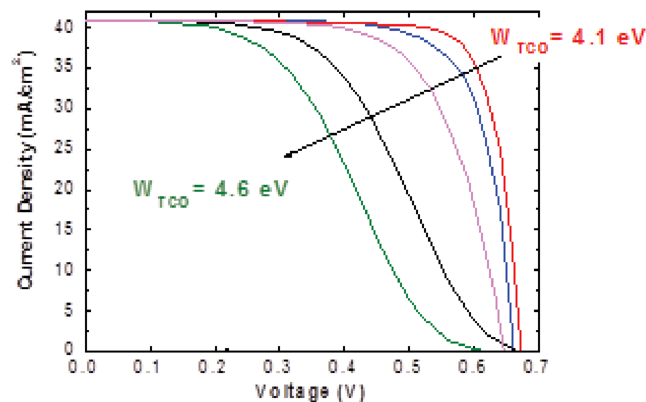

Fig. 1. Simulated J-V characteristics under AM1.5 illumination of the TCO/n-SiO_x/a-Si:H/(p)c-Si HJ solar cell as a function of the W_{TCO} value.

The deformation of the J-V curve is due to the relative position of the Fermi level of the TCO and n-SiO_x layers. The effect is shown in Figure 2, where the simulated energy band diagram of the HJ solar cell under sunlight condition is reported in case of W_{TCO} = 4.1 eV (a) and W_{TCO} = 4.6 eV (b) for two bias voltages (0 and 0.42 V). For W_{TCO} = 4.1 eV, the TCO Fermi level lies in equilibrium with the Fermi level of the n-SiO_x layer, thus avoiding the depletion within the emitter layer. When W_{TCO} increases to 4.6 eV, the n-SiO_x layer is depleted and the conduction band offset at the interface with (p)c-Si becomes a barrier against electron harvesting. The effect of the barrier is more evident when the solar cell works in moderate forward voltage. At the same time the device built-in potential is reduced from 1.52 V to 1.2 V.

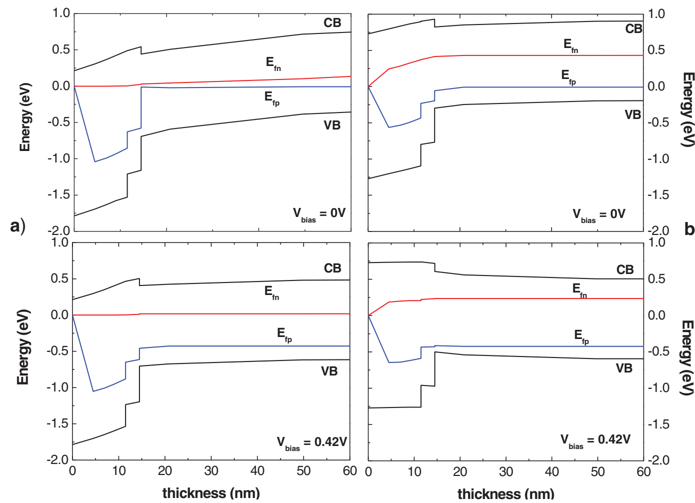

Fig.2. Simulated energy band diagram at the heterojunction interface under sunlight for V_{bias} = 0 (top) and 0.42 V (bottom) in case of W_{TCO} = 4.1 eV (a) and W_{TCO} = 4.6 eV (b). E_{fn} and E_{fp} represent the electron and hole quasi Fermi levels.

The evolution of the J-V curve with W_{TCO} has been confirmed experimentally. As an example, figure 3 shows the J-V curves corresponding to W_{TCO} of 4.17 and 4.3 eV (cell CL5 and CL7 of table 2) . All the solar cells with $W_{TCO} \geq$ 4.3 eV exhibited the behaviour of two diodes working in opposite directions (S-shape), due to the undesired band banding that affects the barrier at the c-Si interface. Additionally, we want to point out that the J_{sc} value around 35 mA/cm^2 confirms the suitable optical properties of the AZO layer and optoelectronic properties of the advanced n-SiO_x emitter.

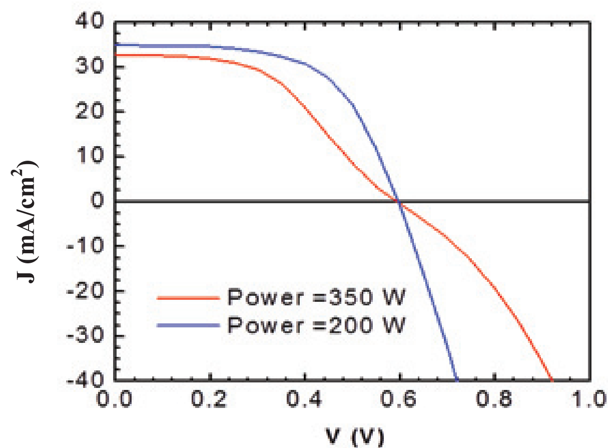

Fig.3. Experimental J-V curves for solar cells with AZO characterized by W_{TCO} of 4.17 and 4.3 eV (deposited at 200 and 350W, respectively).

To evaluate the potential of the n-SiO_x/(p)c-Si HJ solar cell, we have simulated the ideal condition of surface defect density at the c-Si/buffer interface reduced to the minimum value of $D_{it} = 10^{11}$ cm^{-2}. The optimal TCO, with resistivity $1x10^{-4}$ Ω*cm and W_{TCO} = 4.1 eV, has been adopted as front layer. This analysis has shown a potential efficiency of 23.6%, as reported in Fig. 4.

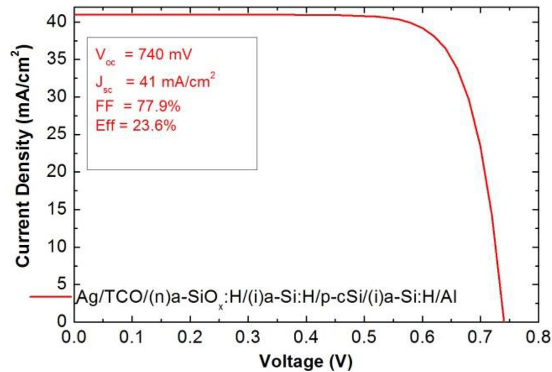

Fig.4. Simulated best performance of the n-SiO_x/(p)c-Si HJ solar cell.

Several solar cells have been fabricated while exploring different deposition conditions for emitter and intrinsic passivation layers. The performance metrics of the different devices are summarized in Table 2. Presently, an efficiency of 15.7 % has been obtained with flat surfaces. Noteworthy is sample CL33, whose V_{oc} of 714 mV is indicative of an almost optimal passivation of the wafer. To emphasize this result, Fig. 5 shows the SunsVoc measurement [12] on the same sample just before the metallization step: An implied V_{oc} above 740 mV is observed. The lower V_{oc} value in the J-V curve under illumination is mainly due to the still non-optimal rear surface collection.

Table 2. Photovoltaic parameters of n-SiO_x/(p)c-Si HJ solar cells with variation of the deposition parameters of emitter and passivation layers.

Sample	Eff (%)	FF (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	A cm^2	Notes
CL5	15.4	73.0	32.8	644	4	flat
CL7	11.9	57.7	31.0	666	4	flat
CL9	13.2	72.8	29.3	621	4	flat
CL10	15.2	**78.5**	31.5	615	4	flat
CL11	13.7	75.7	29.6	610	4	flat
CL12	11.8	65.2	30.2	599	1	flat
CL16	9.4	53.0	28.9	613	1	flat
CL32	15.3	62.5	**36.6**	670	1	textured
CL33	13.1	65.8	27.8	**714**	6.25	flat

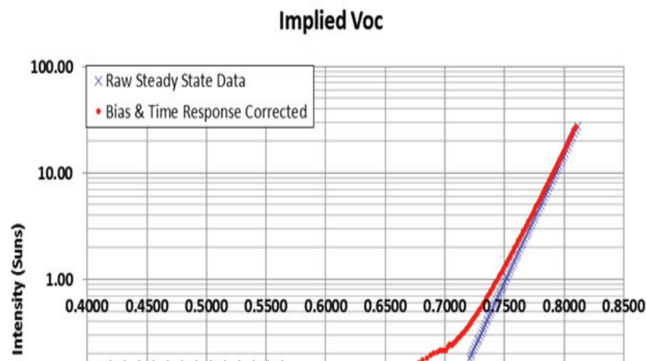

Fig.5. SunsVoc of the HJ solar cell CL33.

4. Conclusion.

We have here reported on the optimization of the promising n-SiO_x/(p)c-Si HJ solar cell configuration. We have experimentally demonstrated that the workfunction of the front TCO layer plays a fundamental role in the solar cell performance. With not appropriate value, an S-shape appears in the J-V curve as an effect of the formation of an undesired barrier working against the electron extraction. By varying the deposition conditions, we have obtained AZO layers with suitable W_{TCO}. With the optimal W_{TCO} value (4.1 eV) the simulations show a potential V_{oc} as high as 740 mV and an efficiency of more than 23%. Experimentally, an efficiency of 15.7 % has been presently reached. However the separate J_{sc}, V_{oc} and FF values achieved with different samples (marked in red in Table 2) show that there is room for improvement and efficiencies above 20% are within reach in a medium-short time scale.

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