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Evidence of bipolar resistive switching memory in perovskite solar cell

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***Abstract*—In hybrid inorganic-organic perovskite solar cells a very stable bipolar resistive switching behavior in the dark current-voltage characteristics at low-voltages has been observed. The possible use of the solar cell as an electrical memory with a moderate on-off contrast but very good stability over a prolonged time has been suggested. The reversible behavior and the long dynamics during the write/erase processes indicate that the physical mechanism behind the switching is related to polarization effects. A detailed analysis of the charge carrier trapping/detrapping, transport, and recombination mechanisms has been performed by taking the ion migration and the consequent charge carrier accumulation within the device into account. The charge transport during the write operation can be described by space-charge-limited conduction process. The formation and subsequent interruption of conducting pathways due to ion migration have been identified as the main cause of the resistive switching within the perovskite material. The strong interaction between the ion movement and the electron transport enables the operation of the perovskite solar cell also as a non-volatile memory.**

***Index Terms*— Charge carrier mobility, Perovskite solar cells, Resistive switching memory, Vacancy migration.**

I. Introduction

IN the last decades resistive random access memory (RRAM) devices have attracted wide interest as a next-generation of non-volatile memory device due to their ultra-low power consumption, fast operation speed, endurance, high scalability, and low costs [1]–[4]. Additionally, thanks to their compatibility with conventional complementary metal-oxide-semiconductor (CMOS) technology, simple architecture (metal/storage layer/metal) and design, RRAM devices are a possible candidate for the future replacement for the NAND Flash technology [2].

In literature electrical bistability has been explained by changes of the electrical [3], ferroelectric [4], and structural properties [5] by an electric field applied. In flash memories, the information storage is achieved by the capture and release processes of charge carriers within a semiconductor or insulator material [1].

One of the first evidence of material related electrical bistability and voltage-controlled negative resistance phenomena has been reported by Hickmott in 1962 in thin oxide films [6]. Subsequently, a large variety of binary and ternary oxides such as Nb_2O_5 Al_2O_3, Ta_2O_5, TiO_2, and $SrTiO_3$, $Ca_2Nb_2O_7$, have been investigated for memory devices, respectively [7], [8]. Reproducible switching has been also reported in amorphous chalcogenide semiconductors [9], amorphous silicon [10], organic materials [11], organic/silicon heterostructure [12] and graphene [13] based devices.

Although inorganic oxide perovskite materials have been already employed in the past for the fabrication of a memory device [14], more recently, non-volatile memories based on hybrid organic-inorganic perovskites have been fabricated. In 2015 Yoo et al. have reported the first RRAM device based on $CH_3NH_3PbI_{3-x}Cl_x$ material with a remarkable bipolar and bistable resistive switching behavior and a low operating voltage of 0.8 V [15]. In 2016 Choi et al. have fabricated a device with an ON/OFF ratio greater than 10^6 and set voltages below 0.15 V [16].

Organic-inorganic halide perovskite material, besides being one of the key materials for high efficiency thin film solar cells [17], has been also used as an active layer for the fabrication of light-emitting diodes [18], photo-detectors [19] and lasers [20]. It has a high optical absorption coefficient, a tunable band gap, ambipolar charge transport, long electron−hole diffusion length and is resistant to high energy radiation [21]. Additionally, the perovskite material shows two distinct phase transitions at about 160 K and 330 K, respectively [22]. This feature can be intentionally used in the memory storage applications for the fabrication of devices towards phase-change memory [5]. The electrical characteristics of the $CH_3NH_3PbI_3$ based device are affected by current hysteretic behavior [23]–[26].

Although the origin of hysteresis remains under debate, several authors suggested the polarization of the ferroelectric domains within the perovskite materials [24], the ion migration [27], [28], and the trapping/detrapping processes that involves intrinsic defects at the contact interfaces [29] as mechanisms of the charge carrier accumulation. It has been reported that there is no strong influence of light on the

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hysteresis in the photocurrent [30]–[32]. This means that the effect of the charge carrier accumulation within the perovskites can be investigated under dark conditions. A condition useful to extract information about defect states and their role as trapping or recombination centers [33].

In this study, a perovskite solar cell has been used as a resistive switching memory showing a reproducible and reliable memory characteristic in terms of write/erase operations, data retention, and endurance properties under dark conditions. The hysteretic behavior of the electrical characteristics has been investigated in terms of the charge carrier accumulation due to the ion migration. The obtained insight can give valuable information regarding the defect drift, charge carrier accumulation, hysteresis, electronic transport and recombination kinetics. These are important aspects also for the reliability of optoelectronic and memory devices based on perovskite.

II. Device Fabrication and Characterization

Fluorine-doped Tin Oxide (FTO) Glass substrate was first patterned and, subsequently cleaned in ultrasonic baths using mild alkaline solution, deionized water, acetone and isopropanol for 10 min and dried with a blow of nitrogen gas. Finally, ozone treatment was done for 30 min. Blocking layer of TiO_2 was deposited onto the substrate by a spin-coating method with 0.15 M Titanium diisopropoxide bis(acetylacetonate) in 1-butanol at 2000 rpm for 60 s; heated at 125°C for 5 min; cooled to room temperature. TiO_2 layer was formed by spin-coating TiO_2 in ethanol (0.1 g/2 ml) at 5000 rpm for 30 s; heated at 125°C for 10 min. The TiO_2 coated substrate was then annealed at 550 °C for 30 min. $CH_3NH_3PbI_3$ layer was formed by sequential deposition of PbI_2 and CH_3NH_3I in two-step spin-coating technique. First PbI_2 (400 mg/ml) was dissolved in DMF at 70°C; spin-coated at 3000 rpm for 30 s on TiO_2 coated FTO glass substrate. CH_3NH_3I (10 mg/ml) was dissolved in isopropyl alcohol; spin-coated sequentially on the as coated wet films (without thermal drying of the PbI_2 film). The substrate was heated at 70°C for 5 min. A black colored thin layer of $CH_3NH_3PbI_3$ was observed. Spiro-MeOTAD compound was used as a hole transporting material and spin-coated. A spiro-OMeTAD solution was prepared by dissolving 72.3 mg of spiro-OMeTAD in 1 ml chlorobenzene, 28.8 µl of 4-tertiary-butyl pyridine and 17.5 µl of lithium bis(trifluoromethanesulfonyl)imide (LiTFSI) solution (520 mg in 1 ml acetonitrile). Finally, silver was thermally evaporated for back contact. We used cell area of 0.04 cm^2 sized shadow mask to deposit silver electrode. Device fabrication processes up to the mesoscopic TiO_2 layer were carried out in ambient atmosphere and further processes such as perovskite film, hole-transport layer (Spiro-OMeTAD), metal contact (Ag) deposition and the electrical characteristics measurement were performed in a N_2 gas filled glove box (Jacomex) which is integrated with a thermal evaporator (Angstrom Engineering) and a solar simulator (Newport). Twelve devices were fabricated and investigated having an average perovskite thickness of about 600 nm.

The perovskite solar cells were characterized under a simulated solar spectrum (AM1.5G, Oriel Sol3A Class AAA simulator) by using a Keithley model 4200 parameter analyzer. The electrical characteristics of the resistive switching behavior of the perovskite solar cell were performed under dark conditions with a Keithley model 2400 in forward and reverse directions, using a sweep speed of 10 mV s^{-1}.

III. Results and Discussions

A. Current hysteresis and charge transport in perovskite solar cell

The investigated perovskite solar cell is composed of a $TiO_2/CH_3NH_3PbI_3$/Spiro-MeOTAD planar heterojunction, deposited on a fluorine-doped tin oxide (FTO) electrode and capped with a silver electrode. In Fig. 1 (a) the cross-section of the solar cell, following the layer sequence FTO/TiO_2/$CH_3NH_3PbI_3$/SPIRO-MeOTAD /Ag, is shown. The perovskite absorber has a thickness of around 600 nm. The current density - voltage (J-V) characteristics of the perovskite solar cell measured with a scan rate of 10 mV/s, under dark conditions (full symbols) and under one sun illumination (open symbols), are shown in Fig. 1 (b). The hysteretic behavior of the J-V curves suggests that there is a difference in the charge carrier collection during the forward and the backward voltage scan directions. In every solar cell the carrier collection is due to the charge carrier generation in the absorber layer and the subsequent transport to the electrical contacts. Since the charge carrier photogeneration and separation processes can be considered to be very fast, only the transport and the transfer is affected by the voltage scan rate [34]. As can be observed in Fig. 1 (b), the charge carrier collection measured under illumination results to be more efficient in the voltage backward direction showing an higher value of the current signal. The same behavior has been also observed for the J-V loop measured under dark conditions. Jena et al. suggest that this behavior can be related to the charge carrier transfer process at the interfaces which results to be more efficient as compared to the transport process within the bulk material [34]. In our case, the power conversion efficiency value, extracted from the J-V curves in

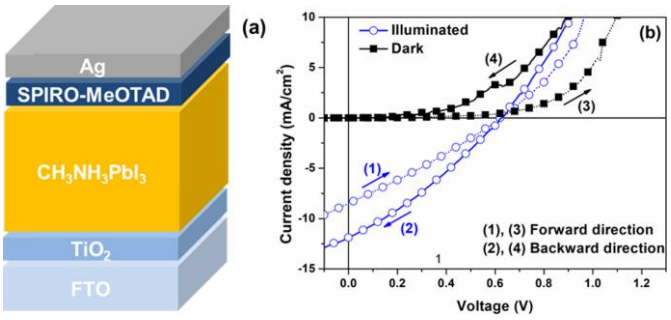

Fig. 1. (a) Schematic illustration of the cross-section of the device structure. (b) Current density–voltage characteristics measured at 300 K under dark conditions (full symbols) and under one sun illumination (open symbols) for the perovskite solar cell at a scan rate of 10 mV/s. Dotted and solid lines refer to performed forward and backward voltage scans, respectively. The arrows indicate the voltage scan directions.

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the forward direction, is about 30% lower than that obtained from the backward direction characteristics. In particular, the investigated device is characterized by the following parameters extracted in backward direction: short circuit current J_{SC} = (11.8 ± 0.4) mA cm^{-2}, open circuit voltage V_{OC} = (620 ± 6) mV, fill factor FF = (30 ± 1)%, power conversion efficiency η = (2.2 ± 0.1)%, series resistance R_s = (12.5 ± 0.4) Ω cm^2 and shunt resistance R_{sh} = (10.0 ± 0.3) KΩ cm^2. The low value of the V_{OC} indicates that the occupation of the highest energy defect states in the band tail results to be severely limited by the presence of recombination centers [35]. As a consequence, the quasi-Fermi level splitting within the device results to be reduced, and, hence, the open circuit voltage of the solar cells is substantially lowered [36], [37]. Although the solar cell shows a R_{sh} value, which is in good agreement with the data reported in the literature, the R_s value is higher than that observed for most high-efficiency perovskite solar cells, with values between 1 and 5 Ω cm^2 [35], [38]. This difference can be attributed to the interfaces between the device layers and the electrode contacts [39]. These findings explain also the low value of the observed FF.

The influence of the defect states on the hysteresis of the J-V curve becomes more evident when the device has been investigated under dark conditions. The measured current-density characteristic exhibits a power-law dependence with the bias voltage as $J \propto V^{\gamma}$, where the voltage exponent $\gamma \geq 2$ [40]. This result indicates that the high trap density reduces the charge carrier mobility and, therefore, the charge carrier transport is space-charge-limited. The applied bias voltage influences the occupation probability of the intrinsic defect within the active layer.

In Fig. 2 the J-V characteristics measured in forward and in backward sweep directions under dark conditions are shown. A "butterfly" shape owing to the four combinations of resistance states between the two resistive memory elements is observed. It is worth noting that the switching of the perovskite solar cell occurs only when the opposite polarity of the bias voltage has been applied before. This means that the RRAM device operates in a bipolar mode (see Fig. 2 (a)). Normally, the bipolar switching is due to the influence of the external electric field on the migration of the charged defects [2]. This finding is consistent with what is found in literature where the perovskite material is considered as an ionic-electronic conductor [30]. In particular, the ion movement modifies the charge carrier dynamics within the device through the compensation of the electric field. The most important role is, in that case, the interface between the contact material and the $CH_3NH_3PbI_3$ absorber layer.

In order to investigate the influence of the intrinsic defects on the charge transport in the perovskite solar cell, the J-V characteristics have been measured under dc voltage bias sweep (0 V → +1 V → 0 V → -1 V → 0 V) on the top Ag contact, whereas the bottom electrode (FTO) has been grounded. In particular, when a positive bias voltage sweep has been applied to the device, a low current density value has been observed, indicating that the device works in a high resistance state (OFF state). Subsequently for an increase of

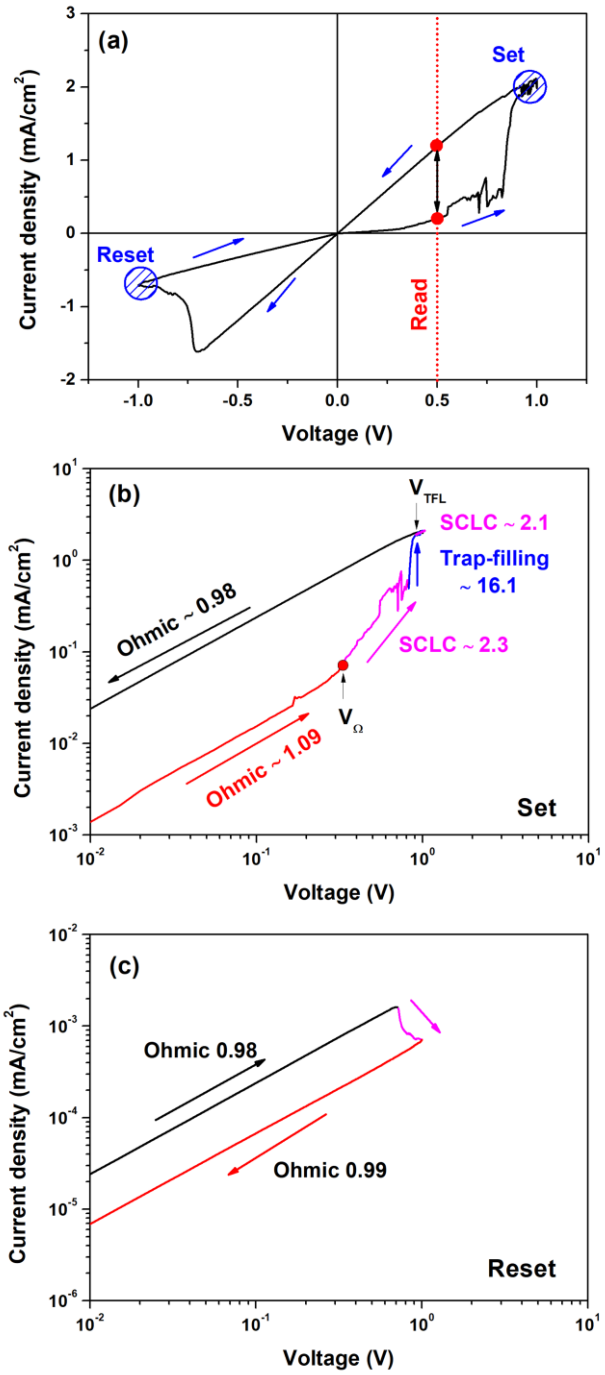

Fig. 2. (a) Current-voltage characteristics measured under dark conditions for the FTO/TiO_2/$CH_3NH_3PbI_3$/SPIRO-MeOTAD/Ag structure solar cell device with switching direction of applied voltages: 0 V→ +1 V → 0 V → -1 V→ 0 V. (b) and (c) plots of log J – log V with fitted conduction mechanism in positive and negative sweeps for the set and the reset processes, respectively.

the bias voltage, in the range between 0.5 and 0.8 V, a more noisy signal for the measured current density value has been noted. The increase of the noise amplitude has been also observed in the J-V characteristics at different scan rates and for all the investigated samples. It should be noted that the increase of the noise ripple has been already reported in literature for polymer composites and polymer:fullerene solar

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cells before the change of the electrical conductivity [41] and morphology of the active layer [33], [42], respectively. This result is a further evidence that the device is ready to switch into a low-resistance state (ON state) that occurs for voltages above to 0.8 V. Once the device is switched in ON state, the application of a negative bias voltage sweep from +1 V to -1 V changes the resistance of the perovskite device from the LRS to HRS (reset process). The reset process occurs when the bias voltage becomes lower than a threshold voltage (V_{RESET} approximately at -0.8 V), after that the device switches into the OFF state corresponding to an HRS. The ON/OFF ratio *r*, defined as the ratio between the current values measured at 0.5 V in ON and in OFF states, respectively, is nearly 6. Several authors report similar values of *r* for their memory devices based on $CH_3NH_3PbI_3$ material [43], [44]. Mathu et al. have recently demonstrated the possibility to control the operational parameters of the memory device through chloride doping of the perovskite material and obtained a very high *r*-value in the order of 10^3 [45].

The switching behavior of the perovskite solar cell can be analyzed by considering three different regions in the current density-voltage characteristics: ohmic, space charge limited current (SCLC) and trap-filled limit (TFL). In order to investigate the conduction mechanisms within the solar cell, the experimental data has been plotted in a double logarithmic scale, for both forward and backward voltage directions, as shown in Fig. 2 (b) and Fig. 2 (c), respectively. At low bias voltage the J-V curve follows a linear behavior ($J \propto V$) indicating that an ohmic conduction mechanism is dominant in the device between 0 V and 0.33 V. In this voltage range the injected electrons from the metal contact cannot fill all the traps and the conduction is dominated by the thermally generated free electrons stored within the perovskite solar cell. Since the voltage V_{Ω}, at which the transition between the ohmic regime and the SCLC regime occurs, has a value of 0.33 V, an estimation of the intrinsic charge carrier density n_0 within the perovskite material has been computed by using the following equation [46]

$$n_0 = \frac{V_{\Omega}\theta\varepsilon_0\varepsilon_r}{dq}. \quad (1)$$

Here, *q* is the elementary charge, *d* is the device thickness, ε_0 is the vacuum permittivity, and ε_r is the relative dielectric constant having a value of about 38 [38]. The quantity θ describes the influence of the trap density on the charge carrier mobility. By increasing the bias voltage to values above V_{Ω}, the amount of the injected charge carriers exceeds the intrinsic carrier density n_0 and the SCLC conduction mechanism becomes dominant. It is worth noting that the SCLC transport observed in J-V curves suggests that charge trapping levels are formed within the perovskite layer [44]. As a result, the current signal follows a power law dependence ($J \propto V^{\gamma}$) with $\gamma \approx 2.3$. Subsequently, a further increase of the bias voltage causes a rapid current increase ($\gamma \approx 16.1$), which reaches the trap-free regime value ($\theta = 1$) at an applied bias voltage

$$V_{TFL} = \frac{qN_T d^2}{\varepsilon_0\varepsilon_r}, \quad (2)$$

where $N_T = 5.25 \times 10^{15}$ cm^{-3} is the density of traps and V_{TFL} has a value of about 0.9 V. The extracted value of the intrinsic defect density within the perovskite material is in good agreement with literature values (ranging between 10^{14} and 10^{16} cm^{-3}) [35], [47]. It is worth noting that, when all the traps are filled, the device works again in the SCLC regime with $J \propto V^{2.1}$, as shown in Fig. 2 (b). As a consequence, the current density can be expressed as [48]

$$J = \frac{9}{8}\theta\mu\varepsilon_0\varepsilon_r\frac{V^2}{d^3}, \quad (3)$$

with $\theta = 1$ and μ is the electron charge carrier mobility. As reported in the literature, θ is the ratio between the *J* values measured in the SCLC regime (at V_{Ω}) and in the trap-filled state (at V_{TFL}), respectively [46].

The resulting value of θ is $\approx 3.6 \times 10^{-2}$ and, therefore, by taking into account (1) the computed n_0 value is about 4.2×10^9 cm^{-3}, consistent with that reported in the literature for perovskite [49]. Additionally, in the trap-free regime ($V \geq V_{TFL}$), the electron mobility extracted from (3) has a value of about 1.1×10^{-4} cm^2 V^{-1} s^{-1}, whereas, for $V < V_{TFL}$ the effective carrier mobility $\mu_{eff} = \theta\,\mu$ is about 4.1×10^{-6} cm^2 V^{-1} s^{-1}. It is worth noting that the value of the charge carrier mobility, extracted from the J-V curves by using SCLC, is one order of magnitude lower than that found in literature for a thick perovskite absorber layer, evaluated by using alternative techniques such as time of flight (TOF) and charge extraction by linearly increasing voltage (CELIV) [50]. For the perovskite-based solar cells, a thicker absorber layer means larger grain size within the film and, therefore, low trap density at the grain boundaries [51]. On the other hand, devices characterized by a large current hysteresis show strong recombination and low values of η. Several authors report the impact of grain boundaries on the power conversion efficiency and stability of organic-inorganic perovskites detected by using noise spectroscopy [35], [52]. It is clear that the film morphology of the absorber layer is strongly influenced by the processing conditions and stoichiometry [53]. However, the two-step deposition method used for the fabrication of the perovskite layer produces a low quality of the film morphology that decreases the device performance compared to the film deposited with the crystallization method [54], [55].

When the V_{TFL} voltage has been reached the device transfers from HRS to LRS and the set event takes place. Subsequently, in the voltage backward direction (1V → 0V) all the electrons remain trapped leading to the observed memory effect. On the other hand, when the bias voltage becomes lower than V_{RESET} = -0.8 V the device state changes in OFF state demonstrating the bipolar nature of the switching. In this respect, the operation electric field (1.5×10^4 V cm^{-1}) results to be comparable to the applied electric field for the switchable effect in $CH_3NH_3PbI_3$ – based devices (< 10^4 V cm

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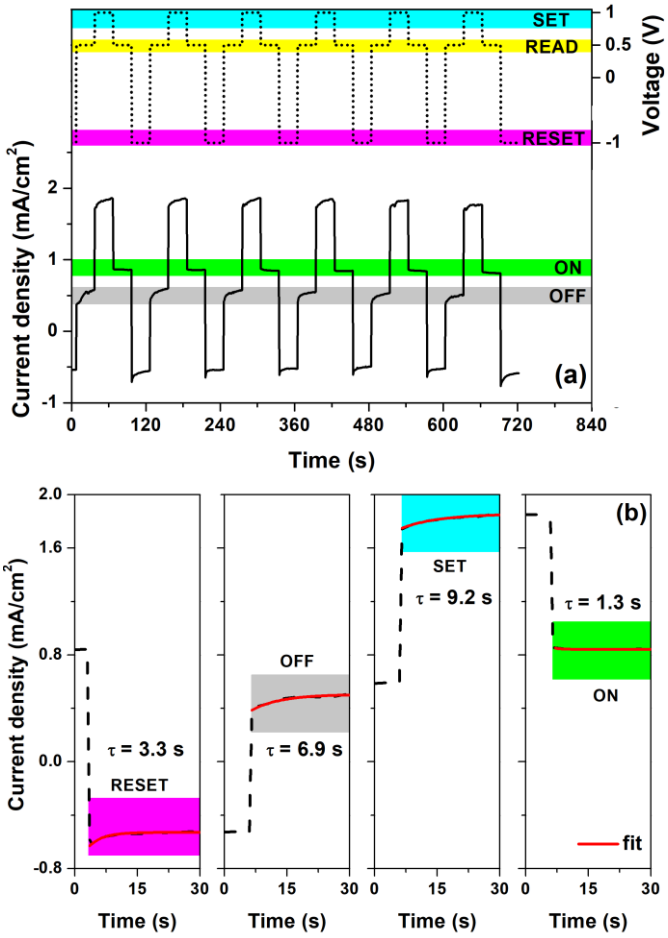

Fig. 3. (a) Time evolution of the voltage control signal applied to the device (dotted line in right y-axis) during the write-read-erase pulse cycles (specifically, 1 V to write, 0.5 V to read, then -1 V to erase and 0.5 V to read), and the corresponding current-density response (solid line in left y-axis). (b) Current-density transients after the reset, read and set events. The solid curves are the best fit obtained by using the following exponential decay function $y = y_0 + Aexp(-t/\tau)$.

$^{-1}$), where the write/erase processes have been explained by the migration of defect ions [16].

B. *Long-time switching behavior*

In order to investigate the reliability of the solar cell as a non-volatile memory device, the switching endurance during a repeated write-read-erase pulse test has been performed. The voltage control signal applied to the memory element is shown in Fig. 3 (a). The readout voltage is fixed at 0.5 V, whereas, the set and the reset voltages are fixed to 1 V and -1 V, respectively. In Fig. 3 (b) the corresponding time evolution of the current response of the perovskite memory measured for 6 operating cycles is shown. In order to evaluate the current-density dynamics, the period of one cycle has been fixed to 120 seconds while the duration of the write, read and erase events have been set to 30 seconds. As can be observed in Fig. 3 (b), the current follows the voltage control signal showing a transient behavior at each switching events. In order to evaluate their dynamics a fitting procedure has been performed by using an exponential decay function described as $y = y_0 + Aexp(-t/\tau)$, where A is the scale factor, y_0 is the background offset, t is the time in seconds and τ is the decay time constant. In Fig. 3 (b) the transients of the J signal, the best fitting curves, and the resulting time constant values τ are shown.

As evidenced, the fit procedure gives τ values on time scales of a few seconds. In particular, the set process results to be three times slower than that observed in the reset process. Moreover, after the change of the device in the ON state, its dynamic is faster than that observed after the switch in the OFF state. By assuming that the device is in the OFF state, when a set event occurs by applying a bias voltage $V \geq V_{TFL}$, the injected electrons start to fill the defect states. In this case, the portion of the unfilled traps influences the charge carrier transport leading to a longer dynamics. After a time of about 10 s (τ = 9.2 s) all the traps can be considered filled and the device has reached the ON state. Subsequently, by applying a reading voltage at 0.5 V, the observed current shows a fast dynamics (τ = 1.3 s) since the device works in the trap-free regime (θ = 1). On the other hand, when the reset event occurs the OFF state is reached after a time of 3.3 s.

This result has been also confirmed by reading the state of the device at 0.5 V. Since the applied voltage is higher than V_{Ω}, the device operates in the SCLC regime. Therefore, the charge transport is influenced by the empty traps, showing a longer time constant with τ = 6.9 s.

In Fig. 4 (a) the time evolution of the current-density response measured for 7 hours under operating conditions, corresponding to more than 200 cycles, is shown. As evidenced, the switching properties are maintained during the cycles and the resistance value measured under HRS and LRS states are about 750 and 370 Ω, respectively. Therefore, the resulting ON/OFF ratio has a value of about 2 for the entire period of operating, as depicted in Fig. 4 (b). It should be noted that the observed value of r during the cycles results to be lower than that measured in the J-V characteristics in Fig. 2 (a). This dissimilarity, already observed in the literature, can be related to the hysteresis that is strongly influenced by the scan rate, the scan direction as well as by the precondition prior measurement [24], [27], [28], [36].

The reliability of the memory device has been investigated by plotting the Weibull distribution of the set and reset resistances of the solar cell. The Weibull distribution function is frequently used in semiconductor failure analysis and can be expressed as [56]

$$F(Q) = 1 - exp\left[-\left(\frac{Q}{\alpha}\right)^{\beta}\right], \quad (4)$$

where $F(Q)$ is the cumulative distribution function, Q is the mean value either in HRS and LRS or r, α is the HRS/LRS/r value at 63rd percentile, and β is the Weibull shape factor often called Weibull slope. In order to estimate the Weibull parameters, (4) can be rewritten in terms of logarithm as follow

$$\ln[-\ln(1-F)] = \beta \ln\left(\frac{Q}{\alpha}\right). \quad (5)$$

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In Fig. 4 (c) the quantity $\beta ln(Q/\alpha)$ as a function of the Q is shown. By using the fitting procedure with (5), solid lines in Fig. 4 (c), the β values have been extracted. As can be observed, the β estimated from the slope in HRS is lower than that observed for LRS. This suggests that the reliability of the system results to be affected by the trap density. This result is consistent with that reported by Muthu et al. for the memory based on the perovskite material where the reliability is strongly influenced by the defect states related to the grain boundary of the material [45]. Additionally, the ratio r shows a higher value of β nearly 55 indicating that the r values have a relatively narrow distribution. The endurance of the device under write-read-erase cycles suggests that the process that originated the memory effect within the perovskite solar cell is strongly reversible. This result, combined with the long time constants, demonstrates that the origin of the hysteresis is consistent with a polarization response of the perovskite absorber. A similar result has been also reported in the literature where ion migration, that influences the hysteresis on the photocurrent extraction efficiency of the perovskite solar cell, is proposed as the dominant mechanism [27].

C. Influence of the ion migration on the electronic transport in resistive switching behavior

The presence of intrinsic point defects that causes charged states in the perovskite material such as vacancies, interstitials, cation substitutions, and antisite substitutions is often reported in the literature [35], [44], [57]. Among these intrinsic defects, only the vacancies, characterized by a low formation energy, are able to form shallow defects accessible in the trapping/detrapping processes [57]. Eames et al. report that in the hybrid perovskites the ionic conduction mechanism is related to the vacancy-mediated ion diffusion, showing that the iodide vacancies V_I are the majority ionic carrier [30]. The diffusion and the accumulation of the charged ions strongly modify the electric field profile and, therefore, the electronic transport and the recombination kinetics within the device. Here, the defect drift is considered as the potential origin of the switching behavior in the $CH_3NH_3PbI_3$-based solar cell. It should be noted that for a most performing device based on perovskite material, no reproducible resistive switching memory response has been observed [35].

In Fig. 5 the proposed ionic conduction mechanism behind the resistive switching memory, based on the drift of the iodide vacancies V_I, for the iodide vacancy configurations are shown. As evidenced in Fig. 5 (a) under low bias voltages lower than V_Ω, the V_I vacancies (open circles) are homogeneously distributed in the perovskite material, and the resulting electronic charge transport is ohmic. By applying a positive bias voltage ($V > V_\Omega$) to the top contact, the V_I vacancies (positively charged) follow the electric field by reaching the negatively charged electrode (FTO/TiO_2), as indicated by the solid arrows shown in Fig. 5 (b). This process leads to the formation of conductive pathways, originated by the accumulation of the iodide vacancies V_I, which become stable and more conductive with the increase of the bias

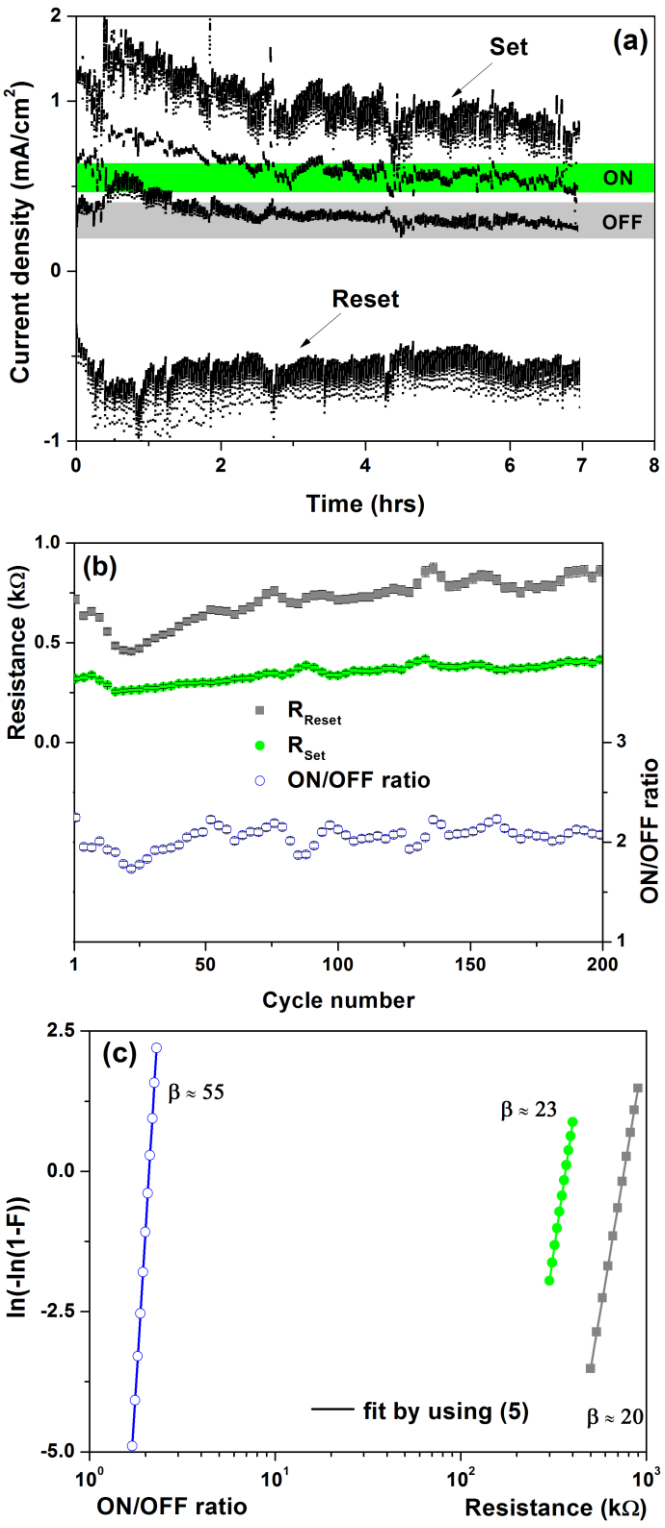

Fig. 4. (a) Time evolution of the current-density response during 200 cycles (specifically, 1 V to write, 0.5 V to read, then -1 V to erase and 0.5 V to read). (b) Cycle stability of the resistance measured in the high resistance state (HRS), in the low resistance state (LRS) (left y-axis) and of the ON/OFF ratio r (right y-axis). The error values are lower than 2% and, therefore, are within the symbols. (c) Weibull cumulative distributions of the HRS, LRS resistances and ON/OFF ratio r during switching endurance for perovskite based memory devices. The solid curves are the best fitting curves obtained by using (5).

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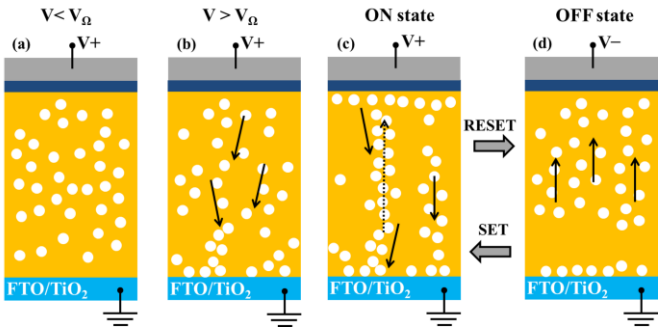

Fig. 5. Schematic illustration of the proposed resistive switching mechanism within the perovskite solar cell based on the J-V characteristics for the iodide vacancy configuration (a) in the pristine state for $V < V_\Omega$, (b) during the trap-filling process, (c) in the ON state for $V \geq V_{TFL}$, and (d) in the OFF state. The bias voltage is applied to the top metal contact, and the solid arrows indicate the moving direction of iodide vacancies upon application of the bias voltage. The dotted arrow denotes the conduction mechanism of the electrons by hopping between the traps, and the open circles represent the iodide vacancies.

voltage. It should be noted that the accumulation of the V_I vacancies leads to the formation of shallow traps that are filled by the injected electrons. In this case, the electronic conduction is dominated by the charged traps following the SCLC mechanism described in (3).

When the traps caused by the V_I vacancies are filled by the electrons for $V \geq V_{TFL}$, a transition in the ON state occurs and the electrons can flow by trap-to-trap hopping as shown in Fig. 2 (b). As evidenced in Fig. 5 (c), the accumulation of the vacancies between the TiO_2/ $CH_3NH_3PbI_3$ interface and along the grain boundaries within the tetragonal phase structure of the perovskite material forms conductive pathways towards the top electrode as displayed by the dotted arrow. In this case, the current-density in the trap-free regime can be expressed as [58]

$$J = \frac{q\Delta_n d}{\tau_{eff}}, \tag{6}$$

where τ_{eff} is the charge carrier lifetime and Δ_n is the amount of the electrons accumulated within the device in the ON state. For bias voltages above V_{TFL}, all the traps are filled and Δ_n can be expressed as $\Delta_n \approx N_T f$ where $f = 1$ is the quasi-Fermi level above the trap energy level. By taking into account the (6), an estimation of the τ_{eff} can be performed. The resulting value τ_{eff} is about 25.2 μs in good agreement with that reported in the literature [35]. Under this bias condition ($V \geq V_{TFL}$), the energy depth of the traps below the conduction band edge can be estimated from [39]

$$E_C - E_T = k_B T ln\left(\frac{N_{tot}}{\Delta_n}\right), \tag{7}$$

where k_B is the Boltzmann constant, T the temperature, and N_{tot} the density of states in the conduction band having a value of about 3×10^{18} cm^{-3} [59]. By using the (7), the energy level E_C - E_T of the traps results to be of about 160 meV demonstrating that the traps involved in the trapping/detrapping processes are shallow. It should be noted that the trap-assisted recombination is the dominant charge carrier loss mechanism in the perovskite solar cell [35], [59]. The charge carrier is first trapped in a charged shallow defect, usually located at the grain boundary, and subsequently it can be emitted or thermalized to a deeper state where a recombination process occurs [35]. According to literature reports the positively charged vacancies are the dominant defect ions within the perovskite material, that produces shallow traps [59], [60]. This evidence suggests that the iodide vacancy accumulated at the grain boundaries and at the device interfaces could be the potential origin of the resistive switching behavior in the solar cell.

On the other hand, when the bias voltage changes polarity and becomes negative the reset event occurs. As evidenced by the solid arrows in Fig. 5 (d), the iodide vacancies drift away from the bottom electrode and the conductive pathway is interrupted. In the OFF state, the conduction mechanism of the RRAM device becomes ohmic.

IV. Conclusion

A detailed analysis of a bipolar resistive switching behavior observed in a perovskite solar cell has been reported. The memory device shows a reproducible bistable resistive switching with operating voltages lower than 1 V and stable endurance, demonstrated for more than 200 write/erase cycles. The reversible behavior of the switching characteristics and the long time constants of the processes suggest that the hysteretic behavior can be related to the polarization effect of the perovskite layer. Since the perovskite material shows a mixed ionic-electronic conduction property, the set/reset processes can be explained by the migration of defect ions within the absorber layer and the consequent formation of conductive pathways within the perovskite layer along the grain boundaries. A potential candidate for the involved ions can be related to the iodide vacancy.

The accumulation of the iodide vacancies leads to the formation of shallow traps that are filled by the injected electrons. During the write process, the electronic conduction is dominated by the charged traps and it is described by the space charge limited current mechanism. In this respect, the charge carrier mobility and lifetime, the trap density, the trap energy depth and the intrinsic carrier concentration of the absorber layer have been evaluated. On the other hand, when the erase process occurs, the ions drift away from the TiO_2/$CH_3NH_3PbI_3$ interface causing in this way the rupture of the conductive filaments. In this case, the intrinsic carrier concentration of the perovskite dominates the charge carrier transport and the electronic conduction becomes ohmic.

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