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Two-dimensional electron systems (2DESs) at the interface between LaAlO$_3$ (LAO) and SrTiO$_3$ (STO) perovskite oxides display a wide class of tunable phenomena ranging from superconductivity to metal-insulator transitions. Most of these effects are strongly sensitive to surface physics and often involve charge transfer mechanisms, which are, however, hard to detect. In this work, we realize hybrid field-effect devices where graphene is used to modulate the transport properties of the LAO/STO 2DES. Different from a conventional gate, graphene is semimetallic and allows us to probe charge transfer with the oxide structure underneath the field-effect electrode. In LAO/STO samples with a low initial carrier density, graphene-covered regions turn insulating when the temperature is lowered to 3 K, but conduction can be restored in the oxide structure by increasing the temperature or by field effect. The evolution of graphene's electron density is found to be inconsistent with a depletion of LAO/STO, but it rather points to a localization of interfacial carriers in the oxide structure. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/1.5026912

The two-dimensional electron system (2DES) at the interface between bulk band insulators LaAlO$_3$ (LAO) and SrTiO$_3$ (STO) has attracted considerable interest from the point of view of fundamental and applied research, due to the plethora of tunable functionalities, such as conductivity,[1,2] superconductivity,[3,4] magnetism,[5,6] and spin-orbit coupling.[7] Modulation of interface conductivity has been achieved using not only electric field effect[2,8–10] but also illumination with visible or near-UV light[11] and surface-wetting by polar/protonated solvents.[12,13] Moreover, the critical LAO thickness for the emergence of the 2DES was significantly modified, following *in situ* deposition of various metals[14] or oxides.[15] These studies have emphasized the extreme sensitivity of the 2DES properties to other materials deposited on the surface,[9,12,14,15] due to chemical and electrostatic effects. Furthermore, the interface electrons at low temperatures and in diluted regime were found to be prone to localization and/or many-body correlation effects.[8,16,17]

Coupling of LAO/STO heterojunctions with graphene top-layers is particularly promising for various reasons. Indeed, graphene can be easily relocated on LAO/STO surfaces, and its excellent electronic properties[18] are very sensitive to the local environment.[19,20] In particular, the peculiar

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interaction with insulating LAO/STO samples enabled the observation up to room temperature of intrinsic quantum phenomena in graphene, such as weak antilocalization,[20] whereas graphene photo-conductivity was exploited to probe the built-in electric field within the LAO layer in both conducting and insulating LAO/STO samples.[19] In addition, graphene was used to control the interface conduction in both macroscopic devices fabricated on conducting LAO/STO samples[21] and nanometric-sized devices, written with a conductive scanning probe tip[9] on insulating samples.[22] Finally, the excellent electric insulation and efficient electrostatic coupling between graphene and LAO/STO-2DES[21] are promising in view of the investigation of possible inter-layer correlated phases that could be probed by Coulomb drag or plasmon spectroscopy,[23] in analogy to graphene-GaAs/AlGaAs systems.[24,25]

In this work, we exploit the semi-metallic nature of graphene to probe charge transfer phenomena[26–28] in LAO/STO samples and correlate them with the observation of a temperature-driven metal-insulator transition (MIT). Hybrid devices are obtained by depositing single layer graphene crystals on top of conducting LAO/STO samples. Graphene can act as a field-effect gate electrode, and its mere presence is already found to systematically reduce the conductivity of the buried 2DES at room temperature, with an effect that is stronger on samples with an initially low carrier density. In the case reported here, such a reduction leads to a transition to an insulating state at 3 K, at zero gate bias. Low-temperature MITs driven by electric field effects have already been studied in LAO/STO systems in a back-gate configuration.[8] An important novelty of our architecture is that the graphene top electrode allows us to probe the surface charge density and potential. Our results offer new useful evidence for the interpretation of similar transitions in the LAO/STO system.

Hybrid devices realized for this study implement a "dual" graphene-LAO/STO field-effect transistor, where each of the two electron systems has multiple contacts that allow performing independent transport measurements. One of the studied devices is depicted in the sketch and optical image in Fig. 1. A crucial aspect of our device architecture is the minimization of contamination at the graphene-LAO interface. To this end, it is first of all important to obtain LAO/STO Hall bars with polymer-free LAO surface. An amorphous STO (a-STO) mask was deposited on bare, TiO_2-terminated STO substrates by a combination of photolithography, room-temperature a-STO deposition, and lift-off.[29] After a delicate oxygen plasma ashing, 8 u.c. of crystalline-LAO (c-LAO) were deposited
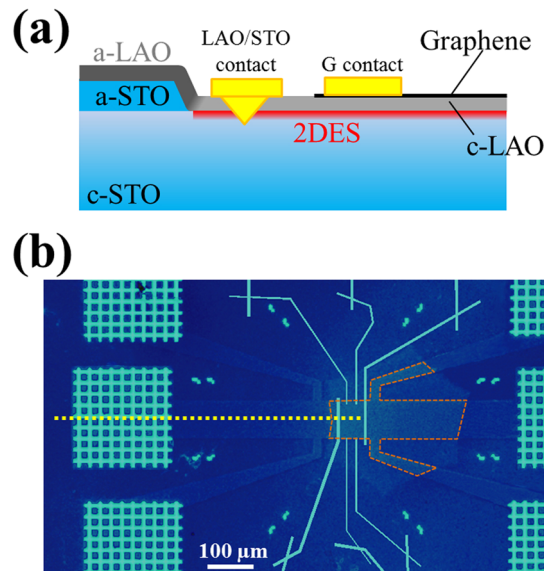

FIG. 1. **Hybrid, graphene-LAO/STO devices with aligned Hall bars**. (a) Schematic drawing of the cross section of the device along the dotted, horizontal line shown in (b) the optical image of the hybrid, patterned graphene-LAO/STO devices for low temperature, electrical transport investigations. The red dashed line indicates the final shape of the graphene crystal after etching.

by RHEED-assisted pulsed laser deposition.[30] An amorphous LAO (a-LAO) film grows on the a-STO mask, as sketched in Fig. 1(a), resulting in an insulating interface outside of the Hall bar, as demonstrated by the large resistance (>1 GΩ) between separate Hall bars.

High-quality, single-layer graphene monocrystals were grown by chemical vapor deposition on Cu substrates[31] and then deterministically transferred through a semi-dry, bubble transfer technique[32] on the LAO/STO Hall bars, using PMMA vectors.[33] Graphene crystals were aligned so as to fully cover the width of the LAO/STO Hall bar between one pair of probes but leave the other pair uncovered to enable the measurement of the electron density in bare LAO/STO. Cr/Au electrodes for graphene and LAO/STO were realized by electron-beam lithography and thermal evaporation; Ohmic contacts between metal electrodes on the surface of LAO and the buried oxide-2DES were established through ultrasonic wire bonding. Finally, graphene Hall bars were defined by etching the original crystal with a low-energy, oxygen-based reactive ion etching outside the LAO/STO Hall bars. The PMMA residues from the graphene transfer and the fabrication processes were minimized through long baths in warm (40 °C) acetone. We avoided high-temperature annealing and the use of oxygen plasma on crystalline LAO/STO regions, which could modify the intrinsic properties of the system. Despite the very large junction area (~10^4 μm^2), excellent electric insulation between graphene and the interfacial 2DES is observed from 3 to 300 K, with vertical resistances higher than 100 MΩ for graphene-oxide bias (V_{GO}) between −0.3 V and 1.5 V, allowing for the exploration of mutual electric field-effects between graphene and the interfacial 2DES (see Sec. II of the supplementary material).

Graphene is found to modify the LAO/STO 2DES conductivity even at zero applied bias V_{GO}. At room temperature, two-probe electrical resistances between contact pairs separated by graphene-covered areas are 50%–100% larger than the ones between geometrically equivalent contacts far from the graphene junction, as shown in Fig. 2(a) for two representative pairs. Prior to graphene deposition, the two-probe resistances of the same pairs differ by less than 5%. Such a difference is systematically observed in all studied devices, in correlation with graphene deposition [see Fig. S1(a) of the supplementary material]. We therefore conclude that the difference stems from the higher resistivity of graphene-covered regions. The impact of the graphene overlayer manifests most drastically at low temperatures, when low-carrier density LAO/STO interfaces underneath graphene becomes insulating. As shown in Fig. 2(a), pairs of LAO/STO contacts separated by the junction region exhibit 2-probe resistances higher than 10 MΩ at 3 K, with typically non-Ohmic behavior. By contrast, contact pairs not separated by graphene-covered regions exhibit typical resistances of 10–20 kΩ. The emergence of an insulating behavior of LAO/STO under graphene appears to be mostly correlated with the initial carrier density, and it is observed in devices fabricated on LAO/STO samples with initial low temperature densities smaller than ≈1.5×10^{13} cm^{-2}, while it was not observed for densities higher than 2×10^{13} cm^{-2}.

Conduction can be restored in various ways. First of all, graphene can be used as a top-gate to repopulate the underlying interface with mobile carriers. In Fig. 2(b), we report the top-gate field-effect characteristics for the pair D1–D2 of oxide-2DES contacts: for V_{GO} below the threshold voltage of 25 mV, the 2-probe conductance is only a few nS and is not modulated by the top-gate, confirming the insulating behavior; beyond this threshold, conductance rises first linearly with increasing V_{GO} and then sub-linearly, when the 2DES conductance below graphene becomes comparable to that of bare LAO/STO. Temperature variation provides a further important way of restoring conduction, and it triggers a reverse insulator-to-metal transition at $V_{GO} = 0$ V. In this case, the graphene overlayer can be used to monitor the interface electronic properties during the process. The field effect of graphene on the oxide 2DES as a function of temperature is shown in Fig. 3(a). The conduction threshold decreases linearly with increasing temperature and the junction becomes conducting at $V_{GO} = 0$ V for T > 6 K. The exact transition temperature was found to depend on the cool-down history and on the device and the chip under test, but its value always falls between 6 and 27 K.

Charge transfer phenomena are frequently invoked to account for the behavior of the LAO/STO carrier density in the presence of overlayers.[14] A unique feature of our system is that the semimetallic nature of graphene allows us to probe[26–28] the variation of the carrier density of the gate. Here, the graphene hole density (p_G) and the electron density of bare LAO/STO ($n_{LAO/STO}$) were measured in the temperature range 3–16 K using the Hall effect. The same protocol could not be adopted for the graphene-covered LAO/STO ($n_{G-LAO/STO}$) since mobility is typically too low to extract a reliable
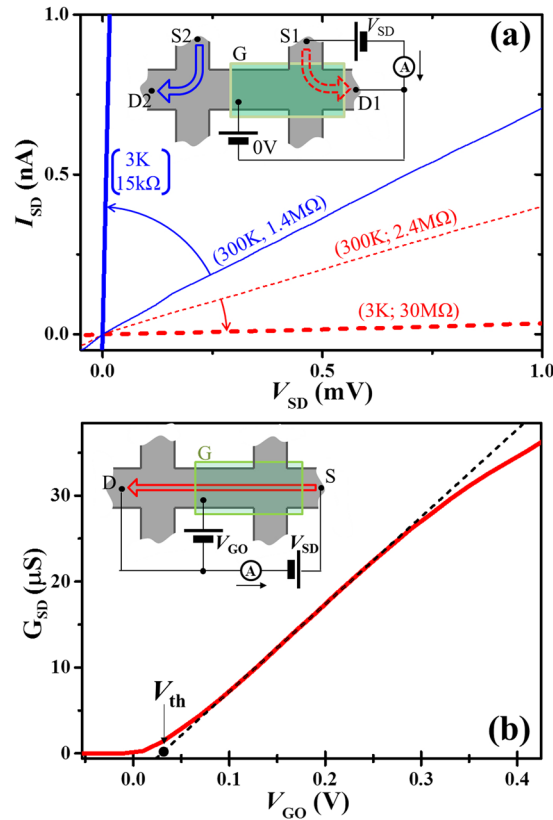
FIG. 2. **Metal-insulator transition in graphene-covered LAO/STO**. (a) Comparison of two-probe I-V characteristics of geometrically symmetric LAO/STO areas covered by graphene (contacts S1-D1, dashed curves) and without graphene (contacts S2-D2, solid curves), at room temperature (thin lines) and at 3 K (thick lines). (b) Two-probe DC conductance of the interfacial-2DES as a function of the top gate bias from graphene, showing the depletion of the LAO/STO interface from mobile charge carriers at 3 K in equilibrium conditions and its repopulation for $V_{GO} > 0$ V. The thin, dashed line is a linear fit to the conductance curve, allowing the extraction of the pinch-off voltage of the 2DES underneath graphene. Insets are schematics of the electrical setups used to acquire the corresponding transport curves.

Hall trace. The density $n_{G-LAO/STO}$ was thus extracted using the pinch-off voltage of the field-effect characteristic [Fig. 3(a)] and a capacitor model (more details in Sec. III of the supplementary material). During the MIT, the carrier density in the LAO/STO junction below graphene goes from $n_{G-LAO/STO} \approx 2.2 \times 10^{12}$ cm^{-2} at 16 K to an insulating state at 3 K. Such a change cannot be attributed to a transfer of electrons from the LAO film or from the bulk STO: this would give rise to a similar decrease of the electron density in the graphene-free oxide-2DES during the MIT, which is not observed in our samples [see Fig. 3(b)]. Furthermore, the mobile electrons apparently lost by the oxide-2DES during the MIT are not transferred to the gate either, as demonstrated by the slightly higher hole density of graphene at 3 K with respect to 16 K [by $\approx 5 \times 10^{10}$ cm^{-2} for the dataset of Fig. 3(b)]. We note that the exact amounts of mobile charge density variations during MITs depend on the specific sample and device under test as well as its thermal history. However, our conclusions remain unchanged, because both graphene and the oxide-2DES underneath were always found to lose mobile electrons during the MIT, unlike the bare oxide-2DES.

The apparent puzzling non-conservation of the total charge density of graphene and LAO/STO interface during the MIT can be accounted for by recognizing that the techniques we used to extract the carrier densities reported in Fig. 3 are only sensitive to mobile electrons. In this picture, the insulating state is not caused by a depletion of the LAO/STO interface, but rather by a localization of the conduction band electrons, and thus by a sharp change of their mobility. A large fraction of these carriers delocalize due to the thermal energy available when the temperature is increased. The insulating state of LAO/STO interfaces undergoing MIT has been compared to that of Anderson
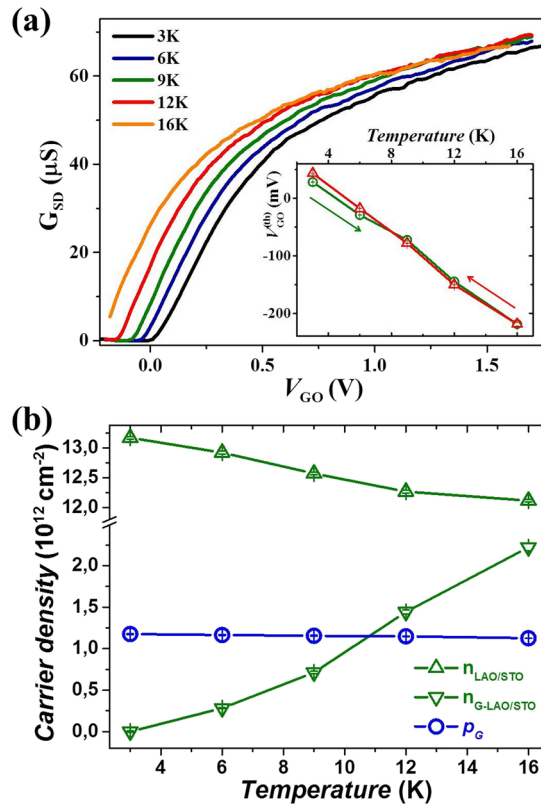
FIG. 3. **Temperature dependence and mobile charge balance**. (a) Two-probe conductance of the oxide-2DES as a function of graphene-top-gate bias at different temperatures in the range 3–16 K, showing the gradual repopulation of the junction region with mobile charges. The inset illustrates the temperature dependence of the conduction threshold during a thermal cycle from 3 to 16 K. The electrical setup is the same as in the inset of Fig. 2(b). (b) Temperature dependence of the carrier densities in graphene (circles) and in the LAO/STO interface inside (down-pointing triangles) and outside (up-pointing triangles) of the junction, demonstrating the absence of charge transfer phenomena from graphene and the opposite behavior of graphene-free and graphene-covered areas of the LAO/STO interface. The lines connecting the symbols are useful guides to the eye.

or polaronic insulators and to disorder-pinned Wigner crystals.[8] All these pictures are in principle compatible with our observations, since a large-scale electrostatic probe cannot distinguish among the different localization mechanisms as long as they are only associated with an in-plane relocation of charge. Differently, the formation of an inhomogeneous planar distribution of carriers might be detectable using patterned micro or nanometric graphene overlayers.

To further corroborate the localization scenario, we propose a simplified model of the disordered LAO/STO interface, which enables a rough estimation of the disorder potential, as well as a qualitative demonstration of the thermal delocalization phenomenon (see also Sec. V of the supplementary material). In particular, the disordered oxide-2DES beneath graphene was described through a smeared density of states of the form $g(\epsilon) = m^*/\pi\hbar^2(1 + \exp(\epsilon/\gamma))$,[35] where γ represents the amplitude of the disorder potential, and the mobility edge was set at $\epsilon = 0$. In this picture, a lower-bound for the disorder energy scale can be obtained by realizing that the mobile charges estimated for $T > T_{MIT}$ must occupy negative-energy states at 0 K. For the dataset in Fig. 3, using the highest-known value of mobile charge density (at 16 K) and assuming $m^* \approx 1.6\,m_0$,[36,37] we obtain $\gamma > 3.1$ meV; more generally, the lower bounds of disorder energy scales in our samples fall in the range 1.6–4.6 meV. The thermal energy needed to delocalize charges is expected to increase with disorder energy: indeed, we observe a partial positive correlation between the critical thermal energy and the lower-bound estimate of disorder, with a relative ratio varying between 0.14 and 0.6 [Fig. S5(b) of the supplementary material]. More importantly, our model qualitatively reproduces the delocalization of charge carriers with increasing temperature. However, the maximum predicted mobile charge at 16 K remains lower

than what is observed in Fig. 3(b) [see Fig. S5(c) of the supplementary material]. This indicates that further refinements of the model, including the effects of quantum capacitances of graphene and the depleted LAO/STO, the quantum paraelectric transition of STO, and the temperature dependence of disorder, are needed to quantitatively reproduce the data.

We note that the amplitude of the disorder potential in our samples is two orders of magnitude higher than in doped STO samples,[36] possibly due to the additional interface disorder introduced by the high-temperature deposition of LAO films and the consequent charge confinement close to the interface. Instead, electrostatic imaging experiments in LAO/STO samples indicate interface-potential fluctuations of the order of 1 meV, due to the striped, structural domains of STO;[38] this value is compatible with our conclusions and represents a lower estimate of interface-disorder, to which additional sources of disorder can add up.

Finally, we tentatively comment on the origin of the different behavior of graphene-covered regions with respect to bare LAO/STO. Whereas metallic overlayers and adsorbates are typically found to strongly influence the carrier density of the LAO/STO 2DES,[9,12,14,15] the observed reduction of conductivity in graphene-covered regions is at odds with graphene's low work function,[34] which should instead lead to a more populated oxide interface.[14] However, we note that the lower chemical reactivity of graphene with respect to metals with a similar work function and its semi-metallic nature could explain the observed discrepancy. Further mechanisms that can account for this asymmetry are the possible differences in the LAO surface chemistry between the graphene-covered and graphene-free regions and the existence of additional scattering channels for oxide-2DES carriers below graphene due to the Coulomb interaction with the graphene-2DES.

In conclusion, we have shown that graphene can be used both as a gate electrode and as a charge probe in a graphene-LAO/STO sample. Graphene is also found to reduce the LAO/STO conductivity at room temperature and a MIT is observed below 9 K. The study of graphene carrier density during the MIT indicates that the modulation of the mobile charge in the LAO/STO interface below graphene is likely associated with localization phenomena and not with charge depletion. Since localization is possibly related to the emergence of spatial inhomogeneities in the carrier density distribution, we foresee that the multiple patterned graphene probes could be used to investigate the spatial homogeneity of charge transfer during localization and metal-insulator transition phenomena.[8] In addition, we note that the electric-field control of the MIT in hybrid graphene-LAO/STO junctions provides electrical switching capabilities that might be useful for digital logic applications, in analogy to Mott transistors.[39]

See supplementary material for additional experimental data on the temperature-dependent transport properties of graphene-LAO/STO systems as well as for a detailed description of the models we adopted to analyze the data and the comparative analysis of the properties of bare and graphene-covered LAO/STO.

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