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ARTICLE

A Phase Change Memory Chip Based on TiSbTe Alloy in 40-nm Standard CMOS Technology

Zhitang Song · YiPeng Zhan · Daolin Cai · Bo Liu · Yifeng Chen · Jiadong Ren

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Abstract In this letter, a phase change random access memory (PCRAM) chip based on $Ti_{0.4}Sb_2Te_3$ alloy material was fabricated in a 40-nm 4-metal level complementary metal-oxide semiconductor (CMOS) technology. The phase change resistor was then integrated after CMOS logic fabrication. The PCRAM was successfully embedded without changing any logic device and process, in which 1.1 V negative-channel metal-oxide semiconductor device was used as the memory cell selector. The currents and the time of SET and RESET operations were found to be 0.2 and 0.5 mA, 100 and 10 ns, respectively. The high speed performance of this chip may highlight the design advantages in many embedded applications.

Keywords PCRAM · $Ti_{0.4}Sb_2Te_3$ alloy · CMOS · NMOS

1 Introduction

Phase change random access memory (PCRAM) has been considered one of the most promising candidates for floating-gate memories replacement [1, 2]. Low voltage, high speed and density, well compatibility with standard complementary metal-oxide semiconductor (CMOS) technology, and superior scalability characteristics place PCRAM in a good position in the emerging memory technology [3–7]. The memory cell is mainly constituted by a thin film of chalcogenide material layer in contact with a metallic heater. When a programing voltage or current is applied to the storage cell, a high current density will flow into the resistive heater, causing the temperature increase due to Joule effect. Since the phase change material in the active region is close to the heater, it will induce the phase transition between the RESET and SET state. To avoid the heating phenomenon, PCRAM chip based on $Ge_2Sb_2Te_5$ (GST) alloy was integrated [8, 9] and applied to mobile electronics to replace Not OR (NOR) flash memory [10]. Since then, PCRAM has become a mainstream technology in high-density non-volatile memory applications [11]. However, the slow SET speed and high RESET power of this kind of PCRAM limit its applications in other fields [12]. It was found that phase change memory (PCM) cell based on $Ti_{0.4}Sb_2Te_3$ (TST) alloy showed one order of magnitude faster SET operation speed and as low as one-fifth RESET operation power compared with GST-based PCM cell at the same size [13, 14].

Compared with the one-bipolar-junction-transistor-and-one-resistor (1B1R) [15] and one-diode-and-one-resistor (1D1R) [16, 17] structured memory cell, the one-transistor-and-one resistor (1T1R) [18–20] memory cell is the simplest and the best compatible in process, in which only additional 2–3 masks accomplishing the chip integration though the cell size of 1T1R structure is larger than that of

Z. Song (✉) · D. Cai (✉) · B. Liu · Y. Chen
State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, People's Republic of China
e-mail: ztsong@itsvr.sim.ac.cn

D. Cai
e-mail: caidl@mail.sim.ac.cn

Y. Zhan · J. Ren
Semiconductor Manufacturing International Corporation, Shanghai 201203, People's Republic of China

the 1B1R and 1D1R structures. In our previous work, an 8-Mb PCRAM experimental chip has been fabricated in a 130-nm 4-metal level standard CMOS technology [18]. However, the larger operation current and smaller RESET/SET resistance ratio are still the crucial issues for PCRAM chip. In this paper, PCM experimental chip based on TST phase change material as storage medium was fabricated in 40-nm technology. The RESET current was reduced and RESET speed was increased successfully.

2 Memory Cell Architecture

Figure 1a shows the structure of 1T1R memory cell whose selector was implemented by a standard 1.1 V negative-channel metal-oxide semiconductor (NMOS) transistor based on the 40-nm CMOS technology. With the purpose of ensuring lower process cost, the 1.1 V NMOS transistor was introduced to reduce the number of lithographic mask compared with the diode and the bipolar. Figure 1b shows a schematic cross section of the 1T1R structure. Figure 1c is a scanning electron microscope (SEM) image of the array along the word line (WL) direction, where the WL was connected to the gate of the NMOS transistor, and the drain of the NMOS transistor was connected to the heater of the storage cell. While, the bite line (BL) was connected to the top of the memory cell through M1, M2, M3, and M4. The TST layer was placed between the heater and the M1. As the heater, the TiN bottom electrode contact (BEC) was fabricated and its diameter is 35 nm.

In the memory cell structure, the BEC area of the storage element is the main factor affecting the RESET current. To minimize the RESET current is a key point for designing the memory cell architecture. Thus, spacer technology was used to reduce the BEC size and subsequently reduce the RESET current. Figure 1c shows the SEM image of the storage element prepared by spacer technology based on 40-nm baseline. The BEC diameter is about 35 nm which is half of the normal size.

3 Chip Performance

The current pulse amplitude and width were measured on the UF3000EX-e tester. Figure 2 shows the current–resistance (*I–R*) curve of the 1T1R memory cell with the resistance as a function of the current under different pulse amplitude for the RESET operation. When the pulse amplitude is less than 0.5 mA, the resistance is unchanged. While, as the pulse amplitude is larger than 0.5 mA, the memory cell changes to RESET state and its resistance is over 100 kΩ. With the pulse amplitude increasing further, the resistance is almost unchanged. Figure 3 shows the time–resistance (*T–R*) curve for the memory cell with the resistance as a function of the pulse width for the RESET operation. When the RESET current width is 10 ns, the memory cell is reset and its resistance maintains the same as the pulse width increases from 10 to 200 ns.

Figure 4 shows the *I–R* curve for the 1T1R memory cell with the resistance as a function of the current under different pulse amplitude for SET operation. When the current pulse amplitude is 0.2 mA, the resistance decreases. With the current pulse increasing to 0.4 mA, the resistance is almost unchanged. While, as the pulse amplitude is over 0.5 mA, the memory cell resistance increases from the low state to the high one. Figure 5 shows the curve of the SET width via resistance for the memory cell. It can be seen that the memory cell is set and the resistance is almost unchanged with the pulse width increasing to 2,000 ns when the set current width is 100 ns. Compared with the cell in Ref. [13], the set speed of the present device is low due to the influence of the parasitic parameters in the periphery circuits.

The resistance value distribution of the experimental chip is shown in Fig. 6. The logarithm of the initial

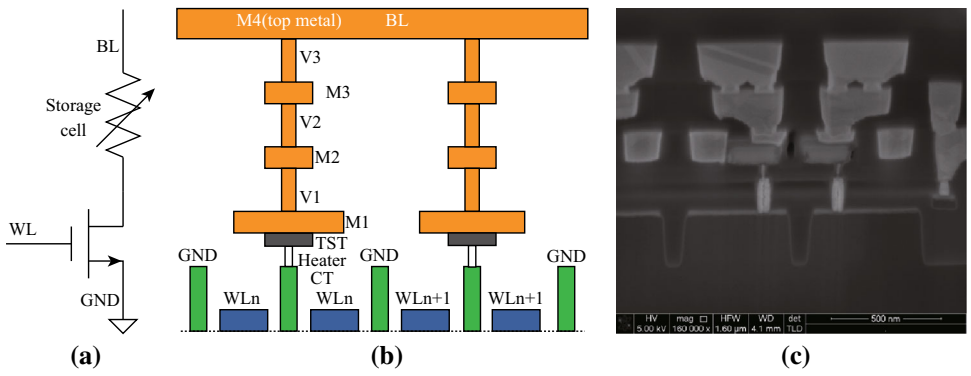

Fig. 1 **a** Schematic of the 1T1R structure memory cell. **b** Schematic cross section of the 1T1R structure. **c** SEM image of a detail of the array along the WL direction

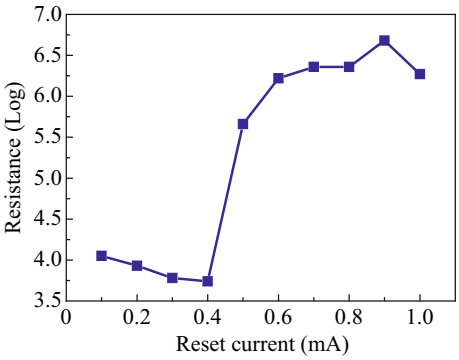

Fig. 2 *I–R* curve of the RESET operation for the 1T1R memory cell

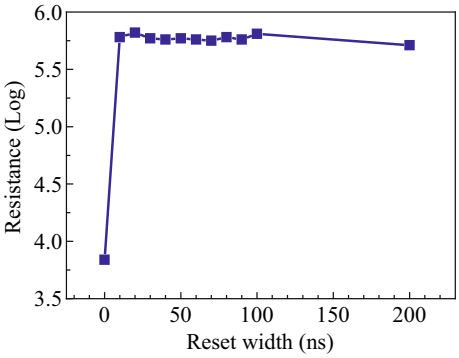

Fig. 3 *T–R* curve of the RESET operation for the 1T1R memory cell

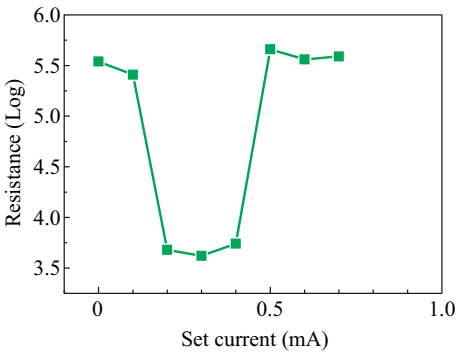

Fig. 4 *I–R* curve of the SET operation for the 1T1R memory cell

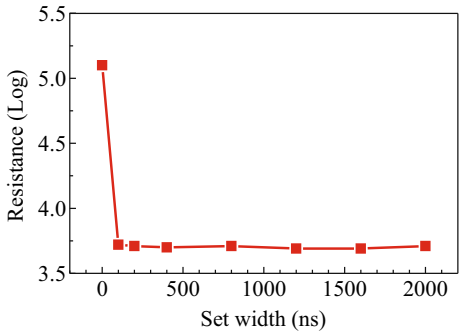

Fig. 5 *T–R* curve the SET operation for the 1T1R memory cell

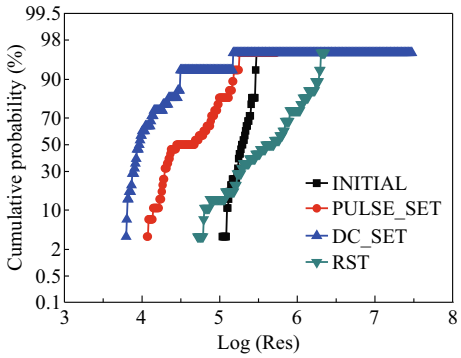

Fig. 6 Resistance value distribution for the experimental chip

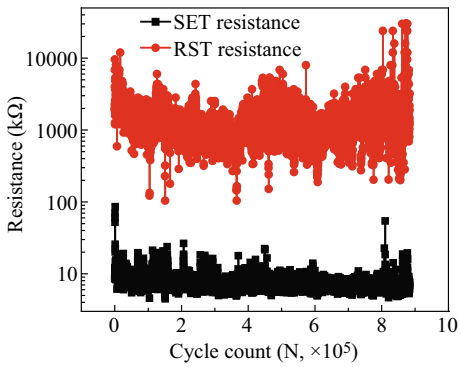

Fig. 7 Reset/set endurance value for the memory cell

resistance is between 5 and 5.5. SET and RESET resistances were obtained by applying a programing current pulse. The logarithm of the SET resistance is between 3.7 and 4.5, whereas, they are between 4.7 and 6.3 for RESET one. The minimal RESET/SET resistance ratio is more than 1 order of magnitude.

A write endurance test was performed by repeating the alternate writing of operation RESET and SET until the write operation failed. The pulses for RESET and SET operations are 0.5 mA $(10\ \text{ns})^{-1}$ and 0.2 mA $(100\ \text{ns})^{-1}$, respectively. As shown in Fig. 7, the results indicate that the RESET/SET endurance is about 10^6 cycles. Since the typical endurance parameter for Flash and some PCRAMs is about 10^6 cycles [21], it can be confirmed that the endurance of the present PCRAM can meet the embedded system applications.

It was also noticed that the present TST device is faster than that of the GST based on 42-nm technology [16]. This may be considered that the Ti-centered atomic motifs play the role of pinning the local structures in both *a*- and *c*-SbTe phases, in which they act as nucleation centers during the phase transition. This will avoid substantial atomic

rearrangement, and in turn facilitate faster- and lower-energy phase transitions [13]. But the operation current of the present TST device is greater than that of the GST device mentioned in Ref. [16]. So it is essential to further optimize the Ti–Sb–Te composition and the device structure to decrease the operation current.

4 Conclusion

A PCRAM experimental chip was fabricated using 40-nm CMOS technology, in which the TST phase change alloy material was integrated by the standard process to form the storage medium due to its low power and fast speed. The pulses for RESET and SET operations are 0.5 mA $(10\ \text{ns})^{-1}$ and 0.2 mA $(100\ \text{ns})^{-1}$, respectively. The SET and RESET resistance distributions were obtained by applying a programing current pulse, and the minimal RESET/SET ratio is more than 1 order of magnitude. The RESET/SET endurance is about 10^6 cycles. This high speed performance achieved in this chip expects to have advantages in many embedded applications.

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