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Roadmap to Gigahertz Organic Transistors

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Despite the large body of research conducted on organic transistors, the transit frequency of organic field-effect transistors has seen virtually no improvement for a decade and remains far below 1 GHz. One reason is that most of the research is still focused on improving the charge-carrier mobility, a parameter that has little influence on the transit frequency of short-channel transistors. By examining the fundamental equations for the transit frequency of field-effect transistors and by extrapolating recent progress on the relevant device parameters, a roadmap to gigahertz organic transistors is derived.

1. Introduction

Thin-film transistors (TFTs) are field-effect transistors manufactured by the sequential deposition of the various device components (e.g., semiconductor, gate dielectric, gate electrode, and source and drain contacts) from the vapor or liquid phase onto a substrate in the form of thin layers.[1] This approach distinguishes TFTs from silicon metal-oxide–semiconductor field-effect transistors (MOSFETs), which require single-crystalline wafers serving as both the substrate and the semiconductor. TFTs, in contrast, can be fabricated directly on a wide range of inexpensive, transparent, flexible, stretchable, biodegradable, and/or biocompatible substrates, such as glass, plastics, paper, metal foils, and textiles, to name just a few. A wide range of semiconductors have been employed for the fabrication of TFTs, most notably metal chalcogenides,[2,3] hydrogenated amorphous silicon (a-Si:H),[4,5] polycrystalline silicon,[6–8] low-temperature polycrystalline silicon (LTPS) produced by excimer laser annealing (ELA),[9,10] metal nitrides,[11] metal-halide perovskites,[12] metal oxides,[13–15] carbon nanotubes,[16] and single-crystalline silicon.[17]

TFTs have found widespread commercial use for the implementation of the pixel circuits in active-matrix displays and large-area image detectors. For example, LTPS TFTs are currently used in 100% of all commercially manufactured active-matrix organic light-emitting diode (AMOLED) displays (600 million in 2018, mostly for smartphones) and in close to 40% of all commercially manufactured liquid-crystal displays (AMLCDs; 2 billion in total in 2018). Hydrogenated amorphous silicon TFTs are used in about 60% of all AMLCDs and in a significant share of large-area X-ray flat-panel detectors for medical, security, and nondestructive-testing applications. InGaZnO TFTs are found in about 2% of AMLCDs and in an increasing share of image detectors.

An important TFT-performance parameter is the transit frequency, which is the highest frequency at which the transistor can be operated. Depending on the panel resolution and the frame rate, the pixel-circuit TFTs need to have transit frequencies of a few megahertz to a few tens of megahertz. If the TFTs are also used for integrated row and column drivers,[18] an even higher transit frequency is required. In general, higher transit frequencies enable a wider range of applications and higher-quality products. Transit frequencies above 1 GHz have been reported for TFTs based on several different semiconductors.[19–22]

Organic TFTs, fabricated using either conjugated polymers or small-molecule semiconductors, are being developed as alternatives to the above-mentioned, mostly, inorganic TFTs. An attractive feature of organic TFTs is that both p-channel and n-channel TFTs can be fabricated at relatively low process temperatures, usually at or near room temperature.[23] However, despite more than three decades of intense research, the highest reported transit frequencies of organic TFTs are still well below 1 GHz. The aim of this Progress Report is to develop a roadmap to gigahertz organic TFTs.

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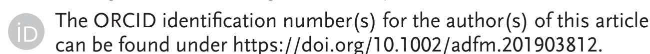
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2. Results and Discussion

The transit frequency of a field-effect transistor is defined as follows

$$f_T = f\left(\frac{|i_D|}{|i_G|} = 1\right) = \frac{g_m}{2\pi C_G} \tag{1}$$

where i_D is the small-signal drain current (which can be written as $i_D = g_m \cdot v_{GS}$, with g_m being the small-signal transconductance and v_{GS} the small-signal gate–source voltage), i_G is the small-signal gate current (which can be written as $i_G = j \cdot 2\pi f \cdot C_G \cdot v_{GS}$, with j being the imaginary unit and f the frequency), and C_G is the gate capacitance. By approximating the gate capacitance C_G as the sum of the geometric gate-to-channel and gate-to-contact capacitances, by assuming that the intrinsic and parasitic capacitances have the same unit-area capacitance, and by calculating the transconductance as $g_m = \partial I_D / \partial V_{GS}$ either for the linear regime (where $V_{DS} < V_{GS} - V_{th}$, with V_{DS} being the large-signal drain–source voltage, V_{GS} the large-signal gate–source voltage, and V_{th} the threshold voltage) or for the saturation regime ($V_{DS} > V_{GS} - V_{th}$), Equation (1) can be written as

$$f_T = \frac{\mu_{eff} V_{DS}}{2\pi L (L + L_{ov,GS} + L_{ov,GD})} \quad (\text{linear regime}, V_{DS} < V_{GS} - V_{th}) \tag{2}$$

$$f_T = \frac{\mu_{eff} (V_{GS} - V_{th})}{2\pi L (L + L_{ov,GS} + L_{ov,GD})} \quad (\text{saturation regime}, V_{DS} > V_{GS} - V_{th}) \tag{3}$$

where μ_{eff} is the effective carrier mobility, L is the channel length, $L_{ov,GS}$ is the parasitic gate-to-source overlap, and $L_{ov,GD}$ is the parasitic gate-to-drain overlap.

Equations (2) and (3) indicate that the transit frequency increases with increasing gate–source and drain–source voltages, which implies that all field-effect transistors can, in principle, reach a transit frequency of 1 GHz, provided dielectric breakdown and self-heating[24] upon application of sufficiently high voltages are avoided. This renders the transit frequency a somewhat meaningless parameter for benchmarking purposes. Instead of the absolute frequency, **Figure 1** therefore shows how the supply-voltage-normalized transit frequency of organic TFTs has been improved over the years, from 2.5 kHz at 20 V in 1995 to 20 MHz at 10 V and 6.7 MHz at 3 V in 2018.[25,36,37] (Note that some of the results in Figure 1 were obtained not by measuring the transit frequency f_T of an individual transistor, but by calculating an equivalent frequency $f_{eq} = 1/(2 \cdot \tau_{stage})$ from a ring oscillator's stage delay τ_{stage}, where the ratio f_{eq}/f_T is usually near 0.5.[40] Also note that the proportionality between f_T and V_{DS} in Equation (2) is observed only in the limit of zero contact resistance, as will be elaborated later.)

The historic development seen in Figure 1 has come through improvements in virtually every aspect of the materials and technology of organic TFTs. As a result of these combined efforts, the voltage-normalized frequency increased by about an order of magnitude every 4 years between 1995 and 2011. But once the low-hanging fruits had been picked, the pace slowed to about a factor of 5 per decade. At this pace, it will take another 20 to 30 years for organic TFTs to reach a frequency of 1 GHz at 3 V, which is the nominal cell voltage of lithium-ion batteries and, thus, the maximum supply voltage in most of the

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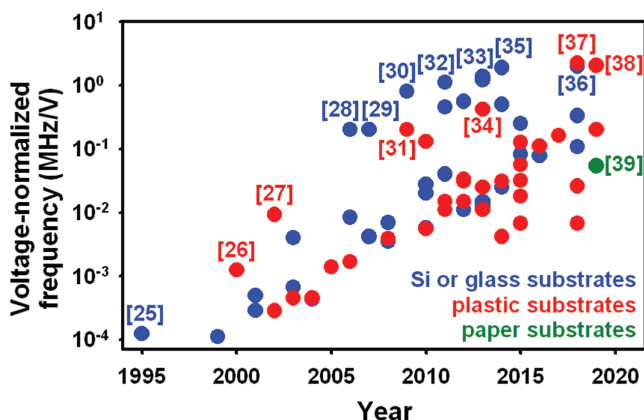

Figure 1. Historic development of the transit frequency f_T normalized to either the gate–source voltage or the drain–source voltage (whichever is larger) of organic thin-film field-effect transistors reported in the literature. In case the data were obtained from measurements on ring oscillators, the equivalent frequency $f_{eq} = 1/(2 \cdot \tau_{stage})$ normalized to the supply voltage is shown.

mobile or wearable electronic systems for which organic TFTs are primarily being developed.

So what can be done in order to reach the goal of gigahertz organic TFTs sooner than that? In **Figure 2**, solutions to Equation (2) are plotted for a drain–source voltage of 3 V and for various effective carrier mobilities (μ_{eff}), channel lengths (L), and gate-to-contact overlaps ($L_{ov} = L_{ov,GS} = L_{ov,GD}$). Figure 2 indicates that a transit frequency of 1 GHz at 3 V is realistic only if the channel length and the gate-to-contact overlaps are smaller than 1 µm.

At such small channel lengths, the TFT performance is determined greatly by the contact resistance. This is evident from the following equations for the effective carrier mobility μ_{eff} and the transit frequency f_T, derived here for the linear regime of operation[41–43]

$$\mu_{eff} = \frac{\mu_0}{1 + \frac{\mu_0}{L} R_C W C_{diel} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right)} \tag{4}$$

$$f_T = \frac{\mu_0}{1 + \frac{\mu_0}{L} R_C W C_{diel} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right)} \frac{V_{DS}}{2\pi L \left(L + L_{ov,GS} + L_{ov,GD} \right)} \tag{5}$$

where R_C is the contact resistance (defined here as the sum of the source resistance and the drain resistance, i.e., $R_C = R_S + R_D$, and assumed to be Ohmic, i.e., independent of the voltage drop across the contacts), μ_0 is the intrinsic channel mobility (i.e., the carrier mobility in the absence of any contact resistance), W is the channel width, and C_{diel} is the gate-dielectric capacitance per unit area. Solutions to Equation (5) are plotted in **Figure 3**. The term $C_{diel}(V_{GS} - V_{th} - V_{DS}/2)$ was set to 10^{-6} A s cm^{-2}, which is a typical value for the gate-induced charge-carrier density in transistors with conventional (as opposed to electrolyte-based) gate insulators.

Figure 3 shows that at the channel lengths required for gigahertz organic TFTs, the transistor performance is essentially unaffected by the intrinsic channel mobility and is instead determined almost entirely by the contact resistance, which will need to be in the range of about 1–10 Ω cm. The roadmap to gigahertz organic TFTs is therefore essentially a roadmap to a contact resistance of about 1–10 Ω cm in sub-micrometer organic TFTs.

When TFTs are fabricated in the staggered device architecture, the contact resistance is determined mainly by the height and the width of the energy barrier at the contact–semiconductor interface, by the gate-to-source and gate-to-drain overlaps, and by the thickness and the conductivity of the semiconductor layer.[44–48] Using area-selective contact doping and a very small semiconductor thickness of 7 nm, Yamamura et al.[36]

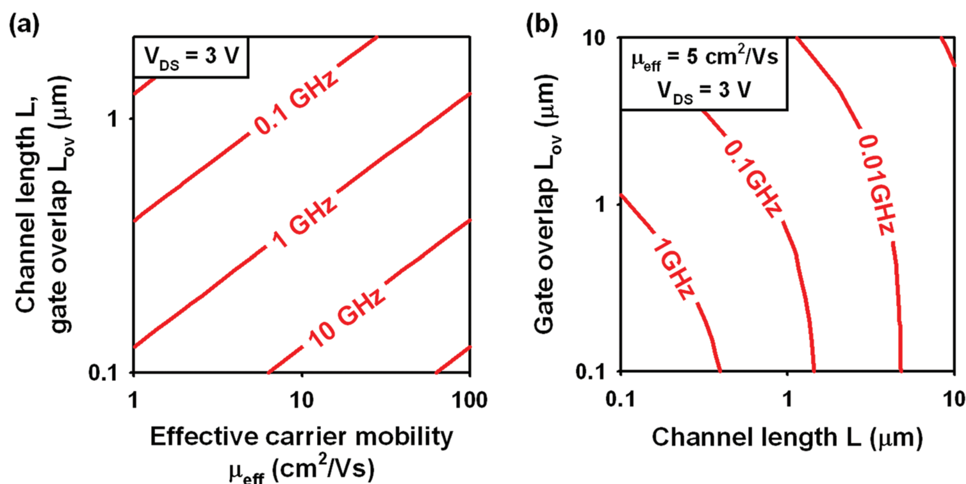

Figure 2. a) Contour plot showing the transit frequency (f_T) calculated using Equation (2) for a drain–source voltage (V_{DS}) of 3 V, effective carrier mobilities (μ_{eff}) ranging from 1 to 100 cm^2 V^{-1} s^{-1} and channel lengths ranging from 0.1 to 2 µm. The channel length, the gate-to-source overlap, and the gate-to-drain overlap are assumed to be identical ($L = L_{ov} = L_{ov,GS} = L_{ov,GD}$). b) Contour plot showing the transit frequency (f_T) calculated using Equation (2) for a drain–source voltage of 3 V, an effective carrier mobility of 5 cm^2 V^{-1} s^{-1} and channel lengths and gate-to-contact overlaps ranging from 0.1 to 10 µm. As can be seen, a transit frequency of 1 GHz at usefully small supply voltages (3 V) will require sub-micrometer channel lengths and gate-to-contact overlaps.

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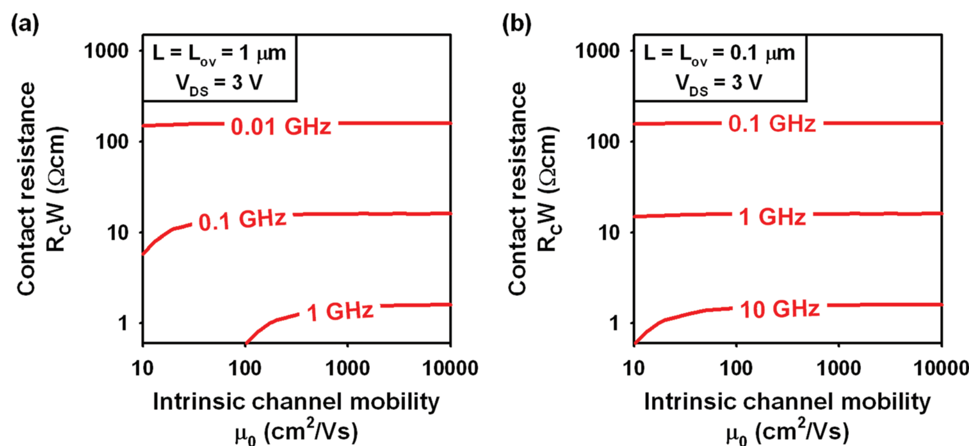

Figure 3. Contour plots showing the transit frequency (f_T) calculated using Equation (5) for a drain–source voltage (V_{DS}) of 3 V, intrinsic channel mobilities (μ_0) ranging from 10 to 10 000 cm^2 V^{-1} s^{-1} and width-normalized contact resistances ($R_C W$) ranging from 1 Ω cm to 1 kΩ cm. The channel length, the gate-to-source overlap, and the gate-to-drain overlap are assumed to be identical ($L = L_{ov} = L_{ov,GS} = L_{ov,GD}$). Calculations were performed for a) $L = L_{ov} =$ 1 µm and b) $L = L_{ov} = 0.1$ µm. The term $C_{diel}(V_{GS} - V_{th} - V_{DS}/2)$ was set to 10^{-6} A s cm^{-2}. As can be seen, the transit frequency is essentially unaffected by the intrinsic channel mobility. In addition to sub-micrometer dimensions, gigahertz organic TFTs will require a contact resistance of ≈1–10 Ω cm.

recently achieved a contact resistance of 46 Ω cm in inverted staggered (bottom-gate, top-contact) organic TFTs, a record for organic TFTs at the time of publication, aside from the electrochemically doped polymer TFTs reported by Braga et al.[49] For TFTs with a channel length of 3 µm and gate-to-source and gate-to-drain overlaps of 2.25 µm, this resulted in a transit frequency of 20 MHz at 10 V, or a voltage-normalized transit frequency of 2 MHz V^{-1}, also a record for organic TFTs at the time of publication. (Note that Yamamura et al. give the sum of the gate-to-source and gate-to-drain overlaps, $L_{ov,GS} + L_{ov,GD} = 4.5$ µm.)

It is difficult to predict to what extent it will be possible to reduce the contact resistance further in this device architecture. On the one hand, while Yamamura et al. showed that reducing the semiconductor thickness from two monolayers to one monolayer is detrimental to the lateral charge-carrier transport, a reduction of the semiconductor thickness to about 5 or 6 nm might nonetheless be possible by using a shorter molecule than the one employed by Yamamura et al., provided it lends itself equally well to the coating process. On the other hand, there is no guarantee that this will lead to a further reduction of the contact resistance, considering how small it already is (46 Ω cm). Also, as discussed previously, a transit frequency of 1 GHz at 10 V will likely require gate-to-source and gate-to-drain overlaps below 1 µm, and for the parameters in ref. [36], this would make the overlaps smaller than the transfer length (which, according to Figure 3c in ref. [36], is slightly greater than 1 µm), which might result in a larger contact resistance. This makes it difficult to predict how much further the contact resistance can be reduced. In **Figure 4**a, we therefore show solutions to Equation (5) for a contact resistance of 46 Ω cm and for gate overlaps of 2.25 µm (as in ref. [36]) and 1 µm (assuming that a contact resistance of 46 Ω cm can be maintained for this overlap). As can be seen, transit frequencies approaching 1 GHz at 10 V are possible under these assumptions by reducing the channel length to about 0.1 µm.

For organic TFTs fabricated in the coplanar architecture, the situation is completely different. Since the contact–semiconductor interface in coplanar TFTs is permanently shielded from the gate field, proper management of the energy barrier at this interface, e.g., by chemical modification, is probably even more important than in staggered organic TFTs (where this interface is shielded from the gate field only in the presence of a carrier channel). In bottom-gate coplanar TFTs, an additional requirement is that the semiconductor must form a continuous layer with adequate microstructure along the raised contact edges and on the surface of the contacts.[50] Both of these issues can be addressed by functionalizing the contact surface with a monolayer of molecules that induce a favorable semiconductor morphology across the contact edges[51] and which have either a large density of electronegative substituents[52,53] or a large dipole moment[54] to tune the interface energy barrier.

Under these provisions, the coplanar architecture may provide a number of benefits. First of all, the contact resistance in coplanar TFTs is independent of the length of the gate-to-source and gate-to-drain overlaps (as long as these overlaps exist and assuming that the contacts extend sufficiently far outside of the area of the gate electrode), which means that the parasitic capacitances can be decreased (and ideally eliminated by self-alignment of the source and drain contacts with respect to the gate electrode) without negatively affecting the contact resistance. Second, the contact resistance is independent of the thickness of the semiconductor layer, which is beneficial whenever precise control of this thickness is difficult, as in the case of vacuum-deposited small-molecule semiconductors. Third, the contact resistance in coplanar TFTs depends strongly on the thickness of the gate dielectric[55] and can thus, in principle, be reduced in a direct and systematic manner. For coplanar organic TFTs with a gate-dielectric thickness of 5.3 nm, a contact resistance of 30 Ω cm was recently reported,[56] resulting in an equivalent frequency of 3.5 MHz at 1.6 V (2.2 MHz V^{-1}) in ring oscillators based on TFTs with a channel length of 1 µm and gate overlaps of 2 µm,[37] and a transit frequency of 10.4 MHz at 3 V (3.5 MHz V^{-1}) obtained from *S*-parameter measurements on TFTs with a channel length of 0.85 µm and gate overlaps of 5 µm (see **Figure 5**). These TFTs were fabricated by stencil lithography,[57] which has a resolution limit of

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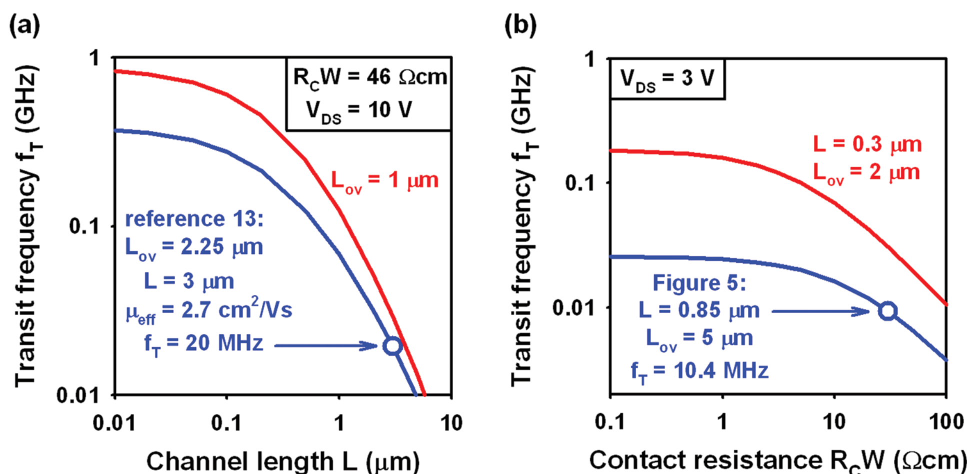

Figure 4. a) Transit frequency (f_T) calculated using Equation (5) and plotted as a function of the channel length (L) for the parameters of the inverted staggered TFTs in ref. [36] ($R_CW = 46\ \Omega$ cm, $C_{diel} = 60$ nF cm^{-2}, $V_{GS} = V_{DS} = 10$ V, $V_{th} = 2$ V). The blue curve was calculated for $L_{ov} = 2.25$ µm, as reported in ref. [36], and the red curve for $L_{ov} = 1$ µm. The intrinsic channel mobility (μ_0) was set to 3 cm^2 V^{-1} s^{-1}, as this is the value for which Equation (4) yields an effective mobility of 2.7 cm^2 V^{-1} s^{-1} for $L = 3$ µm, as reported in ref. [36]. (For TFTs fabricated on silicon substrates, ref. [36] gives an intrinsic channel mobility greater than 10 cm^2 V^{-1} s^{-1}, but the TFTs considered here were fabricated on glass.) As can be seen, a transit frequency close to 1 GHz at 10 V is possible in staggered organic TFTs by reducing the channel length to about 0.1 µm and the gate-to-contact overlaps to about 1 µm. b) Transit frequency calculated using Equation (5) and plotted as a function of the width-normalized contact resistance for the parameters of the inverted coplanar TFTs fabricated by stencil lithography shown in Figure 5 ($\mu_0 = 5$ cm^2 V^{-1} s^{-1}, $C_{diel} = 700$ nF cm^{-2}, $V_{GS} = V_{DS} = 3$ V, $V_{th} = 1$ V). The blue curve was calculated for $L = 0.85$ µm and $L_{ov} = 5$ µm, as in Figure 5, and the red curve for $L = 0.3$ µm and $L_{ov} = 2$ µm, which is approximately the resolution limit of stencil lithography. As can be seen, the maximum transit frequency achievable using stencil lithography is about 100 MHz at 3 V.

≈0.3 µm for the channel length[58] and ≈2 µm for the gate-to-source and gate-to-drain overlaps.[59] Figure 4b shows the transit frequency at a drain–source voltage of 3 V calculated using Equation (5) and plotted as a function of the width-normalized contact resistance for the dimensions of the TFT in Figure 5 ($L = 0.85$ µm, $L_{ov} = 5$ µm) and for the minimum dimensions achievable by stencil lithography[58,59] ($L = 0.3$ µm, $L_{ov} = 2$ µm). Figure 4b indicates that the highest transit frequency that can realistically be expected for organic TFTs fabricated by stencil lithography is ≈30 MHz at 3 V for a contact resistance of 30 Ω cm and ≈100 MHz at 3 V in the event that the contact resistance can be reduced to about 5 Ω cm, e.g., by functionalizing the contact surfaces with better-performing molecules[52–54] or by reducing the gate-dielectric thickness.[55]

Figure 4 shows that transit frequencies beyond 30 MHz V^{-1} will likely require channel lengths and gate-to-contact overlaps well below 1 µm. As a higher-resolution alternative to stencil lithography, we have therefore used electron-beam lithography and fabricated organic TFTs with channel lengths and gate-to-contact overlaps of 200 nm, as shown in **Figure 6**. Unfortunately, the contact resistance of these TFTs is about 800 Ω cm, i.e., more than an order of magnitude larger than the contact resistance of the stencil-patterned TFTs (30 Ω cm). This could be due to contamination of the contact surfaces during the lift-off process or a less favorable microstructure of the organic semiconductor across the edges of the contacts when these are patterned by electron-beam lithography, rather than stencil lithography. As a result of the larger contact resistance, the width-normalized transconductance is more than an order of magnitude smaller than that of the stencil-patterned TFTs in ref. [37] and Figure 5, and the transit frequency estimated using Equation (5) is about 9 MHz at 1 V. In other words, the benefit of the smaller critical dimensions is partially lost due to the larger contact resistance.

In order to put the results from Figures 4b and 6 into perspective, the transit frequency calculated using Equation (5) for a drain–source voltage of 3 V is plotted in **Figure 7**a as a function of the critical dimensions and the width-normalized contact resistance. The channel length, the gate-to-source overlap, and the gate-to-drain overlap are assumed to be identical ($L = L_{ov} = L_{ov,GS} = L_{ov,GD}$). Three scenarios are highlighted in Figure 7a. The blue symbol represents the parameters of the TFTs fabricated by stencil lithography shown in Figure 5 (critical dimensions on the order of 2 µm and a contact resistance of 30 Ω cm), the green symbol represents the parameters of the TFT fabricated by electron-beam lithography shown in Figure 6 (critical dimensions of 200 nm and a contact resistance of 800 Ω cm), and the red symbol represents a hypothetical TFT that combines critical dimensions of 200 nm with a contact resistance of 30 Ω cm. Figure 7b illustrates the dependence of the transit frequency on the drain–source voltage for various values of the contact resistance.

According to Figure 7, a TFT with the same contact resistance as the TFTs fabricated by stencil lithography shown in Figure 5 ($R_CW = 30\ \Omega$ cm) and with the same critical dimensions as the TFT fabricated by electron-beam lithography shown in Figure 6 ($L = L_{ov,GS} = L_{ov,GD} = 200$ nm) would have a transit frequency of 190 MHz at 1 V and 230 MHz at 3 V (red symbols in Figure 7). A transit frequency of 1 GHz at these voltages will require a further reduction of the contact resistance below about 10 Ω cm and a further reduction of the channel length and the gate-to-contact overlaps below about 200 nm.

The fundamental scaling laws developed for silicon MOSFETs in the 1970s[60,61] dictate that the ratio between the channel

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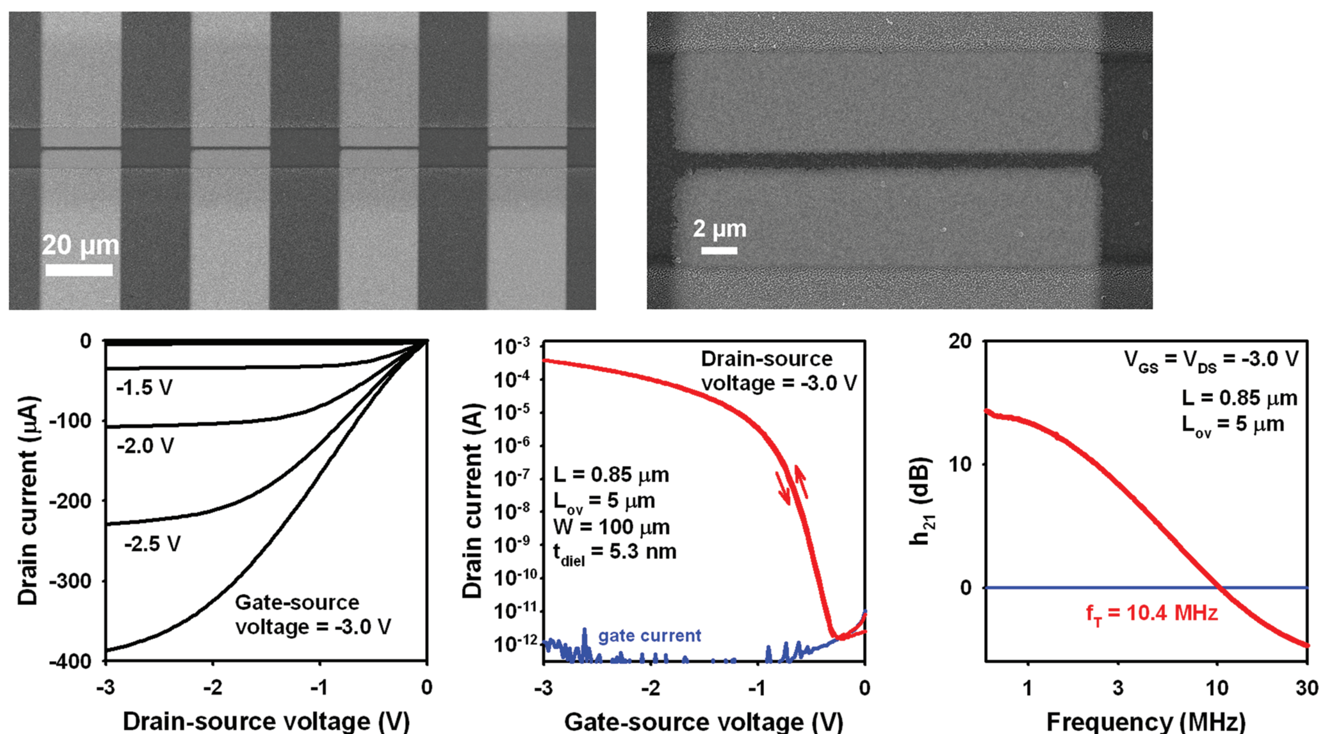

Figure 5. Microscopy images and static and dynamic characteristics of an inverted coplanar TFT with a channel length of 0.85 µm and gate-to-source and gate-to-drain overlaps of 5 µm fabricated on a flexible polyethylene naphthalate (PEN) substrate by stencil lithography using the vacuum-deposited small-molecule semiconductor 2,9-diphenyl-dinaphtho[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DPh-DNTT) and a gate dielectric based on oxygen-plasma-grown aluminum oxide and an alkylphosphonic acid self-assembled monolayer with a total thickness of 5.3 nm and a capacitance of 700 nF cm^{-2}.[37,56] The TFT has a contact resistance of 30 Ω cm (extracted from transmission-line measurements performed on the same substrate), a width-normalized transconductance of 3 S m^{-1}, a subthreshold slope of 70 mV decade^{-1}, an on/off current ratio of 10^8, and a transit frequency of 10.4 MHz determined from *S*-parameter measurements[33] performed at gate–source and drain–source voltages of −3 V.

length and the gate-dielectric thickness of a field-effect transistor should be no smaller than about 50, in order to ensure that the electric potential in the semiconductor is controlled by the transverse electric field, rather than the lateral electric field. This implies a maximum gate-dielectric thickness of 20 nm for a channel length of 1 µm and a thickness of 2 nm for a channel length of 100 nm. These are the values derived under the assumption that the permittivities of the semiconductor and the gate dielectric are similar. The use of a gate dielectric with a larger permittivity will alleviate the dielectric-thickness requirement. For example, silicon MOSFETs, where high-permittivity gate oxides have been in use since 2007, are currently (10 and 7 nm nodes) manufactured with a channel length of 15–20 nm, and a gate dielectric consisting of SiO_2 with a thickness of 0.5–0.8 nm (grown by thermal oxidation) and HfO_2 with a thickness of 1–1.5 nm (deposited by atomic layer deposition).[62] The concept of a double-layer gate dielectric that combines a high-permittivity dielectric (with a thickness just sufficient to suppress quantum-mechanical tunneling) and a thin layer of a low-permittivity dielectric (to shield the semiconductor from the undesirable polarization effects of the high-permittivity dielectric[63–65]) is, in principle, also applicable to organic TFTs, although the choice of the materials, especially for the low-permittivity dielectric interfacing the organic semiconductor, will likely be different.[66–71] Nevertheless, the total physical thickness of such a double-layer gate dielectric will need to be no greater than about 5 nm for a channel length of 100 nm. The main concern with such thin gate dielectrics is the magnitude of the gate current. However, given the necessarily small size of high-frequency TFTs, this is unlikely to be a serious issue. For example, for a channel length and gate-to-contact overlaps of 100 nm, and a channel width of 3 µm, the effective gate area is only 10^{-8} cm^2, so even if the gate-current density was 1 A cm^{-2}, the absolute gate current would not exceed 10^{-8} A. Gate dielectrics with a thickness of about 5 nm and a gate-leakage current density below 10^{-5} A cm^{-2} have already been used in the fabrication of organic TFTs,[72] and from these values, a gate current of less than 10^{-13} A is projected for an effective gate area of 10^{-8} cm^2 (see also Figure 6). As long as the gate dielectric has a sufficiently small defect density and its thickness is above the value at which leakage currents due to quantum-mechanical tunneling become an issue, the gate dielectric is not expected to pose insurmountable challenges.

3. Conclusions

1) Gigahertz organic TFTs will require channel lengths and gate-to-contact overlaps well below 1 µm. At these channel lengths, the transit frequency is essentially unaffected by the charge-carrier mobility and is instead determined mainly by the contact resistance, which will need to be smaller than ≈10 Ω cm.

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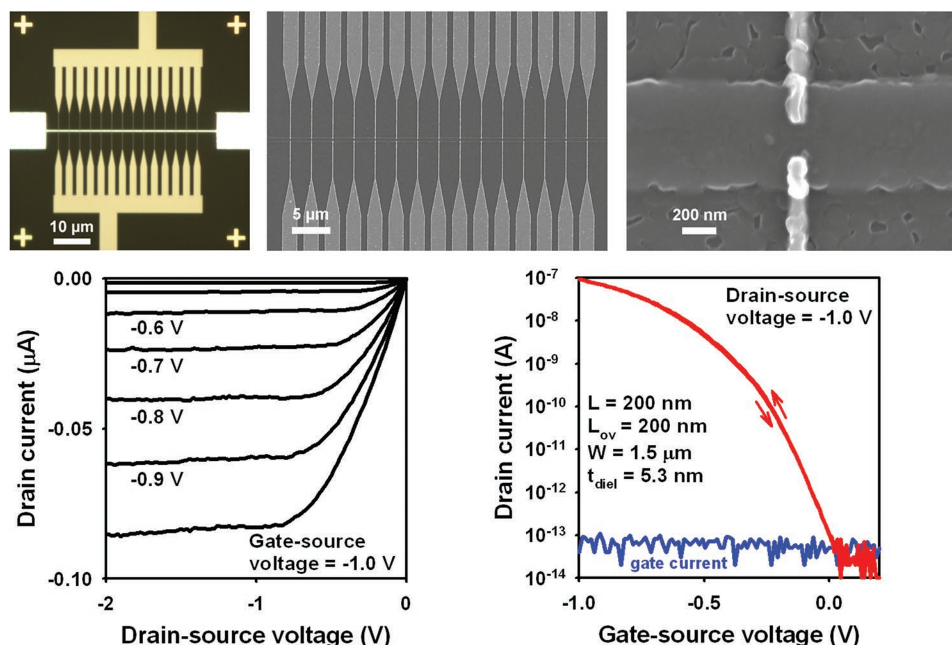

Figure 6. Microscopy images and measured current–voltage characteristics of an inverted coplanar TFT with a channel length, and gate-to-source and gate-to-drain overlaps of 200 nm fabricated on a glass substrate by electron-beam lithography using the vacuum-deposited small-molecule semiconductor dinaphtho[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT) and a gate dielectric based on oxygen-plasma-grown aluminum oxide and an alkylphosphonic acid self-assembled monolayer with a total thickness of 5.3 nm and a capacitance of 700 nF cm^{-2}. The TFT has a contact resistance of about 800 Ω cm (estimated from the linear region of the output curve at $V_{GS} = -1$ V), a width-normalized transconductance of 0.2 S m^{-1}, an intrinsic gain of about 300, a subthreshold slope of 72 mV decade^{-1}, and an on/off current ratio of 3×10^6.

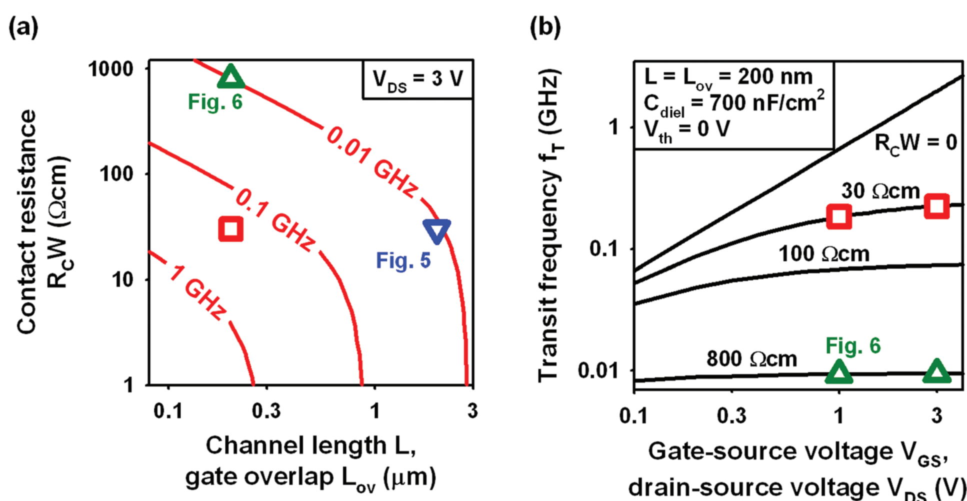

Figure 7. a) Contour plot showing the transit frequency (f_T) calculated using Equation (5) for an intrinsic channel mobility (μ_0) of 5 cm^2 V^{-1} s^{-1} and a drain–source voltage (V_{DS}) of 3 V. The channel length, the gate-to-source overlap, and the gate-to-drain overlap are assumed to be identical ($L = L_{ov} = L_{ov,GS} = L_{ov,GD}$). The term $C_{diel}(V_{GS} - V_{th} - V_{DS}/2)$ was set to 10^{-6} A s cm^{-2}. The blue symbol represents the TFT fabricated by stencil lithography shown in Figure 5. (The true dimensions of the TFT in Figure 5 are $L = 0.85$ µm, $L_{ov} = 5$ µm; for the purpose of the graph shown here, this has been approximated as $L = L_{ov} = 2$ µm. The width-normalized contact resistance is 30 Ω cm.) The green symbol represents the TFT fabricated by electron-beam lithography shown in Figure 6 ($L = L_{ov} = 200$ nm, $R_CW = 800$ Ω cm; calculated here for $V_{GS} = V_{DS} = 3$ V, instead of 1 V), and the red symbol represents a hypothetical TFT combining $L = L_{ov} = 200$ nm and $R_CW = 30$ Ω cm. b) Transit frequency calculated using Equation (5) and plotted as a function of the applied gate–source and drain–source voltages, assuming $V_{GS} = V_{DS}$ and $V_{th} = 0$ V, so that the TFT is always in the linear regime, which is one of the assumptions underlying Equation (5). If the contact resistance is zero, the transit frequency is proportional to the drain–source voltage, consistent with Equation (2). The more strongly the total device resistance is dominated by the contact resistance, the weaker is the dependence of the transit frequency on the drain–source voltage. For the TFT in Figure 6, transit frequencies of 9.3 MHz at 1 V and 9.4 MHz at 3 V are calculated (green symbols). For the hypothetical TFT with $L = L_{ov} = 200$ nm and $R_CW = 30$ Ω cm, the calculated transit frequencies are 190 MHz at 1 V and 230 MHz at 3 V (red symbols).

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2) In the event that the transit frequency is limited not by the ratio between the transconductance and the gate capacitance, but by the saturation of the charge-carrier velocity in the semiconductor ($f_T = v_{sat}/(2\pi L)$),[73] the channel length may have to be even smaller than indicated above. For example, if the carrier velocity were to saturate at 10^5 cm s^{-1}, a transit frequency of 1 GHz might require a channel length below 100 nm.
3) Regarding the question of how to fabricate nanoscale organic TFTs on flexible, large-area substrates with sufficient yield and uniformity in a scalable and cost-effective manner, a number of techniques have been developed over the past few years; one of these is nanoimprint lithography,[74–79] which has been used to demonstrate functional organic TFTs with channel lengths as small as 70 nm and which can be combined with self-alignment techniques to define nanoscale gate-to-contact overlaps.[80,81]

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

contact resistance, nanoscale transistors, organic thin-film transistors

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