HV-CMOS Design and Characterization of a Smart Rotor Coil Driver for Automotive Alternators

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***Abstract*—The work presents a single-chip integrated rotor coil driver (RCD) that can be used in automotive alternators. It integrates the power switch with the control circuitry and the diagnostics; with respect to the state of the art, new functionalities are integrated such as full reverse polarity protection and programmable output slope control against in-rush currents and current spike transients. The paper will discuss the driver IC design from the choice of the architecture to the real silicon implementation. The proposed innovative RCD has been implemented in a 0.35 μm HV-CMOS technology and has been embedded in a mechatronic brush-holder regulator system-on-chip for an automotive alternator. The simulation results and experimental measurements prove the effectiveness of the proposed RCD facing the harshest automotive conditions.**

***Index Terms*—Alternator regulator, automotive electronics, high voltage (HV) integrated circuits (ICs), smart driver ICs.**

I. Introduction

THE continuous evolution of microelectronic circuits for harsh environments [1]–[4], integrating on the same chip HV devices for power management or actuator driving and low-power circuits for signal processing and communication [5]–[8], allows improving the performance of automotive mechatronic systems for safety, driver assistance, vehicle dynamic control, engine, and power transmission management [9]–[13].

The research on vehicle electronic control units (ECU) is mainly focused on the reduction of fuel consumption, which requires improving the efficiency of all car's subsystems. A major contribution is related to the alternator, which transforms the mechanical power, picked up on the engine, in electrical power delivered to the battery and to the electrical loads of the car [13]–[19]. The alternator power machine consists of the rotor and stator coils, which generate an alternating voltage, and the rectifier diode bridge, whose output is the dc voltage for battery and loads, see Fig. 1. The rotor coil, belt driven by the pulley and rotating with the engine, generates a magnetic field that is induced in the three phase stator. Regulated alternators operate modulating the field current in the rotor coil, EXC output in Fig. 1, to maintain an ad hoc voltage at the output of the rectifier bridge, V_{BAT} in Fig. 1. New mixed-signal architectures for the regulator IC of next generation vehicles have been recently proposed in [19]–[21]. They feature a power excitation block, driving the rotor coil, interfaced to a low-power processing core including: 1) a phase block, measuring the amplitude and frequency of two stator phases (PH1, PH2 in Fig. 1), 2) a battery block, measuring the status of the battery voltage at node V_{BAT}, 3) an I/O communication block providing a digital serial interface to a master ECU,4) a digital control core implementing the closed-loop regulation algorithm.

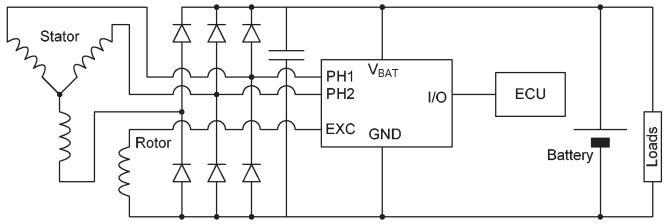

Fig. 1. Regulated alternator block diagram.

The design of the rotor coil current driver (RCD) poses several challenges still to be overcome in state of the art. The RCD for next vehicle generation should not be a simple pulse width modulation (PWM) power switch, but programmable output current slope control functionalities are required against in-rush currents and current spike transients. This way electromagnetic interference and compatibility (EMI/EMC) issues are reduced, and the device reliability is increased. Protection and monitoring circuitry should be integrated in the smart driver; the former to face overcurrent or open/short-circuit or reverse voltage polarity conditions, while the latter is needed for a continuous control of the load response. The RCD block shall be directly interfaced to the digital core of the voltage regulator IC, which receives from the RCD the information on the rotor coil current and, after measuring battery voltage and stator phases, sends to the RCD proper driving commands according to a closed-loop control algorithm. More in details, the digital core sends to the RCD the order to increase or decrease the rotor coil current changing the duty cycle of a PWM excitation signal having a fixed frequency of some hundreds of hertz.

The alternator, which is mounted close to the engine, has to work in one of the most critical and harsh environment that can

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be found in a car [1], [14], [18]–[20]. The RCD shall sustain temperature levels typically closed to 100 °C, but peaks up to 180 °C can be reached. The alternator mechanical moving parts easily generate electrostatic charge, so the RCD must manage very high electrostatic discharge (ESD) level, up to 8 kV, while the industry standard for automotive ASICs is only 4 kV [4] for the most critical devices. To sustain so high ESD levels and other sparkling pulses due to harness coupling, special clamp structures on the regulator pins are necessary.

To have a sufficient voltage to charge the battery, the current that flows on the rotor coil is in the order of some Amps, typically about 3 or 4 A. During cold and cranking condition, the rotor current can even go up to 8 A, and fast current spikes up to 15 A are observed in case of rotor short circuit [19]. During load dump, also voltage peaks of several tens of volts must be sustained while during cold cranking the device has to operate with only about 6 V as battery voltage. Furthermore, to minimize conduction losses on the power switch, the power device should be designed so that the parasitic ON resistance is low, e.g., below 100 mΩ, thus limiting voltage drops to few hundreds of mV. Finally, the RCD has to fulfill the very stringent quality requirements of automotive applications.

To address all the above challenges, this work presents the design, implementation in 0.35 μm HV-CMOS technology and characterization of a novel smart RCD, which can be integrated as hard macrocell in the new generation of alternator regulator systems. Hereafter, Section II reviews state-of-art ICs for alternator coil driving, highlighting the main issues still not solved also in recent published works. Section III details the architecture of the proposed RCD and the main adopted circuit solutions. The layout and chip implementation of the RCD and its characterization through experimental measurements are reported in Section IV. Conclusions are drawn in Section V.

II. Review of State-of-Art Alternator Coil Driver ICs

Alternator coil drivers were mainly realized as simple power switch controlled through a PWM signal. Recently, intelligent power switch (IPS) [1], [20]–[23] for automotive applications have been published, integrating on-chip the power switch device plus circuitry for diagnostic/protection and interfacing to a digital core. However, most of published IPS [1], [22]–[26] cannot sustain the high voltage and/or current requirements of an alternator since they are targeting fine control of loads with lower power levels, such as lamps/LEDs for automotive lighting. A smart driver specific for rotor coil excitation has been proposed in the second half of 2011 [20], integrated in an alternator regulator. The IC in [20] sustains dc battery voltage of 27 V and peak voltage of 40 V, excitation current of 5 A at maximum temperature (150 °C), ESD of several kV. Protection and monitoring mechanisms are integrated on-chip. Also, the alternator voltage regulator circuit in [20] integrates a rotor coil driver with characteristics similar to [21].

However, two main limits are still to be overcome in the state of the art; they will be addressed, together with all the other issues highlighted in Section I, by the RCD design in Sections III and IV.

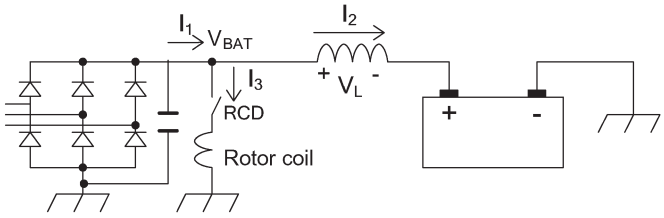

Fig. 2. Connection of alternator output, battery, and rotor coil with its driver.

First, in [20] reverse polarity protection is limited to −2.4 V transients of few seconds. The battery voltage is positive during the typical life of the alternator, but can happen that the battery is mounted at reverse during car service. In this case, a lot of current shall flow through the diodes in the rectifier bridge and through the driver IC. The current in the rectifier bridge cannot damage the alternator, because they are designed to carry that very high current, but the current that flows in the driver IC can damage it and make the alternator unusable. A reverse polarity protection for few seconds as in [20] and [21] is not enough for a full protection against accidental reverse connections during car maintenance.

Moreover, in [21] is missing a programmable output current slope control to face in-rush currents at turning-on and -off phases and overcurrent transients causing EMI issues and reducing the device lifetime. The in-rush current can be seriously dangerous for the device when the parasitic inductance of the battery-alternator wire (see Fig. 2) is high. In Fig. 2, the current that flows from the rectifier bridge (I_1) is almost constant and depends on the magnetic field on the stator coils and hence on the rotor coil current. During the turn-on phase, if the current I_3 increases very rapidly, according to (1), the current I_2 will decrease rapidly as consequence. According to (2), due to the parasitic inductance of the wire $L_{\rm w}$, there will be a fast negative voltage spike on $V_{\rm BAT}$. During the turn-off phase, a dual condition happens: if the current I_3 decreases rapidly, I_2 will increase rapidly as consequence and a fast positive voltage spike on $V_{\rm BAT}$ can be observed. Those spikes are not acceptable because they can generate EMI problems to other electronic devices. To solve this issue, the current I_3 cannot increase or decrease too rapidly. On the other hand, the current I_3 cannot increase or decrease too slowly because the internal power dissipation in the RCD would increase too much. Therefore, a slope control on the RCD must be implemented

$$\Delta I_1 = \Delta I_2 + \Delta I_3, \quad \text{since } \Delta I_1 \cong 0 \rightarrow \Delta I_2 \cong -\Delta I_3 \quad (1)$$

$$V_{\rm L} = L_{\rm w} \cdot \partial I_2/\partial t = -L_{\rm w} \cdot \partial I_3/\partial t. \quad (2)$$

III. Rotor Coil Driver Design in HV-CMOS Technology

1) Rotor Coil Driver Block Diagram: The proposed RCD, implemented in Austriamicrosystems HV-CMOS 0.35 μm ASIC technology [8], has been designed to completely fulfill the requirements that can be found in automotive grade devices. Particularly, the RCD can operate with battery voltage between 6 V and 50 V, covering both cold cranking and load dump events. Furthermore, it can sustain permanent reverse polarity

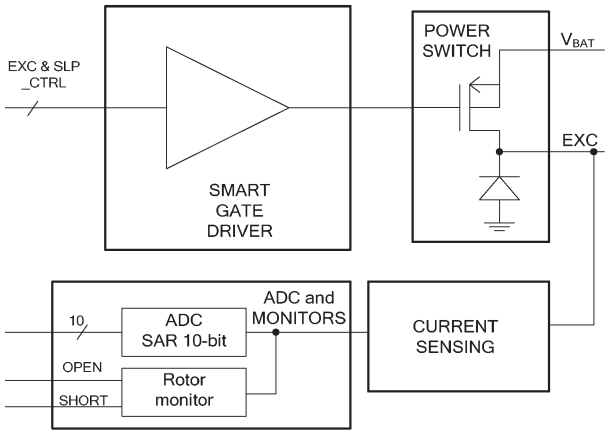

Fig. 3. Alternator coil driver shematic.

on battery down to -3.2 V, which is the maximum forward voltage across the series of two diodes in the rectifier bridge in Fig. 2, and unexpected battery voltage surges up to 55 V. The coil driver scheme, showed in Fig. 3, can be divided into four different blocks: smart gate driver, power switch, current sensing, ADC, and monitors.

The interface toward the processing core of the voltage regulator system is composed by the following output signals: two flags, OPEN and SHORT, signaling if the current in the rotor coil is under or over programmable current thresholds and a 10-bit signal providing a measure of the rotor coil current. The inputs are EXC_CTRL and SLP_CTRL. The digital core sends to the smart gate driver in Fig. 3 the order to increase or decrease the rotor current changing the duty cycle of the PWM EXC_CTRL signal.

The gate of the high side switch is driven by a PWM signal with a fixed frequency f_{PWM} in a range of some hundreds of Hertz, set at 250 Hz in this work. Rotor current is modulated changing the duty cycle of the PWM signal from minimum, typically set at 5%, to 100% (maximum field). Fast transients in the current sunk from the battery can generate undesired overshoots, oscillations, and ringing on the battery voltage. To avoid them, for EMC compliance, the current through the high side has a slope controlled transient during the switching on and off transitions, as detailed in Section III-A3. The digital core can select the current slope through the SLP_CTRL signal.

2) Power Switch: One of the most important blocks is the high-side power switch, which is a p-type HV lateral diffused (LD) MOS [8] with 3.3-V thin gate oxide, included in the HV-CMOS technology from Austriamicrosystems (H35). The main operating and absolute parameters of the HV-PMOS power switch are shown in Table I, which also shows a comparison with the LD HV-NMOS of the same technology.

Both PMOS and NMOS HV devices fulfill the operating battery range, but the choice of PMOS instead of NMOS is due to two main factors: reverse polarity protection and charge pump avoidance. Using the PMOS is possible, driving the bulk terminal properly, to avoid current flow in parasitic devices when the battery voltage is below zero, as shown in Fig. 4. Using the NMOS as in [20], [21] that behavior cannot be achieved using a standard HV-CMOS technology, but a more

TABLE I
HV-PMOS AND HV-NMOS OPERATING AND ABSOLUTE RATINGS (R_{n} IS THE R_{DSon} PER UNIT AREA OF THE HV-NMOS IN THE TARGET TECHNOLOGY [8])

	HV-PMOS	HV-NMOS
Operating Junction Temperature	-40 °C to 150 °C	-40 °C to 150 °C
Absolute Junction Temperature	-40 °C to 180 °C	-40 °C to 180 °C
Maximum Drain-Source Voltage (operating/absolute)	-50 V / -55V	50 V / 55 V
Maximum Drain-Source Breakdown Voltage	-70 V	70 V
Maximum Gate-Source Voltage (operating/absolute)	-3.6 V / - 5V	3.6 V / 5 V
ON Resistance	$1.3 \cdot R_{\mathrm{n}}$	R_{n}

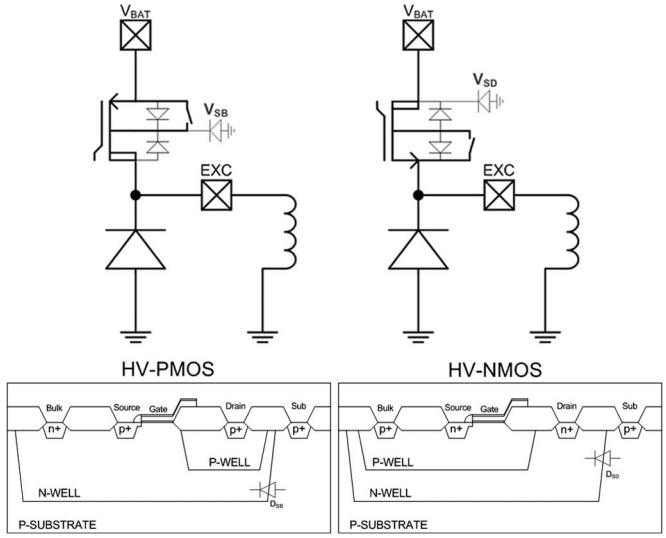

Fig. 4. PMOS versus NMOS comparison during reverse battery condition.

expensive technology must be used to avoid the diode between drain and substrate.

Another advantage using PMOS instead of NMOS is that a charge pump is not needed. Indeed, the gate capacitance of the switch is in the order of some nF and is almost the same when a PMOS or an NMOS is used, so the charge pump for gate driving requires big integrated capacitors. In fact, considering that in the alternator system additional pins for external bypass capacitors are not provided, integrated capacitors must be used. If a rise time of about 10 μs is considered, they have to be in the range of 100 pF, requiring a lot of silicon area. Considering also that in the choosen HV-CMOS technology the R_{DSon} of the HV-PMOS is not much higher than the NMOS one, see Table I, the use of NMOS with big capacitors for the chargepump could have an higher die size and silicon cost than the use of PMOS. Avoiding charge pump circuitry permits also to reduce the EMC conducted emissions and simplify the driving circuitry, becouse no advanced techniques, like spread spectrum, are needed to reduce EMI in charge pump design. Basing on the previous considerations, in the considered HV-CMOS technology, the use of PMOS instead of NMOS permits to reduce the total area occupation and then the silicon cost, permits to achieve full reverse polarity protection and also permits to have better performances in terms of EMC radiated noise.

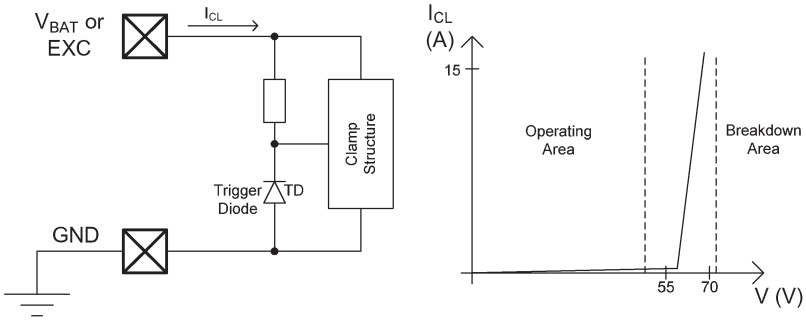

Fig. 5. ESD clamping structure and typical I–V characteristic.

As far as EMC is concerned, in addition to current slope control and the avoidance of charge pump circuitry, EMC decoupling capacitors have been implemented on the supply of clocked blocks in the RCD (e.g., the SAR ADC). To avoid crosstalk between different blocks due to shared supply, a layout design strategy with dedicated metal routing for supply and ground has been implemented.

To withstand ESD pulses and other sparkling pulses due to harness coupling, dedicated clamping structures able to dissipate up to 55 mJ have been added on $V_{\rm BAT}$ and EXC terminals of the RCD. Those structures [3] include a trigger diode and a clamp structure, as shown in Fig. 5 and permit to achieve 8 kV ESD level.

As far as the safe operating area (SOA) is concerned, in the proposed RCD design, the HV-PMOS operates always in the safe voltage and current condition ($V_{\rm SD}$ always below 55 V and $I_{\rm SD}$ below 8 A). Since the HV-PMOS acts as switch, it operates almost all the time with $I_{\rm SD}$ equal to 0 when $V_{\rm SD}$ is high or with very low $V_{\rm SD}$ when the $I_{\rm SD}$ is high and hence its power dissipation is minimized. Only during the turn-on and turn-off transient phases, the PMOS operates in saturation, with both $V_{\rm SD}$ and $I_{\rm SD}$ different from 0. During transient phases, the power dissipation is the order of tens of watts, but for a very limited time defined by the slope control circuit (the energy and power dissipation of the PMOS when operating in saturation region is further discussed in Section III-A3).

3) Smart Gate-Driver: The smart gate driver is the block that drives the gate of the PMOS power switch in Figs. 3 and 6 to obtain the rotor coil current control. Fig. 6 highlights this block (the power MOS is the device M_1) which operates in two different modes, one during the turn-on and turn-off transients (switch S1 in Fig. 6 in position 3), and one during the on and off steady states (switch S1 in Fig. 6 in positions 2 and 1, respectively).

When the turn-on command is received through the EXC_CTRL signal, the gate driver unit starts driving the gate of M1 in order to have a slope-controlled current flowing in the PMOS. The switch S1 is closed in position 3, connecting together the gates of the two PMOS (M1 and M2). The digital-controlled current ramp generator in Fig. 6 starts generating a current ramp on the OUT pin. Because M1 and M2 act as a current mirror, a current ramp on M2 forces a current ramp also in M1. The current that flows in M1 is obtained by scaling the current that flows in M2 by the dimensional factor ratio of the two PMOS devices, $K_{\rm M1M2}$, which amounts to about 1600.

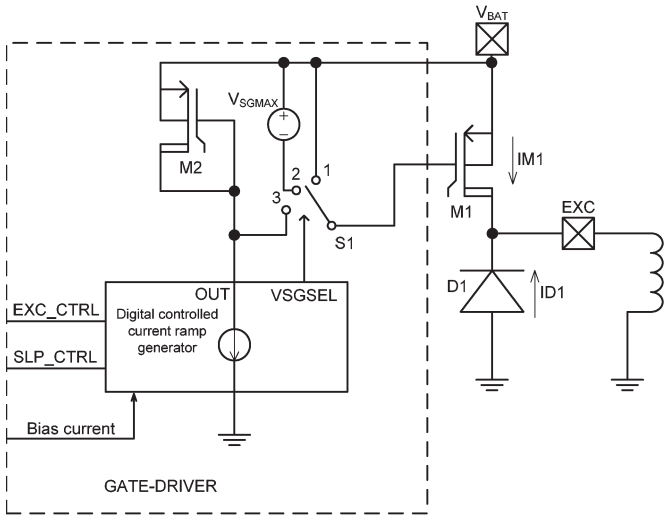

Fig. 6. Gate-driver block diagram.

The slope can be changed in two different ways: setting high the SLP_CTRL signal doubles the slope and adjusting the bias current in the gate driver permits a finest selection of the output current slope. In the proposed IC, both of those strategies are implemented: for the bias current both temperature coefficient and absolute value can be trimmed; trough the SLP_CTRL signal the slope can be set to the trimmed value or to the double.

As consequence, as reported in (3), by controlling during turn-on and turn-off transients, the shape and slope of the Iout signal, which is limited at a maximum at few mA, it is possible controlling the shape and slope of the rotor coil current IM1, which is in the order of several Amperes.

Since IM1 in Fig. 6 is the rotor coil current I_3 in Fig. 1 and (2), then the control of the rotor coil current slope realized by the proposed gate driver allows avoiding overvoltage phenomena and spike generation due to a fast current slope

$$\mathrm{IM1}(t) = K_{\rm M1M2} \cdot \mathrm{IM2} = K_{\rm M1M2} \cdot I\mathrm{out}. \tag{3}$$

On the other hand, the slope of the current IM1 cannot be too slow. This is because during the turn-on and turn-off transients, when the rotor current is flowing in D1 and M1, like shown in Fig. 7, the PMOS works in saturation region and large $t_{\rm ON}/t_{\rm OFF}$ values would lead to high energy dissipation. During transients, the output voltage and current of the PMOS M1 are both different from 0: the current IM1 can be modeled as a ramp

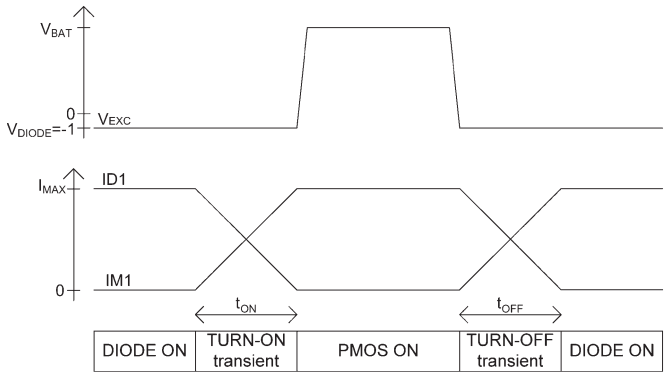

Fig. 7. Gate-driver transients.

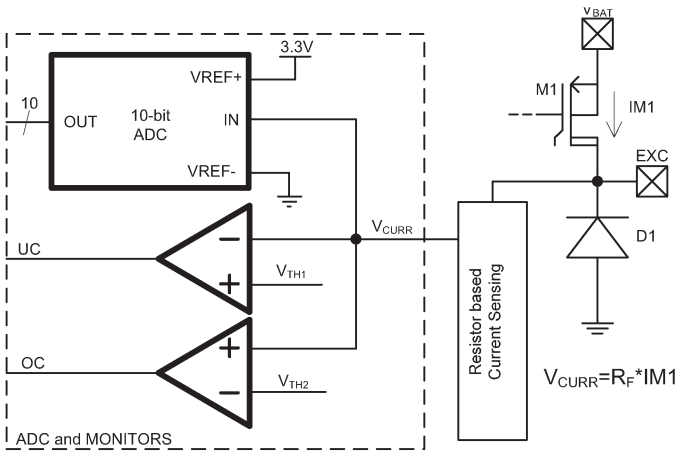

Fig. 8. ADC and monitors block diagram.

going from 0 to I_{MAX} (when turning-on, the opposite when turning-off), while the M1 output voltage is almost constant, clamped at $V_{\mathrm{SD}} = V_{\mathrm{BAT}} - V_{\mathrm{EXC}} = V_{\mathrm{BAT}} + \mathrm{Vdiode}$[1] since D1 is on. As consequence, the energy dissipated at each switching transient can be modeled as in (4). The average power dissipation P_{DAVG}, with a PWM switching frequency f_{PWM}, can be modeled as in

$$E_{\mathrm{DON}} = t_{\mathrm{ON}} \cdot (V_{\mathrm{SD}} \cdot I_{\mathrm{MAX}})/2$$
$$E_{\mathrm{DOFF}} = t_{\mathrm{OFF}} \cdot (V_{\mathrm{SD}} \cdot I_{\mathrm{MAX}})/2 \quad (4)$$
$$P_{\mathrm{DAVG}} = f_{\mathrm{PWM}} \cdot (E_{\mathrm{DON}} + E_{\mathrm{DOFF}}). \quad (5)$$

For typical values of $V_{\mathrm{BAT}} = 14$ V, $V\mathrm{diode} = 1$ V, $I_{\mathrm{MAX}} = 5$ A, $f_{\mathrm{PWM}} = 250$ Hz, and a current slope controlled at 200 mA/μs (slow control set of our RCD, see Section IV), t_{ON} and t_{OFF} amount to 25 μs. Therefore, E_{DON} and E_{DOFF} are always less than 1 mJ and P_{DAVG} is less than 0.5 W. In the worst case scenario of $I_{\mathrm{MAX}} = 8$ A and $V_{\mathrm{BAT}} = 50$ V, then P_{DAVG} is about 4 W, which can be reduced to 2 W using a faster slope control at 400 mA/μs (fast control set of our RCD, see Section IV). The P_{DAVG} contribution should be added to the power dissipation when the PMOS is on, due to non null R_{DSon} resistance: $P_{\mathrm{DON}} = D \cdot R_{\mathrm{DSon}} \cdot I^2_{\mathrm{MAX}}$ being D the duty cycle of the PWM driving command. For typical values of $I_{\mathrm{MAX}} = 5$ A and $R_{\mathrm{DSon}} = 60$ mΩ and worst case values of $I_{\mathrm{MAX}} = 8$ A and $R_{\mathrm{DSon}} = 100$ mΩ then P_{DON} is up to 1.5 W and 6.4 W, respectively. The RCD power stage has been designed so that such power dissipation values can be sustained. From the above case example is clear that, by properly controlling the current slope in the range of hundreds of mA/μs, the main contribution to power dissipation is due to P_{DON}. On the contrary, if the current slope is not controlled, and is in the range of tens of mA/μs, then the above P_{DAVG} power dissipation becomes the dominating contribution reaching critical values for the HV-PMOS.

After analyzing the behavior of the smart gate driver during transients, hereafter its configuration during on and off steady states is discussed. During the on steady state to lower the R_{DSon} and minimize the power dissipation, the switch S1 in Fig. 6 is closed in position 2, connecting the output of the gate driver to V_{SGMAX} and forcing the maximum allowed V_{SG} to lower the R_{DSon} resistance of the PMOS. To be noted that the gate driver is supplied between V_{BAT} and ground, but its output is limited between V_{BAT} and $V_{\mathrm{BAT}} - V_{\mathrm{SGMAX}}$, which is generated subtracting a bandgap stabilized voltage reference of about 3.5 V from V_{BAT}. Since V_{SGMAX} has been generated using a bandgap circuit its value is stable in a wide temperature range and is always within the maximum operating value of 3.6 V reported in Table I.

During the off steady state, the switch S1 in Fig. 6 is closed in position 1 and the output of the gate driver is V_{BAT} forcing the HV-PMOS off ($V_{\mathrm{SG}} = V_{\mathrm{SGMIN}} = 0$).

4) Current Sensing and Monitors: The current sensing block in Fig. 8 is in charge to read back the current flowing in the switch and to send this information to the digital part. Moreover, it informs the digital part if a fail status is reached.

It sends to the digital part two diagnostic flags: the OPEN flag is set when the coil current is below a fixed threshold (about 20 mA) to inform that the rotor coil is disconnected, and the SHORT flag is set when the current is higher than the maximum allowed current (programmable between 8.5 to 12 A) to detect fast current spikes, e.g., due to a short on the rotor coil windings. The used ADC is a 10-bit successive approximation converter (SAR) with a main clock of 704 kHz and a sample rate of 64 kHz. Such frequencies allow for fine time resolution of the alternator regulator as foreseen in recent works [19], [20]. A complete block diagram of this block is shown in Fig. 8.

The V_{TH1} and V_{TH2} thresholds are calculated following:

$$V_{\mathrm{TH1}} = R_{\mathrm{f}} \cdot I_{\mathrm{TH1}}; \quad I_{\mathrm{TH1}} = 0.02 \text{ A}$$
$$V_{\mathrm{TH2}} = R_{\mathrm{f}} \cdot I_{\mathrm{TH2}}; \quad 8.5 \text{ A} < I_{\mathrm{TH2}} < 12 \text{ A}. \quad (6)$$

An integrated temperature sensor is also present forcing in off state the power switch when the measured temperature value is beyond a programmable threshold. Moreover, the reference current used in the ADC is temperature stabilized since it is generated as the sum of a proportional to absolute temperature current and of a complementary to absolute temperature current. A trimming structure on the overcurrent detector and a software calibration on the output of the ADC have been also implemented. Particularly, during the calibration phase, a

[1] Vdiode is the voltage-drop across D1, roughly 1 V in this design, when the current is flowing through the diode.

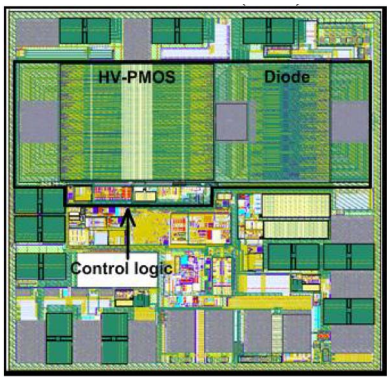

Fig. 9. Alternator voltage regulator layout with the designed rotor coil driver.

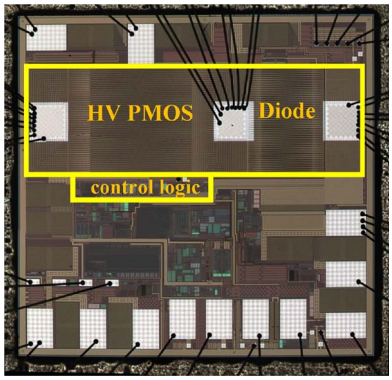

Fig. 10. Alternator voltage regulator chip with the designed rotor coil driver.

TABLE II
IC AREA OCCUPATION

Block	Rotor coil driver	HV-PMOS	Diode	control logic
Area, %	29%	16 %	10%	~3%

fixed current is imposed on the rotor coil and the same current is acquired through the ADC. Doing the calibration with two different current values is possible to compensate the offset and gain error of the ADC.

IV. LAYOUT AND EXPERIMENTAL RESULTS

The proposed coil driver has been realized in 0.35 μm HV-CMOS technology and integrated in an alternator voltage regulator. Figs. 9 and 10 show the layout and the photo of the chip for the fabricated voltage regulator IC. Table II highlights the area contribution of the RCD, 29% of the total regulator area which is 40 mm^2. The main contribution is due to the HV-PMOS and diode, see Fig. 9, which are 16% and 10% of the total regulator while the low-voltage control logic occupation is limited to about 3%. Table III shows the electrical and environmental operating and absolute ranges of the RCD, determined by design choices and verified by experimental measurements on realized IC samples. The main area contribution of the RCD is due to the HV- PMOS to limit its R_{DSon} to less than 100 mΩ, 62 mΩ typical. To be noted that from Table III the current slope is controlled within a range of hundreds of mA/μs which ensures avoiding spike and overvoltage phenomena (too fast slope) and excessive power dissipation (too slow slope).

TABLE III
MEASURED ELECTRICAL AND ENVIRONMENTAL RATINGS

	Min	Typ	Max
Absolute Junction Temperature (°C)	-40		180
Operating Junction Temperature (°C)	-40	40	150
Absolute Battery voltage (V)	-3.2		55
Operating Battery voltage (V)	6	14.4	50
PMOS R_{DSon} (mΩ)	43	62	96
Trimmable overcurrent detection (A)	8.5	-	12
Current slope slow (mA/μs)	150	200	250
Current slope fast (mA/μs)	300	400	500
ESD-HBM (kV)	-8	-	8

It is worth noting that to meet "zero defect" automotive requirements in the design phase, it has been verified that every device in the RCD is working in the SOA with the lifetime acceleration factor close to 1 in order to increase the mean time to failure.

As already discussed in Section III ESD, EMC and on-chip diagnostic and protection issues have been addressed and a "design for testability" flow has been followed to achieve full analog coverage. Since high temperature power cycling is important for automotive applications needing long lifecycle [27], [28], high temperature operating life (HTOL) qualification tests have been implemented and, to recognize weak devices at test, part average testing and statistical bin analysis techniques have been addressed. A detailed description of the followed ASIC design flow with the HV-CMOS AMS technology is reported in [8].

The current consumption of the RCD is 1.91 mA from a 3.3-V voltage supply and 4.14 mA, plus the load current flowing through the HV-PMOS M1, from the battery in typical conditions. In worst case the current consumption rises to 2.08 mA from the 3.3 V supply and 4.29 mA from the battery plus the load current flowing through the HV-PMOS M1. To communicate with the IC, sending the configuration and trimming bits and reading back the status and the ADC outputs, a testboard has been manufactured. The serial communication protocol has been implemented using the Labview software and a DAQ board. The RCD has been thermally characterized in the range -40 °C to 180 °C using the Thermostream TP04300A system. Hereafter, some measurement results are shown. As example Fig. 11 shows the measured variation versus temperature of the R_{DSon} of the PMOS, which is always quite below the 100 mΩ target in the operating range from -40 °C to 150 °C (tests have been done with currents from 0.1 A to 2 A obtaining similar results). The RCD can operate up to the max absolute temperature of 180 °C before reaching an "overtemperature protection threshold." Above 180 °C, the integrated temperature protection switches off the driver to avoid silicon damage. To be noted that during RCD testing and validation, it has been verified that the device can temporary work above 150 °C and 180 °C, but lifetime validation tests, such as the HTOL qualification test, have been done at 150 °C.

As example of thermal characterization in the extended range -40 °C to 180 °C, Fig. 12 shows the measured variation versus temperature of 1) Vdiode, the voltage drop of the diode D1 in Fig. 6, and 2) the V_{SG} of the HV-PMOS when the transistor is in on-state ($V_{\mathrm{SG}} = V_{\mathrm{SGMAX}}$). Fig. 12 demonstrates the good stability versus temperature of the designed driver.

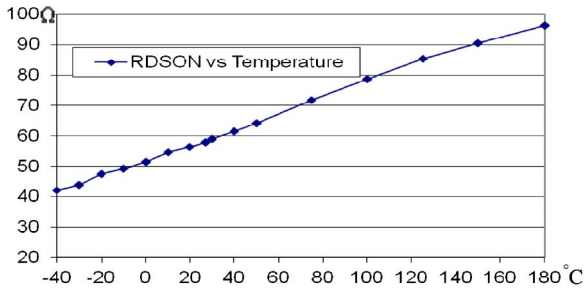

Fig. 11. R_{DSon} of the HV-PMOS versus temperature.

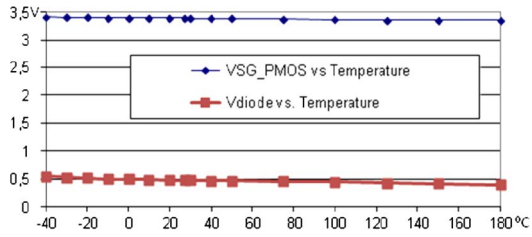

Fig. 12. V_{SG} of the HV-PMOS in on state ($V_{\mathrm{SG}} = V_{\mathrm{SGMAX}}$) and Vdiode versus temperature.

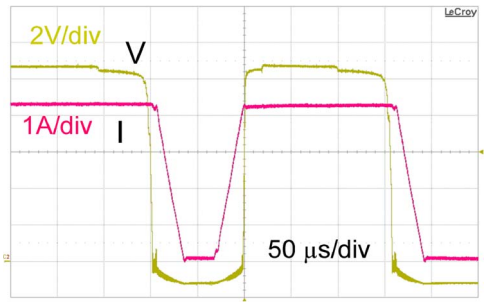

Fig. 13. Voltage and current in the rotor coil.

The reliability of the RCD has been proven forcing the driver to switch permanently at maximum duty cycle and at maximum ambient temperature in order to reach junction temperature around 150 °C without performance degradation.

Fig. 13 shows the typical behavior of voltage and current in the rotor coil. Details of the turn-on and the turn-off phases changing the slope control bit are visible in Figs. 14 and 15.

In Fig. 14, the measurements are done setting the SLP_CTRL bit cleared (slow current slope: 200 mA/μs), and the measured value is about 197 mA/μs, while in Fig. 15 the SLP_CTRL bit is set (fast current slope: 400 mA/μs) and the measured current slope is about 383 mA/μs.

In Fig. 16, the blue line shows the current read-back that can be obtained from the integrated SAR ADC, compared with the real coil current. As it can be noted, the linearity of the read-back and ADC circuits is good. The equation of the fitting line is reported hereafter being y the current read-back from the ADC and x the real coil current

$$y = 1.2378x + 0.2514. \tag{7}$$

The gain/offset mismatch of the characteristic has been corrected through a software calibration phase obtaining the pink line in Fig. 16.

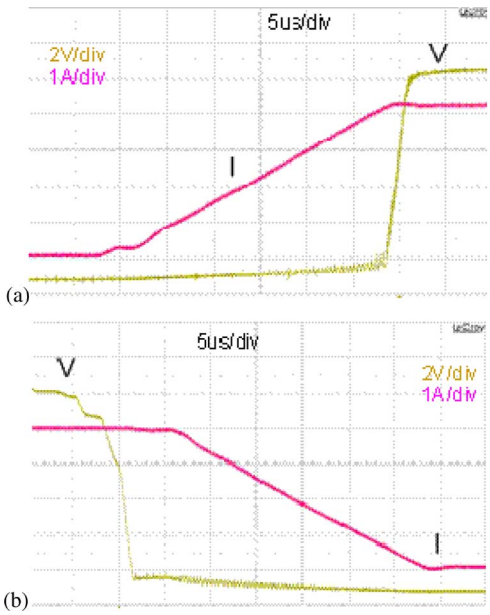

Fig. 14. (a) Turn-on and (b) turn-off phases with slow current slope set.

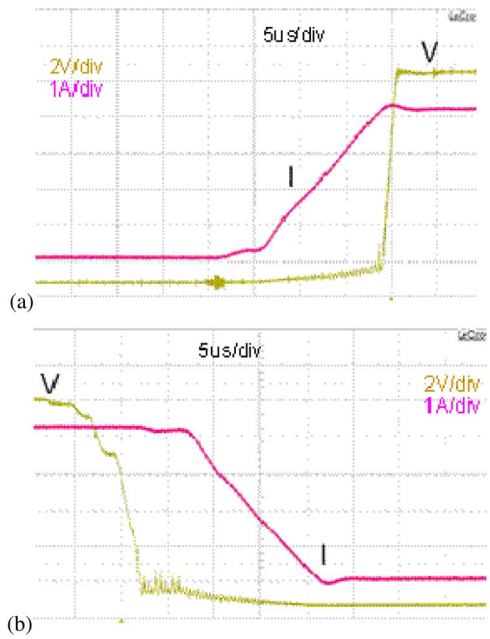

Fig. 15. (a) Turn-on and (b) turn-off phases with fast slope current set.

V. Conclusion

The work presents the design, implementation in 0.35 μm HV-MOS technology and experimental characterization of a novel RCD that can be integrated in regulators for the new generation of automotive alternators. Table IV compares the main characteristics of the proposed RCD with those of the coil driver sub-blocks of alternator voltage regulators recently proposed in the state of the art [20], [21]. The driver presented in this work includes the power switch with low-voltage circuitry for diagnostics and interfacing toward a digital control unit. New functionalities are integrated with respect to the state of the art of integrated drivers for alternator rotor coil, such as

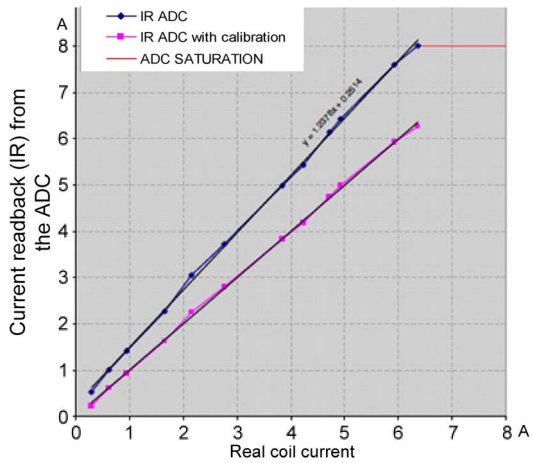

Fig. 16. Current read-back obtained from the integrated ADC: output current versus real coil current with (pink line) and without (blue line) calibration.

TABLE IV
COMPARISON VERSUS THE STATE OF ART

	Our	[20]	[21]
Temperature Range	-40 °C to 180 °C	-40 °C to 150 °C	-40 °C to 150 °C
Maximum battery voltage	55 V	40 V	40 V
PMOS R_{DSon}	62 mΩ	80 mΩ	N/A
Overcurrent detection	Trimmable, 8.5 A to 12 A	10 A	9 A to 18 A
New features vs. state of the art	Protection against fixed reverse polarity, programmable current slope control		
ESD-HBM (kV)	±8	±8	±4

full reverse polarity protection and programmable output slope control against in-rush currents and current spike transients.

The achieved experimental results prove the effectiveness of the proposed RCD that can sustain a temperature range from -40 °C to 180 °C, ESD level up to 8 kV, voltage levels up to 55 V. The current slope can be controlled and the current detection is configurable from 8.5 A to 12 A. The area is dominated by the power stage where the MOS is sized to have a R_{DSon} resistance below 100 mΩ, 62 mΩ typical.

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