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Numerical simulation and experimental characterization of Emitter Wrap Through solar cells with Deep Grooved Base contact (EWT-DGB)

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Abstract

In this work we present an Emitter Wrap Through cell with Deep Grooved Base contact (EWT-DGB), designed for both 1-sun and concentrating applications. The proposed approach, which consists in a deep grooved hole array composed by holes of two alternating doping type, allows both a reduction of the cell series resistance and an increase in collection efficiency also by using relatively thick substrates with low lifetime. The measured experimental data including dark J-V characteristics, figures of merit (FOMs) under illumination and external quantum efficiency (EQE) are compared to the results of 3-D drift-diffusion TCAD numerical simulations. Moreover, the impact of the hole spacing and of process-dependent physical parameters (interface defects) on FOMs is investigated by means of simulations.

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Keywords: Silicon solar cells; Emitter Wrap Through (EWT) solar cells, 3-D numerical simulations, photovoltaic

1. Introduction

Practical Back-contact Back-junction (BC-BJ) solar cells achieve high conversion efficiency (above 24 % [1,2]) mainly thanks to the absence of front contact optical shading. BC-BJ schemes are also promising for high current solar cells such as concentrator photovoltaic (CPV) [3]. The strong dependency of the device performance on the charge carrier lifetime and wafer thickness limits the application of BC-BJ cells to high quality Floating Zone silicon

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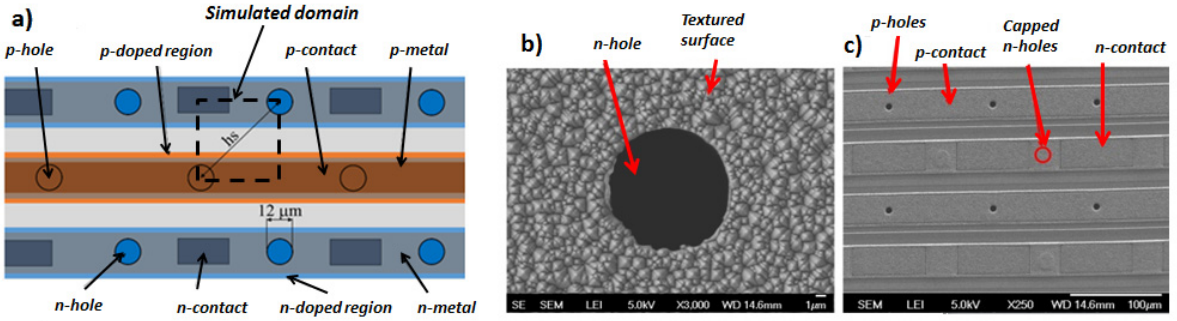

Fig. 1. (a) Scheme (not in scale) of the back cell surface of the EWT-DGB solar cell with the detail of simulation domain considered; (b) SEM image of a hole rim on the texturized front surface and c) SEM image of the back surface of the cell.

with large charge carrier lifetime (hundreds to thousands of microseconds) or very thin substrates [3]. In this regard, the emitter wrap-through (EWT) cell concept was originally proposed as a technique to accomplish high efficiency and to overcome the limitations in terms of substrate requirements [4]. In such a scheme, all contacts are placed on the rear while the emitter is still located near the front surface. By extending the emitter to the walls of holes etched through the substrate the connection between the front surface active emitter and its contacts is provided. The main advantage of the EWT approach is the possibility to collect high current densities without the need of high bulk lifetimes substrates, thanks to the large coverage of electrically interconnected emitter areas.

EWT solar cells have been treated in detail by the PV community. Improvements adopted in order to achieve high efficiency values were discussed in [5-8]. Moreover, Faika et al. [9] presented a fabrication approach adopting an Al-P-codiffusion, Harder et al. [10] proposed a laser-processed technique and Cho et al. [11] discussed high efficiency EWT solar cells featuring a non-uniform silicon-nitride passivation layer. In addition, the limiting aspects of the EWT concept have been deeply investigated in [12].

Regarding the numerical modeling of the EWT solar cells, Smith et al. [13] proposed an equivalent electrical circuit. 1-D and 2-D physics-based numerical simulations of EWT solar cells have been performed by several groups and implemented in different simulation tools [14-17]. Furthermore, 3-D numerical simulations were successfully carried out in Sentaurus TCAD by Ulzhöfer et al. [18].

In this work, we present a silicon solar cell scheme conceived on the basis of the Emitter Wrap Through design, and featuring Deep Grooved Base contacts (EWT-DGB). The proposed cell scheme is aimed at preserving the advantages of the EWT design pushing this technology towards the CPV. Differently from the common EWT scheme, the cell is provided of two arrays of alternatively n-doped and p-doped pass-through holes (also named vias), grooved through the silicon wafer by means of a Deep Reactive Ion Etching (DRIE) process following a chessboard scheme (Fig. 1). Moreover, the distance among the n-doped holes is reduced down to tens of microns and the vias diameter is scaled down to 12 µm. In this way, the n-holes pass through the p-type silicon wafer and form an effective vertical p-n junction.

Since n-holes pitch is much smaller than wafer thickness, an enhancement of collection efficiency is awaited in the EWT-DGB cells and a reduced parasitic resistance in the substrate is attended, providing an increase in Fill Factor (FF). This feature is particularly interesting for both 1-sun and CPV applications (where extremely high currents flow through the cell).

EWT-DGB cells with different hole spacing have been fabricated by using thick substrates (280 µm) with low lifetime (about 60 µs) and have been studied in this work. The relatively high substrate thickness is chosen in order to permit the carrier collection in the entire spectrum, especially in its red portion, as successfully demonstrated by the External Quantum Efficiency (EQE) analysis. Regarding the lifetime, the adoption of this substrate of medium-quality is ascribed to the fact that our purpose is to design an architecture which reduces the sensitivity to the substrate quality. In fact, as discussed in this paper, the proposed EWT-DGB approach results in several advantages respect to a conventional PESC solar cell realized by adopting both the same fabrication process and silicon substrate [19].

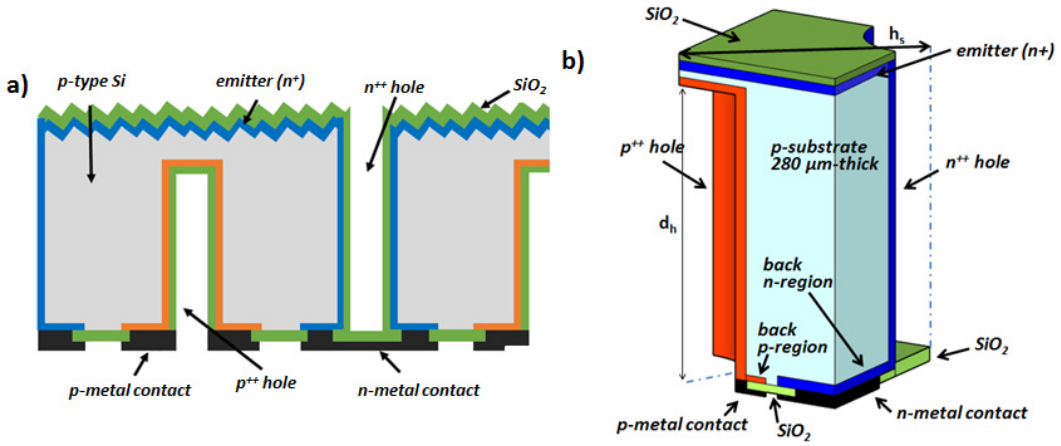

Fig. 2. (a) Scheme (not in scale) of the vertical section of the EWT-DGB solar cell ; (b) sketch of the considered 3-D simulation domain, where h_S denotes the distance between the n- and p-hole second picture.

The first produced prototypes of EWT-DGB solar cells, featuring conversion efficiency approaching 19% and Fill Factor of 80% at 1-sun, are accurately described in this paper. In addition, numerical simulations by a Technology Computer Aided Design (TCAD) tool have been performed to reproduce the measured data to study the sensitivity of the main FOMs on critical process-dependent physical parameters.

The paper is organized as follows. In section 2 we describe in detail the cell design and the main steps of the fabrication process. In section 3 we outline the numerical simulation methodology and the physical models adopted to reproduce the measured data. Lastly, in section 4, we discuss both the experimental and simulated results in terms of dark J-V characteristics and characterization under 1-sun illumination. Moreover, the impact of a geometrical parameter such as the hole spacing and of other critical process-dependent physical parameters are investigated by means of numerical simulations.

2. Cell design and fabrication process

The first cell prototypes, featuring an active area of 16 mm^2, have been manufactured in a CMOS like pilot line. The studied device is fabricated on a 280 µm-thick p-type mono-crystalline silicon wafer with a resistivity of 0.5 Ωcm. The vias array, which feature diameter of 12 µm, is defined by means of photolithography and etched with a Bosch process by using a Deep Recative Ion Etching (DRIE) equipment [19]. The holes are alternatively doped with phosphorous (n-hole, 15 Ω/sq) and boron (p-hole, 140 Ω/sq) by means of two different solid source diffusions. The n-holes pass through the cell substrate and wrap the front surface emitter to n^{++}-doped region on the back surface. The 260 µm-deep p-doped holes are contacted to the back p-doped region (Fig. 2a). The front surface is textured by random pyramids and phosphorous doped (80 Ω/sq). A protective SiO_2 layer is thermally grown on the holes surface and on the textured surface, where acts as both passivating layer and anti-reflective coating. The leayout features two separated p^{++} and n^{++} doped regions on the back surface,. The emitter and base contacts were opened on these high-doped regions by means of a photolithographic step followed by a dry RIE etching,and an interdigitated metal grid leads the signal to two lateral busbar, used to contact the cell to its package.

Three different cell prototypes, which differ in terms of hole spacing h_S (the distance between n- and p-doped holes), have been realized: h_S = 43 µm, 50 µm and 78 µm. In order to characterize the samples, the cells have been packaged with silver loaded conductive epoxy adhesive onto a printed circuit boards appositely designed to perform four-probe measurements.

3. Simulation methodology

3-D numerical simulations are performed on a simulation domain chosen by exploiting the symmetry of the structure (Fig. 1a). In Fig. 2b we report a 3-D sketch of the considered EWT-DGB cell. Three different cells are modelled, with different hole spacing h_S (43 μm, 50 μm and 78 μm, respectively). The adopted substrate resistivity ρ_S is 0.5 Ωcm and the measured minority charge carrier lifetime is 62 μs. Doping profiles of emitter and doped regions on the back are opportunely defined in order to reproduce the experimental sheet resistance values. The sheet resistance values of doped regions as well as the assigned surface recombination velocity (SRV) values at the various interfaces are reported in Table 1.

Table 1. Physical parameters adopted in the simulations.

Parameter	Unit	Value
Front emitter sheet resistance	Ω/sq	80
p-hole sheet resistance	Ω/sq	140
n-hole sheet resistance	Ω/sq	15
Front Emitter Region/SiO_2 interface SRV	cm/s	$5.8 \cdot 10^3$ [20]
Substrate/SiO_2 interface SRV	cm/s	$5.8 \cdot 10^3$ [20]
Back p-doped region/SiO_2 interface SRV	cm/s	10^3 [20]
Back n-doped region/SiO_2 interface SRV	cm/s	$3 \cdot 10^4$ [20]

3.1. Calibration process

Numerical simulations are performed by means of a TCAD mixed-mode device simulator [21] where the solar cell is included in an electrical circuit, which directly takes into account for the shunt resistance (R_{SH}) and the series resistance (R_s). These parameters are extracted from the fitting of the measured dark J-V characteristics by adopting an equivalent electric circuit composed by three diodes (D_1, D_2 and D_3 with ideality factor of 1, 2 and 1.3, respectively, and saturation current densities J_{01}, J_{02} and J_{03}), in addition to R_{SH} and R_s [22].

The saturation current densities values of the equivalent electrical circuit adopted for the fitting of the measured dark J-V characteristics (shown in Fig. 3) are reported in Table 2.

Table 2. Saturation current densities values of the adopted equivalent electrical model used for the fitting of the measured dark J-V characteristics

h_S (μm)	J_{01} (A/cm^2)	J_{02} (A/cm^2)	J_{03} (A/cm^2)
43	$1.7 \cdot 10^{-12}$	$4 \cdot 10^{-8}$	$7 \cdot 10^{-10}$
50	$1.7 \cdot 10^{-12}$	$1 \cdot 10^{-7}$	$5 \cdot 10^{-10}$
78	$9.6 \cdot 10^{-13}$	$4 \cdot 10^{-8}$	$3 \cdot 10^{-10}$

The calibration process is aimed at obtaining a satisfactory fitting between the simulated dark J-V characteristic with the experimental one, for the sample with h_S = 50 μm case. In this regard, we have tuned the SRV at holes internal surfaces (basically to reproduce the saturation current density J_{01} associated to diode D_1) and the carrier lifetime value in a region around the n-type doped hole (n-hole region). This region is few μm-deep and also includes the depletion region of the n^+-p junction. The n-hole region is representative of a portion of device volume where a high concentration of defects is localized, mainly due to the deep etching process used to fabricate holes. The effective charge carrier lifetime value in such region is a tuning parameter used to reproduce the experimental value of the saturation current densities of diode D_2 and diode D_3 (J_{02} and J_{03}, respectively). It is worth noting that V_{OC} is highly affected by the recombination losses ascribed to the n-hole region, as discussed in section 4.

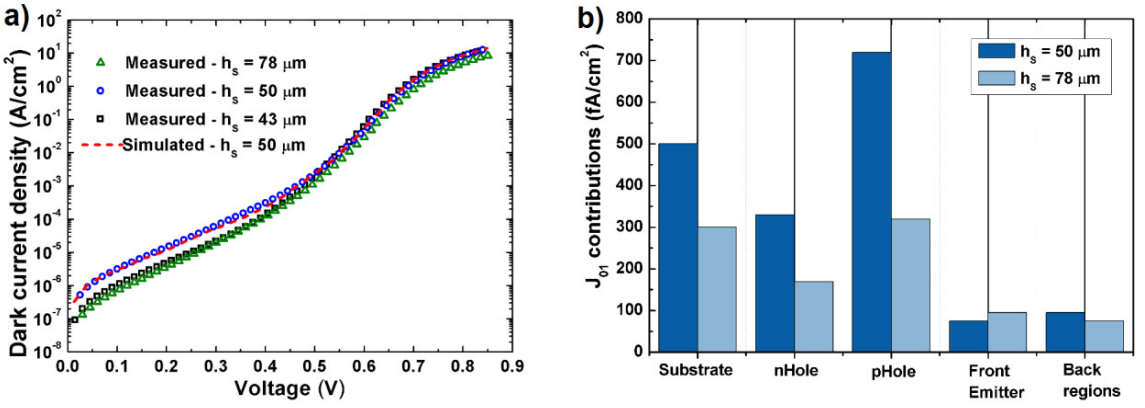

Fig. 3. (a) Measured dark J-V characteristics for three different hole spacing h_S: 43 μm, 50 μm and 78 μm and simulated dark J-V characteristic (red dotted line) in case of h_S = 50 μm; (b) Comparison of the J_{01} region-wise contributions at region level in case of h_S = 50 μm and h_S = 78 μm.

Summarizing, in addition to the physical parameter values reported in Table 1, in the simulations of the h_S = 50 μm geometry we have adopted a SRV value at holes internal surfaces of $4 \cdot 10^4$ cm/s and a n-hole region lifetime of 0.18 μs to satisfactory reproduce the experimental dark J-V characteristics as reported in Fig. 3a.

3.2. Physical models

TCAD device simulations [21] are performed by considering the parameters of physical models already successfully adopted in [23-34], based on the reviews on numerical device simulation for crystalline silicon solar cells [20,35]. In detail, Fermi–Dirac statistics is assumed and, in order to account for the revised value of the intrinsic carrier density well accepted in photovoltaic community ($n_i = 9.65 \cdot 10^9$ cm^-, the Bandgap narrowing model (BGN) proposed by Schenk [36,37] is used. The model proposed by Klaassen [38,39] is adopted to account for the doping dependent carrier mobility. Auger and radiative recombination models are parameterized according to Dziewior and Schmid [40] and Trupke [41], respectively. Moreover, we take into account for Shockley–Read–Hall (SRH) recombination losses and the parameters for degraded boron-doped FZ-Si are chosen according to [42].

The spatially resolved optical generation rate profile was calculated by a raytracer tool considering the internal bottom reflectivity at different material stacks at the back interface (Fig. 2a). A Phong diffusive boundary condition is adopted to model the typical roughness in such material stacks [43].

4. Results and discussion

4.1. Dark analysis

The adopted values of physical parameters discussed in the section 3 allow us to satisfactory reproduce, by means of numerical simulation, the measured dark J-V characteristic of the EWT-DGB cell featuring h_S of 50 μm, as can be observed in Fig. 3a (where the measured curves in case of two different h_S, 43 μm and 78 μm, are also reported).

From Table 2 we observe that higher hole spacing (78 μm) leads to lower recombination losses described by the J_{01} contributions with respect to h_S = 50 μm, while by reducing h_S to 43 μm significant differences are not appreciable. In this regard, by starting from the same physical parameters successfully tuned for the h_S = 50 μm cell, we have carried out numerical simulations under dark condition of other two EWT-DGB cells featuring h_S of 43 μm and 78 μm, respectively. As expected, simulations do not show any difference in terms of recombination losses between the two smaller hole spacing 43 μm and 50 μm. On the contrary, simulations confirm that, by increasing

the hole spacing up to 78 μm, the J_{01} contribution significantly decreases. In detail, this reduction is ascribed to the lowering of recombination losses in the substrate and in both holes' regions as illustrated in Fig. 3b.

It is worth noting that, as reported in Table 2 and as shown in Fig. 3a, the total dark current density at low-voltage bias (<0.5 V) is not strictly related to the hole spacing. As a matter of fact, the dark J-V characteristic at relatively low bias is dominated by recombination in the n-hole region which are affected by etching process conditions. In order to reproduce the measured dark J-V characteristics, the n-hole region effective lifetime is therefore finely tuned.

4.2. 1-sun characterization

Table 3 reports the measured FOMs of the three fabricated EWT-DGB cells (h_S = 43 μm , 50 μm and 78 μm). In addition, the results of the simulation under 1-sun illumination are also shown for the corresponding different geometries, obtained by adopting the physical models used for the dark J-V characteristic fitting of the h_S = 50 μm case (section 3).

Regarding measured FOMs, the J_{SC} is approximately 40 mA/cm^2 thanks to the absence of metallization pattern on the front surface and to the high quantum efficiency, as shown in the following. The V_{OC} is equal to 595 mV in case of h_S = 78 μm and it decreases down to 575 mV by reducing the hole spacing, as predicted by simulations. This reduction in V_{OC} can be explained in terms of J_{01} reduction (see subsection 4.1) and of recombination losses in the region around n-holes (n-hole region) described by diode D_3 of the equivalent circuital model (Table 2). The conversion efficiency is in the range of 18.1 % – 18.6 % for all the samples, even though simulations suggest an higher efficiency for the samples with larger h_S. The resulting performance in terms of efficiency are in any case lower than those reported in other works of the state-of-the-art silicon solar cells. In terms of FF, the n-hole region (J_{02} contribution, Table 2) limits the FF in case of h_S = 50 μm while for the h_S = 43 μm and h_S = 78 μm cases, for which J_{02} is comparable, we observe higher FF. Both experimental data and simulations show that samples with higher hole spacing have better overall performance. On the other hand, cells with lower h_S could be preferred under concentrated light, where the parasitic resistance of the substrate limits the conversion efficiency.

By analysing the simulated FOMs we note that in the case h_S = 50 μm simulations are in agreement with the experimental data within the considered uncertainties. As discussed in subsection 4.1, in order to obtain a satisfactory FOMs fitting (especially in terms of FF) also for h_S = 43 μm and h_S = 78 μm cases, a further fine tuning of the n-hole region lifetime is required to take into account for the samples variability of the defects occurring in that region.

Table 3. Measured and simulated FOMs of the considered EWT-DGB solar cells for the three different hole spacing h_S considered in this study. The relative uncertainties of experimental values are indicated in the brackets.

h_S (μm)		V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
43	Measured	575 (1%)	38.9 (2%)	81.1 (5%)	18.1 (5%)
	Simulated	575	39.9	80.5	18.5
50	Measured	582 (1%)	40.1 (2%)	79.6 (5%)	18.6 (5%)
	Simulated	578	40.2	79.7	18.6
78	Measured	597 (1%)	38.5 (2%)	80.4 (5%)	18.5 (5%)
	Simulated	595	40.7	81.3	19.5

4.3. External and internal quantum efficiency

The experimental and simulated external quantum efficiency (EQE) characteristics are shown in Fig. 4a where the data of the h_S = 50 μm case are considered. As comparison, the EQE curve of a conventional PESC cell [19], with same physical dimensions, fabricated on the same silicon substrate and by using a similar technological process, is reported in the figure and used as reference.

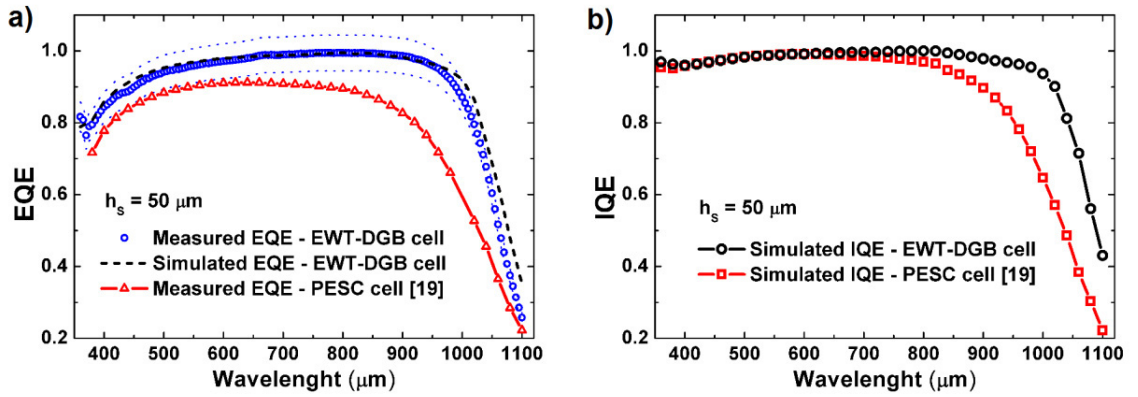

Fig. 4. (a) Simulated and measured external quantum efficiency (EQE) with the corresponding bounds of the experimental uncertainty (light blue dashed lines) of the EWT-DGB solar cell featuring hole spacing h_S of 50 μm. Measured EQE of a PESC cell [19] is also illustrated; (b) Simulated Internal Quantum Efficiency (IQE) of the EWT-DGB solar cell (h_S = 50 μm) and of the PESC cell [19].

It is worth noting the higher EQE of the EWT-DGB structure (in particular in the IR portion of the spectrum) with respect to the PESC cell. This enhancement can be explained by: i) higher optical absorption in the whole spectrum due to suppression of the front metal grid, and ii) the further enhancement in the IR portion of the spectrum due to the better collection properties of the vertical junction as confirmed by the analysis of the simulated Internal Quantum Efficiency (IQE) (Fig. 4b).

4.4. Impact of interfacial defects on FOMs

Numerical simulations have been exploited to investigate the effect of interfacial defects on the cell FOMs. We account for such defects by imposing a surface recombination velocity (surface SRH model) at each interface including front, back passivated and holes interfaces. In this study we consider only the case of h_S = 50 μm.

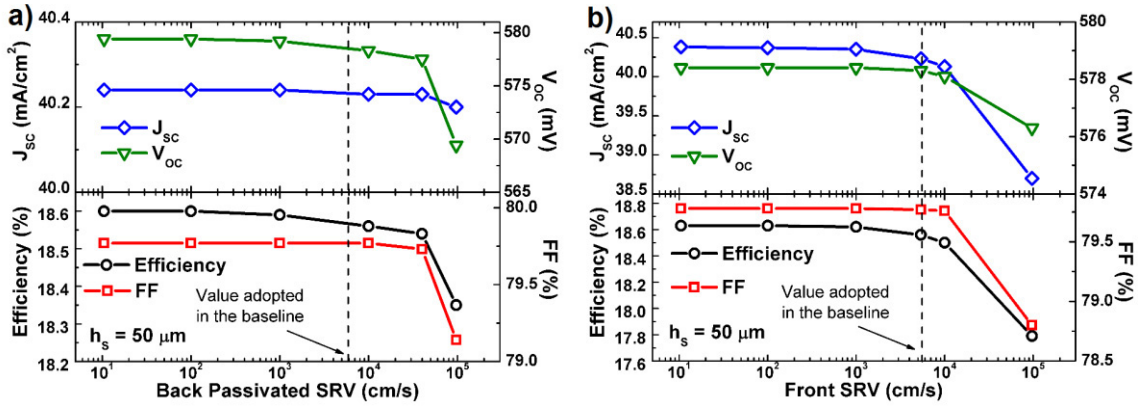

Fig. 5. (a) Simulated values of Figure of Merit (FOMs) the considered EWT-DGB solar cell (hole spacing h_S = 50 μm) versus Surface Recombination Velocity (SRV) at back passivated interface; (b) Simulated values of Figure of Merit (FOMs) the considered EWT-DGB solar cell (hole spacing h_S = 50 μm) versus Surface Recombination Velocity (SRV) at front interface. The black dashed lines denotes the SRV values used for the simulation of the baseline cell (h_S = 50 μm) which reproduce the experimental data.

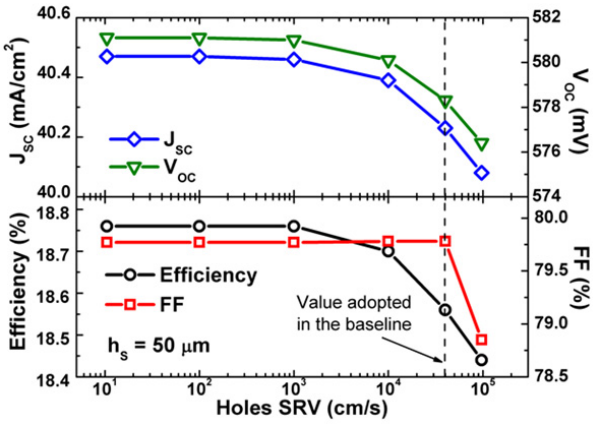

Fig. 6. (a) Simulated values of Figure of Merit (FOMs) the considered EWT-DGB solar cell (hole spacing h_S = 50 µm) versus Surface Recombination Velocity (SRV) at p- and n-hole interface. The black dashed lines denotes the SRV values used for the simulation of the baseline cell (h_S = 50 µm) which reproduce the experimental data.

Fig. 5 shows the impact of the SRV of the cell front interface and of the back passivated interface on FOMs while Fig. 6 illustrates the impact of the SRV of the hole surfaces. A negligible impact in terms of J_{SC} and FF has been observed except for the case of the front SRV where J_{SC} variations justify the efficiency trend. Moreover, holes SRV significantly affects V_{OC} and then the efficiency. It is worth noting that a simultaneous reduction of the studied (front, back and hole interfaces) SRVs down to 10^3 cm/s leads to an efficiency increase up to 19 $\%_{abs}$.

5. Conclusions

In this work we have proposed a new cell concept based on EWT scheme (Deep Grooved Base contact solar cell, EWT-DGB) where an high density hole matrix arranged in two alternating doping type (p and n) is fabricated by means of deep reactive-ion etching technique. In particular, n-holes pass through the cell substrate and wrap the front surface emitter to the back surface, while the p-holes act as collecting electrodes, allowing a reduction of the resistive losses due to the substrate, feature particularly important for CPV applications. Thick substrates with low lifetime (about 60 µs) are used to produce cells approaching 19% efficiency and Fill Factor of 80% under 1-sun illumination and ensuring an efficient photon absorption within the spectrum from UV to IR. Starting from experimental data we have performed 3-D numerical simulations which allow to reproduce the measured dark J-V characteristic and the figures of merit under illuminated conditions of an EWT-DGB with distance between two holes differently doped (hole spacing) of 50 µm. The calculated External Quantum Efficiency is compared to the measured one and a matching within the adopted experimental uncertainty is obtained. The EQE curve confirms the advantages of this design in terms of carries collection especially in the red portion of the spectrum. Numerical simulations are also exploited to analyse the impact on figures of merits of the hole spacing and to compare the simulated trends with the measured ones. We conclude that higher hole spacing leads to higher V_{OC}. Lastly, a simulation study aimed at investigating the impact on performance of some interfacial defects is carried out. The analysis shows that reduction of the studied SRV down to 10^3 cm/s will lead an efficiency increase up to 19 $\%_{abs}$.

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