2D Materials



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# Ultra-scaled $MoS_2$ transistors and circuits fabricated without nanolithography

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**Abstract.**

The future scaling of semiconductor devices can be continued only by the development of novel nanofabrication techniques and atomically thin transistor channels. Here we demonstrate ultra-scaled $MoS_2$ field-effect transistors (FETs) realized by shadow evaporation method which does not require nanofabrication. The method enables large-scale fabrication of $MoS_2$ FETs with fully gated 10-nm long channels. The realized ultra-scaled $MoS_2$ FETs exhibit very small hysteresis of current-voltage characteristics, record high drain currents of $\sim$ 560 A/m, very good drain current saturation for such ultra-short devices, subthreshold swing $\sim$ 120 mV/dec, and drain current on/off ratio $\sim 10^6$ in air ambient. The fabricated ultra-scaled $MoS_2$ FETs are also used to realize logic gates in n-type depletion-load technology. The inverters exhibit a voltage gain of $\sim$ 50 at a power supply voltage of only 1.5 V and are capable of in/out signal matching.

*Keywords*: $MoS_2$, field-effect transistors, short-channel effects, logic gates, transistor scaling

## 1. Introduction

Scaling of Si field-effect transistors (FETs) in integrated circuits is rapidly approaching physical limits [1–3]. The negative impact of the short-channel effects [4] on the performance of aggressively scaled Si FETs (with channel lengths $\sim$ 20 nm) is currently mitigated by the use of very thin ($<$ 10 nm) Si channels, typically etched in the shape of fins [5]. Further downscaling of FETs would require even thinner channels, imposing a demand for atomically thin homogeneous semiconductor channels [6–8]. Two-dimensional semiconductor materials (e.g., monolayer $MoS_2$) are good candidates for such channels, because they are inherently atomically thin, have a uniform thickness, and are free from dangling bonds. Their application in the ultra-scaled FETs is limited mainly by the fabrication challenges because both the channel length ($L_{\rm ch}$) and gate length ($L$) of such FETs should be at the 10-nm scale. Ideally, the entire channel should be gated ($L_{\rm ch} = L$) to eliminate the ungated (access) parts of the channel.

After the first demonstration of the exfoliated monolayer $MoS_2$ FETs [9], there have been several attempts to integrate atomically thin $MoS_2$ channels in ultra-scaled FETs. Monolayer $MoS_2$ grown by chemical vapor deposition (CVD) have been used in FETs with $L \sim 10$ nm exhibiting drain currents $I_{\rm D} \sim 400$ A/m (normalized by the channel width $W$), but with $L_{\rm ch} \sim 50$ nm [10]. Even shorter gate lengths ($L \sim 1$ nm) have been demonstrated in exfoliated multilayer $MoS_2$ FETs with carbon nanotube gates, albeit with $L_{\rm ch} \sim 500$ nm [11]. The technological challenge of realizing ultra-scaled FETs with $L_{\rm ch} \sim L$ could be overcome by fabricating FETs with self-aligned contacts in which the gate overlaps the source/drain contacts and covers the entire channel [12]. In this case, the physical gate length $> L_{\rm ch}$, but it allows gating of the entire channel because $L_{\rm ch} = L$. Although such FETs are unsuitable for very high-frequency applications due to the overlap capacitances between the contacts, they could provide an insight into the operation of the ultra-scaled $MoS_2$ FETs. However, all ultra-scaled $MoS_2$ FETs which have been realized in this way so far were based on technologies which cannot be implemented on a large scale. Self-assembly of block copolymers have been used to fabricate back-gated $MoS_2$ FETs with $L = 7.5$ nm, but required guiding Au lines and produced only multiple FETs connected in series [13]. Sub-10 nm top-gated $MoS_2$ FETs have also been realized, but only on top of cracks in $Bi_2O_3$ [14] or grain boundaries of graphene [15].

Here we demonstrate 10-nm $MoS_2$ FETs fabricated on a large scale without high-resolution patterning. This was achieved by fabricating the long-channel $MoS_2$ FETs by conventional lithography, and then reducing the length of the channel down to 10 nm by a shadow evaporation [16–21] of Au. The devices were fabricated on a local Al back gate with an ultra-thin high-k oxide ($AlO_x$) in order to efficiently gate the entire channel ($L_{\rm ch} = L$). Both exfoliated $MoS_2$ and monolayer $MoS_2$ grown by CVD were used in fabrication. The realized 10-nm $MoS_2$ FETs exhibit very small hysteresis of current-voltage characteristics, drain current $I_{\rm D} \sim 560$ A/m, and subthreshold swing $S_{\rm th} \sim 120$ mV/dec in air ambient. We also realized the n-type depletion mode digital

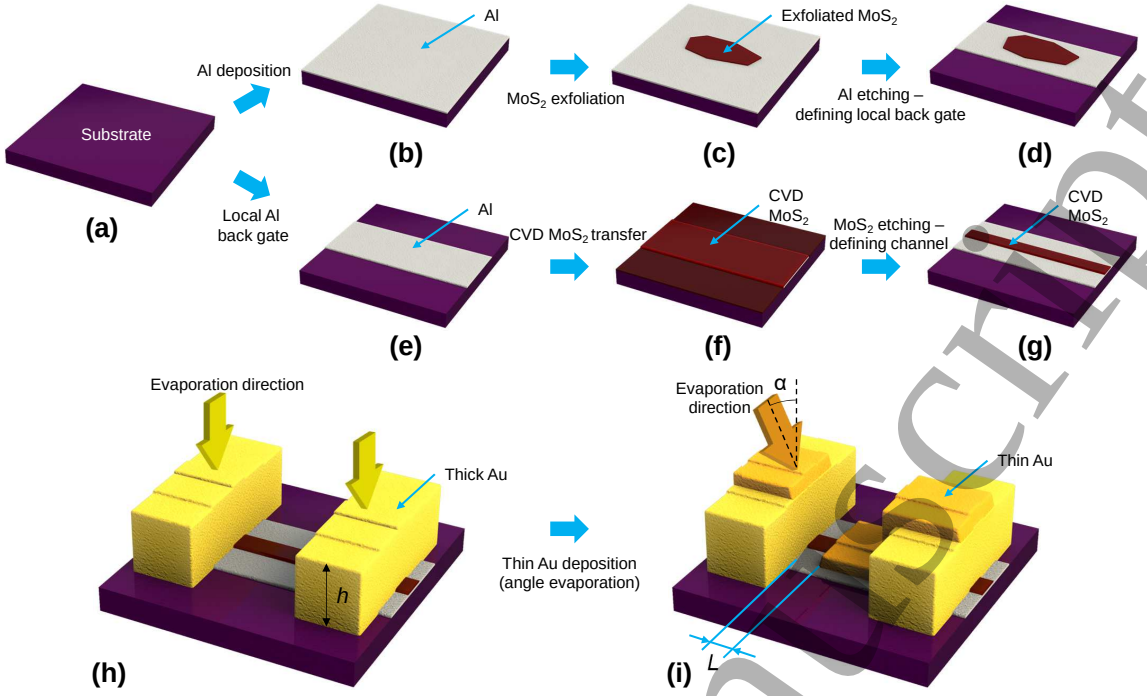


**Figure 1.** Schematic of the fabrication steps used to realize 10 nm $MoS_2$ FETs. (a) The devices were fabricated on standard $SiO_2$/Si substrates. (b) In the case of exfoliated $MoS_2$, the entire surface of the substrate was covered by a thin layer of Al deposited by electron-beam (e-beam) evaporation. A thin native oxide ($AlO_x$) layer was formed on the top surface of Al after the sample was exposed to ambient air. (c) $MoS_2$ was exfoliated on top of the $AlO_x$/Al layer. (d) A local back gate was defined after etching the $AlO_x$/Al gate stack around the exfoliated $MoS_2$ flakes. (e) In the case of CVD $MoS_2$, the gate structure was defined in the first step by patterning and lift off of Al. As in (b), the gate stack was formed by exposing the samples to air ambient. (f) CVD $MoS_2$ was transferred to the entire chip. (g) CVD $MoS_2$ was etched to define the channel. (h) Patterning and lift off were used to define thick source and drain Au contacts on top of the structures realized in (d) or (g). (i) A nanogap was formed next to the contact which shadows the $MoS_2$ channel from the material evaporated under angle $\alpha > 0$ with respect to the vertical axis of the sample.

inverters with 10-nm $MoS_2$ FETs which exhibited high voltage gain ($A_v \sim -50$) and input/output signal matching.

## 2. Results and Discussion

Fabrication of ultra-scaled $MoS_2$ FETs is schematically depicted in Fig. 1. In the case of exfoliated $MoS_2$, a thin (25 nm) Al layer was initially evaporated on a standard $SiO_2$/Si substrate (Fig. 1(a)-(b)). The atomic force microscopy (AFM) image of one such substrate is shown in Supporting Information Fig. S1. The substrate was then exposed to air ambient to form a native oxide ($AlO_x$) at the top surface of Al [10, 12]. The native oxide layer had a thickness $t_{ox} \sim 4$ nm and was used as a gate insulator. In the next step, $MoS_2$ was exfoliated on top of the $AlO_x$/Al gate stack (Fig. 1(c)). In

order to reduce the overlap between the gate and source/drain contacts, the gate stack was then etched away, apart from the areas supporting the $MoS_2$ flakes (Fig. 1(d)). In the case of CVD-grown $MoS_2$ FETs, the gates were already patterned in the first step (Fig. 1(e)) and then CVD $MoS_2$ was deposited on top (Fig. 1(f)). The FET channel was then defined by etching CVD $MoS_2$ (Fig. 1(g)).

In both cases, the source and drain contacts, separated by $\sim 1$ μm, were subsequently fabricated by standard lithography, evaporating a thick layer (thickness $h = 60$ nm) of Au (Fig. 1(h)). In the final step, a thin (22 nm) layer of Au was evaporated under tilt in order to create a small gap next to the contacts [18–21] which shadow the $MoS_2$ channels (Fig. 1(i)). The size of the gap was controlled by the evaporation angle $\alpha$ and the thickness of initial source and drain contacts ($h$). Therefore, the resolution of the initial lithographic process used to fabricate the initial source and drain contacts did not have any influence on the gap size. Gaps with the lengths $L_{\mathrm{ch}}$ between 10 and 20 nm were realized in this way.

Fig. 2(a) shows a nanogap between the source and drain contacts in one of the exfoliated multilayer $MoS_2$ FETs, immediately after the shadow evaporation (large area images are shown in Fig. S2 and Fig. S3 and tilted images in Fig. S4). The edges of the contacts, defining the gap, are not perfectly smooth due to unavoidable imperfections in the profile of the developed resist (used in the lithographic process to define the initial source and drain contacts) and finite grain size of the evaporated Au film. These imperfections limit the minimum gap size to $\sim 8$ nm in contacts realized on exfoliated $MoS_2$. At smaller gap sizes (Fig. S5 shows a 5-nm gap), the material protruding across the gap (as in the encircled part of the gap shown in Fig. 2(a)) may coalesce and short circuit the contacts. Even if not connected (as in Fig. 2(a)), such protrusions deteriorate the electrical properties of the FETs due to parasitic tunneling currents flowing between them. This is typically manifested in the reduction of the on/off ratio (Fig. 2(c)).

The electrical properties of the FETs were improved by thermal annealing. Fig. 2(b) shows the same section of the nanogap from Fig. 2(a) after annealing in vacuum. The protrusions which are not connected tend to recede to the corresponding contacts upon annealing, as evidenced by the encircled part of the gap in Fig. 2(b). Although this slightly increases the minimum gap size to $\sim 10$ nm on exfoliated $MoS_2$, it also significantly reduces the tunneling currents and improves the electrical properties of the FETs, as shown in Fig. 2(c). Annealed FETs exhibited $\sim 10$ times smaller drain off-current (due to reduced tunneling) but also higher drain on-current as annealing reduces the source and drain contact resistances [9]. This resulted in $\sim 100$ larger drain on/off current ratio (which increased from $10^3$ to $10^5$) and a smaller subthreshold swing after annealing.

The output curves of the nonannealed FETs exhibited very poor drain current saturation (Fig. S6) due to parasitic tunneling currents which flow in parallel to the channel drain current. On the other hand, the annealed FETs exhibited a very good saturation for such short devices, with output conductance $g_{\mathrm{d}} \sim 10$ S/m (normalized by the channel width $W$), as shown in Fig. 2(d) for $V_{\mathrm{GS}} < 1$ V. The highest measured

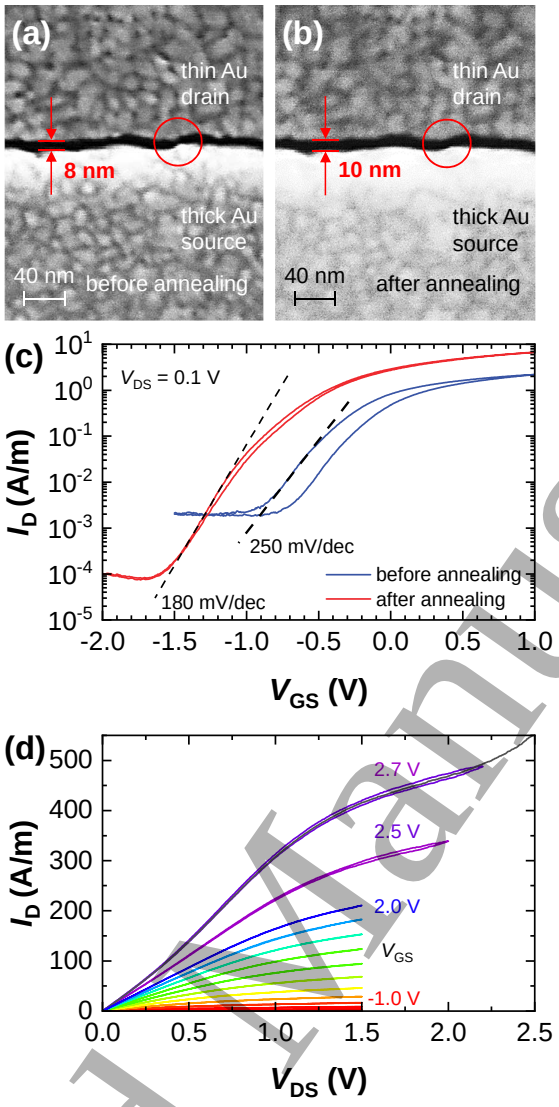


**Figure 2.** Nanogap in exfoliated $MoS_2$ FETs. (a) A scanning electron microscopy (SEM) image of an $\sim 8$ nm long nanogap separating the source and drain contacts. The top (thin) contact was obtained by e-beam evaporation of Au shadowed by the bottom (thick) contact creating the nanogap. The circle indicates protrusions responsible for tunneling across the gap. The FET was made on a $\sim 6$ nm thick exfoliated $MoS_2$ (Fig. S3). (b) The same nanogap after thermal annealing. The annealing melts sharp protrusions which defuse towards bulk metal, making the nanogap more uniform, as can be seen in the encircled area. (c) The transfer characteristics of the FET shown in (a) and (b) before (blue line) and after (red line) annealing, measured at $V_{DS} = 0.1$ V. Despite the removal of the tunneling sites, the on current increases almost three times due to the reduction of contact resistance [9]. The drain current on/off ratio improves by two orders of magnitude and subthreshold swing reduces from 250 mV/dec to 180 mV/dec after thermal annealing. (d) The output characteristics of the same 10 nm $MoS_2$ FET after annealing. The gate-source voltage values are 2.7 V (two measurements shown), 2.5 V, and in the range from $-1$ V to 2 V (with a step of 0.2 V). Despite large $V_{GS}$ and $V_{DS}$, the gate leakage current did not influence the drain current (Fig. S7).

drain current was $I_D = 560$ A/m, which is the highest demonstrated drain current in $MoS_2$ FETs in air ambient so far [10, 15, 22–29]. The largest transconductance was $g_m = 662$ S/m at $V_{DS} = 2$ V and $V_{GS} = 2.5$ V (Fig. 2(d)), while the highest intrinsic transistor gain was $A = g_m/g_d \sim 11$ on all output curves. The measured transconductance results in the highest extrinsic electric field mobility $\mu = 3$ cm$^2$/Vs. The obtained extrinsic mobility is small because it includes the contribution of the contact resistance, as discussed in the Methods section. Despite small extrinsic mobility, the transconductance is comparable to that of graphene field-effect transistors with a gate length of $\sim 1$ μm [30] due to a very short gate.

The obtained extrinsic electric field mobility in exfoliated multilayer $MoS_2$ FETs is comparable to that of short-channel devices comprising exfoliated monolayer $MoS_2$ [14]. However, multilayer $MoS_2$ cannot fully follow the surface roughness of the gate (Fig. S8). This reduced the direct contact between the $MoS_2$ channel and the gate which reduced the gate capacitance. The reduced gate capacitance leads to larger than expected [10, 13, 14, 31] subthreshold swing ($S_{th} \sim 180$ mV/dec) and drain induced barrier lowering ($\sim 230$ mV/V).

The ultra-scaled FETs were also made of CVD-grown monolayer $MoS_2$ [32]. The minimum gap size in such FETs was between 10 and 20 nm (Fig. 3(a) and Fig. S9), which was larger than that of the exfoliated $MoS_2$ FETs. We found that use of CVD $MoS_2$ required larger initial gaps because annealing was not very effective in eliminating the protrusions on CVD $MoS_2$. This is probably due to the pinning of protrusions on the imperfections in the CVD grown material and underlying roughness of the gate (which has more influence on the surface roughness of the CVD monolayer compared to the exfoliated multilayer $MoS_2$). However, CVD monolayer $MoS_2$ FETs were found to have larger drain current on/off ratio ($\sim 10^6$) and smaller subthreshold swing ($S_{th} \sim 120$ mV/dec) compared to the exfoliated multilayer $MoS_2$ FETs (Fig. 3(a)). This is because of the larger bandgap in monolayer $MoS_2$ with respect to multilayer $MoS_2$ and slightly larger gate length in CVD FETs. Use of CVD-grown material also allowed a large-scale fabrication of FETs, which was not possible with the exfoliated material. However, there are limitations in the large-scale fabrication of the FETs, as discussed in the Methods section and Fig. S10.

The largest measured drain current in CVD monolayer $MoS_2$ FETs was $I_D = 360$ A/m (Fig. 3(b)), which is comparable to the highest drain current reported for such FETs [10], even though the latter were obtained by pulsed measurements in vacuum; here, the measurements were performed in air ambient without pulsing voltages. The largest transconductance was $g_m = 170$ S/m at $V_{DS} = 2$ V and $V_{GS} = 1.6$ V (Fig. 3(b)), which resulted in the highest extrinsic electric field mobility $\mu = 1.2$ cm$^2$/Vs. In this case, the mobility was lower than that of the exfoliated FETs due to the additional processing step used to transfer $MoS_2$ from the growth substrate to the substrate on which the local back gates were prefabricated. This process (described in the Methods section) is not required for top-gated FETs, which were fabricated directly on the growth substrate [10], and it deteriorated the quality of the transferred CVD monolayer $MoS_2$.

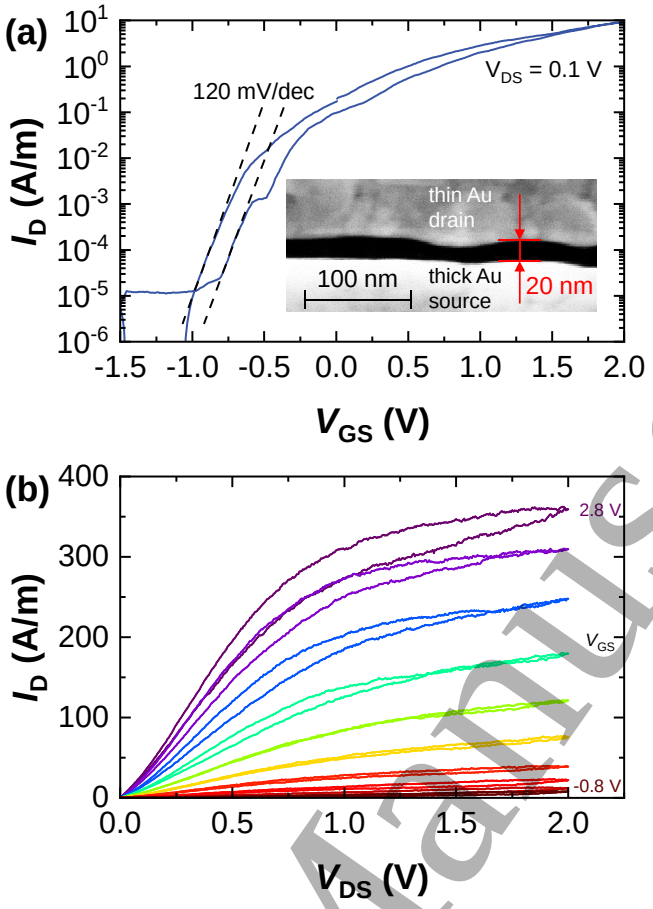


**Figure 3.** The electrical characteristics of 20 nm CVD monolayer $MoS_2$ FETs. (a) The transfer characteristic of the FET shown in the inset, measured at $V_{DS} = 0.1$ V. The gate leakage current did not influence the subthreshold swing but it was responsible for the constant drain current for $V_{GS} < -1$ V (Fig. S11). The inset shows an SEM image of a CVD monolayer $MoS_2$ FET with a channel length of 20 nm. (b) The output characteristics of the same FET measured at gate-source voltages in the range from $-0.8$ V to 2.8 V with a step of 0.4 V.

The ultra-scaled $MoS_2$ FETs were used to realize logic gates in the n-type depletion-load technology. Fig. 4(a) shows the static voltage transfer characteristics of an $MoS_2$ inverter. In most of the realized FETs, the threshold voltage was slightly negative ($V_{th} \sim -0.2$ V) leading to a weak conduction of the load FET (the top FET in the inverter in Fig. 4(a)) in which $V_{GS} = 0$ V. Besides, $V_{th} \sim -0.2$ V results in the threshold voltage of the logic gates $< V_{DD}/2$. At large enough positive input voltages ($V_{IN} > 0.4$ V), the driver FET (the bottom FET in the inverter) was therefore much more conductive than the load FET and the output voltage was approximately equal to zero, leading to a rail-to-rail operation. Small conductivity of the load FET and good saturation of the FETs led to a steep drop of the output voltage $V_{OUT}$ as the input voltage $V_{IN}$ is increased (at $V_{IN} \sim 0.15$ V). This resulted in a large voltage gain $A_v$ $-50$ (Fig. 4(b)), which is remarkably high for such short devices.

The threshold voltage of the logic gates, which was below $V_{DD}/2$, prevented

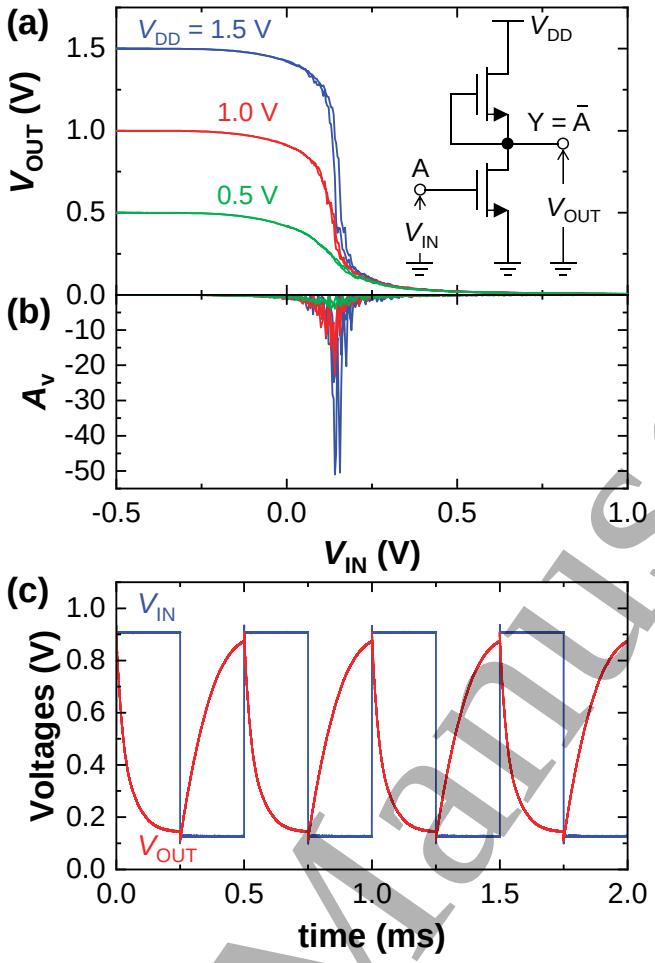


**Figure 4.** The ultra-scaled $MoS_2$ inverters in depletion-load technology. (a) The static voltage transfer characteristics (the output voltage $V_{OUT}$ vs. the input voltage $V_{IN}$) of an inverter at three different power supply voltages $V_{DD}$ of 0.5 V, 1 V, and 1.5 V. The inset shows the schematic of an inverter. (b) The calculated low-frequency voltage gain $A_v = dV_{OUT}/dV_{IN}$. (c) The digital waveforms measured in an inverter whose static voltage transfer characteristic is shown in Fig. S12. The waveforms demonstrate in/out signal matching capabilities of the inverter. The clock rate of the input signal is 2 kHz.

matching between the input and output signals, despite very high voltage gain. In addition, the current drive capabilities of the load FET were significantly reduced due to its poor conductivity. As a consequence, the realized logic gates could not be clocked above a few Hz, which is typical for this type of the load FETs [33]. This problem was overcome by using more conductive load FETs at $V_{GS} = 0$ V, i.e., the load FETs with a more negative threshold voltage. This is demonstrated in Fig. 4(c) which shows the digital waveforms measured in one of the inverters in which the load FET had $V_{th} = -0.4$ V. Due to better conductivity of the load FET, the output voltage decreased slower as the input voltage was increased, effectively shifting the threshold voltage of the logic gates to $\sim V_{DD}/2$ (Fig. S12). Although this reduced the voltage gain and output voltage swing (and therefore increased the static power dissipation), it allowed signal

matching, as shown in Fig. 4(c). In addition, a higher operating frequency was reached compared to that of the high-gain logic gates with low-conductivity load FETs [33], as demonstrated in Fig. 4(c). However, this frequency is still much smaller than the cutoff frequency of the highly conductive FETs (Fig. S13).

## 3. Conclusion

We have demonstrated facile and scalable technique for the fabrication of ultrashort channel $MoS_2$ FETs which does not require nanolithography. The technique is general (i.e., it can be applied to any semiconductor transistor channel) and based on shadowing evaporated material by the standard prefabricated source and drain contacts. We realized both exfoliated and CVD $MoS_2$ FETs in which the entire transistor channel, with a length between 10 and 20 nm, was gated. The realized $MoS_2$ FETs exhibit good drain current saturation demonstrating the suppression of the short-channel effects in atomically thin transistors. The ultra-scaled $MoS_2$ FETs were used to realize logic gates in the n-type depletion-load technology with a voltage gain of $\sim -50$. The load FETs with a higher current drive were used to improve the operating frequency and signal matching of the logic gates at the expense of the voltage gain. The tradeoff between the speed and voltage gain demonstrates a need for the implementation of the ultra-scaled FETs in future complementary metal-oxide-semiconductor (e.g., $MoS_2$) technology.

## 4. Methods

Degenerately doped Si chips with thermally grown 290 nm thick $SiO_2$ were used in the fabrication of the ultra-scaled $MoS_2$ FETs. Prior to the deposition of Al, the substrates were thoroughly cleaned in an acetone bath and rinsed with isopropanol. The gates were fabricated by thermal evaporation of 25 nm of Al in an e-beam evaporator at a base pressure of $1.2 \times 10^6$ mbar. After Al deposition, the samples were kept in air for one day to oxidize the top surface of Al. This created an $Al/AlO_x$ gate stack with a gate oxide capacitance $C_{ox} = 1.4$ μF/cm$^2$ [10,34]. Although such native gate oxide has larger surface roughness than the underlying $SiO_2$ substrate (Fig. S1), we found that the gate leakage current did not have influence on the drain current (Fig. S7 and Fig. S11) if the gate oxide voltage was kept below 2.8 V. The typical gate oxide breakdown voltage was $\sim 2.9$ V.

Both exfoliated and CVD $MoS_2$ were used in fabrication. Micromechanical exfoliation of $MoS_2$ (SPI supplies) was performed by a Scotch tape method directly on the substrates on which 25 nm of Al was previously evaporated (Fig. 1(c)). After exfoliation, $MoS_2$ flakes were located by an optical microscope and then characterized by an AFM (Veeco Innova) to find the thickness of the flakes. Due to a poor contrast of $MoS_2$ on Al, it was not possible to locate monolayer $MoS_2$ and therefore the flakes with thicknesses between 5 and 15 nm were used in device fabrication.

$MoS_2$ was grown directly on $SiO_2$ via solid-source CVD [27]. In particular, $SiO_2$ was

treated with hexamethyldisilazane, and then decorated $\sim$ 25 µL of 100 µM perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt. The substrate was placed face down on an alumina crucible with $\sim$ 0.5 mg of $MoO_3$ powder, and loaded in to a tube furnace 30 cm downstream of $\sim$ 100 mg of S powder. The tube was evacuated and flushed with Ar gas and brought back to atmospheric pressure. Temperature was ramped to 850 °C and held for 15 min with 30 sccm Ar flow, before being cooled to room temperature. After the growth, CVD $MoS_2$ was transferred from the growth substrate to the final substrate containing pre patterned gates (Fig. 1(f)). Due to a strong adhesion of the CVD grown $MoS_2$ to the growth substrate, the transfer to the final substrate required evaporation of 60 nm of Au [35,36] on $MoS_2$ and spin coating of a poly(methyl methacrylate) (PMMA) layer on top of Au. The resulting PMMA/Au/$MoS_2$ stack was picked up from the growth substrate by a polydimethylsiloxane (PDMS) stamp. Once the PMMA/Au/$MoS_2$ stack was detached from the growth substrate, it was placed on the final substrate. There, the entire stack was heated to 160 °C for 5 min to remove the PDMS stamp. PMMA was removed then in the acetone bath, followed by Au etching using KI:I solution (Sigma Aldrich). After etching of Au, the $MoS_2$ channel was defined by plasma etching using $SF_6$ (base pressure 80 mbar, flow rate 10 sccm, and power 50 W) for 25 sec. A larger hysteresis and smaller mobility in CVD $MoS_2$ FETs were attributed to the damaging effect of the transfer procedure.

All patterning was performed by e-beam lithography (Raith eLINE) at 10 kV using different types of PMMA (molecular weights between 250,000 and 950,000) as e-beam resists. However, high-resolution patterning was not required because the initially fabricated contacts had dimensions $\sim$ 1 µm. Any other low-resolution method (e.g., conventional optical lithography) could have also been used in the fabrication of the initial contacts.

In the case of exfoliated $MoS_2$, Al surrounding the $MoS_2$ flakes was etched away (Fig. 1(d)) to reduce the overlap between the gate and source/drain contacts, i.e., to reduce the gate leakage current and parasitic components. Tetramethylammonium hydroxide was used for 15 s to completely etch away 25 nm of Al. After etching, Al sample was kept in acetone for 2 hours to remove the PMMA mask.

The initial 60-nm thick Au source and drain contacts (Fig. 1(h)) were fabricated by evaporating Au at a normal incidence in the e-beam evaporator at a base pressure $\sim 1.2\times10^{-6}$ mbar. After fabricating the initial thick Au contacts, the second lithography process was used to define the pattern for thin Au contacts (Fig. 1(i)). A thin layer of Au (22 nm) was deposited in the same e-beam evaporator, but this time the samples were tilted by $\alpha = 15°$ with respect to the direction of the evaporated Au. The directionality of the e-beam evaporation process effectively increases shadowing [37,38] both from the resist and thick contacts resulting in an oblique profile of the contacts, as discussed in Fig. S4.

The device fabrication was performed in parallel, i.e., all FETs on a wafer were fabricated at the same time. However, successful large-scale fabrication of the FETs also requires maintaining a constant gate length across a wafer. The gate length uniformity

is affected by the thickness uniformity of the initial thick contacts deposited by e-beam evaporation [39]. The gate length uniformity of our process technology is discussed in Fig. S10 which demonstrates that smoother substrate is required for better uniformity. Therefore, the successful large-scale fabrication of the FETs would require very smooth deposition of the gate material, e.g., by atomic layer deposition.

After the fabrication of nanogaps, the samples were annealed at 250 °C in vacuum (pressure $< 5\times10^{-6}$ mbar) for 1 hour. Annealing cleaned the nanogaps from protrusions and improved metal contact to $MoS_2$. Thermal annealing was performed in vacuum to prevent any damage to $MoS_2$ due to oxygen or humidity at higher temperature. The samples were heated to 250 °C at a rate of 10 °C/min. After annealing, the samples were allowed to spontaneously cool down to room temperature in vacuum.

The extrinsic electric-field mobility was calculated from the measured transfer curves. We fabricated both long ($L \sim 1$ μm) and short ($L \sim 10$ nm) channel FETs on a global $SiO_2$/Si back gate as a reference. We found that typical extrinsic mobility in long channel FETs on $SiO_2$ was $\sim 55$ cm$^2$/Vs reducing down to $\sim 4$ cm$^2$/Vs in short channel FETs. The reason for such small extrinsic mobility in short-channel devices is the contact resistance which is comparable to the resistance of short channels. The obtained value of $\sim 4$ cm$^2$/Vs on $SiO_2$ was close to $\sim 3$ cm$^2$/Vs obtained in short-channel devices on $AlO_x$.

All electrical measurements were performed in air ambient in FormFactor probe stations EP6 and Summit 11000. The electrical characterizations of the FETs and inverters were performed by Keithley 2611B source-measure units, a function generator (Tektronic AFG 3022B), and an oscilloscope (Keysight DS09064A). The small hysteresis in the samples was a consequence of adsorption of water from humidity in air [40–42] and charge traps in the gate oxide [43]. The SEM imaging was performed in Raith eLINE at 10 kV. The inverters were realized by externally connecting the fabricated FETs.

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