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Zhou, J. orcid.org/0000-0003-3578-2121, Do, H.-B. orcid.org/0000-0003-3274-5050 and De Souza, M.M. orcid.org/0000-0002-7804-7154 (2023) Impact of an underlying 2DEG on the performance of a p-channel MOSFET in GaN. ACS Applied Electronic Materials, 5 (6). pp. 3309-3315. ISSN 2637-6113

https://doi.org/10.1021/acsaelm.3c00350

ACS APPLIED ELECTRONIC MATERIALS

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Article

Impact of an Underlying 2DEG on the Performance of a p-Channel MOSFET in GaN

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Cite This: *ACS Appl. Electron. Mater.* 2023, 5, 3309−3315

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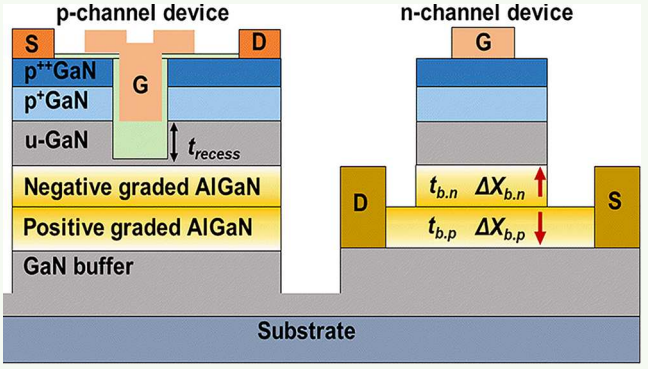
ABSTRACT: The influence of an underlying 2-dimensional electron gas (2DEG) on the performance of a normally off p-type metal oxide semiconductor field effect transistor (MOSFET) based on GaN/AlGaN/GaN double heterojunction is analyzed via simulations. By reducing the concentration of the 2DEG, a greater potential can be dropped across the GaN channel, resulting in enhanced electrostatic control. Therefore, to minimize the deleterious impact on the on-state performance, a composite graded back-to-back AlGaN barrier that enables a trade-off between n-channel devices and Enhancement-mode (E-mode) p-channel is investigated. In simulations, a scaled p-channel GaN device with L_G = 200 nm, L_{SD} = 600 nm achieves an I_{ON} of 65 mA/mm, an increase of 44.4% compared to a device with an AlGaN barrier with fixed Al mole fraction, I_{ON}/I_{OFF} of ∼10^{12}, and $|V_{th}|$ of | − 1.3 V|. For the n-channel device, the back-to-back barrier overcomes the reduction of I_{ON} induced by the p-GaN gate resulting in an I_{ON} of 860 mA/mm, an increase of 19.7% compared with the counterpart with the conventional barrier with 0.5 V positive V_{th} shift.



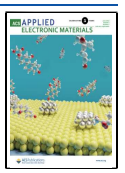
KEYWORDS: *2DHG, E-mode, GaN, MOSFET, p-channel, n-channel, AlGaN, graded channel*

INTRODUCTION

Gallium nitride (GaN) power devices utilizing a two-dimensional electron gas (2DEG) are promising in applications requiring high voltage, high speed, and low power consumption due to the superior wide-bandgap material properties in comparison with silicon.[1−3] The monolithic integration of a power device with its gate driver is required to suppress oscillations during high-frequency operation that can irrevocably damage the device.[4] GaN-based p-channel devices offer the possibility of on-chip complementary logic; however, owing to the low mobility, poor current density, and high resistivity of contacts, such devices are not yet in manufacture.

Several p-channel devices with polarization-induced two-dimensional hole gas (2DHG) at the heterointerface have been reported.[5−10] Similar to a 2DEG, the 2DHG has characteristics of high density and temperature independence.[11] However, to achieve a GaN-based complementary metal-oxide-semiconductor (CMOS) technology, p-channel devices with high on-current, enhancement-mode (E-mode), and high on/off ratio are desired to be integrated with a related n-channel power device on the same platform.[7,12−15] Recently, due to the commercialization of E-mode p-GaN gate high electron mobility power transistors (HEMTs),[1] p-channel MOSFETs (pFETs) with the same p-GaN/AlGaN/GaN-based epitaxial structure have attracted great interest.[16−19] Among them, E-mode pFETs with (I_{ON}/I_{OFF}) of 3 × 10^8 and a high threshold voltage (V_{th}) of | − 2.2 V| were demonstrated.[19] However, the improved on-current (I_{ON}) of 18.5 mA/mm by 1.5 nm AlN spacer[19] is still much lower than that of a generic E-mode n-channel device.[20] Moreover, in a GaN/AlGaN/GaN-based architecture, an I_{ON} of 125 mA/mm was attained at V_{DS} = − 20 V for the p-FETs with Schottky gate structure,[21] but the limitation of leakage in a Schottky gate causes I_{ON}/I_{OFF} < 10^5. On the other hand, an ultrawide bandgap semiconductor AlN/GaN/AlN-based platform shows potential to increase the current density by maximizing the polarization discontinuity[22−24] and indicates excellent output power performance in mm-wave integrated circuits,[25,26] which makes it promising in RF and high-power application. A remarkable I_{ON} of 428 mA/mm was obtained in a pFET on this platform,[24] with an I_{ON}/I_{OFF} of 10^2 and V_{th} of 4 V. Recently, I_{ON} > 100 mA/mm and I_{ON}/I_{OFF} > 10^7 were achieved by a self-aligned gate and FinFET architecture based on the p-GaN/u-GaN/AlGaN/

Received: March 15, 2023
Accepted: May 29, 2023
Published: June 8, 2023



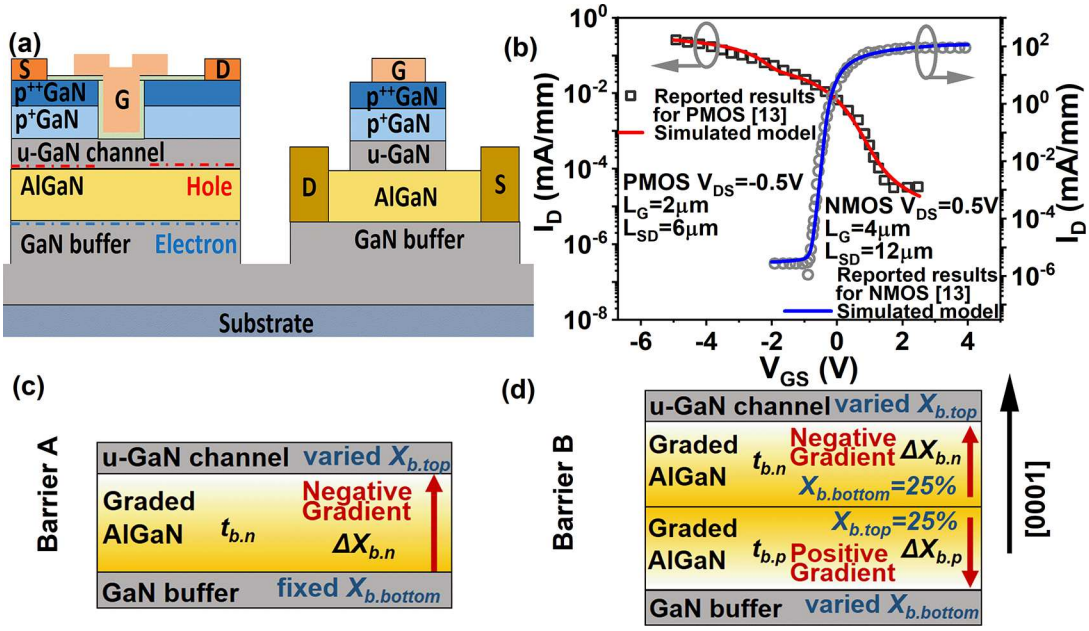


Figure 1. (a) Schematic of the benchmarked p-FET and n-FET from.[13] (b) Verification of the simulation models with experimental $I_D - V_G$ characteristics[13] of p-FET and n-FET in Silvaco TCAD. Reprinted with permission from ref 13. Copyright [2020][*IEEE Electron Device Lett.*]. The platform structure consists of: (c) Barrier A: A single negatively graded AlGaN. (d). Barrier B: Composite AlGaN, the upper layer is negatively graded AlGaN with $X_{b.\ bottom}$ = 25% on top of a positively graded AlGaN with fixed $X_{b.\ top}$ = 25%.

GaN epitaxial structure.[27] However, normally off operation was achieved by a 40 nm fin width and 50 nm gate recess which can easily convert the device into D-mode if not accurately controlled, as pointed out by the authors. Moreover, a p-GaN/u-GaN/1.5 nm AlN/AlGaN-based p-channel self-aligned FinFET with a fin width of 20 nm was shown to realize an I_{ON} of 300 mA/mm but an I_{ON}/I_{OFF} ratio of only 200.[28] Furthermore, besides gate length, reducing gate width can improve the mobility and current density in GaN HEMTs, and the effective modulation of I_{ON}, I_{OFF}, and electric field makes the gate width a key parameter for further optimization of GaN HEMTs.[29]

Considering the commercial maturity of the p-GaN/AlGaN/GaN platform and to avoid impurity scattering at the p-GaN/AlGaN interface, a p-GaN/u-GaN/AlGaN/GaN epitaxial structure, with the potential for monolithic integration without any regrowth, is selected in this work. In addition, the graded AlGaN layer can benefit the linearity and breakdown voltage of GaN HEMTs in RF applications.[30] We examine the impact of the densities of 2DHG and 2DEG on the performance of a p-channel FET via simulation and explore graded AlGaN barriers to alleviate the tradeoff between the densities of the 2DHG and 2DEG.

METHODOLOGY

Figure 1a shows the schematic of the platform consisting from top to bottom of 20 nm of p^{++}GaN doped with Mg concentration of 6×10^{19} cm^{-3}, 50 nm of p^{+}GaN (Mg: 1×10^{19} cm^{-3}), 20 nm of undoped GaN (u-GaN) as a channel layer (t_{ch}), and 20 nm of $Al_{0.2}Ga_{0.8}N$ barrier layer (t_b) below which lies a 150 nm-thick u-GaN and buffer layer reported in ref 13. Our simulations are first benchmarked based on the reported epitaxial stack in Silvaco TCAD using a gate length (L_G) of 2 and 4 μm for p-channel and n-channel devices, respectively, reported in ref 13. The source to drain distance (L_{SD}) is 6 and 12 μm for the p- and n-FET, respectively. In the p-FET, the gate oxide is 20 nm Al_2O_3, with the recessed gate etched out of the p^{++}GaN and p^{+}GaN to support E-mode operation. Based on Hall measurements, a mobility value of 10 cm^2/Vs of holes in a 2DHG is used.[13] Figure S1 reveals that the mobility of holes in the 3DHG is ~10.4 cm^2/Vs and its peak value changes relatively with the density of 3DHG in the graded AlGaN in our simulation model (Supporting Information A). In addition, a negative fixed interface charge and trap density at the oxide/GaN interface of 6.4×10^{12} and 3×10^{12} cm^{-2}, respectively, are introduced in our model to match the reported experimental $I_D - V_{GS}$ curves in Figure 1b.[13] Two kinds of graded AlGaN barriers are introduced in this work. Along the [0001] growth direction, the negatively graded AlGaN has an Al mole fraction (X_b) that is linearly reduced from the bottom ($X_{b.\ bottom}$, close to the buffer layer) to the top ($X_{b.\ top}$, close to the u-GaN channel), viz., $\Delta X_{b.\ n} = X_{b.\ bottom} - X_{b.\ top}$. On the other hand, a positively graded AlGaN has an opposite structure, i.e., $\Delta X_{b.\ p} = X_{b.\ top} - X_{b.\ bottom}$. In addition, several new kinds of composite barriers with varied thickness of negatively graded barriers ($t_{b.\ n}$) and positively graded barrier ($t_{b.\ p}$) are listed in Table 1. Barrier A is a single negatively graded AlGaN layer with fixed $X_{b.\ bottom}$ and varied $X_{b.\ top}$ displayed in Figure 1c. Figure 1d exhibits a dual back-to-back graded AlGaN Barrier B, and the upper layer is negatively graded AlGaN with 25% $X_{b.\ bottom}$ and changed $X_{b.\ top}$, whereas the layer beneath is positively graded AlGaN with 25% $X_{b.\ top}$ and varied $X_{b.\ bottom}$. $\Delta X_{b.\ p}$ is kept the same as $\Delta X_{b.\ n}$. In this work, our assumption of a 4.95% Al/nm gradient[31] and 5 nm graded AlGaN with 23% $\Delta X_{b.\ p}$[32] make the 5 nm graded AlGaN with 25% gradient to be practically possible. Considering that the p-GaN gate in n-FETs on this platform requires layers to be etched up to the positively graded AlGaN, a precise etch stop at the negative/positively graded AlGaN interface is essential.

https://doi.org/10.1021/acsaelm.3c00350
ACS Appl. Electron. Mater. 2023, 5, 3309−3315

Table 1. Details of Optimized Barrier Layers

ID	barrier parameters
barrier A	negatively graded AlGaN
barrier A1	$t_{b.\ n}$ = 20 nm, $X_{b.\ bottom}$ = 20%
arrier A2	$t_{b.\ n}$ = 20 nm, $X_{b.\ bottom}$ = 25%

ID	upper layer parameters	lower layer parameters
barrier B	negatively graded AlGaN, $X_{b.\ bottom}$ = 25%	positively graded AlGaN, $X_{b.\ top}$ = 25%
barrier B1	$t_{b.\ n}$ = 5 nm	$t_{b.\ p}$ = 15 nm
barrier B2	$t_{b.\ n}$ = 10 nm	$t_{b.\ p}$ = 10 nm
barrier B3	$t_{b.\ n}$ =1 5 nm	$t_{b.\ p}$ = 5 nm

RESULTS AND EVALUATION

To examine the influence of the underlying 2DEG density on the performance of p-FETs, the $Al_{0.2}Ga_{0.8}N$ barrier layer of the epitaxial structure in Figure 1a is replaced by Barrier A1, whereas the effects of a single positively graded AlGaN (counterpart of Barrier A) on both n- and p-channel FETs are shown in Figure S2 (Supporting Information B). Figure 2a reveals that the hole density (n_H) increases as the underlying electron density (n_E) is reduced by an increase of $\Delta X_{b.\ n}$. Although a 1.5 times improvement is achieved for n_H with 10% $\Delta X_{b.\ n}$, n_E reduces dramatically by 12 orders and below a value of 10/cm^2, which will severely degrade n-channel devices. According to Figure 2b, for Barrier A1, when $\Delta X_{b.\ n}$ is increased to 8%, the on-current ($|I_{ON}|$) of the PMOS is doubled compared with the standard device with $Al_{0.2}Ga_{0.8}N$ barrier at V_{DS} = − 0.5 V, whereas the on/off ratio (I_{ON}/I_{OFF}) reduces from 10^5 to 10^0. In contrast, a threefold drop of I_{ON} occurs in the n-channel device with Barrier A1 as $\Delta X_{b.\ n}$ is raised from 0 to 8% as shown in the inset of Figure 2b, which means the negatively graded barrier unilaterally benefits I_{ON} for p-FETs. Moreover, unlike in p-FETs, I_{ON}/I_{OFF} in n-FETs is immune to the changes of $\Delta X_{b.\ n}$ and n_E. The reason is because although graded AlGaN barriers redistribute channel carriers, the off-state current (I_{OFF}) of n-channel devices, in practice, is mainly affected by traps in the buffer layer- or surface-related conduction.[33]

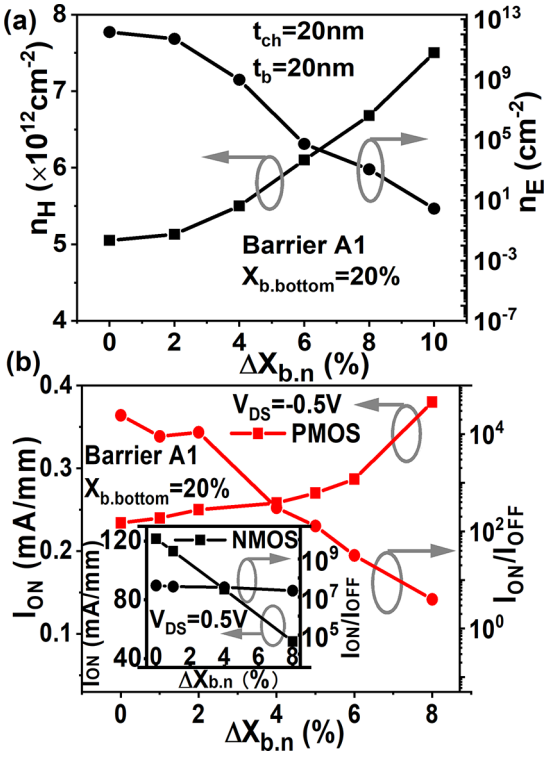


Figure 2. (a) n_H in p-channel and n_E in n-channel with respect to a change in $\Delta X_{b.\ n}$ based on the platform with Barrier A1. (b) I_{ON} and I_{ON}/I_{OFF} as a function of $\Delta X_{b.\ n}$ at V_{DS}= −0.5 V for PMOS with Barrier A1. The inset indicates I_{ON} and I_{ON}/I_{OFF} as a function of $\Delta X_{b.\ n}$ at V_{DS} = 0.5 V for NMOS with Barrier A1.

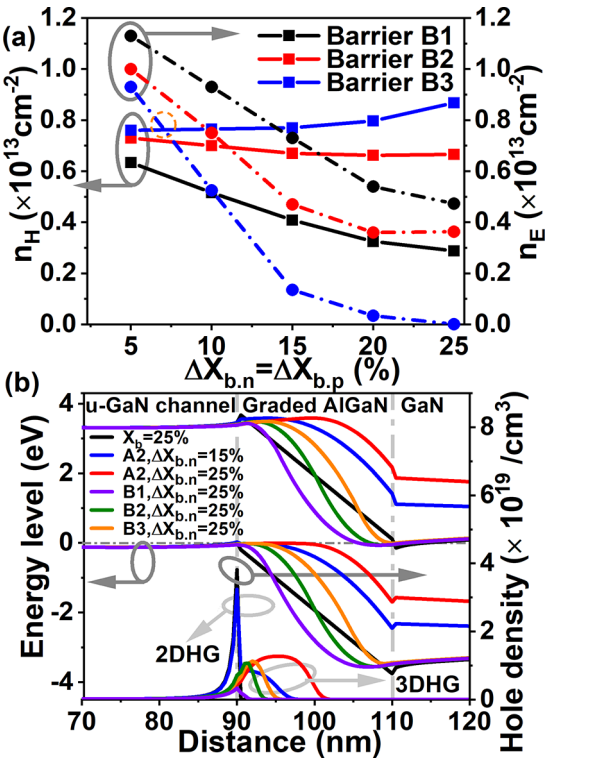


Figure 3. (a) Comparison of n_H and n_E as a function of $\Delta X_{b.\ n}$ in the composite AlGaN barriers of t_b = 20 nm that consist of Barriers B1, B2, and B3. (b) Comparison of band diagram and distribution of hole concentration between the devices with fixed $Al_{0.25}Ga_{0.75}N$ barrier layer, Barrier A2 with 15 and 25% $\Delta X_{b.\ n}$ and Barriers B1, B2, and B3 with 25% $\Delta X_{b.\ n}$ at V_g = V_d = 0 V.

Figure 3a demonstrates that the hole density (n_H) increases as the underlying electron density (n_E) is reduced by an increase of $\Delta X_{b.\ n}$. Although a 1.5 times improvement is achieved for n_H with 10% $\Delta X_{b.\ n}$, n_E reduces dramatically by 12 orders and below a value of 10/cm^2, which will severely degrade n-channel devices. According to Figure 2b, for Barrier A1, when $\Delta X_{b.\ n}$ is increased to 8%, the on-current ($|I_{ON}|$) of the PMOS is doubled compared with the standard device with $Al_{0.2}Ga_{0.8}N$ barrier at V_{DS} = − 0.5 V, whereas the on/off ratio (I_{ON}/I_{OFF}) reduces from 10^5 to 10^0. In contrast, a threefold drop of I_{ON} occurs in the n-channel device with Barrier A1 as $\Delta X_{b.\ n}$ is raised from 0 to 8% as shown in the inset of Figure 2b, which means the negatively graded barrier unilaterally benefits I_{ON} for p-FETs. Moreover, unlike in p-FETs, I_{ON}/I_{OFF} in n-FETs is immune to the changes of $\Delta X_{b.\ n}$ and n_E. The reason is because although graded AlGaN barriers redistribute channel carriers, the off-state current (I_{OFF}) of n-channel devices, in practice, is mainly affected by traps in the buffer layer- or surface-related conduction.[33]

This one-way gain makes the single-graded barrier layer disadvantageous to p- or n-channel devices and complementary integration, and requires an additional positively graded AlGaN below the negatively graded AlGaN layer (Figure 1d) as investigated in Figure 3a. It is obvious from Figure 3a that with Barrier B, both n_E and n_H show degradation with increased $\Delta X_{b.\ n(b.\ p)}$ when the thickness of the positively graded AlGaN $t_{b.\ p}$ increases, which means polarization-induced holes and electrons in a back-to-back graded AlGaN with optimized $t_{b.\ n}$, $t_{b.\ p}$, and $\Delta X_{b.\ n(b.\ p)}$ are mutually restricted instead of unilaterally suppressed. In this structure, the optimized tradeoff points between n_H and n_E are obtained in Barrier B3 with $\Delta X_{b.\ n(b.\ p)}$ = 7% resulting in a concentration of ~7.8 × 10^{12}cm^{-2}for both holes and electrons.

Figure 3b demonstrates that the hole quantum well is weakened by the negatively graded barrier layer at the u-GaN channel/AlGaN barrier interface. When comparing $Al_{0.25}N_{0.75}$

https://doi.org/10.1021/acsaelm.3c00350
ACS Appl. Electron. Mater. 2023, 5, 3309−3315

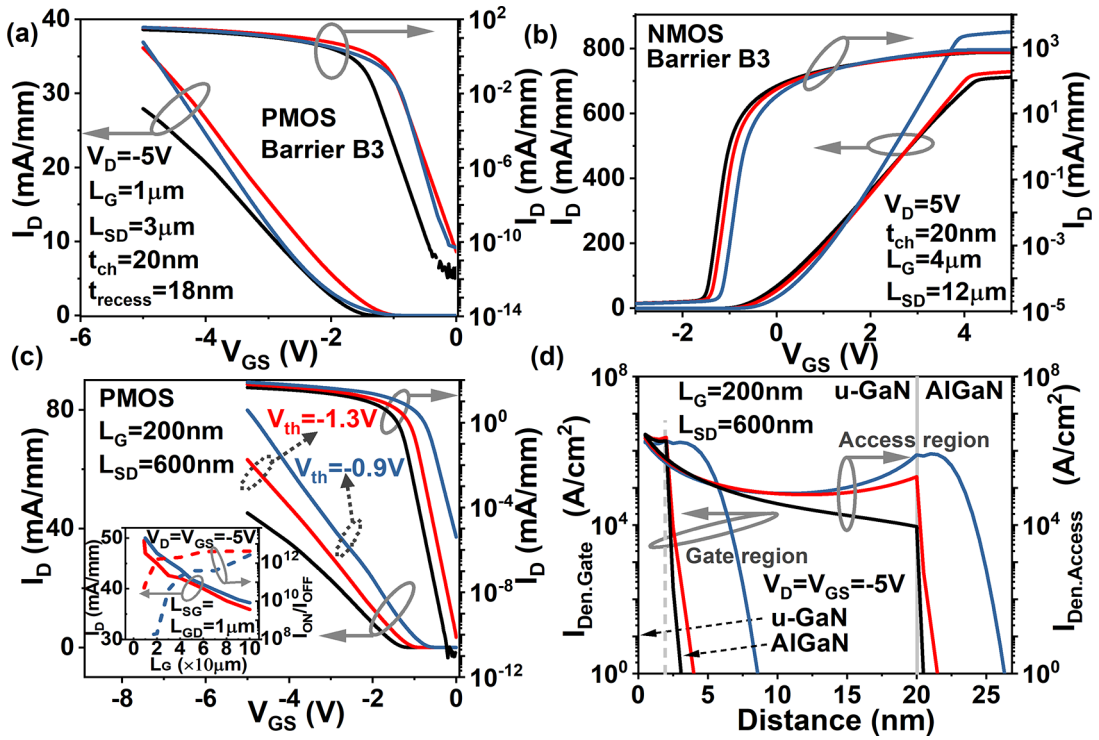


Figure 4. Black line: fixed $Al_{0.25}Ga_{0.75}N$ barrier layer; Red line: Barrier B3 with 7% $\Delta X_{b.\,n(b.\,p)}$; Blue line: Barrier B3 with 25% $\Delta X_{b.\,n(b.\,p)}$. (a) Comparison of the transfer characteristics in linear and log scale between PMOS with different barriers at L_G = 1 μm, L_{SD} = 3 μm, t_{recess} = 18 nm, and V_D = − 5 V. (b) $I_D - V_{GS}$ characteristics in log and linear scale of n-channel devices based on the same platform as Abstract figure at L_G = 4 μm, L_{SD} = 12 μm, and V_D = 5 V. (c) Comparison of the $I_D - V_{GS}$ curves in linear and log scale between the scaled PMOS with $Al_{0.25}Ga_{0.75}N$ and Barrier B3 at L_G = 200 nm, L_{SD} = 600 nm, t_{recess} = 18 nm, and V_D = − 5 V. The inset reveals I_D and I_{ON}/I_{OFF} at $V_D = V_{GS}$ = − 5 V with a change in gate length with fixed $L_{SG} = L_{GD}$ = 1 μm for PMOS with Barrier B3. (d) Comparison of current density around the u-GaN channel/AlGaN interface under the gate and access region between PMOS with various barriers at L_G = 200 nm, L_{SD} = 600 nm, and $V_D = V_{GS}$ = − 5 V.

with Barrier A2, the larger $\Delta X_{b.\,n}$ introduces a curvature of the barrier layer, resulting in the quantum well at the u-GaN/AlGaN junction becoming flatter and wider. It is observed that in Barrier A2, this "flat" quantum well not only accumulates a 2DHG at the u-GaN/AlGaN interface but also induces a three-dimensional hole gas (3DHG) in the barrier layer. It is well known that a graded barrier layer results in polarization doping without impurity dopants, which can improve the conductivity of the graded layer.[34] In addition, as $\Delta X_{b.\,n}$ reaches the maximum value of 25%, the 2DHG at the u-GaN/AlGaN interface in Barrier A2 disappears and only a broad and flat 3DHG distribution in the barrier layer is observed. This 3DHG also broadens the channel width to achieve a higher current density in p-FETs. However, the conduction band at the AlGaN/GaN buffer interface is raised away from the Fermi level in Barrier A2 due to the large $\Delta X_{b.\,n}$, which contributes to the potential in the barrier layer being shifted toward negative values and the hole confinement subsequently reduced in Barrier A2. As a result, the ability of the polarization field for blocking punch-through leakage paths into the buffer layer is weakened.

On the other hand, when the positively graded AlGaN is introduced, it is seen from Figure 3b that the conduction band reverts to the Fermi level at V_{GS} = 0 V and lies below the Fermi level at the AlGaN/GaN interface with an extension into the AlGaN barrier layer. The band offset in Barrier B with a thicker $t_{b.\,p}$ is larger and sharper. Consequently, the width and peak of the 3DHG across the negatively graded barrier are limited by $t_{b.\,p}$ as shown in Figure 3b. Thus, despite the maximum $\Delta X_{b.\,n}$, n_H still reduces with larger $t_{b.\,p}$ as Figure 3a indicates. Furthermore, Figure 3b illustrates that based on Barriers B2&B3 with 25% $\Delta X_{b.\,n(b.\,p)}$, quantum wells at the GaN channel/AlGaN and AlGaN/GaN buffer interfaces both turn "flat" and are pinned to the Fermi level with a large band offset at the AlGaN/GaN interface. Consequently, the distributions of the potential and polarization-induced charges are rebuilt in the barrier layer with excellent hole confinement in the channel, which is surmised to suppress the leakage in p-channel devices.

Abstract figure displays the new back-to-back graded AlGaN barrier-based platform for complementary integration. To achieve an E-mode and high I_{ON}/I_{OFF} for PMOS, a gate recess depth in the u-GaN channel layer (t_{recess}) of 18 nm is used. Moreover, in n-channel devices, to prevent degradation of on-current caused by the reduced n_E as shown in Figure 3a, the top negative AlGaN is etched away beneath the p-GaN gate. Barrier B3 with a tradeoff of 7% $\Delta X_{b.\,n}$ and a maximum of 25% $\Delta X_{b.\,n}$ are applied to NMOS with L_G = 4 μm and scaled PMOS with L_G = 1 μm as shown in Figure 4a,b. Figure 4a reveals that the on-state current density of p-channel devices with Barrier B3 is increased compared to the counterpart with a fixed Al mole fraction due to the polarization doping and enlarged n_H by a negatively graded AlGaN. In addition, unlike the deterioration of I_{ON}/I_{OFF} in a single negatively graded AlGaN, $I_{ON}/I_{OFF} > 10^{12}$ with Barrier B3 and the large $\Delta X_{b.\,n}$ prove that the positively graded AlGaN improves hole confinement and band offset in the composite AlGaN barrier to suppress the leakage current into the GaN buffer layer in the PMOS in Figure 3b.

https://doi.org/10.1021/acsaelm.3c00350
ACS Appl. Electron. Mater. 2023, 5, 3309−3315

At $V_D = V_{GS} = 5$ V, I_{ON} of n-channel devices with Barriers B3 is improved by 19.7% compared with a device with fixed Al mole fraction as shown in Figure 4b. Similar to the role of a negatively graded AlGaN in PMOS, the positively graded AlGaN enhances the channel depth with 3DEG polarization doping and redistributes the potential and electrons in n-channel devices, which means the mutual limitation between the hole and electron channels in the GaN/AlGaN/GaN-based epitaxial platform and the decrease of I_{ON} induced by the p-GaN gate in n-channel devices is overcome by the back-to-back graded AlGaN. In addition, n-channel devices with Barrier B3 all reveal a drift of V_{th} toward the positive direction with no change in the off-state current level. The reason is that the negatively graded AlGaN in the p-GaN gate region depletes the electrons below and I_{OFF} in n-FETs is dominated by surface-related conduction and buffer layer characteristics.[33] To realize a better gate electrostatic control for n-FETs, the thinner u-GaN channel thickness and fin-gate structure are feasible. Moreover, Figure S3b illustrates the effects of under-etch and over-etch of the p-GaN gate region on the performance of n-FETs (Supporting Information C). The maximum degradation of I_{ON} observed is ∼30%. Furthermore, we have shown that the figure of merit (FOM = $V_{BV}^2/R_{on,\,sp}$) can be improved by 3 times in a GaN power HEMT with the back-to-back graded AlGaN compared to the one with a conventional $Al_{0.25}Ga_{0.75}N$.[35]

The impact of gate length scaling is investigated at $V_D = V_{GS} = -5$ V in Figure 4c, via a Barrier B3-based PMOS, with L_G = 200 nm and L_{SD} = 600 nm, which is shown to increase $|I_{ON}|$ from 45mA/mm, for a fixed $Al_{0.25}Ga_{0.75}N$ barrier, to 65mA/mm with large I_{ON}/I_{OFF} of ∼10^{12} and threshold voltage $|-V_{th}|$ of $|-1.3$ V|. A further improvement of $|I_{ON}|$ of 23% with $|-V_{th}|$ of $|-0.9$ V| with Barrier B3 is possible with 25%$\Delta X_{b.\,n}$; however, I_{ON}/I_{OFF} decreases significantly by 5 orders, which indicates that in a shorter gate, it is difficult to deplete holes with a wider channel depth. The inset of Figure 4c illustrates that $|I_{ON}|$ of the PMOS with Barrier B3 of 7% $\Delta X_{b.\,n}$ is increased by 39% when L_G is reduced from 1 μm to 90 nm with source-to-gate (L_{SG}) and gate-to-drain (L_{GD}) length maintained at 1 μm. Meanwhile, I_{ON}/I_{OFF} of the PMOS with Barrier B3 of 7%$\Delta X_{b.\,n}$ stays above 10^{12} as $L_G \geq 200$ nm. The inset of Figure 4c also indicates that although the larger hole spread of Barrier B3 of 25%$\Delta X_{b.\,n}$ enhances $|I_{ON}|$ during scaling of L_G, I_{ON}/I_{OFF} is worsened significantly owing to insufficient depletion region across the 3DHG slab.

Figure 4d demonstrates a comparison of the current density distribution from a u-GaN channel to the AlGaN barrier under the gate region ($I_{Den.\,Gate}$) and the access region between the gate and drain ($I_{Den.\,Access}$) in a PMOS with $Al_{0.25}Ga_{0.75}N$ and Barrier B3 at 200 nm L_G. In Figure 4d, at −5 V of V_D and V_{GS}, $I_{Den.\,Gate}$, and $I_{Den.\,Access}$ both achieve a spread distribution across the AlGaN barrier with Barrier B3 with 25% $\Delta X_{b.\,n}$-based PMOS, which proves that the extended "flat" quantum well at the u-GaN/AlGaN interface. This occurs because a large gradient leads to holes drifting into the negative barrier layer instead of the limited 2-dimensional transport direction in the abrupt quantum well and also leakage currents are more likely to flow through these areas. Furthermore, 25% $\Delta X_{b.\,n}$ induces the widest 3DHG slab across the barrier, which results in an improved barrier conductivity and broadened current flow path that is difficult to be depleted and controlled by a short gate. Therefore, the leakage current is more controllable in Barrier B3 with 7% $\Delta X_{b.\,n}$ during gate scaling. Utilizing a fin gate configuration has the potential to suppress the leakage current and take full advantage of the back-to-back graded AlGaN barrier with large gradient.

CONCLUSIONS

This work provides a new back-to-back graded barrier platform for GaN-based CMOS. It is seen that the underlying 2DEG of PMOS is lowered by increasing $\Delta X_{b.\,n}$ in the negatively graded AlGaN buffer layer, which results in a significantly higher on-current density. A recess gate E-mode p-channel MOSFET with L_G = 200 nm and t_{recess} = 18 nm demonstrates $|I_{ON}|$ = 65mA/mm, $I_{ON}/I_{OFF} \approx 10^{12}$ and $|-V_{th}| = |-1.3$ V| is realized by the back-to-back graded barrier with an optimum 7% $\Delta X_{b.\,n(b.\,p)}$. Furthermore, for the back-to-back graded AlGaN barrier layer, not only does the negatively graded AlGaN on the top result in high current density and conductivity in p-channel devices but also the positively graded AlGaN below contributes to a rise of the on-state current by 19.7% in n-channel devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.3c00350.

Mobility model for 2DHG and 3DHG; effects of single positively graded barrier on n-FETs and p-FETs; influences of the under-etch and over-etch for p-GaN gate region on n-FETs (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was motivated by the EPSRC through Challenge Network Grant CN/FEAS/PCON.

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