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Evaluation of turn-off d*V*/d*t* controllability and switching characteristics of 1.2 kV GaN polarisation superjunction heterostructure field-effect transistors

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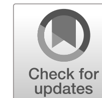

Evaluation of turn-off d*V*/d*t* controllability and switching characteristics of 1.2 kV GaN polarisation superjunction heterostructure field-effect transistors

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Gallium nitride (GaN) devices inherently offer many advantages over silicon power devices, including a higher operating frequency, lower on-state resistance and higher operating temperature capabilities, which can enable higher power density and more efficient power electronics. Turn-off d*V*/d*t* controllability plays a key role in determining common-mode voltage in electrical drives and traction inverter applications. The fast-switching edges of GaN can introduce challenges such as electromagnetic interference, premature insulation failure and high overshoot voltages. In this paper, the device working principle, characteristics and d*V*/d*t* controllability of 1.2 kV GaN polarisation superjunction (PSJ) heterostructure FETs (HFETs) are presented. The effect of gate driving parameters and load conditions on turn-off d*V*/d*t* are investigated. It is shown that in PSJ HFETs the d*V*/d*t* can be effectively controlled to as low as 1 kV μs^{-1} by controlling the gate, with a minimum increase in switching losses. These results are highly encouraging for the application of the devices in motor drives. © 2023 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

1. Introduction

As power electronic systems move toward higher operating frequencies and power densities, the need for high-speed, robust power semiconductor devices becomes more significant. Gallium nitride (GaN) is emerging as the next generation power semiconductor material due to its inherently superior material properties compared with silicon (Si). The first GaN high electron mobility transistor (HEMT) utilising an AlGaN/GaN heterostructure based on sapphire was introduced in 1993, and the first GaN p–n homojunction diode in 1989.[1,2] Since then, several lateral GaN devices have been implemented in various applications such as lighting, rf and, more recently, low-voltage (up to 600 V) applications.[3] GaN-based devices exhibit a higher breakdown voltage, lower specific on-state resistance and faster switching speed than their silicon counterparts, which enables GaN to be utilised in high power density and high-efficiency power electronics applications.[4–10] The extremely fast switching edges of GaN facilitate hf operation that results in smaller passive components and increased power density. However, in certain applications such as traction inverters and industrial motor drives, d*V*/d*t* controllability is essential, and the switching slew rates need to be adjusted without significant increase in energy losses. In electric motor drive applications, excessive d*V*/d*t* slew rates and high overshoot voltages can lead to premature degradation of winding insulation, failure and a detrimental bearing current that limit the lifetime and reduce efficiency.[11–15] Also, a high d*V*/d*t* contributes to conducted and radiated electromagnetic interference, which will necessitate additional filter components.[15] A high slew rate results in common-mode voltages at motor terminals which directly affects system reliability and performance.[16] Therefore, d*V*/d*t* should be limited to the application requirements to mitigate the issues arising from sharp switching edges. Several studies have been done to address such issues, which often incur the use of large and bulky passive filters to achieve the desired d*V*/d*t*, adding to the overall weight, cost and complexity of the system.[15,17,18] Alternatively, d*V*/d*t* can be controlled directly by power switching devices and gate drive circuitry and a gate resistor. Various methods have been proposed for controlling d*V*/d*t* of silicon and silicon carbide devices that involve the use of passive gate components and active gate circuitry.[19]

Conventional GaN on silicon devices do not show slew rates lower than 20 kV μs^{-1},[20,21] which can limit their use in conventional motor drives. Moreover, the lateral structure of GaN HEMTs is susceptible to field crowding near gate terminals that prevents them supporting high breakdown voltages.[22,23] To manage the electric field, several field plates are generally used to alleviate the field stress and achieve high-voltage devices.[22–26] However, the use of field plates adds additional processing steps and increases manufacturing costs and area.[3] The use of a low-cost Si substrate for higher-voltage devices requires thicker buffer and transition layers due to lattice mismatch[27] and vertical breakdown.[3] The commercially available GaN on silicon devices are therefore limited to 600–650 V. Conventionally, to achieve a high breakdown voltage with low on-state resistance, superjunction or conductivity modulation schemes are implemented in FETs and bipolar devices, respectively, to overcome the one-dimensional (1D) material limits. In silicon, the concept of superjunction works on the principle of charge balance that is achieved by the precise control of p-type and n-type doping concentrations within the drift region.[3,28–30] This helps to distribute the electric field evenly within the drift region under the off-state. GaN polarisation superjunction (PSJ) devices work on a similar basis to conventional superjunctions, except that they do not involve doping and the charge balance is realised via polarisation charges. The presence of high densities of both positive and negative polarisation charges due to the double heterostructure leads to an evenly distributed electric field in the drift

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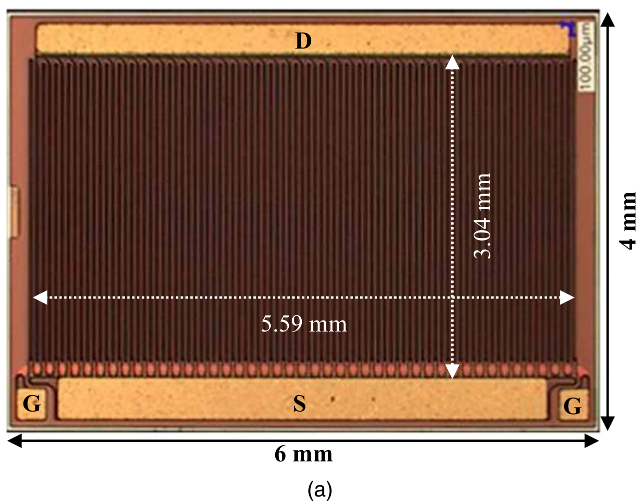
region with a minimum drift region length; these devices therefore have the potential to operate beyond the 1D material limits.[22] Various other designs based on PSJ technology have also been reported in the literature.[31,32]

The high d*V*/d*t* slew rates of GaN devices make them susceptible to hf oscillations. To fully utilise the potential of GaN power devices it is necessary to understand their switching and controllability mechanisms. However, so far there is no literature that focuses on d*V*/d*t* controllability of high-voltage GaN devices beyond 650 V and little has been done to demonstrate this. This work presents for the first time the device characteristics, working principle and turn-off d*V*/d*t* switching controllability of 1.2 kV GaN PSJ heterostructure FETs (HFETs) fabricated on a sapphire substrate. The effect of the gate drive parameters on d*V*/d*t* are investigated. The influence of load voltage and current are also investigated. Furthermore, the turn-off energy loss is analysed with respect to d*V*/d*t*.

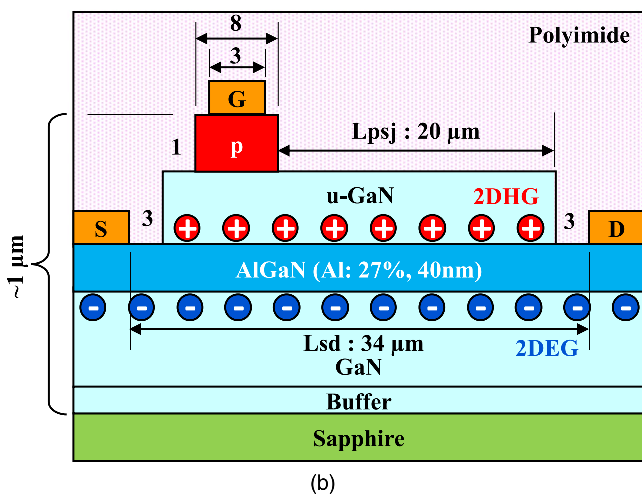
2. Device characteristics and working mechanisms

2.1. Structure and working mechanisms

The top view of a 1.2 kV GaN PSJ HFET bare die is illustrated in Fig. 1(a) and the device cross-sectional structure is depicted in Fig. 1(b). The number of fingers connected to the drain and source terminals are 43 and 44, respectively.



(a)



(b)

Fig. 1. (a) Top view of a 1.2 kV GaN PSJ HFET chip and (b) a cross-sectional view of the device structure. Gate, drain and source are marked as G, D and S, respectively.

The device shares many similarities with the 1.2 kV GaN PSJ hybrid Schottky diode previously reported, except that the p-GaN region is separated to form a gate.[33] The active area is shown in Fig. 1(a). The total length of the gate is 241 mm. The length of the drift region (L_{PSJ}) is 20 μm, which enables the device to support more than 1.2 kV with a typical breakdown voltage of around 2 kV at −20V gate voltage at RT. The leakage current measured at RT at 1200 V is 0.9 μA. PSJ GaN devices require an ohmic p-GaN region to connect to the two-dimensional hole gas (2DHG) to enable injection or extraction of holes for high breakdown voltage and collapse-free operation. The existence of an uninterrupted two-dimensional electron gas (2DEG) channel within the device structure results in a normally-on depletion mode device which conducts at 0 V gate bias with −4.75 V threshold voltage measured at a drain current of 1 mA and drain voltage of 1 V. During the on-state, the ultra-dense 2DEG provides a low-resistance channel for current conduction between the drain and source terminals. The channel resistance can be reduced by application of positive gate bias during the turn-on. However, the positive gate drive voltage is limited to ∼3 V due to the presence of two parasitic p–n junction diodes, (1) between the gate and source and (2) between the gate and drain with an onset voltage of ∼3.4 V. Exceeding this limit leads to the injection of minority carriers and an excessive gate leakage current which can potentially degrade the device. During the off-state, the polarisation charges in the 2DEG and 2DHG are depleted through drain and gate terminals, respectively. This results in a charge balance state with an even distribution of electric field that enables the device to withstand a high blocking voltage. Unlike MOSFETs, GaN PSJ devices do not have a body diode. Thus, they do not suffer from reverse recovery during the switching transients. Moreover, a hybrid GaN Schottky diode can be paralleled/integrated if required.

2.2. Forward characteristics

The output *I*–*V* characteristics of the device were measured in pulse mode at 25 °C as shown in Fig. 2.

The typical on-state resistance of the device at 25 °C and 5 A amounts to 95 mΩ and 140 mΩ at gate voltages of 3 V and 0 V, respectively. With the application of a positive gate voltage, the electron density in the 2DEG channel increases further in the drift region due to accumulation. This is because the gate extends into the drift region via the 2DHG, which enables electrons to accumulate and results in decreased on-state resistance. The relation between on-state resistance and junction temperature is illustrated in Fig. 3.

The device has a positive temperature coefficient even at extremely low temperatures. The change of temperature directly affects lattice scattering and reduces mobility, causing the resistance of the device to increase. While the sensitivity changes with the applied gate voltage, the temperature coefficient remains positive. This highlights the potential of the GaN device for parallel operation without the risk of thermal runaway. The transfer characteristics of the device were measured at different temperatures, as shown

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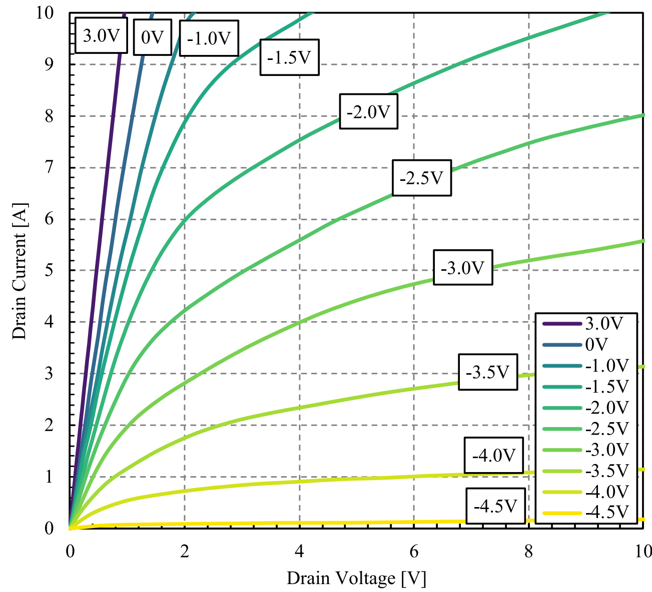

Fig. 2. Output I–V characteristics of the GaN PSJ HFET at 25 °C. The pulse width is 250 μs.

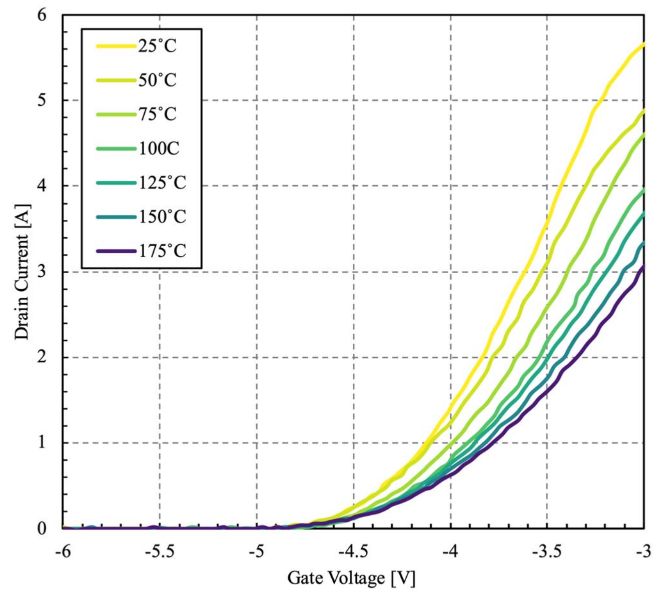

Fig. 4. Transfer characteristics of the GaN PSJ HFET at different junction temperatures. The drain–source voltage (V_{ds}) is 10 V.

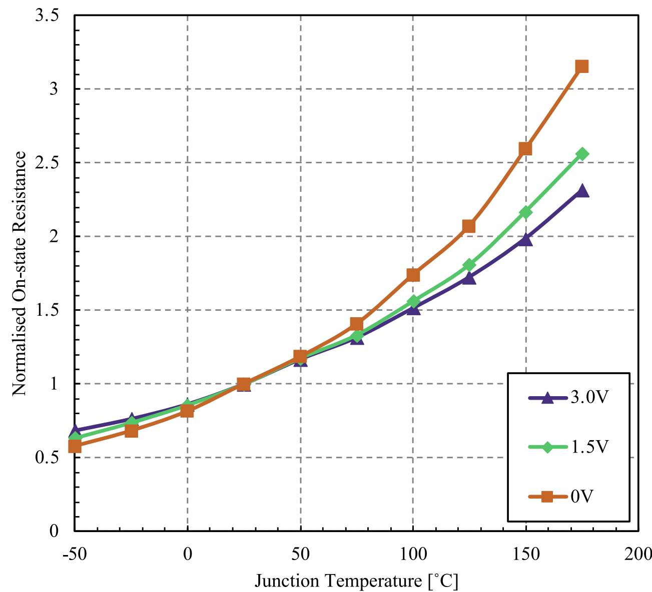

Fig. 3. Normalised drain-source on-state resistance at different junction temperatures.

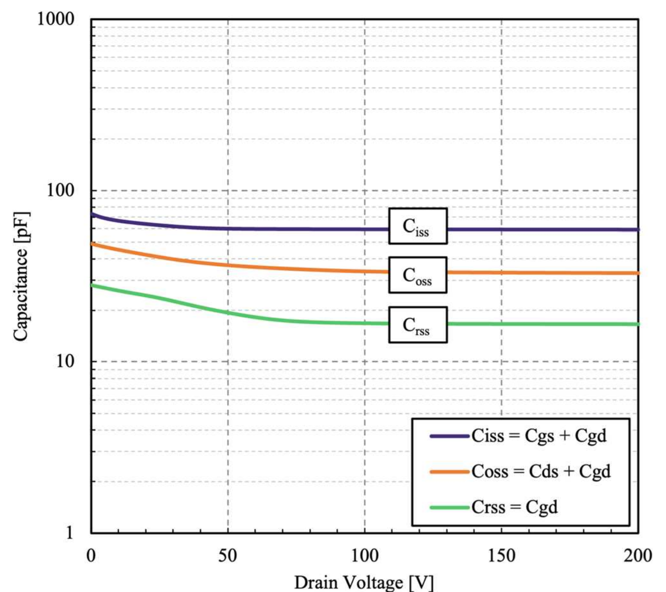

Fig. 5. Capacitance versus voltage measured at 1 MHz frequency. The gate voltage is −20 V.

in Fig. 4. Critically, the threshold voltage shift with increase in temperature is minimum.

2.3. Capacitance characteristics

The parasitic junction capacitance characteristics reveal key information about device switching behaviour. The parasitic capacitances of the device were measured using an Agilent B1505 power device analyser and are presented in Fig. 5.

The low capacitance values result in faster switching transitions. GaN PSJ devices utilise the gate–drain capacitance ($C_{gd} \equiv C_{rss}$) to achieve optimum dV/dt controllability without significantly affecting the switching losses. This capacitance is primarily due to the overlap of the 2DHG and 2DEG over the PSJ length. The measured value of the gate–drain capacitance and the corresponding charge (Q_{gd}) of the PSJ device is 22 nC at 600 V and 5 A. This value is similar to the Q_{gd} of similarly rated 1.2 kV SiC MOSFETs, which ranges from 3 nC to 23 nC between different manufacturers.[34,35]

3. Experimental methods and d*V*/d*t* mechanism

The device switching speed is defined by its parasitic capacitances and the rate at which they can be charged or discharged. The maximum dV/dt occurs in the Miller region, which is governed by C_{gd}, as defined in Eq. (1)

$$\frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}} = \frac{V_{gs}}{R_g.C_{gd}}. \tag{1}$$

Thus, dV/dt can be controlled by the gate resistor or gate voltage. Once the voltage across the device reaches the supply voltage, an overshoot occurs due to the presence of stray inductances, which can be defined by Eq. (2)

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$$V_{\mathrm{overshoot}} = L_{\mathrm{stray}}.\frac{dI_{\mathrm{drain}}}{dt}. \quad (2)$$

It is important to minimise the stray inductances to avoid a large overshoot voltage. At high switching slew rates, the effect of parasitic components (inductances and capacitances) becomes significant and limits the switching performance.[10,36]

To evaluate and analyse the switching behaviour of the GaN PSJ HFET, a clamped inductive switching test bench was set up as illustrated in Fig. 6 along with the typical switching waveforms of the device during the turn-off event.

The setup uses a 1.185 mH inductive load (L_{load}). A 1200 V Schottky barrier diode was used as the freewheeling diode (D_{FWD}). The input supply voltage (V_{DC}), gate drive voltage (V_{GS}), gate resistor (R_{G}) and drain current are varied during each experiment and will be specified for each corresponding section. The experiments are divided into two parts. In part one (Sect. 4.1), the effect of the gate drive circuit on dV/dt controllability is analysed. The gate resistor R_{G} and the gate drive voltage ($V_{\mathrm{GS\text{-}OFF}}$) are variable in this part. The supply voltage and current are kept constant at 600 V and 5 A, respectively. In part two (Sect. 4.2), the effect of load conditions on dV/dt is investigated. In this part, the load voltage and current are variable while the gate drive voltage and gate resistor are fixed at −15 V and 22 Ω, respectively. The rise time (t_{rise}) is defined by the voltage switching transition time interval from 10% to 90% of the supply voltage. The dV/dt is then determined by the rate of change in the voltage during the switching transient over the rise time. This corresponds to the slope of the drain voltage, dV/dt = $0.8V_{\mathrm{DC}}/t_{\mathrm{rise}}$. The turn-off energy loss is then calculated using Eq. (3)

$$E_{\mathrm{off}} = \int V_{\mathrm{drain}}.I_{\mathrm{drain}}\,dt. \quad (3)$$

The integration is performed during the turn-off switching transient.

4. Turn-off d*V*/d*t* controllability

4.1. Variable gate drive voltage and gate resistor

In the following, the measurement results of the GaN PSJ HFET turn-off switching transients are analysed at different gate driving conditions. The tests were conducted at a fixed input supply voltage of 600 V and drain current of 5 A. The gate resistor was varied from 4.7 Ω to 150 Ω at different turn-off gate voltages (the turn-on gate voltage was fixed at 2 V).

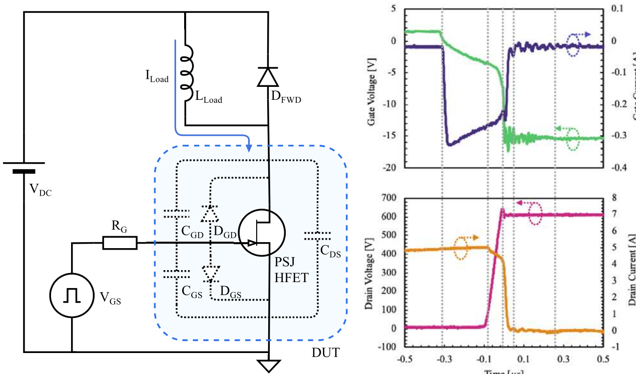

Fig. 6. Experimental setup and the typical turn-off switching waveforms.

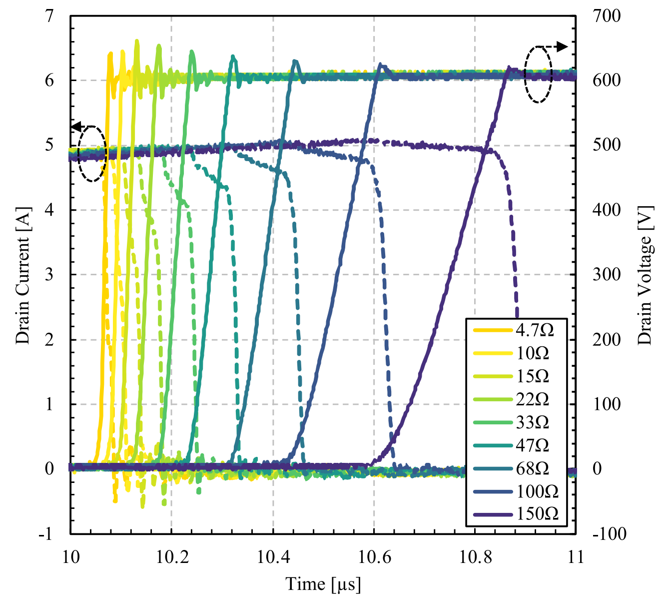

Fig. 7. Measured turn-off switching waveforms of the GaN PSJ HFET at different external gate resistances. The turn-off gate voltage is −15 V.

The switching waveforms at different gate resistances are shown in Fig. 7.

The voltage rise time is 15 ns at a gate resistance of 4.7 Ω. Increasing the external gate resistance limits the current supplied to the gate and the rate at which the gate capacitances are charged, and therefore the switching slows down. Also, it can be observed that at low gate resistances of 10 Ω and below, the peak overshoot voltage is reduced. This is entirely due to the effect of stray inductances combined with a high dV/dt that results in voltage ringing after the drain voltage transition. This leads to excessive leakage current during the overshoot period that consequently causes the peak overshoot to be reduced.

Figure 8 shows the turn-off switching of the device at different gate voltages from −10 V to −20 V. The positive gate voltage and gate resistor are 2 V and 22 Ω, respectively.

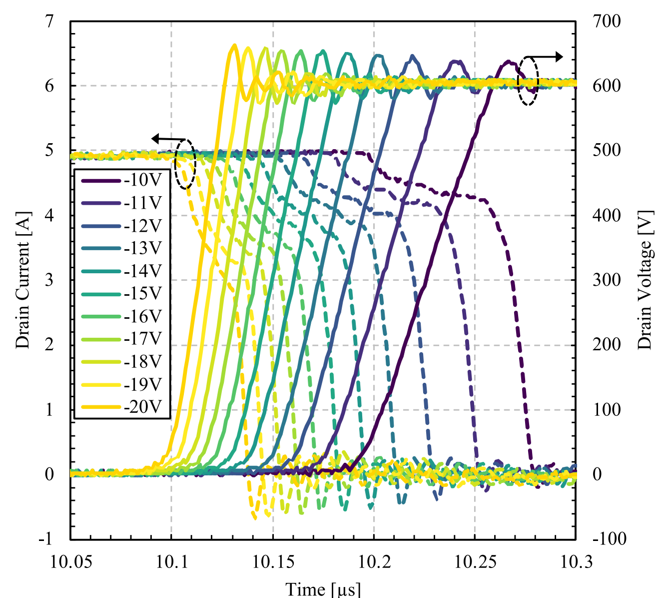

Fig. 8. Measured turn-off switching waveforms of the GaN PSJ HFET at different gate drive voltages. The positive gate voltage is 2 V and the external gate resistance is 22 Ω.

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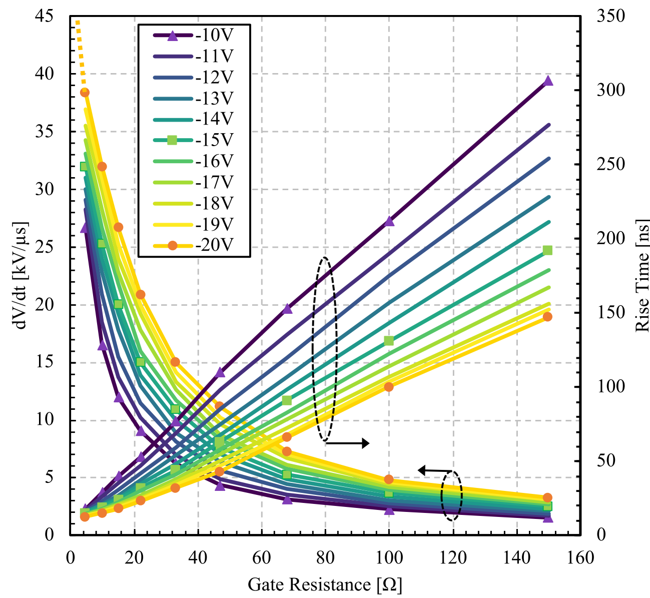

Fig. 9. Measured d*V*/d*t* and rise time of the GaN PSJ HFET at different gate voltages and external gate resistances.

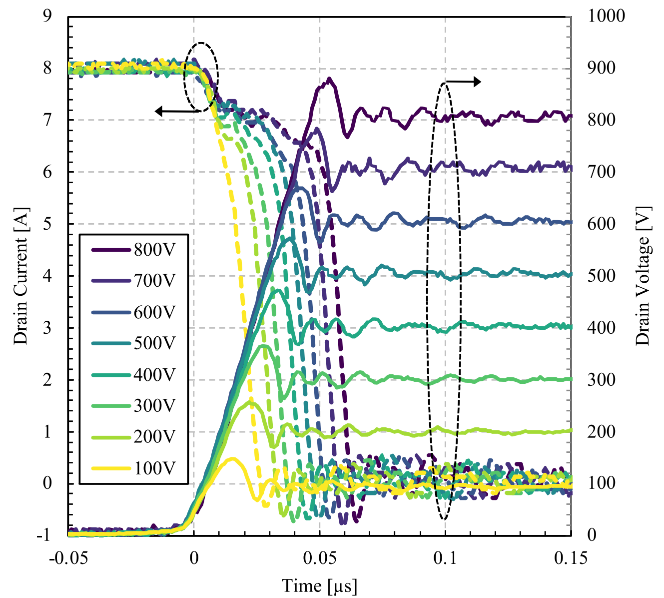

Fig. 11. Measured turn-off switching waveforms of the GaN PSJ HFET at different switching voltages. The switching current is constant at 8 A.

Similar to gate resistor control, increasing the turn-off gate voltage results in the gate capacitances charging at a faster rate, leading to an increased switching speed. The switching test was repeated at different gate resistances from 4.7 Ω to 150 Ω. The d*V*/d*t* and rise time were extracted from the recorded data, as presented in Fig. 9.

The device achieves a maximum d*V*/d*t* of 39 kV μs^{-1} at a gate resistance and gate voltage of 4.7 Ω and −20 V, respectively. The d*V*/d*t* can reach very high values with small gate resistors. By increasing the gate resistance, d*V*/d*t* can be slowed down to less than 1 kV μs^{-1}. The results show that controllability can be realised by controlling the gate driving conditions to achieve the optimum d*V*/d*t* for a given application. The corresponding turn-off energy loss is then derived from the measured switching data, as shown in Fig. 10.

As the gate resistance increases, the switching transition becomes slower, resulting in a higher energy loss. This shows the trade-off between d*V*/d*t* and turn-off energy loss. It is important to note that the turn-off energy is an order lower at least compared to that in silicon insulated-gate bipolar transistors.

4.2. Variable load voltage and current

In the following section, the switching behaviour of the device is investigated at different load conditions. During the test, the gate drive voltage and gate resistor were fixed at 2 V to −15 V and 22 Ω, respectively. The input DC supply voltage and current were varied from 100 V to 800 V and 1 A to 8 A and the corresponding data were recorded. Figure 11 shows the device turn-off switching waveforms at different supply voltages while the current is fixed at 8 A.

The supply voltage has a direct impact on the electric field during the turn-off. Therefore, d*V*/d*t* increases with the supply voltage. Figure 12 shows the turn-off switching waveforms at different current levels at 600 V supply voltage.

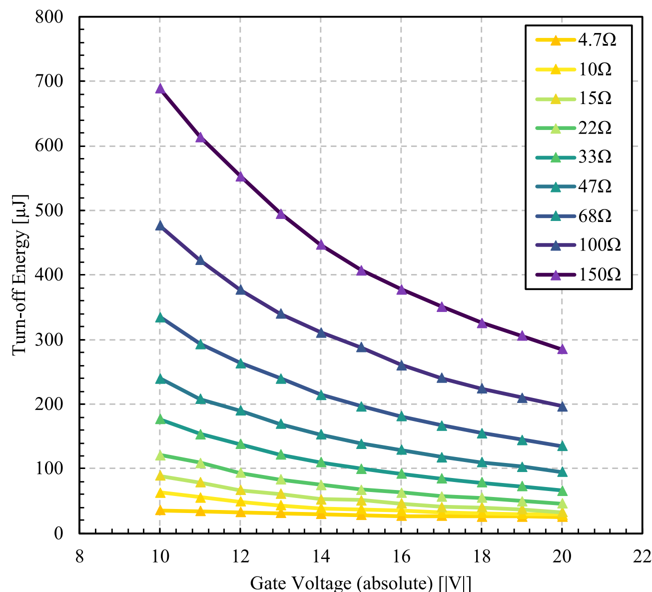

Fig. 10. Measured turn-off energy at different gate resistor values and negative turn-off gate voltages (horizontal axis).

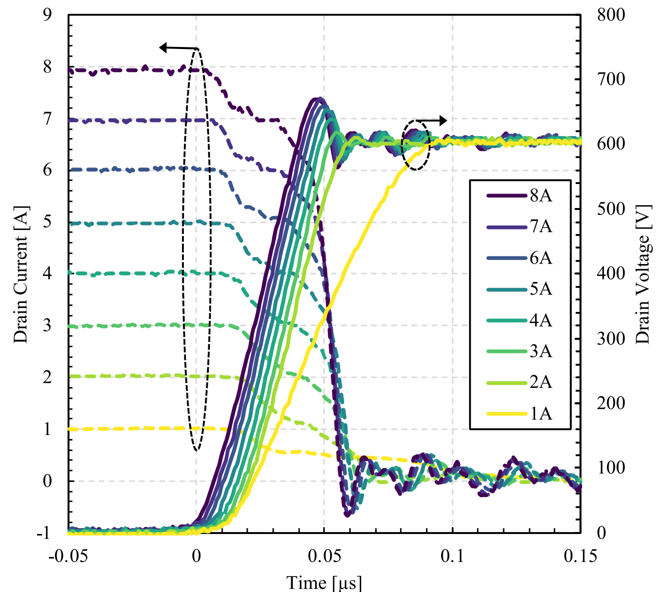

Fig. 12. Measured turn-off switching waveforms of the GaN PSJ HFET at different load currents. The supply voltage is constant at 600 V.

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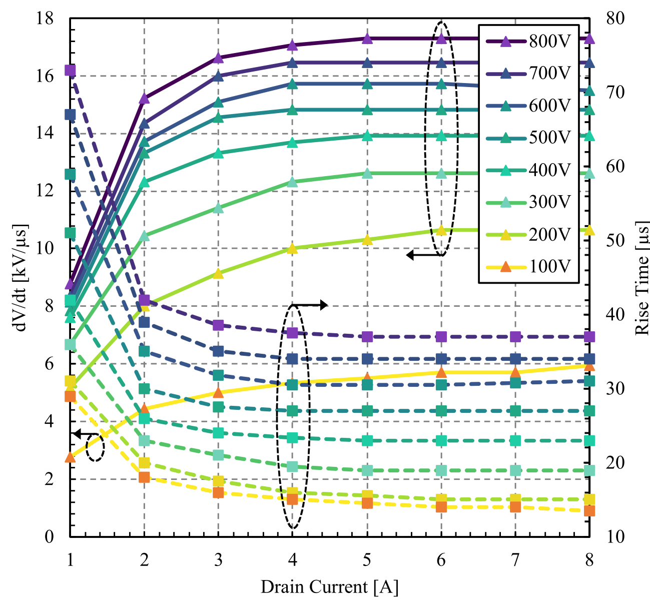

Fig. 13. The d*V*/d*t* and rise time of the GaN PSJ HFET at different load conditions.

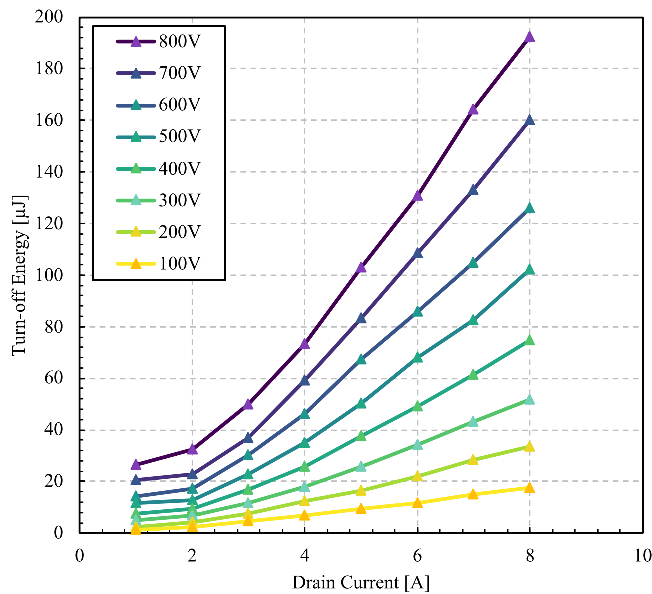

Fig. 14. Measured turn-off energy at different load voltage and current levels.

At low switching currents, the voltage rise time is affected by the parasitic capacitances. The predominant parasitic capacitances include the output capacitance of the switching device and the parallel parasitic capacitance of the freewheeling diode and load (as shown in Fig. 4). Also, the voltage probe capacitance has an effect, but it is small. During the turn-off transition, the current starts to divert from the device to the freewheeling diode while these parasitic capacitances are charged. Thus, at low switching current, d*V*/d*t* is affected by the parasitic capacitances. The corresponding d*V*/d*t* and rise time were extracted for different load conditions, as shown in Fig. 13.

As can be observed, d*V*/d*t* increases as the supply voltage increases. However, the impact of load current is minimal. Based on the switching data, the turn-off energy was calculated and is illustrated in Fig. 14.

As the load current and switching voltage rises, the dissipated power increases, resulting in increased switching losses.

5. Conclusion

In this paper, the device characteristics, working principle and turn-off d*V*/d*t* controllability of 1.2 kV GaN PSJ HFETs are presented for the first time. The fast-switching nature of GaN PSJ devices can facilitate the construction of hf, ultra-high power density power electronics. To fully utilise the advantages of GaN devices it is necessary to have control over their switching characteristics. It has been demonstrated that GaN PSJ devices can operate at a very small d*V*/d*t* suitable for electrical motor drive applications as well as at high d*V*/d*t* values suitable for switch mode power supplies. However, depending on the application, the slew rate may need to be reduced or controlled. The experimental results show the d*V*/d*t* of GaN PSJ HFETs can be controlled by means of gate control, including a gate resistor or gate drive voltage, to achieve the optimum slew rate according to the application. The effective use of device capacitance, gate resistor and gate drive voltage can result in enhanced switching controllability while maintaining low switching energy losses. Combination of such options is not available in other devices to our knowledge. It was also demonstrated that the load current does not significantly affect the controllability under normal operating conditions. The results show minimal energy losses during the switching transition, which helps in the design of high-power density converters with high efficiency. Overall, GaN PSJ HFETs could be a cost-effective, more environmentally favourable solution, particularly for hf, high-efficiency power electronic applications and for electric traction systems.

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