Resonant Dual Active Bridge Partial Power Converter for Electric Vehicle Fast Charging Stations

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***Abstract*—This paper presents an analysis and design of a DC-DC charging unit for an electric vehicle fast charging station. Due to the benefits that partial power processing achieves in terms of size reduction and efficiency improvement, it is decided to implement a partial power converter architecture. This type of architectures reduce the power to be processed by the converter, but they require an isolated topology. Therefore, a dual active bridge series resonant converter is selected for the study due to its benefits in terms of soft switching conditions. Design wise, it is decided to ensure zero voltage switching at the secondary side of the converter. Indeed, one of the benefits of the implemented partial power converter is the reduced voltage that exists at the primary side. This way, lower voltage overshoots and switching losses are expected. Finally, via simulations, it is confirmed that partial power processing can be achieved with a resonant converter and that zero voltage switching operation is ensured at the secondary side through the entire charging process.**

Keywords—fast charging station, electric vehicle, partial power converter, dual active bridge, resonant converter

I. INTRODUCTION

Partial power processing (PPP) based solutions have become more and more popular in recent years [1]–[3]. This type of architectures aim to reduce the power to be processed by the converter. This way, lower sized, cheaper and more efficient converters can be achieved. Regarding their applications, PPP based converters can be found at data centers [4], renewable energies [5]–[7], energy storage system (ESS) balancing and integration [8]–[10] and, last but not least, electric vehicle (EV) fast charging [11]–[13]. Focusing on EV fast charging applications, Fig. 1 presents different charging station solutions [14]. All of them are divided in two main stages (a rectification stage and a DC-DC charging unit). However, each solution stablishes the isolation border on a different point. For example, Fig. 1a proposes an isolated DC-DC charging unit, whereas, Fig. 1b establishes it at the power rectifier. Also, in some cases, a line frequency transformer is implemented before the rectification stage, see Fig. 1c. This paper will focus on the design of the DC-DC converter, which is connected between a common DC bus and the ESS of the EV. To be more precise, it will be a non-isolated DC-DC converter as the one presented in Fig. 1b and Fig. 1c. Indeed, although PPP based solutions can never ensure galvanic isolation between the source and the load, usually they require isolated topologies to avoid short-circuits. For example, authors from [11] implement a phase-shifted full bridge (PSFB) topology and they conclude that the PPP based converter, compared to its full power version, achieves an efficiency improvement of 0.6 % at full-load and 1.6 % at 50 % load. This improvement is due to the reduced processed power by the converter (27 %). Also, authors from [13] implement a PSFB and they obtain improvements in terms of efficiency (from 95.1 % to 98.3 %) when implementing a PPP solution on a EV fast charging application. Apart from that, authors from [15], [16] also analyze the possibility of implementing alternative isolated topologies, such as a dual active bridge (DAB) or a Flyback. Concerning the Flyback topology, [16] concludes that it cannot be considered PPP, since its ratio of non-active power is similar to a conventional boost converter.

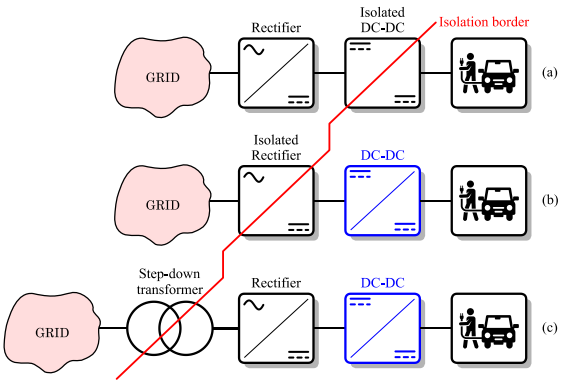

Fig. 1. Simplified single-wire diagram of different EV fast charging stations. In blue, the converters under analysis in this paper.

Bearing this in mind, the present article aims to extend the analysis of isolated topologies on PPP architectures for EV fast charging applications. Until now, no resonant topology has been implemented in a PPP architecture and, for this reason,

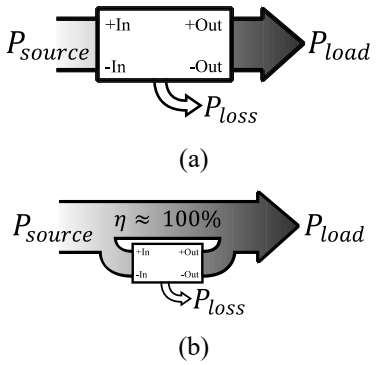

Fig. 2. Power flow diagram. (a) FPP. (b) PPP.

this article contributes by presenting the design and analysis of a fixed frequency dual active bridge series resonant converter (DAB-SRC). The control methodology of this topology does not vary very much from a DAB and all the switches inside it achieve zero voltage switching (ZVS) or zero current switching (ZCS) for a wider operation range [17]. The paper is organized as follows: Section II describes the concept of PPP, Section III defines the case study and the steps followed for the design of the DAB-SRC, Section IV presents the main simulation results, Section V summarizes the obtained conclusions and, finally, Section VI lists the proposed future lines.

II. DESCRIPTION OF THE PPP CONCEPT

The main objective of PPP architectures is to reduce the power to be processed by the converter. As example, Fig. 2 compares the power flow of a converter based on Full Power Processing (FPP) and a converter based on PPP. On the one hand, the FPP converter (Fig. 2a) is designed to process the 100 % of the power consumed by the load. On the other hand, a converter based on PPP (Fig. 2b) just processes a reduced fraction of the total power that flows from the source to the load. This way, the losses generated by the power converter are reduced, as well as its size and cost. Equations (1),(2) describe how the efficiency of the converter ($\eta_{converter}$) affects the efficiency of the system (η_{system}) in a different manner depending on if it is based on FPP or PPP. As it can observed in (1), $\eta_{converter}$ and η_{system} have the same value, since the FPP converter processes the total power of the system. However, regarding the PPP, $\eta_{converter}$ and η_{system} are related by the processed power ratio of the converter (K_{pr}), see (3).

$$\eta_{system_{FPP}} = \frac{P_{load}}{P_{source}} = \eta_{converter} = \frac{P_{out}}{P_{in}} \quad (1)$$

$$\eta_{system_{PPP}} = 1 - K_{pr} \cdot (1 - \eta_{converter}) \quad (2)$$

$$K_{pr} = \frac{P_{in}}{P_{source}} \quad (3)$$

Where, P_{in}, P_{out} are the input and output power of the converter.

According to the literature, there exist three different PPP strategies for DC-DC applications [18]: differential power converters (DPC), partial power converters (PPC) and mixed strategies. In the first place, DPCs have as main objective to correct current unbalances between series connected elements. These strategies are also known as current diverters and they are widely used for ESS or PV modules balancing. In the second place, there are the partial power converters (PPC), which control the power flow between a source and a load with different voltage level. This type of strategies fit perfectly with the concerned application (power control between a DC bus and the EV, Fig. 1). Last but not least, there are the mixed strategies. The disadvantages of DPC and PPC converters give reason to investigate alternative architectures, so here are grouped them. Focusing on PPCs, as example, Fig. 3 presents an input-series-output-parallel (ISOP) type PPC architecture. This architecture is designed for voltage step-down applications and, in order to avoid a short-circuit of V_{load}, it requires an isolated topology. Nevertheless, the final solution cannot be considered as galvanically isolated, since the grounds from V_{source} and V_{load} must be connected to each other. The next step is to calculate the K_{pr} curve of the ISOP architecture. To do so, Kirchhoff's laws are applied on it, obtaining equations (4) and (5). Then, substituting (4),(5) in (3), the K_{pr} curve of the ISOP architecture is obtained in function of the static voltage gain ($G_V = V_{load}/V_{source}$), see (6). Fig. 4 shows the K_{pr} curve from (6) compared to a full power converter (FPC). As it can be observed, the FPC always processes the 100 % of the power that goes from the source to the load, no matter G_V. However, the PPC processes less power as G_V gets closer to 1. This means that the closer V_{source} and V_{load} are between them, the lower power is processed by the converter. Considering the voltage variability of the ESS inside the EV, a variable K_{pr} is expected through the charging process. Therefore, a correct design of the topology inside the ISOP step-down architecture is essential to optimize its performance along the entire charge.

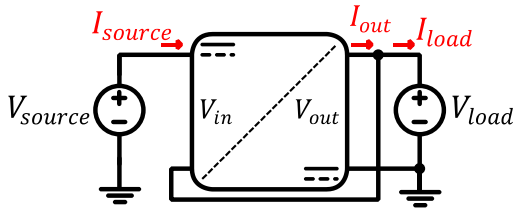

Fig. 3. ISOP step-down PPC architecture.

$$V_{source} - V_{in} = V_{load} \quad (4)$$

$$I_{source} + I_{out} = I_{load} \quad (5)$$

$$K_{pr_{ISOP}} = 1 - G_V \quad (6)$$

III. CASE STUDY AND DESIGN OF THE DAB-SRC

The present section is divided into 2 main subsections: description of the application and design of the DAB-SRC implemented on an ISOP type PPC.

A. Description of the EV charging unit

As presented before, this paper will focus on the analysis and design of the DC-DC charging unit shown in Fig. 1. This power converter is connected between a constant DC bus (after the

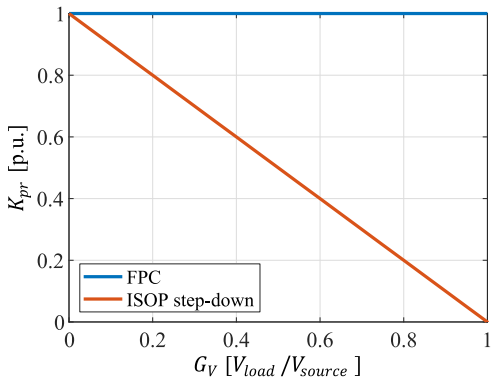

Fig. 4. Processed power ratio of a FPC and an ISOP PPC architecture.

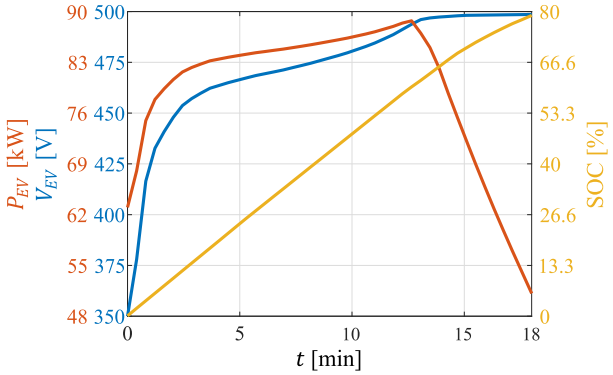

Fig. 5. Modelled voltage, power and SOC curves of the EV fast charging application.

rectifier) and a variable load (EV's ESS). Concerning the DC bus, it is stablished at 600 V [19], whereas EV's voltage, power and state of charge (SOC) curves are presented in Fig. 5. As it can be observed, a fast charging process of an EV (up to a SOC value of 80 %) is modelled, where the voltage curve varies from 350 V to 500 V and the peak power value is defined around 90 kW. In summary, Table 1 specifies the main electrical parameters of the application.

Then, assuming that the ISOP step-down architecture from Fig. 3 is implemented, it is obvious that an isolated topology must be selected. In this case, bearing in mind the main objective of this paper, a fixed frequency DAB-SRC is selected. Fig. 6 shows a simplified electric diagram of the final solution. Its modulation strategy consists of a conventional phase-shift modulation (PSM). Then, concerning the design parameters of the DAB-SRC, Table 2 defines the input/output voltage, power and frequency levels of the converter. On the one hand, V_{in} consists of the difference between V_{DC} and V_{EV} from Table 1. This way, the maximum voltage that the primary side semiconductors will observe is reduced to 250V. On the other hand, the output voltage contains the same values as V_{EV}, since it is connected in parallel. Finally, applying equation (6), the peak power to be processed by the converter is estimated around 21 kW. This occurs at the beginning of the charging process. Although P_{EV} increases as the ESS charges (Fig. 5), the power processed by the converter decreases. This is because V_{EV} is getting closer to the voltage value of the DC bus (600 V), reducing the K_{pr}.

Table 1. Electrical parameters of the modelled EV fast charging station.

Parameter	Value
V_{DC} [V]	600
V_{EV} [V]	350 ÷ 500
P_{EV} [kW]	90

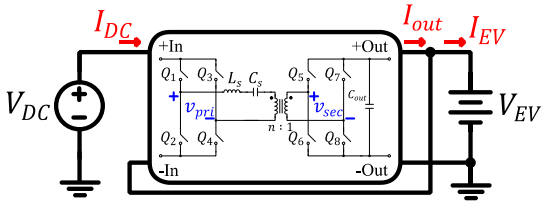

Fig. 6. DAB-SRC topology implemented on an ISOP step-down architecture.

Table 2. Design parameters of the DC-DC charging unit.

Parameter	Value
V_{in} [V]	250 ÷ 100
V_{out} [V]	350 ÷ 500
$P_{converter}$ [kW]	21.43
f_{sw} [kHz]	10

B. Design of the DAB-SRC on an ISOP PPC architecture

The main three parameters that must be defined by the user when designing a fixed frequency DAB-SRC are the voltage gain (M), the normalized frequency (F) and the quality factor (Q). Through the present subsection, a design methodology to select their appropriate values is described.

In the first place, assuming that the resonant current and voltage are near sinusoidal, they can be approximated by only its fundamental component [20]. In consequence, the switching current of the primary and secondary side semiconductors can be evaluated by applying equations (7),(8), respectively.

$$i_{sw,pu}(t_0) = \frac{4}{\pi \cdot X_{pu}} \cdot (-1 + M \cdot \cos\phi) \quad (7)$$

$$i_{sw,pu}\left(\frac{\phi}{\omega_s}\right) = \frac{4}{\pi \cdot X_{pu}} \cdot (M - \cos\phi) \quad (8)$$

Where ϕ is the phase-shift between the two AC voltages (v_{pri} and v_{sec}, from Fig. 6), ω_s=2πf_{sw}, M=$n \cdot V_{out}/V_{in}$ and X_{pu} is defined by (9). It is necessary to know that n represents the transformation ratio of the transformer.

$$X_{pu} = Q \cdot \left(F - \frac{1}{F}\right) \quad (9)$$

If $i_{sw,pu}(t_0)$ is negative, the primary side semiconductors will commute with zero voltage switching (ZVS), whereas if $i_{sw,pu}\left(\frac{\phi}{\omega_s}\right)$ is positive, ZVS is ensured for the secondary side semiconductors. Fig. 7 shows the obtained ZVS regions at each side for different values of M. Due to the reduced voltage that will exist at the primary side (see V_{in} from Table 2), authors observe that ensuring ZVS at the secondary side is more critical. Therefore, based on the curves from Fig. 7b, it is concluded that M>1. Then, Fig. 8 presents the design curves that are used for defining the exact values of M, F and Q [20].

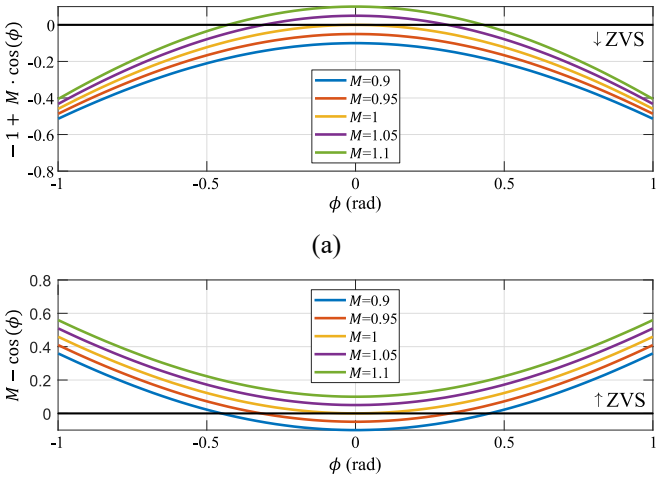

Fig. 7. ZVS switching region of the (a) primary side semiconductors and (b) secondary side semiconductors.

Based on (10), Fig. 8a and Fig. 8b present the resonant peak current at full load for different values of Q and F. Implementing (11), Fig. 8c shows the resonant capacitor peak voltage at full load. Then, using (12), the ratio of the apparent power to the active power at full load is shown in Fig. 8d.

$$I_{p,pu} = \frac{4}{\pi \cdot Q \cdot (F - 1/F)} \cdot \sqrt{1 + M^2 - 2 \cdot M \cdot cos\phi} \quad (10)$$

$$V_{p,pu} = \frac{4}{\pi \cdot (F^2 - 1)} \cdot \sqrt{1 + M^2 - 2 \cdot M \cdot cos\phi} \quad (11)$$

$$\text{kVA/kW} = \frac{\pi^2 \cdot (Q \cdot F + Q/F)}{8 \cdot cos^2\,\theta} \quad (12)$$

Where, the value of M for full load condition is obtained from (13) by substituting P_{pu} for M^2 [20]. This expression indicates the transferred active power by the converter.

$$P_{pu} = \frac{8 \cdot M \cdot sin\phi}{\pi^2 \cdot Q \cdot (F - 1/F)} \quad (13)$$

Based on the curves from Fig. 7b, M=1.05 is selected to ensure ZVS at the turn on of the secondary side switches. Then, from Fig. 8d, it is observed that a F value of 1.1 processes similar apparent power values than F =1.05. Nevertheless, observing Fig. 8b, the current peak is reduced when M>1. Therefore, F=1.1 is chosen for the design. Based on Fig. 8a and Fig. 8c, it is clear that a lower resonant current and resonant capacitor voltage is achieved with lower Q values. For this reason, Q=1 is selected. To sum up, the defined values are M=1.05, F=1.1 and Q=1.

The next step is to calculate the design values of n, L_s and C_s from Fig. 6. In the first place, by using (14), n=0.75 is obtained. In the second place, the load resistance reflected to the primary side and the resonant frequency are calculated with (15) and (16), respectively (R'_{load}=1.84Ω and f_r=9.09kHz). Then, based on the results from (14)-(16), the value of the resonant inductance and the resonant capacitor are calculated using (17),(18) (L_s=32.17µH and C_s=9.53µF).

$$n = \frac{V_{in_{max}} \cdot M}{V_{out_{min}}} \quad (14)$$

$$R'_{load} = \frac{V^2_{out_{min}}}{P_{converter_{max}}} \cdot n^2 \quad (15)$$

$$f_r = \frac{f_{sw}}{F} \quad (16)$$

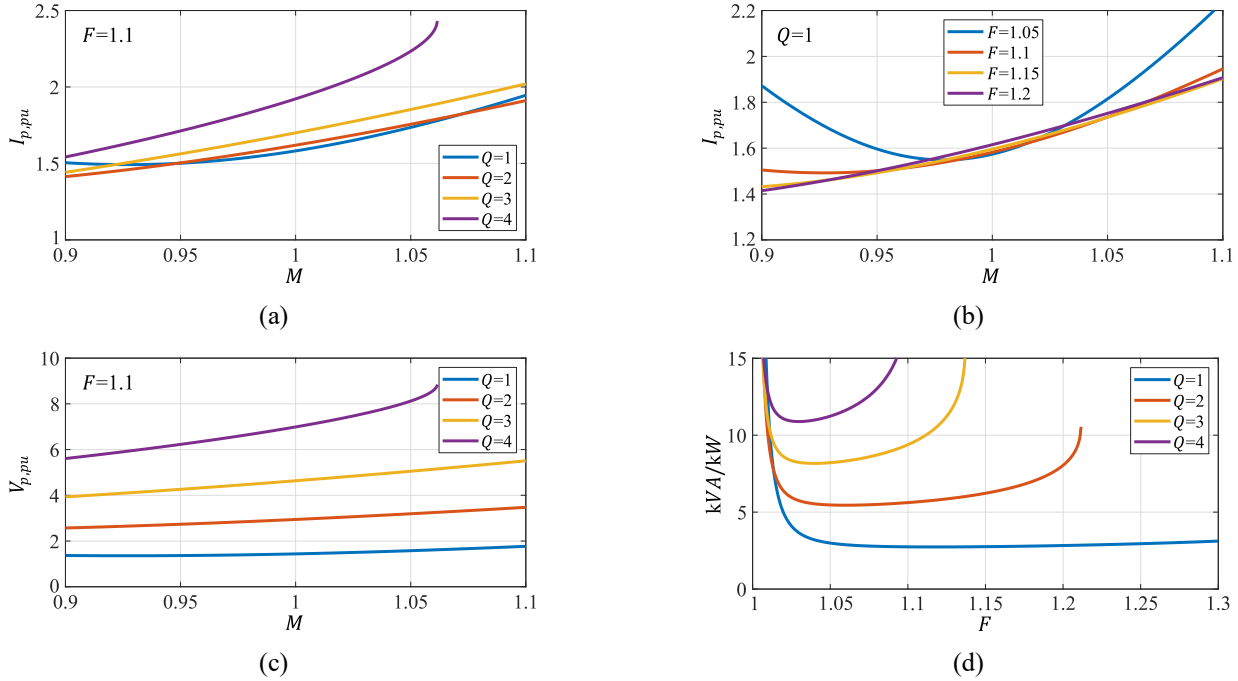

Fig. 8. (a) Normalized peak current with F=1.1 and different Q values. (b) Normalized peak current with Q=1 and different F values. (c) Normalized resonant capacitor voltage with F=1.1 and different Q values. (d) Tank kVA/kW of output power with different Q values.

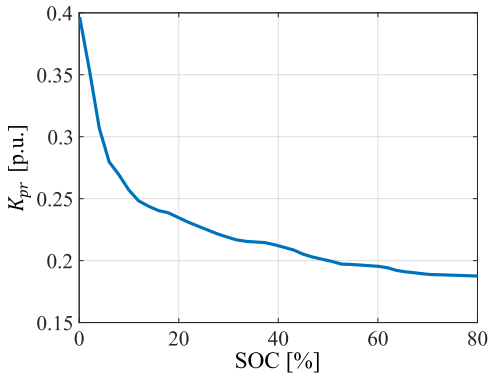

Fig. 9. Processed power ratio of the DAB-SRC through the charging process.

$$L_s = \frac{Q \cdot R'_{load}}{\omega_r} \quad (17)$$

$$C_s = \frac{1}{\omega_r^2 \cdot L_s} \quad (18)$$

Where $V_{in_{max}}$, $V_{out_{min}}$ and $P_{converter_{max}}$ are based on the values from Table 2 and ω_r=2πf_r.

IV. Simulation Results

In order to validate the design of the DAB-SRC, simulations have been carried out in MatLAB.

On the one hand, Fig. 9 shows the K_{pr} curve achieved by the DAB-SRC through the charging process. As it can be observed, the maximum processed power ratio of the converter is around a 40 % of the total power. This value decreases up to an 18.7 % as the ESS inside the EV charges. This is because V_{EV} is getting closer to V_{DC}, which causes a G_V value closer to 1 (6). On the other hand, Fig. 10a and Fig. 10b present the steady state waveforms of the resonant inductor current and the AC voltages at two extreme working points: the start and the end of the charging process, respectively. In both cases, the converter is processing the maximum power and, as it can be observed, a positive value of I_L is obtained at t_ϕ, which ensures ZVS operation of the secondary side semiconductors. Regarding the primary side semiconductors, they will commute with hard switching (HS) conditions due to the positive value of I_L at t_0. However, since the voltage value of v_{pri} is reduced to the difference between V_{DC} and V_{EV}, lower voltage overshoots and switching losses are expected.

V. Conclusions

In the present paper a design of an EV charging unit for a fast charging station is described. With the aim of achieving a more efficient and lower sized solution, a PPC architecture is implemented. Regarding the converter topology, a DAB-SRC is proposed due to its benefits in terms of ZVS and its bi-directionality for vehicle to load functions. Then, due to the reduced voltage that exists at the primary side, it is concluded that ensuring ZVS operation of the secondary side semiconductors is more critical. Indeed, the maximum expected voltage at the primary is 250 V, whereas at the secondary is 500 V. In consequence, lower voltage overshoots and switching losses are expected. Then, a detailed analysis on the steps

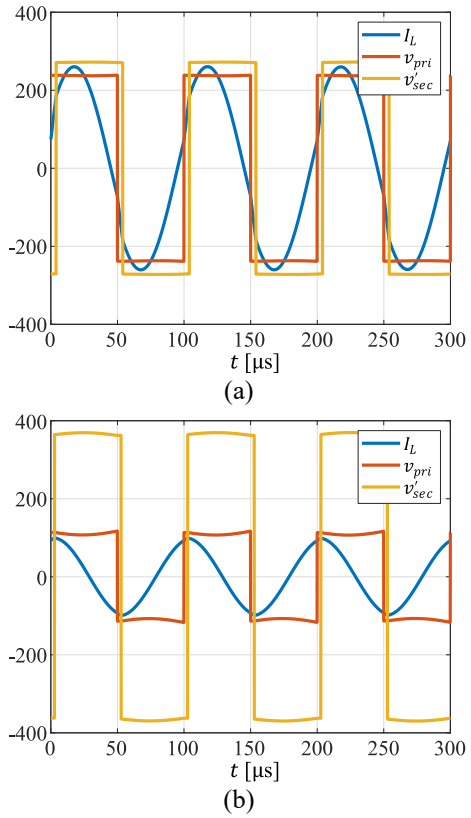

Fig. 10. Steady state waveforms of the resonant inductor current (I_L) and AC voltage signals (a) at the start of the charging process (b) at the end of the charging process.

followed through the design of the DAB-SRC has been presented. There, different parameters such as ZVS region, resonant peak current/voltage value and processed apparent power have been compared. Finally, via simulations, it has been demonstrated that partial power processing can be achieved with a DAB-SRC.

VI. Future Lines

With the aim of improving the present paper, the next future lines are proposed:

- Extend the ZVS region analysis by comparing the results of the DAB-SRC against other isolated topologies as the DAB or the PSFB.
- Build a small-scale prototype that confirms the obtained results.

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