A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad and I. Baraia, "Medium Voltage–High Power Converter Topologies Comparison Procedure, for a 6.6 kV Drive Application Using 4.5 kV IGBT Modules," in IEEE Transactions on Industrial Electronics, vol. 59, no. 3, pp. 1462-1476, March 2012.

DOI: https://doi.org/10.1109/TIE.2011.2162213

# Medium Voltage - High Power Converter Topologies Comparison Procedure, for a 6.6kV Drive Application using 4.5kV IGBT Modules

Alain Sanchez-Ruiz, *Student Member, IEEE*, Mikel Mazuela, *Student Member, IEEE*, Silverio Alvarez, Gonzalo Abad, *Member, IEEE*, and Igor Baraia

***Abstract*—This paper presents a general comparison procedure for Medium Voltage – High Power multilevel converter topologies and semiconductors, which is mainly based on analysing the performance limits of the converters output characteristics such as the output voltage, current, active power, efficiency, etc. Afterwards, the general procedure is applied to compare some of the most relevant converter topologies oriented to a 6.6kV drive application supplying quadratic torque loads and using 4.5kV IGBT modules. The paper concludes evaluating the comparison factors of the different converter topologies and selected semiconductors obtained by the proposed procedure. The proposed procedure can potentially be extrapolated to any desired application framework.**

***Index Terms*—Comparison Procedure, Medium Voltage (MV) - High Power Applications Converter, Multilevel Converters, Cascaded H-Bridge (CHB), Flying Capacitors (FC), Neutral Point Clamped (NPC), Semiconductors, Insulated Gate Bipolar Transistor (IGBT), AC Drives.**

## I. Introduction

THE power converters evolution is a widely reported topic among the scientific community. The importance of Medium Voltage and High Power converters has increased spectacularly due to the introduction of power electronics in applications such as [1], [2]:

- Grid oriented applications [3], [4], [5] (transmission and distribution, power quality improvement, generation, renewable energies, etc.).
- Industrial applications [6], [7] (drives for pumps, fans, rolling mills, induction heating, high power rectifiers, etc.).
- Traction applications [8] (trains, electric vehicle, marine, etc.).

In fact, with the aim of satisfying all the different applications requirements for which those power converters are used, several converter topologies and semiconductors have been developed in recent years.

On the one hand, the silicon based existing semiconductors technology is in continuous development, in order to improve the performance of the components, increasing their voltage and current rating, reliability, modularity, etc. A clear trend in the recent evolution of the semiconductors imposed by the market demands has been the increase of their voltage rating. For instance, IGBT modules have reached experimentally the 8kV of collector-emitter voltage ($V_{ce}$) [9], while the IGBT press-packs have been uncovered as a good solution for 6.5kV of $V_{ce}$ [10]. Moreover, 10kV IGCTs have been also developed experimentally [11]. Nowadays, IGBTs and IGCTs are commercially available at a maximum voltage rating of 6.5kV. Added to this, new semiconductor technologies are being developed, such as SiC based semiconductors [12] or diamond based ones [13].

On the other hand, considering the trend of using Voltage Source Converters (VSC) with increasing converter output voltage and power, the restriction of the classical two level converter imposed by the voltage rating of the semiconductors and the need of using semiconductors series connection, has lead to the development of multilevel topologies, [2], [6], [14], [15]. Although the most common topology is the 3 Level Neutral Point Clamped Voltage Source Converter (3L NPC VSC, [16]), emerging topologies are nowadays being treated, such as Flying Capacitor Converter (FC [17]), Stacked MultiCell Converter (SMC [18]), Modular Multilevel Converter (MMC [19]), Active Neutral Point Clamped Converter (ANPC [20]), etc.; each of them focused on strengthening different converters characteristics, in order to be used under different operating conditions.

Using those technological efforts, a wide range of commercial equipments offer is nowadays available in the market of the Medium Voltage and High Power applications [1], [7]. For instance, several equipment solutions can be found in the Industrial Drives market using different converter and semiconductor technologies. While some companies use the classical 3L NPC VSC with IGCTs, others apply this solution using IGBTs. Furthermore, other solutions like Cascaded H-Bridge, Current Source Converters and other topologies find a relevant place in the market [1]. However, neither the topology nor the semiconductor choice is straightforward, and each designer and company looks for its better trade-off taking into account technical, commercial, logistical and financial considerations.

Manuscript received November 9, 2010; revised January 21, 2011 and April 20, 2011. Accepted for publication July 4, 2011.



A. Sanchez-Ruiz, M. Mazuela, G. Abad and I. Baraia are with the Electronics and Computing Department, University of Mondragon, 20500 Mondragon, Spain (e-mail: asanchez@mondragon.edu; mmazuela@mondragon.edu; gabad@mondragon.edu; ibaraia@mondragon.edu).

S. Alvarez is with Ingeteam Technology S.A., 48170 Zamudio, Spain (e-mail: silverio.alvarez@ingeteam.com).

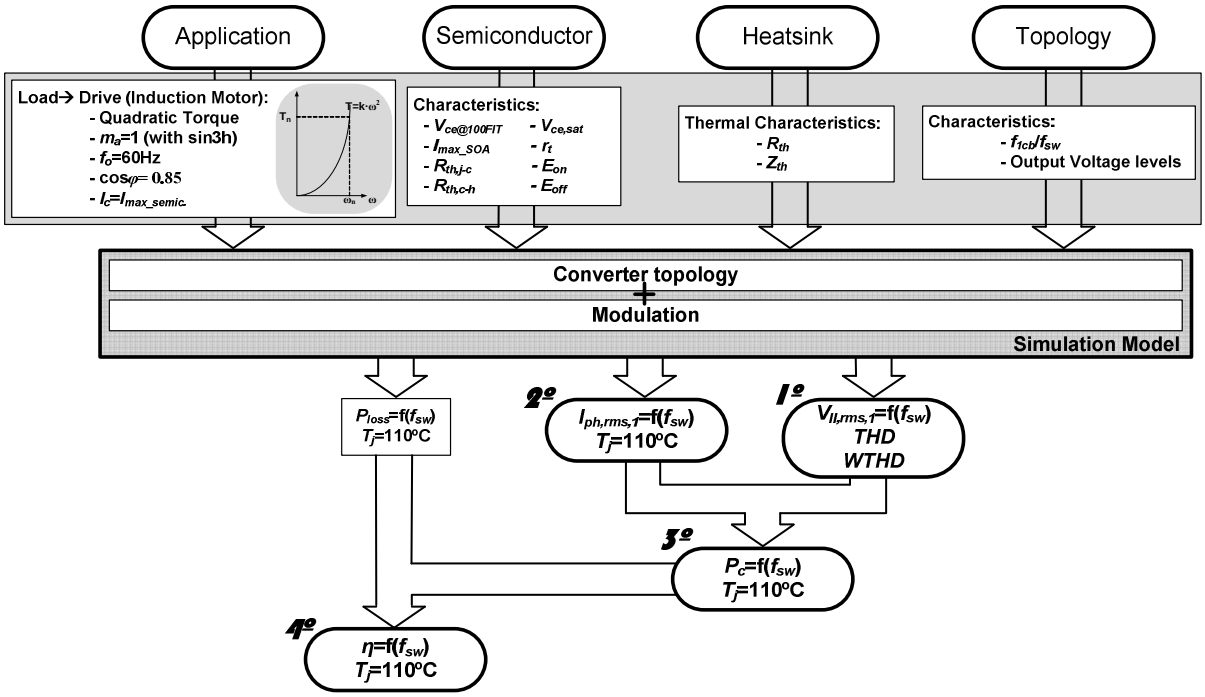



Fig. 1. Simplified block diagram of the converter selection procedure.

From the technical point of view, the selection of a suitable topology or semiconductor for a specific application becomes relevant. With this aim, several procedures and comparisons have been exposed [8], [21], [22], [23], [24], [25]. Therefore, this paper serves a new proposed topology/semiconductor selection and comparison procedure oriented to high power converter topologies. Minimization of the procedure computational cost has been an additional consideration when developing it. Such a tool, added to the requirements of the application where the converter is going to be applied, gives an approximate comparison (real accuracy is not looked for) between the different studied solutions, and can set the guidelines in order to carry out a proper selection.

As an example of the applicability of the procedure, the comparison and analysis of six chosen converter topologies for a 6.6kV drive supplying a quadratic torque load is served, using in all of them 4.5kV HV IGBT modules. Among the selected high power converter topologies, some commercially well known [2] ones are selected, while other possible and non-commercial configurations are also considered. Three of the analyzed topologies deal with a common DC bus: the 3L NPC with 2 series-connected IGBTs, the 5 Level FC, and the 5 Level SMC. The other three topologies use three isolated DC sources: the 5 Level H-Bridge NPC (5L HB NPC), the 5 Level H-Bridge FC (5L HB FC), and the 5 Level H-Bridge Neutral Point Piloted (5L HB NPP).

The obtained results roughly summarize the advantages and disadvantages of each solution and help the designer to find out a trade-off on the topology selection according to its preferences and restrictions.

## II. Proposed Converter Comparison Procedure

The proposed procedure basic block diagram is graphically illustrated in Fig. 1. As it is shown, the core block of the procedure is the detailed simulation model of the converter and the load. To create the simulation model, the necessary inputs are: the characteristics of the semiconductor with its associated heat-sink, and the VSC topology under study together with its associated modulation pattern. Besides, the application where the converter is going to operate determines the operating conditions of the simulation model. The four inputs are completely dependent on each other. Hence, with all this information and based on an interactive simulation process, the converter comparison procedure determines the main output characteristics of the converter as a function of the semiconductors' switching frequency ($f_{sw}$). These main output characteristics are:

- Output voltage ($V_{ll,rms,1}$=f($f_{sw}$)).
- Maximum output current ($I_{ph,rms,1}$=f($f_{sw}$)).
- Maximum converter output active power ($P_c$=f($f_{sw}$)).
- Efficiency ($\eta$=f($f_{sw}$)).

Nevertheless, it is important to remark that this analysis is only focused on the operation limits of the converter and its characteristics when carried to that limits. Other analyses, such as a deep study of cost or reliability, are excluded from this research work, [25].

Consequently, as it is demonstrated along this paper, the analysis of the output characteristics provided by the procedure for different considered inputs, (see Fig. 1), makes it possible to compare and conclude which solution is more suitable according to the designer criteria, under defined circumstances, needs and priorities.

The following sections introduce briefly the input and output characteristic data required and provided respectively by the proposed converter comparison procedure.

### A. Procedure Inputs

As Fig. 1 serves, four different procedure inputs can be differenced.

The first procedure input to define is the application where the comparison is going to be carried out, which defines the operating conditions, as well as the comparison framework for a pair topology-semiconductor. Among the operating conditions defined by the application, the intended output current ($I_{ph,rms,1}$), output voltage ($V_{ll,rms,1}$)-modulation index ($m_a$), output frequency ($f_o$), power factor ($\cos\phi$), etc can be found. Therefore, the comparison framework imposes the output characteristics to be optimized by the designer (available power, efficiency, THD, etc.).

Additionally, the selected semiconductors voltage rating and converter topology is carried out trading-off the maximum intended phase to phase voltage ($V_{ll,\max}$) and the semiconductors blocking capability ($V_{ce,sw}$). This maximum blocking voltage is directly influenced by the hardware construction; henceforth, the collector-emitter 100 FIT (Failure In Time rate) voltage ($V_{ce@100FIT}$) will be considered as the maximum switching voltage $V_{ce,sw}$, [23]. Furthermore, special attention must be paid to the semiconductors switching and conducting characteristics, which together with the heat-sink and the cooling system ($R_{th}$, $Z_{th}$), have a direct influence on the converter power losses and junction temperatures of semiconductors, thus, on the available output current.

Finally, each compared topology requires a certain number of semiconductors in order to provide the required output voltage. Therefore, the topology configuration, together with the number of the semiconductors and their disposition will define the final output characteristics of the converter.

### B. Simulation Model

Together with the converter topology, the modulation strategy must be settled in order to define the Simulation Model. Several modulation techniques can be applied for one specific topology. The choice of the modulation has a direct influence on the output voltage value and waveform quality (*THDv* -Total Harmonic Distortion or *WTHDv* -Weighted Total Harmonic Distortion) [26], and even in converter power losses; but also in other possible functionalities of the converter that have not been taken into account, such as voltage balancing, common mode voltage reduction, etc. [27]. In addition, when implementing the modulation, restrictions such as dead-times ($t_{DT}$), maximum-minimum conduction times ($t_{on\_\max}$ and $t_{on\_\min}$ respectively), etc. must be also considered, because their effect on the output characteristics of the converter (mainly $V_{ll}$) can be significantly important. Those times are defined according to the semiconductors switching characteristics, [28].

Moreover, the power losses of the semiconductors ($P_{loss}$) and their equivalent thermal circuits ($R_{th}$, $Z_{th}$) must be also included in the Simulation Model, in order to evaluate the semiconductors junction temperatures ($T_j$) and, therefore, to identify the converter thermal limits. This evaluation is done by estimating the semiconductors power losses, as [29] and [30] demonstrate. Although an estimation inaccuracy may derive from the use of this type of estimators [31], the use of this philosophy is widely applied for pre-design analysis.

### C. Maximum Output Voltage Analysis

Among the output indicators evaluated by the procedure, the first one is the analysis of the output voltage ($V_{ll}$) evolution with the switching frequency ($f_{sw}$). This analysis is focused on two terms:

- The fundamental voltage evolution, $V_{ll,rms,1}$=f($f_{sw}$).
- And the output voltage quality evolution, given by their *THDv*=f($f_{sw}$) and *WTHDv*=f($f_{sw}$) characteristics.

The $V_{ll,rms,1}$ output characteristic is obtained simulating the converter at several switching frequency values and measuring the voltage fundamental component from its spectral analysis (FFT). Those $V_{ll,rms,1}$,$f_{sw}$ pairs are interpolated ($V_{ll,rms,1}$=f($f_{sw}$)) by a third order function, applying the Least Square (LS) Method. In this way, the fundamental voltage values at switching frequencies that have not been simulated can be derived using

$$V_{ll,rms,1} = k_3 \cdot (f_{sw})^3 + k_2 \cdot (f_{sw})^2 + k_1 \cdot f_{sw} + k_0 \,. \qquad (1)$$

Following the same process, the output voltage *THDv* and *WTHDv* [26] are obtained measuring the fundamental and harmonics value at different switching frequencies, applying:

$$THDv[\%] = \frac{\sqrt{\sum_{h=2}^{\infty}(V_h)^2}}{V_1} \cdot 100 \,, \quad WTHDv[\%] = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2}}{V_1} \cdot 100 \,. \qquad (2)$$

### D. Maximum Output Current Analysis

Besides, with the purpose of evaluating the output current ($I_{ph,rms,1}$) evolution versus the switching frequency ($f_{sw}$), the following two limits need to be considered:

- The semiconductor current thermal limit ($I_{ph,rms,1}$), which is imposed by the maximum admissible semiconductor junction temperature ($T_{j,\max}$). The $T_j$ of all the semiconductors of the converter must be evaluated in order to find out which component settles the thermal limit under the considered operating conditions.
- The maximum semiconductor current, restricted by its Safe Operating Area, is influenced by the semiconductor switching conditions (DC voltage, driving characteristics, parasitic elements, etc.). This limit is a constant value ($I_{\max\_SOA}$) not influenced by the $f_{sw}$. This $I_{\max\_SOA}$ limits the whole converter output maximum current, henceforth, called:

$$I_{ph,rms,1,\max} = \frac{I_{\max\_SOA}}{\sqrt{2}} \cdot \quad (3)$$

In order to obtain the thermal output limit, the procedure shown in Fig. 2 is applied. The objective of those operations is to obtain the converter output current limits with as fewer simulations as needed.

The first assumption considers that the steady state semiconductor junction temperature evolution at fixed $I_{ph,rms,1}$ shows a linear evolution when varying $f_{sw}$, (step 1 in Fig. 2), thus, it can be approximated by:

$$T_j(f_{sw}, I_{ph,rms,1}) \approx k_5(I_{ph,rms,1}) + k_4(I_{ph,rms,1}) \cdot f_{sw} \cdot \quad (4)$$

Consequently, simulating three $f_{sw}$ points per $I_{ph,rms,1}$ value is more than enough to obtain the $T_j$ evolution ($k_5$ and $k_4$ constants) for a fixed $I_{ph,rms,1}$ by the use of the Least Square Method (step2). After obtaining the $T_j$=f($f_{sw}$) function, the definition of the maximum operating junction temperature ($T_{j,\max}$) of the semiconductors allows obtaining the whole converter $f_{sw,\max}$ for a given $I_{ph,rms,1}$ value (step 3) by solving the $f_{sw}$ in equation (4) at a $T_j$ equal to $T_{j,\max}$. Note that for each $I_{ph,rms,1}$ all the semiconductors of the topology have to be evaluated. From all this data only the most restrictive semiconductor junction temperature is annotated. Thus, repeating the procedure for a certain number of $I_{ph,rms,1}$ values, several couples of ($f_{sw,\max}$,$I_{ph,rms,1}$) are obtained (step 4).

After obtaining the ($f_{sw,\max}$,$I_{ph,rms,1}$) points, those are interpolated to a third order function by means of the Least Square Method (step 5). This equation, $I_{ph,rms,1}$=f($f_{sw}$), represents the thermal limitation of the converter in terms of output current.

$$I_{ph,rms,1} = k_9 \cdot (f_{sw})^3 + k_8 \cdot (f_{sw})^2 + k_7 \cdot f_{sw} + k_6 \cdot \quad (5)$$

The use of five ($f_{sw,\max}$,$I_{ph,rms,1}$) simulations points provides a good computation vs error trade-off when obtaining $I_{ph,rms,1}$=f($f_{sw}$), This implies the need of only 15 simulations for the same procedure input conditions (see Fig. 1).

Finally, once the thermal limit is calculated, the limit imposed by the semiconductor SOA current limit ($I_{ph,rms,1,\max}$) must be applied. Additionally, the switching frequency constraints ($f_{sw,\min}$, $f_{sw,\max}$) limit the operating $f_{sw}$ range (step 6). All the four operating restrictions (thermal limit, $I_{ph,rms,1,\max}$, $f_{sw,\min}$, $f_{sw,\max}$) delimit the output current characteristic at the selected procedure inputs: $I_{ph,rms,1}$=f($f_{sw}$).

### *E. Maximum Output Power Analysis*

Once the output voltage and output current characteristics versus the switching frequency have been obtained, the maximum output power characteristic ($P_c$=f($f_{sw}$)) can be calculated by evaluating both of them (1), (5) in the same $f_{sw}$ points. The maximum achievable output power is obtained by multiplication of the $V_{ll,rms,1}$=f($f_{sw}$) and $I_{ph,rms,1}$=f($f_{sw}$) calculated points, as serves

$$P_c = \sqrt{3} \cdot V_{ll,rms,1}(f_{sw}) \cdot I_{ph,rms,1}(f_{sw}) \cdot \cos\varphi \cdot \quad (6)$$

Moreover, with the aim of introducing all the operating constraints, the switching frequency ($f_{sw,\min}$, $f_{sw,\max}$) and the maximum output active power ($P_{c,\max}$=f($f_{sw}$)) limits must be applied. The $P_{c,\max}$ can be defined as follows:

$$P_{c,\max} = \sqrt{3} \cdot V_{ll,rms,1}(f_{sw}) \cdot I_{ph,rms,1,\max} \cdot \cos\varphi \cdot \quad (7)$$

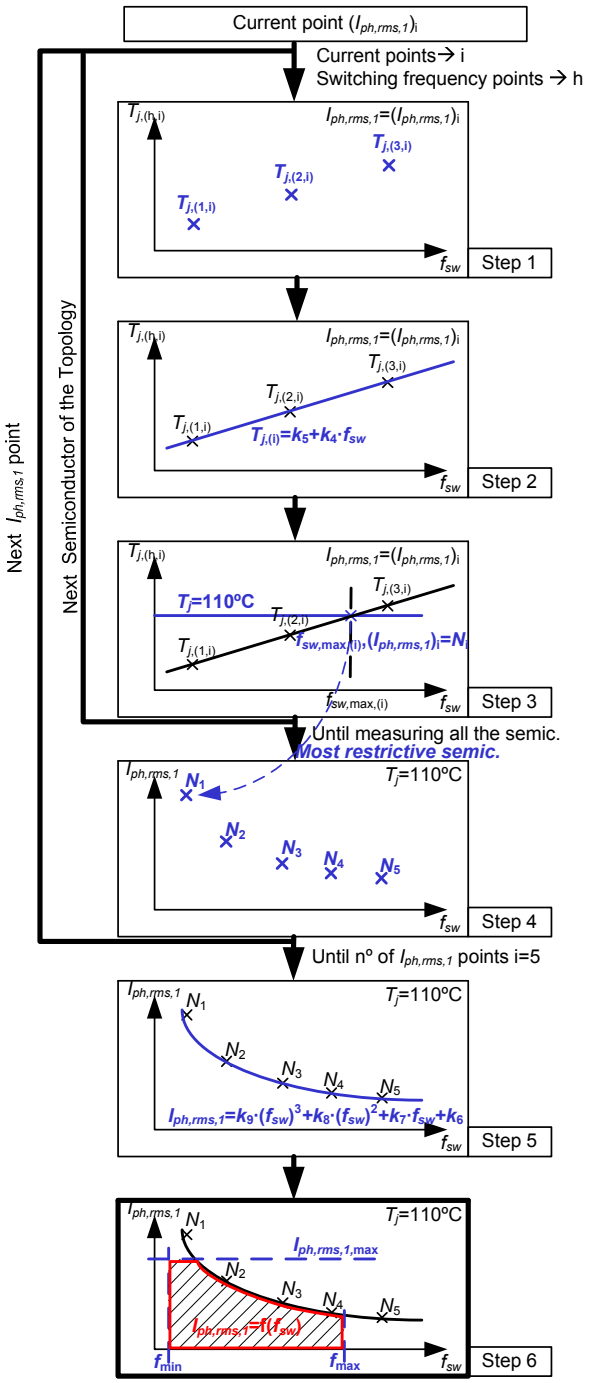



Fig. 2. Process illustration for the generation of the $I_{ph,rms,1}$=f($f_{sw}$) converter characteristic.

Therefore, with no extra simulations, the converter power limit can be evaluated: $P_c$=f($f_{sw}$); completing the third indicator proposed in Fig. 1.

### *F. Efficiency Analysis*

The silicon efficiency analysis $\eta$=f($f_{sw}$) is derived from the evaluation of the total semiconductor power losses $P_{loss}$=f($f_{sw}$) and the maximum output power $P_c$=f($f_{sw}$) characteristic:

$$\eta = \left( \frac{P_c(f_{sw})}{P_c(f_{sw}) + P_{loss}(f_{sw})} \right) \cdot 100\ [\%] \cdot \qquad (8)$$

While the $P_c$=f($f_{sw}$) characteristic is already derived, additional calculations are needed for derivation of $P_{loss}$=f($f_{sw}$). Thus, when applying the process for the current limits calculation (steps 1 to 4 of Fig. 2) and semiconductors $T_j$ is evaluated, the total semiconductors power losses measurements are carried out, as the $\eta$ calculating process illustrates (steps 1 to 4 of Fig. 3). Similarly to the Maximum Output Current Analysis, subsection II.D, five ($P_{loss}$,$f_{sw,max}$) points are calculated and interpolated in order to obtain the $P_{loss}$=f($f_{sw}$) characteristic of the converter (step 5 of Fig. 3):

$$P_{loss} = k_{13} \cdot (f_{sw})^3 + k_{12} \cdot (f_{sw})^2 + k_{11} \cdot f_{sw} + k_{10} \cdot \qquad (9)$$

To conclude the evaluation of (8), the converter power losses ratio ($r_{Ploss}$, depicted in step 6), and the ideal efficiency (step 7) are evaluated. Finally, applying the $P_{c,max}$ restrictions (step 6, Fig. 2), the final silicon efficiency characteristic of the converter, $\eta$=f($f_{sw}$) is provided (step 8).

Note that this efficiency characteristic is only an indicative of the total semiconductors' power losses. The converter efficiency can be considerably different if other power losses of the converter are evaluated and considered (passive component losses, auxiliary losses, etc.).

### *G. Other Characteristics*

Apart from the given results, mostly focused on the voltage quality and semiconductor power losses, many more several characteristics should be taken into account when trying to offer as much realistic comparison as possible. Among those characteristics, this study considers three additional main converter features that do have a direct influence on the cost and reliability of the converter:

- The stored energy is proportional to the number of inductances and capacitors used in a defined converter topology. The higher the stored energy, the bigger the volume of the converter generally is.
- The number of semiconductors needed has a direct influence on the cost and complexity of the converter. In general, if a comparison of converters with the same chosen semiconductor is done, a higher number of semiconductors may mean less reliability. If a converter comparison is made by the use of different $V_{ce}$ semiconductors, the total installed switch power ($S_S$) is recommended to be equal, in order to obtain a proper reliability characteristic, [22]. Moreover, the

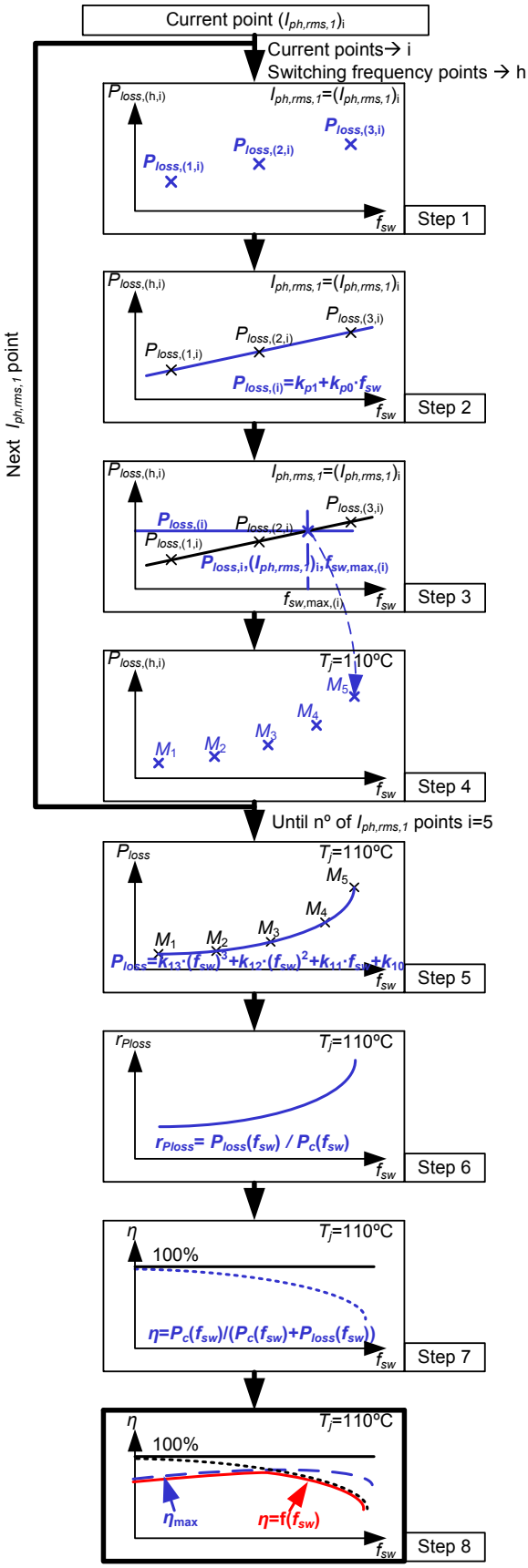



Fig. 3. Process illustration for the generation of the $\eta$=f($f_{sw}$) converter characteristic.

serialized components might reduce the reliability of the converter due to the extra circuits needed.

- Finally, another interesting characteristic is the power losses distribution among the semiconductors. A balanced distribution of power losses among all the semiconductors means a better semiconductor utilization ratio. This assumption supposes obtaining higher output power capability with the same installed power. However, if the same semiconductor is used for all the topologies, the $P_c/S_S$ ratio is clearly seen in the number of semiconductors needed by each topology.

It is important to remark that some other elements not taken into account is this study, may also have noticeable influence on the converter reliability, [25].

## III. Comparison Framework

Once the proposed procedure is presented, the selected converter topologies are going to be studied under a specific comparison framework. Therefore, the load characteristics, the semiconductor-heat-sink specifications and the modulation considerations need to be defined.

### *A. Procedure Input Data (Semiconductors, Heat-sinks and Load Characteristics)*

As introduced, the served comparison framework is focused on the selection of a 6.6kV converter topology, always using 4.5kV HV IGBT modules. The same semiconductors are used in all the considered topologies. Moreover, the selected application is an adjustable speed drive applied to supply quadratic loads such as fans, pumps, blowers, etc. [2], [32]. The main characteristic of this type of loads is the quadratic torque-speed load relationship ($T = k_{14} \cdot \omega^2$), where the worst operating point for the semiconductors is identified to be when the maximum output voltage and current (maximum output active power) is supplied by the converter (maximum torque, maximum speed). At this operating point, the output frequency $f_o$ is considered to be 60Hz, and the power factor cos$\phi$=0.85 (typical approximate value for a high power induction machine).

TABLE I
SELECTED SEMICONDUCTORS

| | MODULE REFERENCE (ABB) | |
|---|---|---|
| **IGBT1** | 5SNA1000G450300 | 4.5kV/1kA |
| **IGBT2** | 5SNA1200G450300 | 4.5kV/1.2kA |
| **DIODE** | 5SLD0650J450300 | 4.5kV/2x650A |

TABLE II
IGBT AND DIODE MODULE HEAT-SINKS' CHARACTERISTICS

| | IGBT MODULE | DIODE MODULE |
|---|---|---|
| $R_{th,h\text{-}a}$ | 5.2ºC/kW | 7.6ºC/kW |
| **MODULE DIMENSIONS** | 140x190mm | 140x130mm |

Two commercial HV IGBT modules (see Table I) are selected to carry on the comparison of the topologies. Both of them are 4.5kV HV IGBTs, with 1kA and 1.2kA of maximum collector current $I_{c,\max}$, respectively. The 100 FIT voltage of both components is 2.8kV. Furthermore, an additional diode module is also chosen for the topologies that need the use of clamp diodes. For a clearer topology comparison (see subsection II.G), neither other semiconductor types (IGCTs, low voltage IGBTs, etc.), nor other $V_{ce}$ IGBTs are considered. It is remarkable to say that only the serialization of a maximum of two semiconductors is considered, being the semiconductors parallelization out of the scope of this work.

Each module is cooled using its own associated water-cooled heat-sink. The heat-sink thermal resistances for the IGBT and diode modules are given in Table II.

The voltage rating of the selected semiconductors has a direct consequence on the selection of the converter topologies to be compared in order to attain the intended 6.6kV output voltage (see section IV). The topology selection on this paper basically seeks to study and compare the classical NPC and FC converter families and a more innovative family such as the SMC family. In this way possible commercial converter configurations, [1], are compared with other alternative topologies found in the literature. Thus, within these three main converter families, and considering the capability to arrange different number of levels and H-Bridge dispositions, six different possible configurations are chosen, all of them providing 6.6kV output voltage with the selected semiconductors.

### *B. Simulation Considerations*

The simulation model is created according to the operating conditions imposed by the defined input data of the procedure. Nevertheless, several simplification assumptions are introduced in the model considering that their impact on the final comparison result is negligible. The following paragraphs summarize the most relevant simulation model considerations adopted in this analysis:

- The semiconductors are modeled as ideal switches. Even the serialization of the semiconductors is assumed to be ideal.
- The DC bus voltage is modeled as ideal DC voltage sources. Hence, the effects of the voltage ripple and unbalance is not treated in the operation of the converter.
- The load is modeled by means of ideal AC current sources. Thus, the output current ripple is not taken into consideration. The load power factor is defined by the phase displacement between the converter voltage reference and the ideal sinusoidal output currents.
- The converter is controlled in open loop using scalar Pulse Width Modulation (PWM) with third harmonic injection, aiming to obtain the maximum converter output voltage ($V_{ll}$) for a given DC bus voltage ($V_{DC}$) [26].
- The modulation index ($m_a$) is assumed to be as served (where $V_{DC}$ is the total DC bus voltage) [26]:

$$m_a = \frac{2 \cdot \sqrt{2}}{\sqrt{3}} \cdot \frac{V_{ll,rms,1}}{V_{DC}} \cdot \tag{10}$$

- Switching frequency $f_{sw}$ constraints are considered in the modulation. The minimum $f_{sw}$ limit, ($f_{\min}$), is fixed

in order to guarantee a proper controller bandwidth according to the maximum converter output frequency ($f_{o,\max}$). The ratio $f_{\min}/f_{o,\max}$ is fixed to 10,

$$f_{\min} = 10 \cdot f_{o,\max}, \quad (11)$$

leading to minimum switching frequency of 600Hz. The hypothetical maximum $f_{sw}$ value to be analyzed ($f_{\max}$), is initially defined in relation with the controller cycle time $t_{CT}$ (task period),

$$f_{\max} = 1/\left(2 \cdot t_{CT,\max}\right). \quad (12)$$

For a conservative controller cycle time of $t_{CT}$=250µs, the $f_{\max}$ values corresponds to 2kHz. Although this maximum switching frequency may result too high for a classical MV - HP drive, the results obtained might be useful in applications where a power derate can be assumed in order to comply with harmonic standards.

- The ideal modulation pattern is combined with the addition of a minimum conduction and blocking times sum ($t_{on\_off\_\min}$=30µs) of the semiconductors and a dead time ($t_{DT}$=20µs) in order to consider the realistic output voltage characteristic of the converter. Those values do not change with $f_{sw}$. The $t_{on\_off\_\min}$ ensures to complete properly the switching transitions of the devices and keep them in a stable state (either conducting or blocking) for a minimum amount of time. Furthermore, the $t_{DT}$ guarantees that two complementary devices are not conductive at the same time during the switching transitions avoiding DC bus short-circuits, [28].
- In order to derive the thermal limits of the converter with the selected semiconductors, the first step is to estimate their power losses. The power losses on each semiconductor of each topology must be evaluated, although for simplicity it has been considered that there exists power losses distribution symmetry among all the phase legs and within a phase leg. Therefore, only the semiconductors of one phase are evaluated. With that aim, an experimentally validated tool, such as the Universal Power Losses Estimator for VSC topologies presented in [30] has been adapted and implemented in the simulation model. The on-state power losses ($P_{cond}$) and switching semiconductor energy losses ($E_{on}$ and $E_{off}$) are evaluated and averaged every switching period $T_{sw}$, according to semiconductors on-state ($V_{ce}(I_c)$) and switching ($E_{on}(I_c)$ and $E_{off}(I_c)$) characteristics and the converter operation conditions ($V_{DC}$, $I_{ph,rms,1}$, $m_a$, $f_{sw}$). The applied semiconductors on-state ($V_{ce}(I_c)$) and switching ($E_{on}(I_c)$ and $E_{off}(I_c)$) characteristics have been modeled using second order functions:

$$P_{cond}(I_c) = V_{CE}(I_c) \cdot I_c = k_{17} \cdot I_c^{\,3} + k_{16} \cdot I_c^{\,2} + k_{15} \cdot I_c \quad (13)$$

$$E_{on}(I_c) = k_{20} \cdot I_c^{\,2} + k_{19} \cdot I_c + k_{18} \quad (14)$$

$$E_{off}(I_c) = k_{23} \cdot I_c^{\,2} + k_{22} \cdot I_c + k_{21}. \quad (15)$$

- In addition to the power losses estimator, a steady-state thermal model ($R_{th}$) is used in order to get the average junction temperatures $T_j$ of the semiconductors, thus, the transient thermal model ($Z_{th}$) has not been modeled. The reason of this assumption is that the operation at 60Hz allows neglecting the $T_j$ ripple around its average value. 110ºC is chosen as the maximum admissible junction temperature ($T_{j,\max}$), whereas the ambient (water) temperature $T_a$ is fixed to 45ºC.

## IV. Studied Converter Topologies

As introduced, six converter topologies are studied in this paper. Those six converter configurations are briefly explained below, adapting to each of them a PWM modulation.

Table III summarizes the output voltage characteristics of the six studied topologies. First of all, the relationship between the phase to DC bus middle point voltages ($V_{X0}$), the apparent switching frequencies ($f_{1cb}$, first carrier band) and the semiconductors switching frequencies ($f_{sw}$) are served. Additionally, the number of levels of the $V_{X0}$ and $V_{ll}$ is summarized.

### *A. Full DC Bus Topologies*

Three of the studied converters are formed by a full DC bus of 11.2kV, which is shared into two half DC buses of 5.6kV ($V_{DC}$/2) by means of capacitors ($C_1$, $C_2$), supplying the three converters legs. The three full DC converters are illustrated in Fig. 4.

The first of those three is the 3L NPC topology [16], Fig. 4a, which is a very well known topology, widely applied in the MV Drives market and commercially available at several AC voltage levels [1]. In order to use this topology for a 6.6kV drive, the series connection of at least 2 semiconductors is required. The $V_{X0}$ voltage comprises three switching levels of amplitude $V_{DC}$/2.

The second full DC bus studied topology is the 5L FC (Fig. 4b). Although, up to nowadays, there is no available commercial equipment applying this topology, it may result interesting to reveal the possibilities offered by this converter. Each of this converter phase leg contains four switching cells and three flying capacitors charged at different voltages ($C_{3\_X}$ ($3 \cdot V_{DC}$/4), $C_{4\_X}$ ($V_{DC}$/2), $C_{5\_X}$ ($V_{DC}$/4)). The voltage of each switching cell is limited by the voltage of their adjacent capacitors to $V_{DC}$/4=2.8kV. Additionally, the triangular carriers of every switching cell are 90º phase shifted. As result, the output phase voltage has five voltage levels with voltage steps of $V_{DC}$/4.

Finally, the last analyzed VSC of the mentioned type, is the SMC 2x2 (Stacked MultiCell 2 cellules, 2 rows) or 5L SMC topology (Fig. 4c), [18]. The converter philosophy consists of joining basic commutation cells, each one formed by a two-level converter ($T/D_{1L\_1}$, $T/D_{1L\_2}$, $T/D_{2H}$). In fact, in this topology, the switches of the first cellule ($T/D_{1L\_1}$-$T/D_{1L\_2}$, $T/D_{2L}$-$T/D_{2H}$ and $T/D_{3H\_1}$-$T/D_{3H\_2}$) are arranged between the main DC bus capacitors and two intermediate flying capacitors ($C_{1\_X}$, $C_{2\_X}$) charged at $V_{DC}$/4=2.8kV. In this case, the upper and lower equivalent switches of each cellule require the series association of two switches, (e.g. $T/D_{1L\_1}$-$T/D_{1L\_2}$ and $T/D_{3H\_1}$-$T/D_{3H\_2}$ in the left side cellule), and the central equivalent switches require the anti-series association (4-segments switch, current and voltage bidirectional) of two 3-segments switches, (e.g.

$T/D_{2H}$-$T/D_{2L}$ in the left side cellule). The same semiconductor arrangement applies to the following cellule. In order to carry out the semiconductors modulation, phase shifted and level shifted triangular carriers are used, as explained in [18]. Consequently, the $V_{X0}$ voltage contains five voltage levels with voltage steps of 2.8kV.

### *B. H-Bridge Topologies*

Besides, three other VSC topologies supplied by three independent isolated DC buses, ($V_{DC}$=5.6kV, two $C_{1\_X}$ and $C_{2\_X}$ capacitors of 2.8kV), are studied. Each single phase is composed by an H-Bridge. The three $V_{X\_b}$ output-ends of each H-Bridge are joined together, forming the artificial $Z_{HB}$ neutral point, whereas the other H-Bridge output ends supply the three phase load. The three H-Bridge topologies configurations are illustrated in Fig. 5. In all cases the unipolar PWM modulation principle is applied, [26].

The first of those three topologies is the here named 5L HB NPC, served in Fig. 5a, [33], which is commercially available [1]. This configuration consists of the association of two 3L NPC legs forming a H-Bridge configuration per output phase, avoiding the series connection of semiconductors. Using this topology, five $V_{DC}$/2 voltage steps per H-Bridge are obtained.

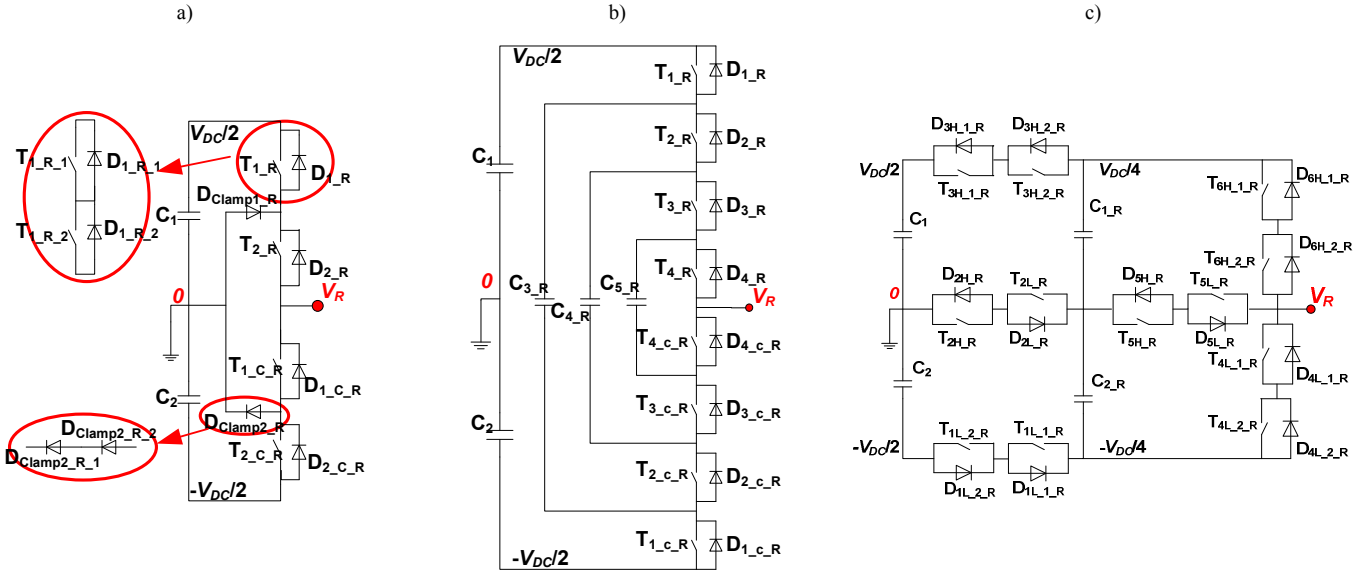



Fig. 4. Studied Full DC Bus VSC topologies. (a) 3L NPC - 2 IGBTs in Series. (b) 5L FC. (c) 5L SMC.

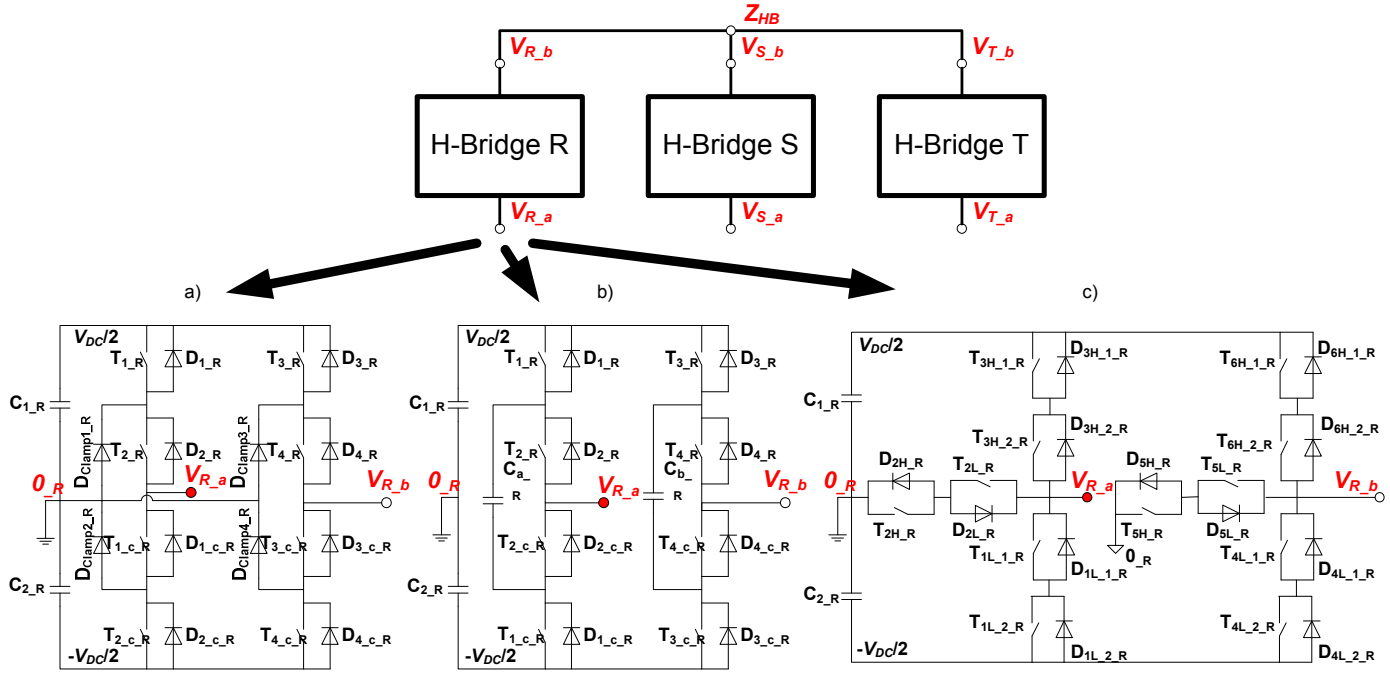



Fig. 5. Studied H-Bridge VSC topologies. (a) 5L HB NPC. (b) 5L HB FC. (c) 5L HB NPP.

The second topology, the 5L HB FC configuration (Fig. 5b), is formed by two 3L FC arms in H-Bridge configuration, [34]. Each 3L FC phase arm contains two switching cells and a flying capacitor charged at $V_{DC}/2$. In this case, the modulation voltage reference is compared with two 90º phase-shifted triangular carriers in order to generate the semiconductor gate signals of each phase leg, [34]. Therefore, the resulting H-Bridge output voltage comprises five voltage levels with voltage steps of $V_{DC}/2$.

To finish with the H-Bridge topologies, the 5L HB NPP is studied (Fig. 5c), which uses two 3L NPP (Neutral Point Piloted) arms, forming the H-Bridge, [35]. The 3L NPP is also referenced as SMC 1x2, [18]. Therefore, as a variant of the SMC converters, the operation of each cell is similar to the one explained for the cells of the 5L SMC in sub-section IV.A. This operating principle results in an H-Bridge output voltage with five voltage levels of $V_{DC}/2$ amplitude.

TABLE III
OUTPUT VOLTAGE CHARACTERISTICS OF THE STUDIED TOPOLOGIES

| | 3L NPC | 5L FC | 5L SMC | 5L HB NPC | 5L HB FC | 5L HB NPP |
|---|---|---|---|---|---|---|
| $f_{1cb}/f_{sw}$ | 1 | 4 | 2 | 2 | 4 | 2 |
| $V_{X0}$ Nº LEVELS | 3 | 5 | 5 | 5 | 5 | 5 |
| $V_{ll}$ Nº LEVELS | 5 | 9 | 9 | 9 | 9 | 9 |

## V. OUTPUT VOLTAGE ANALYSIS

This section provides the application of the maximum output voltage analysis (section II.C), for the comparison of the selected converters (section IV), in the framework explained in section III.

### *A. Fundamental Component: $V_{ll,rms,1}=f(f_{sw})$*

Firstly, the fundamental component of the output voltage ($V_{ll.rms,1}$) versus the switching frequency of the semiconductors ($f_{sw}$) is presented.

Fig. 6 shows the obtained characteristic for each topology. It can be noticed that the 5L HB NPC and 5L HB NPP have exactly the same $V_{ll,rms,1}$ vs $f_{sw}$ characteristics and very similar to the ones of the 3L NPC and 5L SMC topologies. All these topologies present a maximum approximately at 1kHz. In the same way, the characteristics of the 5L FC and the 5L HB FC topologies are very close each other and reach a maximum at the lowest switching frequency $f_{sw}$=600Hz. Above 1kHz all the topologies show a decrease of the output voltage with the increase of the switching frequency. This effect is related to the influence of the minimum conduction and blocking time ($t_{on\_off\_min}$) and the dead time ($t_{DT}$), and it is more remarkable in the FC topologies since all the switching cells operate in commutation permanently showing the highest apparent output frequency ($f_{1cb}$=4·$f_{sw}$).

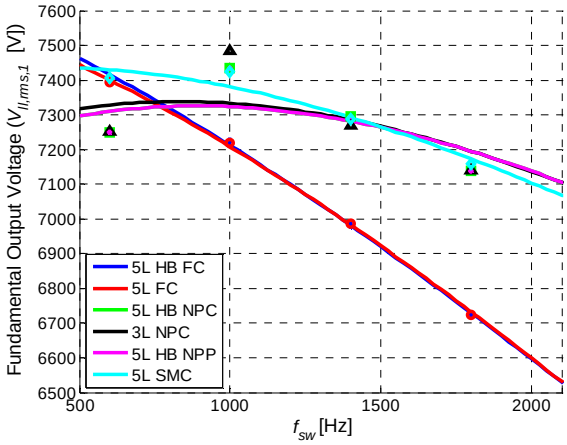



Fig. 6. Fundamental output voltage ($V_{ll,rms,1}$) vs switching frequency ($f_{sw}$) for the studied topologies: $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV.

### *A. Voltage Quality*

Furthermore, the voltage quality of each topology is evaluated in terms of voltage Total Harmonic Distortion (*THDv*) and Weighted Total Harmonic Distortion (*WTHDv*).

Fig. 7 shows the evolution with the $f_{sw}$ of the $V_{ll,rms,1}$ *THDv* provided by each studied topology. On the one hand, it can be noted that the 5L FC topology shows the lowest *THDv* at $f_{sw}$=600Hz, but the 5L SMC and the 5L HB NPP show the lowest *THDv* in most of the $f_{sw}$ range, which is related to their higher $V_{ll,rms,1}$ and a $f_{1cb}$=2·$f_{sw}$. On the other hand, the 3L NPC topology shows the highest *THDv* value. Additionally, in all topologies, the *THDv* value increases with the $f_{sw}$, which is explained by the fact that the $V_{ll,rms,1}$ decreases with the $f_{sw}$ and the harmonics remain nearly the same.

Concerning the *WTHDv*, Fig. 8, each topology presents a minimum value at different $f_{sw}$. The FC topologies provide lower *WTHDv* in the low $f_{sw}$ range, whereas at higher $f_{sw}$ values the 5L SMC, 5L HB NPC and 5L HB NPP present a better behavior. Again, this fact is explained by the reduction of the $V_{ll,rms,1}$ with the $f_{sw}$ in all topologies and more remarkably in the FC topologies.

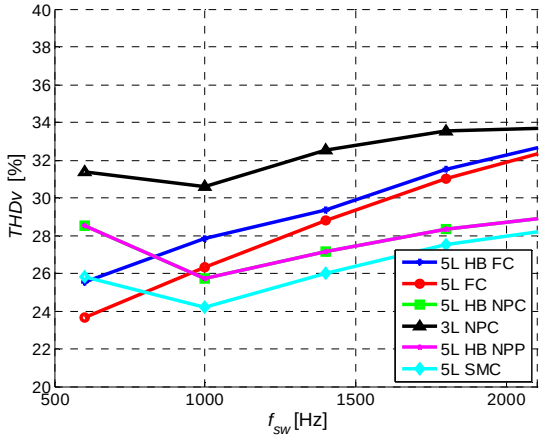



Fig. 7. Output voltage ($V_{ll,rms,1}$) *THDv* vs switching frequency ($f_{sw}$) for the studied topologies: $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV.

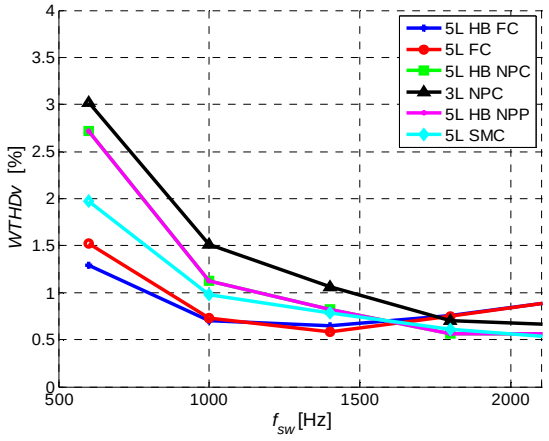



Fig. 8. Output voltage ($V_{ll,rms,1}$) *WTHDv* vs switching frequency ($f_{sw}$) for the studied topologies: $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV.

## VI. Output Current Analysis

This section presents the maximum output current analysis of the selected topologies. Hence, according to the procedure explained in chapter II.D, the $I_{ph,rms,1}$=f($f_{sw}$) characteristics are obtained.

Fig. 9 and Fig. 10 show the $I_{ph,rms,1}$=f($f_{sw}$) characteristics for IGBT1 and IGBT2, respectively. Moreover, the four limiting constraints (thermal limits, $I_{ph,rms,1,\max}$, $f_{\min}$, $f_{\max}$) are illustrated, defining the attainable $I_{ph,rms,1}$ versus $f_{sw}$ operating area of the converters. Among the six studied topologies, in terms of output current, they can be divided in 3 groups: the NPC (3L NPC, 5L HB NPC), the FC (5L HB FC, 5L FC) and the SMC (5L HB NPP, 5L SMC) topologies. On each group, the concerning topologies reveal the same output current behavior $I_{ph,rms,1}$=f($f_{sw}$).

Analyzing the results, the SMC topologies clearly provide the best current performance, due to the reduction in the switching losses of the serialized semiconductors (the most critical ones), which operate at half the $V_{ce@100FIT}$ ($V_{ce,sw}$=$V_{ce@100FIT}$/2) instead of the whole 100 FIT voltage for the rest of the topologies. After the SMC topologies, the NPC topologies present a better output current characteristic, although they are quite close to the characteristic of the FC topologies at low $f_{sw}$.

Comparing the characteristics provided both IGBTs (Fig. 9 and Fig. 10) at a defined $f_{sw}$ (Fig. 11), it is remarkable that IGBT1 provides slightly better thermal limit characteristic than IGBT2. This is explained by the fact that with those IGBTs the switching losses are dominant to the conduction losses, presenting IGBT1 lower switching losses characteristic than IGBT2. Therefore, the capability of conducting more current is penalized with high power losses. Nevertheless, at low switching frequencies or when the switching losses are not dominant, the output current limit is imposed by the semiconductors $I_{\max\_SOA}$, and not by the thermal limit, which reveals the interest of considering the use of IGBT2 to increase the converter output current. This fact is noticeable in the SMC topologies, where the output current SOA limit is dominant at higher $f_{sw}$ values.

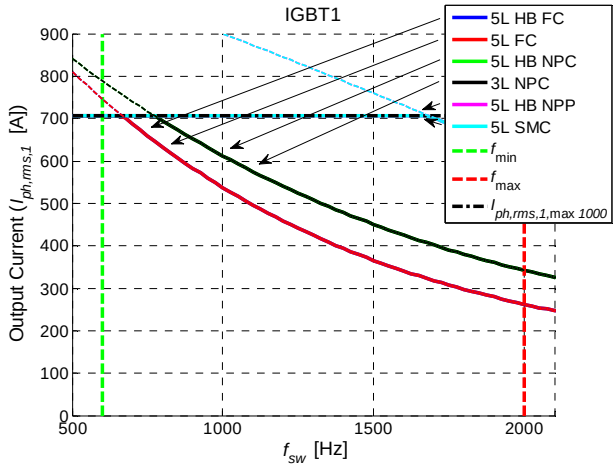



Fig. 9. $I_{ph,rms,1}$=f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,\max}$=110ºC. IGBT1 ($V_{ce}$=4.5kV/$I_c$=1kA).

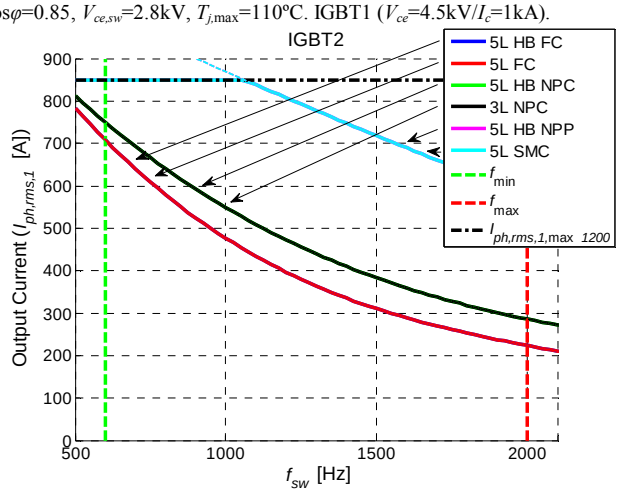



Fig. 10. $I_{ph,rms,1}$=f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,\max}$=110ºC. IGBT2 ($V_{ce}$=4.5kV/$I_c$=1.2kA).

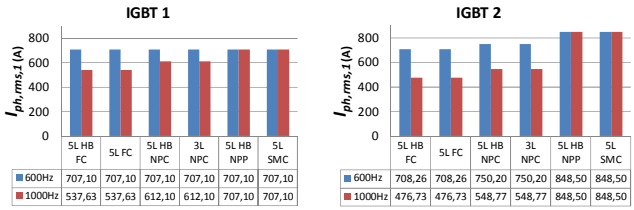



Fig. 11. Topologies attainable output current $I_{ph,rms,1}$ at two specific $f_{sw}$ (600Hz and 1kHz) for IGBT1 and IGBT2.

For instance, at $f_{sw}$=1kHz, IGBT2 allows an output current of $I_{ph,rms,1}$=848.5A compared to the $I_{ph,rms,1}$=707.1A of IGBT1 for the SMC topologies. However, IGBT1 provides slightly higher output current than IGBT2 for the NPC and FC topologies. At 600Hz, the current limit for all the topologies with IGBT1 is fixed by its $I_{ph,rms,1,\max}$=707.1A, whereas with IGBT2 only the SMC and NPC topologies provide considerably higher current, $I_{ph,rms,1}$=848.5A and $I_{ph,rms,1}$=750.2A respectively. Notice that for the SMC topologies, IGBT1 and IGBT2 have the same current limit at 600Hz as at 1kHz because in both cases the limit is fixed by the $I_{ph,rms,1,\max}$.

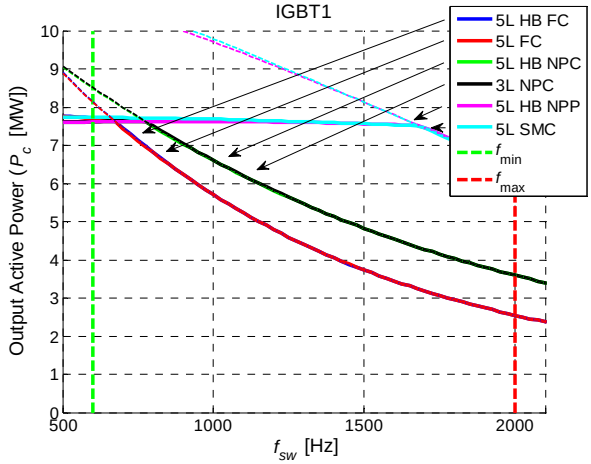



Fig. 12. $P_c$=f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,max}$=110ºC. IGBT1 ($V_{ce}$=4.5kV/$I_c$=1kA).

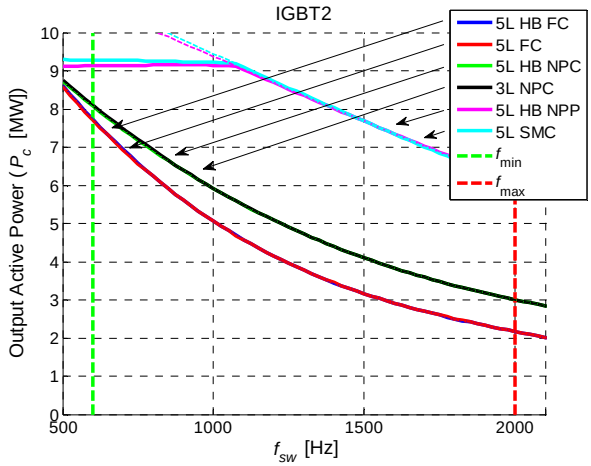
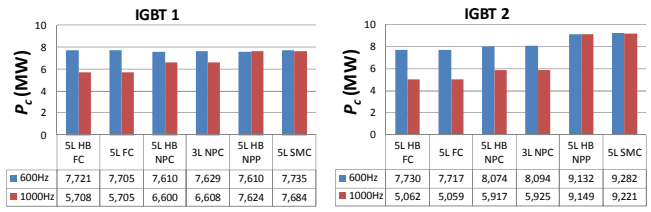



Fig. 13. $P_c$= f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,max}$= 110ºC. IGBT2 ($V_{ce}$=4.5kV/$I_c$=1.2kA).




| IGBT 1 | 5L HB FC | 5L FC | 5L HB NPC | 3L NPC | 5L HB NPP | 5L SMC |
|---|---|---|---|---|---|---|
| 600Hz | 7,721 | 7,705 | 7,610 | 7,629 | 7,610 | 7,735 |
| 1000Hz | 5,708 | 5,705 | 6,600 | 6,608 | 7,624 | 7,684 |

| IGBT 2 | 5L HB FC | 5L FC | 5L HB NPC | 3L NPC | 5L HB NPP | 5L SMC |
|---|---|---|---|---|---|---|
| 600Hz | 7,730 | 7,717 | 8,074 | 8,094 | 9,132 | 9,282 |
| 1000Hz | 5,062 | 5,059 | 5,917 | 5,925 | 9,149 | 9,221 |

Fig. 14. Topologies attainable output power $P_c$ at two specific $f_{sw}$ (600Hz and 1kHz) for IGBT1 and IGBT2.

## VII. Output Power Analysis

Once the output voltage (section V) and output current (section V.A) characteristics for each converter topology are obtained, the converter output power characteristics $P_c$=f($f_{sw}$) is derived (section II.E).

Fig. 12 and Fig. 13 serve the output power limits for the six studied topologies. Converters response is divided in three main groups in the same way as the current evolves. As depicted in Fig. 12 (IGBT1), all the power characteristics are limited by the $P_{c,max}$ ($I_{ph,rms,1,max}$) limit in the lower switching frequency range. However, with IGBT2, Fig. 13, only the SMC topologies allow reaching the $P_{c,max}$ limit of the semiconductor. In the rest of the topologies the thermal limit is the most restrictive limit. This means that for both semiconductors, the SMC family provides the maximum power among the studied topologies, followed by the NPC topologies and finally the FC topologies. Fig. 14 summarizes the output power attainable values for all topologies with IGBT1 and IGBT2 at two defined switching frequencies, $f_{sw}$=600Hz and $f_{sw}$=1kHz. The maximum output power values are provided by the 5L SMC (9.282MW) and 5L HB NPP (9.132MW) at both switching frequencies ($P_{c,max}$ limit) with IGBT2. At $f_{sw}$=600Hz, all the topologies provide more power with IGBT2. However, at $f_{sw}$=1kHz, the NPC and FC topologies can provide more power with IGBT1 rather than with IGBT2.

## VIII. Efficiency Analysis

In order to complete the topologies evaluation, the efficiency characteristic $\eta$=f($f_{sw}$) of each one is obtained for the semiconductors in consideration, sub-section II.F.

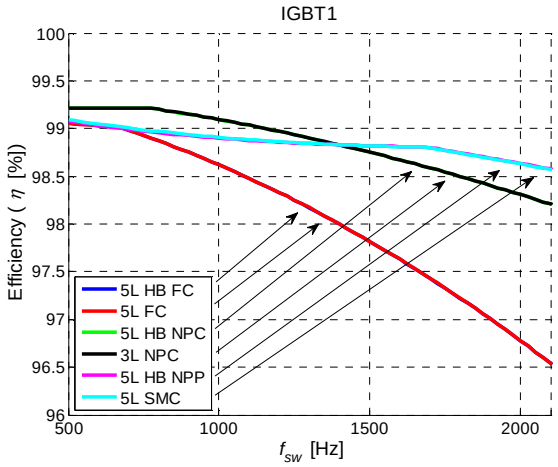



Fig. 15. $\eta$=f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,max}$=110ºC. IGBT1 ($V_{ce}$=4.5kV/$I_c$=1kA).

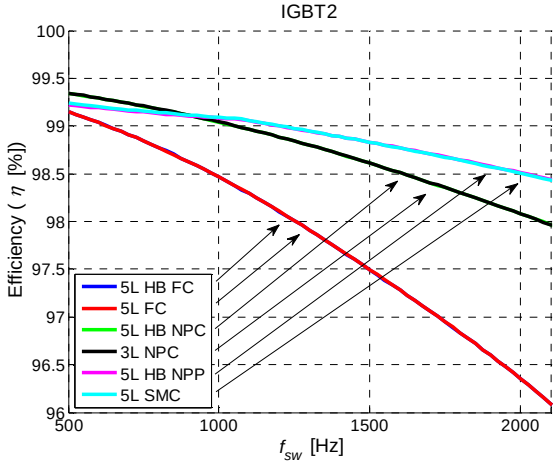



Fig. 16. $\eta$=f($f_{sw}$) for all the studied topologies. $f_o$=60Hz, $m_a$=1.15, cos$\varphi$=0.85, $V_{ce,sw}$=2.8kV, $T_{j,max}$=110ºC. IGBT2 ($V_{ce}$=4.5kV/$I_c$=1.2kA).

Fig. 15 and Fig. 16 show the efficiency characteristic of the studied topologies with IGBT1 and IGBT2. In the most part of the $f_{sw}$ range, the efficiency performance of the different topologies follows the same tendency as the output power characteristics. The best efficiency evolution with the

$f_{sw}$ is provided by the 5L SMC and 5L HB NPP; although at low switching frequencies, the NPC topologies show a slightly higher efficiency. Nevertheless, at those low switching frequencies, the efficiency difference among the topologies is not very relevant and in all the cases its value is around 99%.

As with the output power characteristic, IGBT2 only provides better efficiency in the lower frequency range. For all the topologies, above a certain switching frequency, IGBT1 allows obtaining better efficiency ratios.

TABLE IV
CAPACITORS REQUIREMENT FOR EACH TOPOLOGY (10% PEAK TO PEAK VOLTAGE RIPPLE, $f_{sw}$=600HZ)

| TOPOLOGY | CAPACITORS VALUES | ENERGY | RMS CURRENT |
|---|---|---|---|
| **3L NPC** | 2XC=0.94MF-5.6KV | 29.5KJ | $I_{C1}$=282A<br>$I_{C2}$=220A |
| **5L FC** | 3XC=0.78MF-2.8KV<br>3XC=0.78MF-5.6KV<br>3XC=0.78MF-8.4KV<br>1XC=0.78MF-11.2KV | 176KJ | $I_{C1}$=294A<br>$I_{C2}$=294A<br>$I_{C3\_X}$=268A<br>$I_{C4\_X}$=258A<br>$I_{C5\_X}$=240A |
| **5L SMC** | 2XC=2MF–5.6KV<br>6XC=1.3MF–2.8KV | 93KJ | $I_{C1}$=285A<br>$I_{C2}$=277A<br>$I_{C1\_X}$=228A<br>$I_{C2\_X}$=220A |
| **5L HB NPC** | 6XC=4.78MF–2.8KV | 112KJ | $I_{C1\_X}$=392.7A<br>$I_{C2\_X}$=397.7A |
| **5L HB FC** | 3XC=4.43MF–5.6KV<br>6XC= 0.75MF–2.8KV | 226KJ | $I_{C1\_X}$=404A<br>$I_{C2\_X}$=404A<br>$I_{CA\_X}$=235A |
| **5L HB NPP** | 6XC=4.78MF–2.8KV | 112KJ | $I_{C1\_X}$=392.7A<br>$I_{C2\_X}$=397.7A |

## IX. OTHER CHARACTERISTICS

As explained in section II.G, other relevant characteristics need to be considered in order to complete a proper comparison of the six studied topologies.

### *A. Capacitors / Stored Energy*

Considering the particularities of each topology, the required capacity and the more relevant figures for each capacitor is calculated by simulation defining a 10% peak to peak voltage ripple of its average voltage operation. Table IV serves for each topology, the count of capacitors and their values in terms of capacity and voltage, the amount of total energy stored and the RMS current of each capacitor.

As an overview, it can be noticed that HB topologies store higher energy than their equivalent topologies with single DC buses. Besides this, the FC topologies require the highest energy storage for both HB and single DC bus topologies. It has to be remarked that the topology requiring the least energy storage is the 3L NPC. Finally, the RMS values of current are reasonably aligned with the stored energies.

### *B. Number of Semiconductors*

Furthermore, Table V serves the semiconductor count for each topology. It is found that the topologies that require the least number of semiconductors are the FC topologies. Moreover, the 5L SMC and 5L HB NPP topologies require the highest number. It is important also to remark that only FC topologies and 5L HB NPC topology do not need series connection of IGBTs, a technological requirement which impose additional efforts for the arrangement and control of the semiconductors.

TABLE V
NUMBER OF REQUIRED SEMICONDUCTORS FOR EACH TOPOLOGY

| TOPOLOGY | TOTAL Nº OF SWITCHES | Nº OF IGBTS | Nº OF DIODES | COUPLES OF IGBTS / DIODES IN SERIES |
|---|---|---|---|---|
| **3L NPC** | 60 | 24 | 36 | 12/18 |
| **5L FC** | 48 | 24 | 24 | 0 |
| **5L SMC** | 72 | 36 | 36 | 12/12 |
| **5L HB NPC** | 60 | 24 | 36 | 0 |
| **5L HB FC** | 48 | 24 | 24 | 0 |
| **5L HB NPP** | 72 | 36 | 36 | 12/12 |

### *C. Semiconductor Power Losses Distribution*

For simplicity in the exposition, Fig. 17 only shows the temperature distribution of the semiconductors, of the 3L NPC, 5L SMC and 5L FC topologies at three different switching frequencies (600Hz, 1kHz and 1.4kHz), as each of them is coupled with the remaining other three topologies. Moreover, only representative semiconductors of each converter are illustrated, as they provide by symmetry the information for the rest of semiconductors.

From Fig. 17, it is found that the FC topology presents the most balanced temperature distribution. Consequently, the best semiconductor utilization is achieved by this converter. In the rest of topologies, the power losses and therefore the temperature distribution is focused on specific semiconductors according to the operating conditions. In the considered conditions of this paper, the outer transistors ($T_1$) of the NPC topologies are the most critical ones, whereas, the serialized outer semiconductors ($T_{1\_L}$) result to be the most critical ones in the SMC topologies.

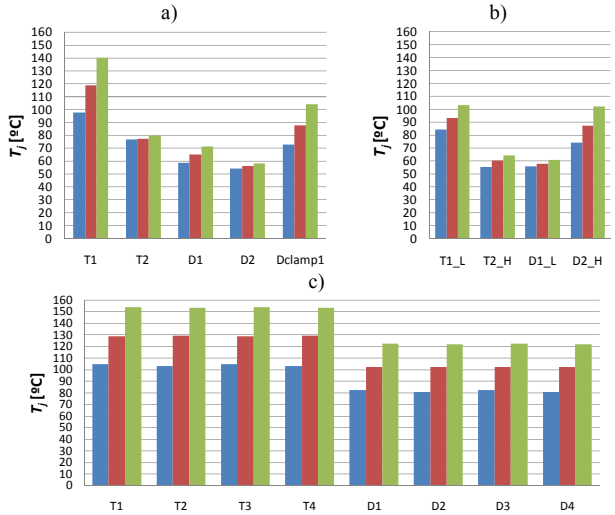



Fig. 17. Temperature distribution for of all semiconductors of different topologies with IGBT1 at $I_{ph,rms,1}$=707.1A ($f_o$=60Hz, $m_a$=1.15, cos$\phi$=0.85, $V_{ce,sw}$=2.8kV, $t_{on\_of\_,min}$=30µs and $t_{D1}$=20µs). (a) 3L NPC, (b) 5L SMC, (c) 5L FC. Three $f_{sw}$ values: 600Hz (blue), 1kHz (red) and 1.4kHz (green).

## X. Comparison and Discussion

Once the most important characteristics for each topology are obtained, the comparison among them can be carried out. The versatility of the characteristics obtained by means of this procedure allows performing easily such comparisons, focusing the priority on different criteria (linked by the $f_{sw}$) such as maximization of the output power/current, voltage quality, efficiency, etc. Here next, two comparison examples are shown, both of the possible operating points of a MV power converter.

### *A. Topologies Comparison at $I_{ph,rms,1}$=620A ($P_c$=6MW at $V_{ll,rms,1}$=6.6kV), IGBT2*

The first comparison criterion is set to obtain an output current of $I_{ph,rms,1}$=620A, which corresponds to an output power of $P_c$=6MW at a motor phase to phase voltage of $V_{ll,rms,1}$=6.6kV. In this case, the comparison is performed with IGBT2. Table VI summarizes the obtained data, together with other relevant data for the comparison among topologies, such as the number of semiconductors, capacitors (normalized at 2.8kV capacitors), etc.

First, the maximum operating switching frequency at $I_{ph,rms,1}$=620A for each topology is obtained from Fig. 10, which means selecting the $f_{sw}$ that suits the operation of the most restrictive semiconductor for each topology at $T_{j,\max}$=110ºC with the cited current point. Then, with the obtained $f_{sw}$ values, the maximum attainable voltage $V_{ll,rms,1}$ for each topology is obtained. Subsequently, with the same $f_{sw}$ values the *THDv* and *WTHDv* data for each topology can be obtained from Fig. 7 and Fig. 8.

It can be noticed that the maximum operating $f_{sw}$ is reached by the 5L SMC and 5L HB NPP topologies (1.8kHz) allowing to obtain the best *WTHDv* values (0.62% and 0.57%). In addition, compared with the other studied topologies, they present a medium capacitor requirement in terms of stored energy and number of capacitors. However, this good performance is achieved thanks to the use of the highest number of IGBTs compared with the other topologies, with the additional need of IGBTs series connection.

The worst performance in terms of *WTHDv* is provided by the 3L NPC and 5L HB NPC topologies (2.1% and 1.72% respectively), although their requirement in terms of stored energy, number of capacitors and number of controlled semiconductors can be considered as its mayor advantage; however, the 3L NPC requires semiconductors series connection. The FC topologies provide an average performance in terms of voltage *WTHD* with the smallest total amount of semiconductors, but with the highest requirements in terms of stored energy and number of capacitors.

In terms of converter efficiency, the NPC topologies show the best performances although the difference is not very significant.

### *B. Topologies Comparison at $f_{sw}$=1000Hz, IGBT1*

In an alternative way, the results obtained by the application of the procedure can be compared, for instance, at equal $f_{sw}$ conditions. Table VII shows the obtained results at $f_{sw}$=1000Hz with IGBT1.

In this case again, the maximum output power and current (SOA limit) is provided by the 5L SMC and 5L HB NPP topologies. However, under these circumstances, they do not provide the best *WTHDv* performances; it is the FC topologies that offer the best *WTHDv* ratios at equal $f_{sw}$, although they serve less output power and currents than the other topologies. In terms of output power and current, the NPC topologies are an intermediate option with the worst voltage *WTHD* ratios.

Concerning the rest of the characteristics (semiconductor count, energy stored in capacitor, efficiency, etc.), the same comments as in the previous comparison apply (see Table VI and subsection X.A).

### *C. Discussion*

According to the brief comparisons of the previous sections, the 5L SMC and 5L HB NPP topologies allow maximizing the achievable output power, with reasonably good voltage *WTHD*s, number of capacitors and stored energy in capacitors. On the contrary, they get these good results thanks to the need of higher number of semiconductors and the need of their serialization. Afterwards, the NPC and FC topologies can achieve comparable output powers and *WTHDv* performances, choosing the appropriate $f_{sw}$ for each topology. The FC topologies require the lowest amount of semiconductors but with the higher amount of capacitors and their corresponding stored energy. The NPC topologies require higher number of diodes rather than FC topologies but lower capacitors requirements.

Other kind of comparisons can be performed from the topologies characteristics obtained by the presented procedure (constant *WTHDv*, constant efficiency, etc.). Nevertheless, this information helps to clearly compare certain properties of several solutions for a certain application. To make a deeper comparison, this information must be complemented with other more ambiguous, but relevant technical and commercial factors that can help the designer to select one or other solution according to its preferences and restrictions such as:

- Total DC bus voltage (11.2kV against 5.6kV).
- Transformer characteristics and requirements (single winding or multi-winding).
- Diode Front End (DFE) and Active Front End (AFE) possible solutions.
- Semiconductors/heat-sinks isolation required strategy.
- Modulation and capacitors voltage balancing complexity.
- Auxiliary systems and needs (drivers, power supplies, pre-charging and discharging circuits, breaking choppers, output filters, etc.).
- Patented topologies.
- Etc.

TABLE VI
TOPOLOGIES OPERATION VALUES AT $I_{ph,rms,1}$=620A ($P_c$=6MW AT $V_{ll,rms,1}$=6.6KV) WITH IGBT2

| | 3L NPC | 5L FC | 5L SMC | 5L HB NPC | 5L HB FC | 5L HB NPP |
|---|---|---|---|---|---|---|
| $f_{sw}$ (Hz) | 850 | 700 | 1800 | 850 | 700 | 1800 |
| $V_{ll,rms,1}$ (V) | 7330 | 7350 | 7200 | 7330 | 7370 | 7200 |
| $P_c$ (MW) | 6.65 | 6.93 | 6.68 | 6.65 | 6.93 | 6.68 |
| *THD* (%) | 30.9 | 24.35 | 27.53 | 26.8 | 26.1 | 28.3 |
| *WTHD* (%) | 2.1 | 1.33 | 0.62 | 1.72 | 1.15 | 0.57 |
| $f_{1cb}$ (Hz) | 850 | 2800 | 3600 | 1700 | 2800 | 3600 |
| Nº IGBTS | 24 | 24 | 36 | 24 | 24 | 36 |
| Nº DIODES | 36 | 24 | 36 | 36 | 24 | 36 |
| SERIES CONNECT. | YES | NO | YES | NO | NO | YES |
| Nº CS (2.8KV) | 4 | 22 | 10 | 6 | 12 | 6 |
| CS ENERGY (KJ) | 30 | 176 | 93 | 112 | 226 | 111 |
| EFFICIENCY (%) | 99.15 | 98.91 | 98.65 | 99.15 | 98.91 | 98.65 |

TABLE VII
TOPOLOGIES OPERATION VALUES AT $f_{sw}$=1KHZ WITH IGBT1

| | 3L NPC | 5L FC | 5L SMC | 5L HB NPC | 5L HB FC | 5L HB NPP |
|---|---|---|---|---|---|---|
| $I_{ph,rms,1}$ (A) | 612 | 538 | 707 | 612 | 538 | 707 |
| $V_{ll,rms,1}$ (V) | 7333 | 7208 | 7381 | 7324 | 7212 | 7324 |
| $P_c$ (MW) | 6.61 | 5.71 | 7.68 | 6.61 | 5.71 | 7.62 |
| *THD* (%) | 30.59 | 26.34 | 24.21 | 25.73 | 27.83 | 25.73 |
| *WTHD* (%) | 1.50 | 0.73 | 0.98 | 1.13 | 0.71 | 1.13 |
| $f_{1cb}$ (Hz) | 1000 | 4000 | 2000 | 2000 | 4000 | 2000 |
| EFFICIENCY (%) | 99.10 | 98.62 | 98.91 | 99.10 | 98.62 | 98.91 |

Furthermore, the application of this procedure can be easily extended to other existing topologies and semiconductors ratings providing a more rich comparison.

## XI. CONCLUSIONS

The comparison procedure presented and evaluated in this paper, has been demonstrated as a useful and powerful tool that helps to quantify the advantages and disadvantages of different converter topologies for a specific application. Despite the fact that the procedure has been applied to a specific drive application, it can also be useful for a wide range of comparison frameworks, for instance:

- Comparison of the most suitable application (reactive power compensation, generation, drive, HVDC, etc.), for a specific converter topology and semiconductor.
- Comparison of the most suitable semiconductor (IGCTs, IGBTs, etc.), for a specific converter topology operating at one or different applications.
- Etc.

Apart from these potential possibilities of comparison, the procedure itself permits to reveal intrinsic characteristics of the semiconductors, topologies and applications studied. For example:

- Which semiconductor rating is better suited to operate at lower or higher switching frequencies.
- The ingeniousness of some topologies looking for power losses reduction and therefore increase of maximum achievable output current, as done in 5L SMC or 5L HB NPP topologies by using the series connection of IGBTs.
- The equivalence and exactly equal behavior in terms of maximum achievable output current of different converter topologies: 5L FC and 5L HB FC, 5L SMC and 5L HB NPP, and 3L NPC and 5L HB NPC couples.
- In an specific operation, for a given converter topology, which are the operating points that produce higher power losses in terms of modulation index, output current, power factor, etc…, i.e. which are the most restrictive points and semiconductors.
- Etc.

Finally, it can be concluded that the research work presented, apart from the already mentioned benefits, allows also converter or semiconductor manufacturers to have a wider perspective about the capacity and possibilities of their products, as well as to help in the decision for their newer products tendencies, providing a more efficient response to their clients.

## XII. REFERENCES


[1] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2219-2230, 2010.

[2] S. Kouro, M. Malinowski, K. Gopakumar, G. Franquelo, J. Pou, J. Rodriguez, B. Wu, and A. Perez, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics,* vol. PP, pp. 1-1, 2010.

[3] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Transactions on Industrial Electronics,* vol. 53, pp. 1002-1016, 2006.

[4] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM," *IEEE Transactions on Industrial Electronics,* vol. 55, pp. 21-29, 2008.

[5] M. Liserre, R. Cardenas-Dobson, M. Molinas, and J. Rodriguez, "Overview of Multi-MW wind turbines and wind parks," *IEEE Transactions on Industrial Electronics,* vol. PP, pp. 1-1, 2011.

[6] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 2930-2945, 2007.

[7] B. K. Bose, "Power Electronics and Motor Drives Recent Progress and Perspective," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 581-588, 2009.

[8] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," *IEEE Transactions on Power Electronics,* vol. 20, pp. 1328-1336, 2005.

[9] M. Rahimo, A. Kopta, S. Eicher, N. Kaminski, F. Bauer, U. Schlapbach, and S. Linder, "Extending the boundary limits of high voltage IGBTs and diodes to above 8 kV," in *Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs (ISPSD 2002)*, 2002, pp. 41-44.

[10] M. Rahimo and S. Klaka, "High voltage semiconductor technologies," in *13th European Conference on Power Electronics and Applications (EPE '09)*, 2009, pp. 1-10.

[11] S. Bernet, E. Carroll, P. Streit, O. Apeldoorn, P. Steimer, and S. Tschirley, "10 kV IGCTs," *IEEE Industry Applications Magazine,* vol. 11, pp. 53-61, 2005.

[12] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si-Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," *IEEE Transactions on Industrial Electronics,* vol. 58, pp. 2872-2882, 2011.

[13] S. Hadlington, "Hot rocks [single crystal diamond for power semiconductor devices]," *IEE Review,* vol. 51, pp. 30-33, 2005.

[14] L. Jih-Sheng and P. Fang Zheng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications,* vol. 32, pp. 509-517, 1996.

[15] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The Age of Multilevel Converters Arrives," *IEEE Industrial Electronics Magazine,* vol. 2, pp. 28-39, Jun. 2008.

[16] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications,* vol. IA-17, pp. 518-523, 1981.

[17] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *23rd Annual IEEE Power Electronics Specialists Conference (PESC '92)*, 1992, pp. 397-403 vol.1.

[18] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 978-987, 2002.

[19] M. Hiller, D. Krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *13th European Conference on Power Electronics and Applications (EPE '09)* 2009, pp. 1-10.

[20] T. Chaudhuri, A. Rufer, and P. K. Steimer, "The Common Cross-Connected Stage for the 5L ANPC Medium Voltage Multilevel Inverter," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2279-2286, 2010.

[21] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters," *IEEE Transactions on Industry Applications,* vol. 43, pp. 1032-1040, 2007.

[22] D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV Medium-Voltage Multilevel Converters for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 2979-2992, 2007.

[23] J. A. Sayago, T. Bruckner, and S. Bernet, "How to Select the System Voltage of MV Drives - A Comparison of Semiconductor Expenses," *IEEE Transactions on Industrial Electronics,* vol. 55, pp. 3381-3390, 2008.

[24] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Comparison of Neutral-Point-Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2297-2306, 2010.

[25] J. W. Kollar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *6th International Conference on Integrated Power Electronics Systems (CIPS 2010)*, 2010.

[26] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters (Principles and Practice)*, 2003.

[27] R. S. Kanchan, P. N. Tekwani, and K. Gopakumar, "Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive," *IEEE Transactions on Power Electronics,* vol. 21, pp. 1676-1683, 2006.

[28] Z. Dongsheng and D. G. Rouaud, "Dead-time effect and compensations of three-level neutral point clamp inverters for high-performance drive applications," *IEEE Transactions on Power Electronics,* vol. 14, pp. 782-788, 1999.

[29] F. Blaabjerg, U. Jaeger, and S. Munk-Nielsen, "Power losses in PWM-VSI inverter using NPT or PT IGBT devices," *IEEE Transactions on Power Electronics,* vol. 10, pp. 358-367, 1995.

[30] S. Alvarez and P. Ladoux, "Universal power losses estimator for low voltage IGCTs switching cells," in *European Conference on Power Electronics and Applications (EPE'05)*, 2005, pp. 5-13.

[31] T. Bruckner and S. Bernet, "Estimation and Measurement of Junction Temperatures in a Three-Level Voltage Source Converter," *IEEE Transactions on Power Electronics,* vol. 22, pp. 3-12, 2007.

[32] F. J. T. E. Ferreira, J. A. C. Fong, and A. T. de Almeida, "Ecoanalysis of Variable-Speed Drives for Flow Regulation in Pumping Systems," *IEEE Transactions on Industrial Electronics,* vol. 58, pp. 2117-2125, 2011.

[33] I. Etxeberria-Otadui, A. Lopez-de-Heredia, J. San-Sebastian, H. Gaztanaga, U. Viscarret, and M. Caballero, "Analysis of a H-NPC topology for an AC traction front-end converter," in *13th Power Electronics and Motion Control Conference (EPE-PEMC 2008)*, 2008, pp. 1555-1561.

[34] A. Ruderman and B. Reznikov, "Three-level H-bridge flying capacitor converter voltage balance dynamics analysis," in *13th European Conference on Power Electronics and Applications (EPE '09)* 2009, pp. 1-10.

[35] V. Guennegues, B. Gollentz, F. Meibody-Tabar, S. Rael, and L. Leclere, "A converter topology for high speed motor drive applications," in *13th European Conference on Power Electronics and Applications (EPE '09)*, 2009, pp. 1-8.


**Alain Sanchez-Ruiz** (S'10) was born in Barakaldo, Spain, in 1985. He received the B.S. and M.S. degrees in Electronics Engineering from the University of Mondragon, Spain, in 2006 and 2009, respectively. He is currently working toward the Ph.D. degree at the University of Mondragon, Spain.

His main research interests include multilevel topologies, modulation techniques and motor drives.

**Mikel Mazuela** (S'11) was born in Irun, Spain, in 1986. He received the B.S. and M.S. degrees in Electronics Engineering from the University of Mondragon, Spain, in 2007 and 2010, respectively. He is currently working toward the Ph.D. degree at the University of Mondragon, Spain.

His main research interests include multilevel topologies, modulation techniques and motor drives.

**Silverio Alvarez** was born in Vitoria – Spain in 1974. He received the M.S. degree from the ENSEEIHT, Toulouse, France, in 1999. He worked as lecturer and associate researcher at the University of Mondragón–Spain from 1999 to 2004. Later, after one-year internship at the ABB Corporate Research Center in Baden-Dattwil – Switzerland, he finished and obtained the Electrical Engineering PhD degree from the Institut National Polytechnique de Toulouse in 2005. In September 2005 he joined Ingeteam Technology where he worked as Medium Voltage Drives product manager and he is currently R&D manager in Power Electronics.

His main research interests include the design and development of High Power / Medium Voltage and High Efficiency Power Converters.

**Gonzalo Abad** (M'07) was born in Bergara, Spain, on October 11, 1976. He received a degree in Electrical Engineering from the University of Mondragon, Spain, in 2000, the M.Sc. degree in Advanced Control from the University of Manchester, U.K., in 2001 and the Ph.D. degree in Electrical engineering from the University of Mondragon, Spain, in 2008.

He joined the Electronics Department of the University of Mondragon, in 2001 and is currently an Associate Professor. He teaches courses in power electronics, power converters, control and robotics.

His main research interests include renewable energies, power conversion and motor drives. He has published several papers in the areas of wind power generation, multilevel power converters and direct torque control of AC drives. He has participated in different industrial projects related to these fields.

**Igor Baraia** was born in Durango, Spain, on September 6, 1980. He received a degree in Electrical Engineering from the University of Mondragon, Spain, in 2004 and the Ph.D. degree in Electrical engineering from the University of Mondragon, Spain, in 2009.

He joined the Electronics Department of the University of Mondragon, in 2009 and is currently an Associate Professor. He teaches courses in power electronics and power converters.

His main research interests include power semiconductor devices and power converters. He has published several papers in the areas of series connection of IGBT/Diode devices and multilevel power converters. He has participated in different industrial projects related to these fields.