FPGA Applications in Signal and Image Processing

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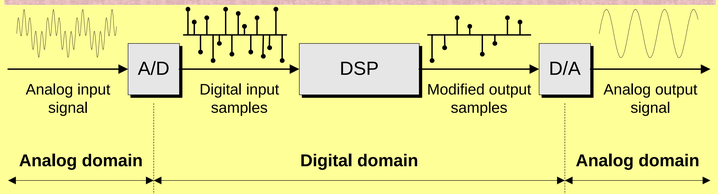
DSP-Based Design

The branch of electronics concerned with the representation and manipulation of signals in digital form. Processing which comprises:

- Image Processing (including medical imaging)
- Non-linear signal processing applications like Artificial Neural Networks

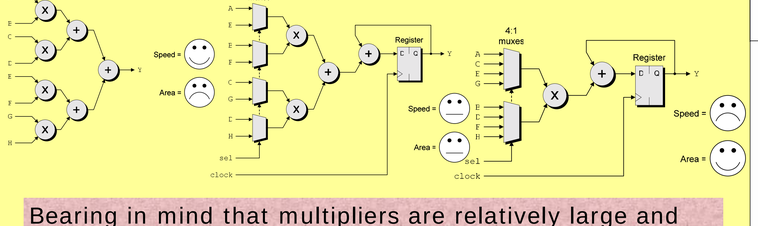


DSP algorithms typically require huge numbers of multiplication and additions. For example the node j in a feed-forward ANN has a basic node function of the type

$$x_j = g\left(f\left(\sum_{i=1}^{N}\omega_j x_i + \varphi_j\right)\right)$$

Where *g()* is the output function and *f()* is the activation/squashing function for which the sigmoid/logistic function is the commonest. Consider the following implementations of the expression:

*Y=(A * B) + (C * D) + (E * F) + (G * H)*

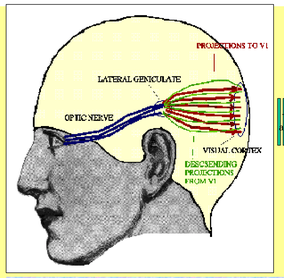


Bearing in mind that multipliers are relatively large and complex than registers and multiplexers, the choice of implementation becomes clear from the above.
"Everybody knows that DSP is the technology driver for the semiconductor industry," says Will Strauss, an analyst with Forward Concepts Co., Tempe, AZ.

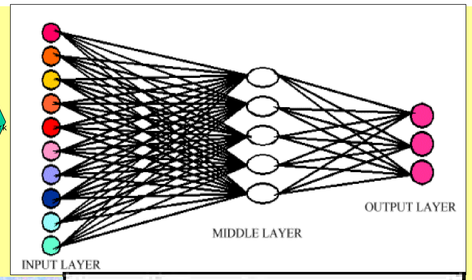
Artificial Neural Networks (ANN)

A massively parallel computing model used purposely for finding smart algorithms to build computing devices for technical use. Systems built with ANN have the following nice features:

- Able to generalize.
- Massively parallel, suitable for hardware implementation.
- Contains an amount of redundancy for "graceful descent".
- Can handle incomplete data.



The Visual system as a Neural Network



Real-world applications

- Industrial Inspection
- Identification & Authentication
- Medical Diagnosis
- Defence

Most of these systems have been implemented in software on conventional sequential computers, due to lack of appropriate hardware. Thus undermining the true potential of the inherent, parallel ANN.

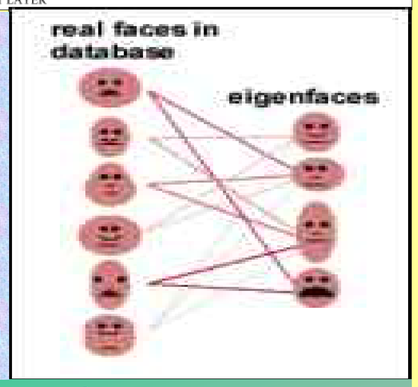
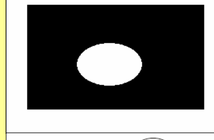
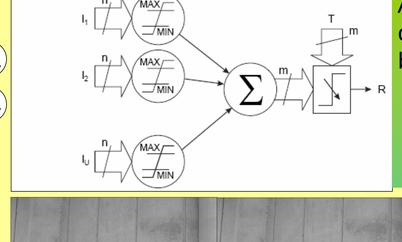


Image Processing

The processing of 2D spatial information (matrix of pixel values), incorporating a great amount of data. This requires a high level of processing capacity only offered by parallel computing. Algorithms in this area can be broken down into pixel-operation functions, segmentation/motion estimation and interpretation.



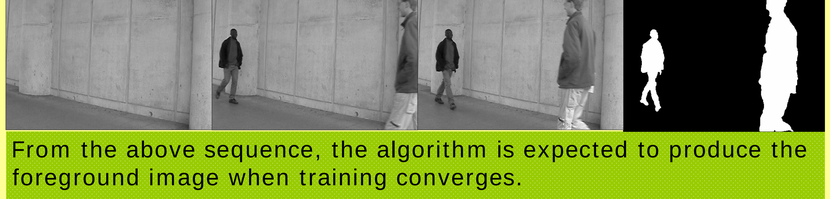
Segmentation always poses a problem. This illustrates a form of ambiguity one will face when segmenting an object from the background(which can be seen as black with white oval or white with black hollow block).



A typical demonstration of the use of ANN in image segmentation, based on MIN/MAX nodes.

$$R = G\left(\sum_{I=1}^{U} F(I)\right) \qquad G(x) = \begin{cases} 0...x < T \\ 1...x \geq T \end{cases}$$

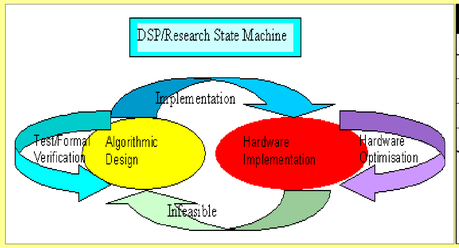
$$F(x) = \begin{cases} 0...x \in (0, MIN) \cup (MAX, 2^n - 1) \\ 1...x \in \langle MIN, MAX \rangle \end{cases}$$



From the above sequence, the algorithm is expected to produce the foreground image when training converges.

Hardware Options

Research is not complete if an algorithm is not feasible to be implemented or the suitable hardware architecture is not available. A good hardware platform should provide good performance including high computation throughput, low power consumption and small design area.



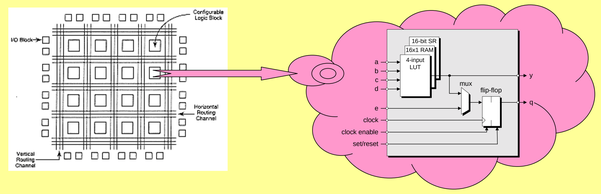
	Flexibility		Performance		
	Prog	Recon	AU	PC	CT
ASIC	Low	Low	Low	Low	High
DSP	Medium	Medium	High	High	Low
(μP)	Medium	High	High	High	Low
FPGA	Medium	High	Low	Medium	Medium

Key

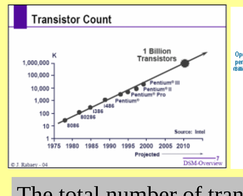
Prog = Programmability
Recon = Reconfigurability
AU = Area Utilization
PC = Power Consumption
CT = Computational Throughput
μP = Microprocessor

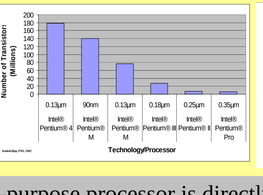
The BIG Question???

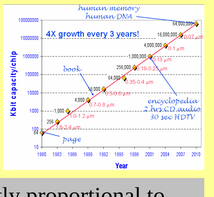
What makes Field Programmable Gate Array (FPGA) so special and feasible for the implementation of these complex, processor and memory hungry systems?



FPGAs allow the DSP designer to "fit the architecture to the algorithm" – that is, the designer can implement as many parallel resources inside the FPGA as necessary to realize the performance required of the system. In general-purpose processors, the resources are fixed as each processor contains a finite number of basic computing functions such as multiply accumulators (MAC). Thus, in a general-purpose DSP processor, the designer must "fit the algorithm to the architecture" and the required performance is not obtainable as in an FPGA.







The total number of transistors found in a general-purpose processor is directly proportional to the DSP performance gap. This calls for a new a better way of implementing such applications or systems.

Outlook

- ANN algorithms with the appropriate hardware can easily be used in solving computationally intensive signal processing problems.
- New implementation platform calls for new design process, for efficiency and accuracy.
- With the 0.1μ technology, ANN can be implemented on FPGA by storing the weights on an on-chip RAM and updated during training.
- ANN can be used in image processing for motion estimation and interpretation.
- The integration of storage and computation within a single FPGA unit are keys that make reconfigurable computing system potential for image processing.

Many Thanks...

- **Nectar Electronics Ltd**.
- Clive **"Max"** Maxfield, *The Design Warrior's Guide to FPGA*, 2004.
- **Radek Holota**, *Neural Network with MIN/MAX Nodes for Image Recognition and its Implementation in Programmable Logic Devices*, 2002.
- **Dag Stranneby & William Walker**, *Digital Signal Processing & Applications*, 2004.
- **Forsyth & Ponce**, *Computer Vision: a modern approach*, 2003.
- **Paul Churchland**, *of the University of California at San Diego*.
- **Jing Ma**, *Signal and Image Processing Via Reconfigurable Computing*, 2003.
- **J. Batlle** et al, *A new FPGA/DSP-Based Parallel Architecture for Real-Time Image Processing, 2002*.
- ***Dan Ganousis***, *Top-Down DSP Design Flow to Silicon Implementation*, March 2004