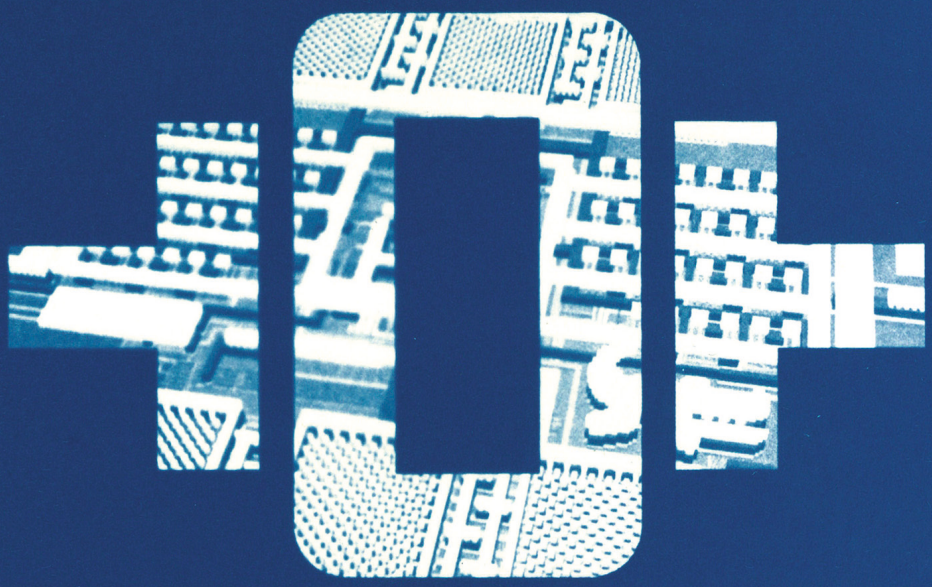
EFFICIENT START-UP OF CRYSTAL OSCILLATORS



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Samenvatting

Het opstarten van de kristaloscillator kost relatief veel tijd, en kan significant bijdragen aan het totale energieverbruik van draadloze systemen waarin de kristaloscillator regelmatig aan- en uit wordt gezet om energie te besparen. In bijvoorbeeld Bluetooth Low Energy systemen kan het herhaaldelijk opstarten van de kristaloscillator tot tientallen procenten van hun totale energieverbruik kosten. Het onderzoeksdoel van dit proefschrift is dan ook om kristaloscillatoren snel op te starten, voor zo min mogelijk energie.

Een vergelijking van de huidige stand der techniek betreffende het opstarten van kristaloscillatoren toont dat systemen met Energie Injectie (EI) sneller opstarten dan circuits met negatieve weerstand ('Negative Resistance Boosting' - NRB). Qua energieverbruik zijn ze echter vergelijkbaar met de beste NRB- en hybride schakelingen, waarbij hybride schakelingen de EI- en NRB-technieken combineren. De grootste uitdaging van energie-injectie is het genereren van een nauwkeurig injectiesignaal, aangezien de injectiefrequentie zeer nauwkeurig moet zijn om ervoor te zorgen dat het injectiesignaal gedurende de gehele injectieduur in fase is met de kristalresonantie.

Dit proefschrift beschrijft zelf-getimede injectie ('self-timed injection') als oplossing voor deze uitdaging. Hierbij wordt de timing van de injectiegolfvorm gegenereerd op basis van de kristaloscillatie zelf, in plaats van te vertrouwen op een aparte injectieoscillator. Het concept van zelfgestuurde injectie is gebaseerd op het meten van de stroom van het kristal, waarbij bij elke nuldoorgang van de stroom de polariteit van de injectiespanning wordt omgewisseld. De belangrijkste ontwerpoverwegingen worden besproken, en simulaties aan de schakeling laten zien dat het ontwerp robuust is tegen proces, spanning en temperatuur (PVT) variaties. Ten slotte tonen metingen aan een prototype, gekoppeld aan een 50 MHz kristal, een opstarttijd van 6 µs en een opstartenergie van 3.7 nJ.

Bij energie injectie levert het herhaaldelijk opladen van de capacitieve belasting een van de grootste bijdragen aan het totale energieverbruik tijdens het opstarten. De capacitieve belasting bestaat uit de (parasitaire) capaciteiten van de kristaloscillator schakeling, alsmede het kristal zelf. Door deze belasting

stapsgewijs te laden en ontladen kan het energieverbruik worden gereduceerd. Uit analyse blijkt dat door in vier stappen te laden en ontladen, een reductie in energieverbruik van een factor twee tot vier mogelijk is. Gecombineerd met verdere verbeteringen aan de zelfgestuurde injectietechniek, zijn zowel sneller opstarten als een lager energieverbruik realiseerbaar. Dit wordt aangetoond in zowel simulaties als metingen aan een gefabriceerd prototype. In vergelijking met zowel de eerste chip die in dit proefschrift wordt beschreven, als de huidige stand der techniek zorgt deze tweede chip voor een aanzienlijke reductie in de opstarttijd en -energie. Gekoppeld aan hetzelfde 50 MHz-kristal en onder gelijkwaardige meetomstandigheden als het eerste prototype, start de oscillator op in 2.8 µs en verbruikt daarbij slechts 1.9 nJ.

Aangezien het ontwerp van energie injectie schakelingen moet worden afgestemd op de specifieke toepassing, wordt inzicht gegeven van de ontwerpruimte en beperkingen. Dit omvat de uitdagingen die specifiek zijn voor zelfgestuurde injectie, maar ook compromissen op systeemniveau die van toepassing zijn op energie-injectie systemen in het algemeen, zoals voedingsspanning, kristalparameters en amplitude in stabiele toestand. Deze analyse is samengevat in een ontwerpparameter gevoeligheid, welke nuttig kan zijn bij het ontwerpen van energie-injectiesystemen, maar ook kan bijdragen aan het eerlijk vergelijken van de prestaties van verschillende kristaloscillator schakelingen. Deze vergelijking is normaal gesproken moeilijk omdat verschillende publicaties zeer verschillende meetomstandigheden gebruiken, waaronder kristaltype, voedingsspanning en amplitude in stabiele toestand. In dit proefschrift worden verschillende schakelingen vergeleken met betrekking tot deze variabelen, alsmede hun efficiëntie. Hoewel het nuttig is om de prestaties van verschillende technieken onder verschillende meetomstandigheden te beoordelen, blijkt hieruit dat identieke – of op zijn minst gelijkwaardige – omstandigheden een vereiste zijn voor een echt volwaardige vergelijking.

Het onderzoeksdoel van dit proefschrift om kristaloscillatoren snel op te starten voor zo min mogelijk energie wordt bereikt door gebruik te maken van een nieuwe techniek; zelfgestuurde injectie, evenals de toepassing van stapsgewijs opladen. De efficiëntie toont aan het gerealiseerde energieverbruik bij het opstarten nog lang niet op het theoretische minimum ligt. Desalniettemin behalen de in dit proefschrift behandelde technieken, in vergelijking met andere energie-injectiemethoden, vergelijkbare opstarttijden terwijl het energieverbruik tijdens het opstarten aanzienlijk lager is.

Abstract

The start-up of the crystal oscillator can be a significant contributor to the latency and the overall energy consumption of (duty-cycled) low-power wireless systems. In Bluetooth Low Energy transceivers, for example, repeatedly starting up the crystal oscillator can cost as much as tens of percents of their total energy consumption. The research goal in this thesis is therefore to quickly start up crystal oscillators for as little energy as possible.

A comparison of the state-of-the-art in crystal oscillator start-up shows that energy injection (EI) systems start up faster than negative resistance boosted (NRB) circuits. In terms of energy consumption, however, they are on par with the best NRB and hybrid circuits, the latter combining EI and NRB techniques. The main challenge in Energy Injection is the generation of a precise injection signal since the injection frequency needs to be very accurate, which is required to ensure that the injection signal is in-phase with the crystal resonance over the entire injection duration.

This work presents self-timed injection to get around this challenge. Rather than relying on an auxiliary injection oscillator, the injection waveform timing is determined from the crystal oscillation itself in self-timed injection. The basic concept relies on measurement of the crystal motional current, where the injection voltage polarity is alternated whenever a zero crossing of the motional current is detected. The main design considerations are discussed, and circuit simulations show robustness against PVT variations. Finally, measurements on a manufactured prototype show a start-up time of 6 µs and a start-up energy of 3.7 nJ for a 50 MHz crystal.

One of the largest contributors to energy consumption in Energy Injection is the repeated charging of the capacitive load, which consists of the crystal oscillator circuit (parasitics) and the crystal. By charging and discharging the load in 4 steps using the concept of step-wise charging, the energy consumption can be reduced by a factor of 2-4 as shown in an analysis. Combined with refinements to the self-timed injection technique, this allows both faster start-up time and lower start-up energy, as demonstrated by simulations, as well as measurements on a fabricated

prototype. This second chip significantly reduces start-up time and energy, compared to the first chip presented in this thesis as well as the state-of-the-art. Connected to the same 50 MHz crystal and using identical measurement conditions as for the first prototype, it starts up in 2.8 µs, consuming only 1.9 nJ in the process.

Since Energy Injection circuits need to be tailored to the application, an overview of the design space and limitations is presented. This includes the challenges specific to self-timed injection, but also system-level trade-offs that apply to Energy Injection systems in general, such as supply voltage, crystal parameters, and steady-state amplitude. This analysis is summarized in a design parameter sensitivity. This can be useful in the design of Energy Injection systems but also aids towards a fair comparison of various crystal oscillator circuits. This comparison is normally difficult since different publications use vastly different measurement conditions, including crystal type, supply voltage, and steady-state amplitude. This work compares circuits concerning their supply voltage, crystal parameters, steady-state amplitude, and efficiency. While useful to assess the performance of different techniques under different measurement conditions, the comparison of various circuits shows that for a truly fair comparison, equal or similar measurement conditions are required.

Overall, the research goal of this thesis is to quickly start up crystal oscillators, for as little energy as possible. This is achieved by the use of a new technique; self-timed injection, as well as the application of step-wise charging to crystal oscillators. The start-up efficiency shows that start-up energy consumption is still far from its theoretical minimum. Nevertheless, the proposed techniques, when compared to other energy injection methods, achieve competitive start-up times while significantly reducing the start-up energy consumption.

Contents

Chapter 1

Introduction

1.1 Motivation

All around us, we see an ever-increasing number of electronic devices, which are increasingly connected to other devices or systems. Think of, for example, remote health monitors such as temperature, heart rate or glucose sensors, toothbrushes that connect to the internet, wireless tags that enable their owner to find their keys, smart home systems for lighting, heating and ventilation, safety devices such as smoke detectors, or crop health monitors. All these devices are connected to each other or the internet, forming a network often called the 'Internet of Things' (IoT).

While some of these devices have access to virtually unlimited power through, for example, a mains connection or vehicular power grid. Many devices, however, are wireless, which not only means that they transmit and receive data wirelessly, but also that they rely on scarce energy supplies such as batteries or energy harvesters. To reduce the requirements on the energy supply, lengthen battery life or enable the use of a smaller battery, their power consumption should be kept at a minimum.

Most devices do not require a permanent high-bandwidth data link. For example, a heart rate monitor does not need to send data more than about once a second, the temperature in a (smart) home changes over minutes, and plant growth is monitored over hours. Rather, these systems send and receive rather small packets of data at a low rate.

Rather than continuously sending data at a low rate, it is more energy efficient to 'duty-cycle' the system. This means that the system is active for a short time to process, send and receive data, and put in a low-power sleep mode in between [1], [2], shutting down all but the minimum required circuit blocks.

A circuit block that is omnipresent in radio systems is the crystal oscillator. This block generates the precise reference frequency, which is usually in the 1 MHz to 50 MHz range. This reference is used in the radio system to derive the radio frequency that is used to transmit and/or receive at exactly the right frequency. The crystal oscillator combines an electronic circuit with an external crystal resonator, usually just called 'crystal'. These crystals can have a very high quality-factor (100.000+), which enables excellent phase noise performance, as well as good frequency stability over environmental variations. Despite the cost and size penalty associated with the use of external crystals, crystal oscillators continue to be used in many radio systems, since there are no suitable alternatives (yet).

There are continuous efforts to reduce the crystal oscillator power consumption [3], or to put it in a low-performance and low-power mode when high performance is not required [4], to make the oscillator power consumption sufficiently low that it can be kept on at all times. However, when going to very low duty cycles (e.g., 0.1% or less) for ultra-low-power communication, it remains more efficient to shut down the entire crystal oscillator when it is not used. The downside is that the crystal oscillator has to be started before it provides a useful output.

This is where the high crystal quality factor becomes unfavorable, as it causes the start-up of typical crystal oscillators to be a very slow process. Up to recently, it took a time in the order of milliseconds [5]–[9], much longer than most other transceiver circuit blocks, that start up in the (tens of) microseconds range [10].

Compared to the time that the radio is actually active, the crystal oscillator start-up time is very long, as illustrated in Figure 1.1, which shows a simplified power consumption profile for a Bluetooth Low Energy system. The long start-up time not only causes delay in the system but also (and perhaps more importantly) comes at the cost of a large energy consumption, since the crystal oscillator consumes power during all the time it is starting up. Even if the power consumption during start-up is relatively small, it amounts to a significant energy consumption, since the start-up energy consumption is the *product* of power consumption and (long) start-up time.

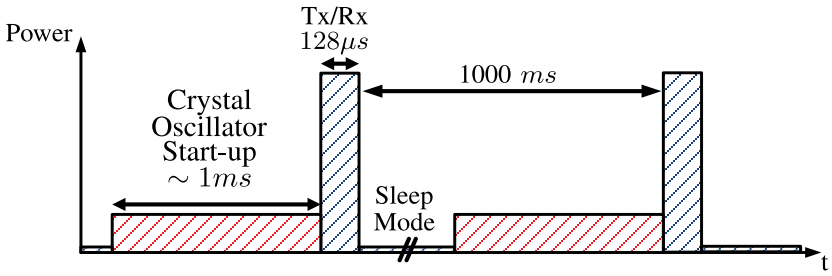


Figure 1.1. Simplified transmit and receive event of a low-power wireless node.

This shows the necessity to minimize both the start-up time *and* energy of the crystal oscillator.

The start-up of crystal oscillators is a subject that has been studied in the eighties [11], [12], but this was limited to start-up times in the order of milliseconds, and does not consider energy consumption. However, as transceiver and data processing circuits become more power efficient over time, they consume less energy, and the crystal oscillator start-up energy consumption becomes a significant portion of total power consumption. For example, in current Bluetooth Low Energy transceivers, starting up the crystal oscillator costs as much as tens of percents of the total energy consumption [13], [14]. When commencing this research, the reduction of the crystal-oscillator start-up time was quickly regaining attention, but research on start-up energy was only scratching the surface.

1.2 Research goal and thesis outline

The research goal in this thesis is to quickly start up crystal oscillators, for as little energy as possible.

The remainder of this thesis is organized as follows:

Chapter 2 discusses the fundamentals of crystal oscillators and how they start up. Furthermore, it gives an overview of the existing work on crystal oscillator start-up circuits. The existing work is categorized into two fundamentally different methods, Negative Resistance Boosting (NRB) and Energy Injection (EI), which are compared in terms of start-up time and start-up energy.

Chapter 3 introduces a new technique to quickly start up crystal oscillators for low energy consumption. The principle of this self-timed energy injection technique is explained. The design choices, analysis and realization of a proof-of-concept chip are covered, followed by simulations and measurements to validate the technique.

Chapter 4 discusses the application of the concept of stepwise charging to the start-up of crystal oscillators and presents improvements to the self-timed energy injection technique to further reduce energy consumption. The design considerations associated with the application of step-wise charging to energy injection circuits are discussed. The proposed techniques are integrated into a proof of concept, on which measurements are presented.

Chapter 5 provides additional insight into the design space of self-timed injection circuits, reflecting on the main challenges and solutions in the realizations of Chapters 3 and 4. Furthermore, design considerations for injection circuits in general are discussed. Finally, insight is provided towards a fair comparison of crystal oscillator start-up circuits.

Chapter 6 concludes this thesis by summarizing the work, along with future research directions and recommendations for improvements to the proposed circuits.

Chapter 2

Survey of crystal oscillator start-up techniques

This chapter covers the fundamentals and state-of-the-art of crystal oscillator start-up techniques.

2.1 Crystal oscillator fundamentals

A crystal oscillator consists of a crystal resonator, combined with an electronic circuit (active circuit) that starts and sustains the oscillation, as shown in Figure 2.1.

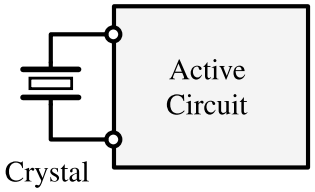


Figure 2.1. Generic Crystal oscillator.

2.1.1 Crystal electrical model

The crystal consists of a piece of piezo-electric material, with electrodes on both sides. Through the piezo-electric effect, the application of an electric potential on the electrodes sets the crystal into motion and vice-versa. The crystal is designed and cut for a specific fundamental frequency, which is very accurate and has very good stability over temperature and aging. Apart from this fundamental mode, the crystal usually exhibits several mechanical resonance modes, which can be harmonics of the fundamental but also spurious modes that are relatively close in frequency. These resonance modes are only weakly coupled, such that each resonance mode can be modeled as separate motional branches, which consist of

an RLC circuit, as shown in Figure 2.2(a) [12]. Each branch models one of the resonance modes with a motional inductance $L_{m,i}$, motional capacitance $C_{m,i}$, and resistance $R_{m,i}$. The electrodes and package parasitics form a capacitance C_p, which is in parallel with the motional branches. The fundamental mode normally has the lowest impedance and highest quality factor, such that the other spurious branches can usually be omitted when modeling practical oscillator circuits, as shown in Figure 2.2(b).

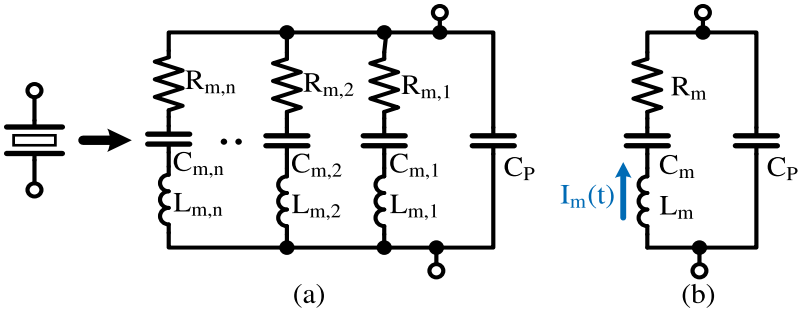


Figure 2.2. (a) Crystal model. (b) Fundamental mode model.

The crystal exhibits two 'natural' resonance frequencies. Firstly, a series resonance, when the crystal is loaded with a short-circuit. In this case, L_m and C_m resonate, forming a minimum in crystal impedance. On the other hand, if the load impedance is infinite, the crystal resonates in parallel resonance, where L_m resonates with the series equivalent of C_m and C_p; $\frac{C_p C_m}{C_p + C_m}$. Note that C_m(fF range) is much smaller than C_p (pF range), such that the difference between the series and parallel resonance modes is very small. The crystal is trimmed by the manufacturer to resonate at a very precise frequency when it is loaded with a specified load capacitance C_L. The added load shifts the resonance to somewhere in between the series and parallel resonance modes.

Regardless of the resonance mode, the oscillation is always an exchange of energy between L_m and the (effective) capacitance. The current $I_m(t)$ is converted to an output voltage across the crystal by the effective load of the motional branch, which is C_p in parallel to Z_{Load}. This makes the current I_m through the motional branch a direct measure for the output voltage and the energy stored in the oscillation, as well as a measure for the output voltage amplitude if it is connected to the specified load. This property comes in handy when considering start-up circuits.

2.1.2 Ideal negative resistance

To understand the start-up of crystal oscillators, we first consider the motional branch without any load, hence also neglecting C_p and C_L, as shown in Figure 2.3.a.

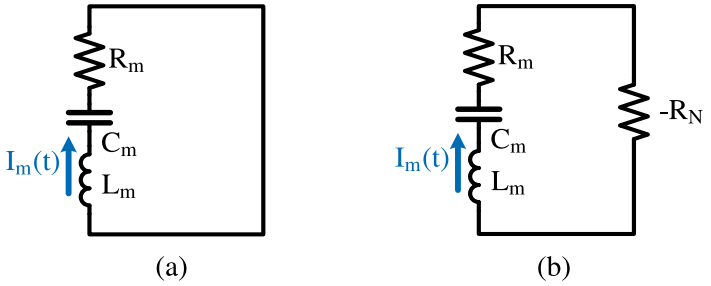


Figure 2.3. (a) Series RLC circuit. (b) Ideal negative resistance oscillator (with $R_N > 0$).

The envelope $\hat{I}_m(t)$ of the oscillating current $I_m(t)$ from an initial motional current $\hat{I}_m(0)$ can be calculated as [15]:

$$\left|\hat{I}_m(t)\right| = \left|\hat{I}_m(0)\right| e^{\frac{-R_m}{2L_m}t} \tag{2.1}$$

This equation shows an exponentially decreasing motional current, with larger values of R_m resulting in faster damping. It should be noted that if R_m is large ($R_m \geq 2\sqrt{L_m/C_m}$), the circuit becomes critically or overdamped, which means that any motional current is quickly damped, without any oscillations at all. However, considering that crystals are designed and used because of their high quality factor, this effect can be neglected.

To sustain, or grow oscillations, an element that adds energy is needed, which in oscillators often is (modeled by) a negative resistance. This is shown in Figure 2.3.b., but notice that C_p and C_L are still left out. Also note the sign of the negative resistance R_N, which is positive for this circuit to function as an oscillator, since *minus* R_N is *negative*.

Similar to Equation (2.1), the growth of the envelope of the oscillating current $I_m(t)$ can be calculated as [15]:

$$\left|\hat{I}_m(t)\right| = \left|\hat{I}_m(0)\right| e^{\frac{R_N - R_m}{2L_m}t} \tag{2.2}$$

R_N effectively 'undamps' the RLC circuit. The oscillation can be sustained if the negative resistance equals the losses in the motional resistance [15]:

$$R_{N,min} = R_m \tag{2.3}$$

If R_N is larger than R_m, the oscillation amplitude grows exponentially, with larger values for R_N resulting in quicker growth. This shows that the negative resistance should be as large as possible to achieve a quick start-up.

Note that if the effective total resistance $R_N - R_m$ becomes *too* large ($R_N - R_m \geq 2\sqrt{L_m/C_m}$), the motional current grows rapidly, but very similar to the case with overdamping, without any oscillations. While this may seem undesirable for an oscillator, it is useful for quick start-up, since it does mean that total energy in the system is rapidly growing. If at some point during this rapid growth, the negative resistance is lowered to the value to sustain oscillation ($R_N = R_m$), the system will oscillate from this large initial condition, hence having achieved a very rapid start-up. However, partly because of the crystals' high Q, and partly because of the limitations in practical circuits that will be discussed in Sections 2.1.3 and 2.2, this 'over-undamping' is not encountered in practical crystal oscillators. Nevertheless, as discussed earlier, the negative resistance should be as large as feasible to achieve quick start-up.

Also, note that the analysis above applies to *series* resonant circuits. For high-Q *parallel* resonant circuits, the duality principle can be applied [15]. In this case, fast start-up is achieved for a large negative *admittance* in parallel, which translates to a very *small* negative resistance.

2.1.3 Practical negative resistance circuit

Figure 2.4 shows a pierce oscillator, a circuit that is typically used for crystal oscillators due to its high frequency stability [12]. The crystal is modeled at the fundamental frequency, with a motional inductance L_m, motional capacitance C_m, and resistance R_m. The active circuit loads the resonator with the specified load capacitance and provides the required energy to sustain oscillation.

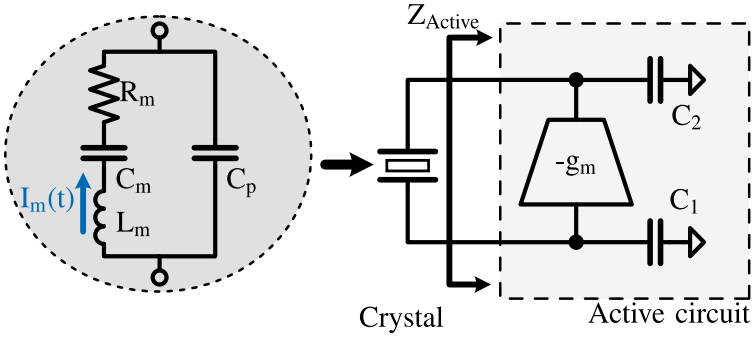


Figure 2.4. Pierce oscillator (with $g_m > 0$).

Normally, $C_1 = C_2 = 2C_L$ to achieve the desired load capacitance for the least total physical capacitor size. Then, assuming the active circuit is linear, which is true as long as the oscillation amplitude is small, the impedance of the active circuit can be calculated as:

$$Z_{active} = -\frac{g_m}{(2C_L\omega)^2} + \frac{1}{j\omega C_L} \tag{2.4}$$

This shows that the impedance consists of the series combination of a real (negative) part as well as an imaginary part equal to the load capacitance, meaning that the oscillator can be modeled as shown in Figure 2.5. The circuit can be split into the crystal motional branch and its load Z_N, which allows insightful analysis [12].

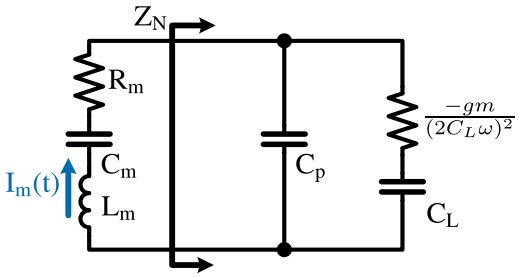


Figure 2.5. Linear circuit equivalent.

The negative resistance R_N, here defined as *minus* the real part of Z_N, can be calculated as [12]:

$$R_N = -Re(Z_N) = \frac{g_m 4C_L^2}{\left(g_m C_p\right)^2 + \left(4\omega\left(C_L^2 + C_L C_p\right)\right)^2} \tag{2.5}$$

Interestingly, this equation is a non-monotonic function of g_m, as shown in Figure 2.6.

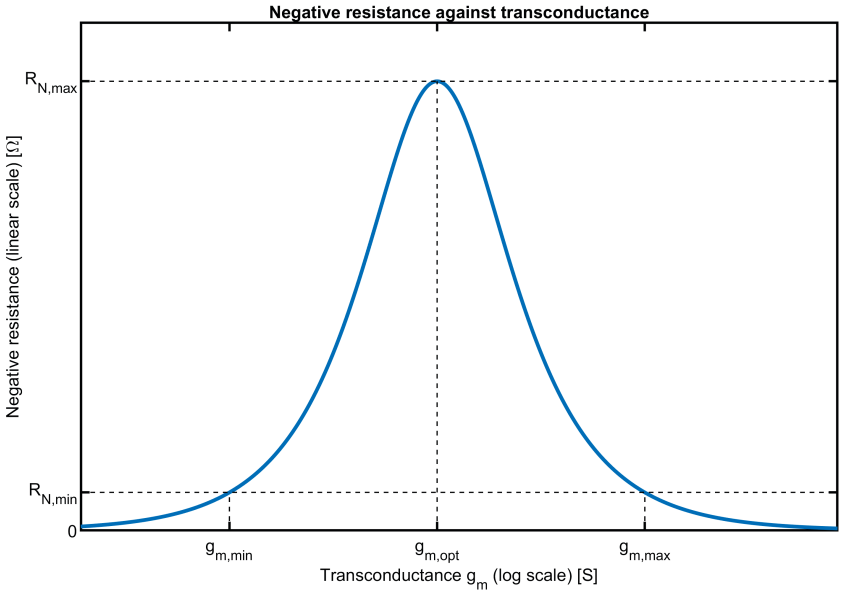


Figure 2.6. Negative resistance as a function of transconductance.

This figure also shows the negative resistance that is required to sustain oscillation, $R_{N,min}$. Note that the solution for $g_{m,max}$ does not fulfill the phase stability criterion, so stable oscillation is not supported for this negative resistance [12], [16].

During start-up, the active circuit has to bring the motional current from its initial condition $I_m(0)$ to $\hat{I}_{m,SS}$. If the oscillator has been off for a relatively long time before it is started again, as is the case in duty-cycled systems, the oscillation has (almost) completely damped. In this case, $I_m(0)$ is typically the result of circuit noise or the result of a small 'single-kick' [11] when the oscillator is turned on, both much smaller than $\hat{I}_{m,SS}$. R_N is normally designed to be large enough to ensure start-up over PVT variations, but as small as possible to minimize power consumption, resulting in long start-up times in the order of milliseconds [5]–[9].

The fastest possible start-up is achieved for the largest achievable negative resistance, which can be calculated as [15]:

$$R_{N,max} = \frac{1}{2\omega C_p(1+\frac{C_p}{C_L})} \tag{2.6}$$

This shows that the maximum negative resistance that can be achieved for a given crystal is limited by the crystal C_p as well as C_L, which normally have fixed values.

For very small C_p ($C_p \to 0$), $R_{N,max}$ approaches infinity, which allows arbitrarily fast start-up, as discussed in the previous subsection. This is consistent with the analysis of the ideal negative resistance (without C_p) in the previous subsection.

$R_{N,max}$ is achieved when the transconductance gm is at its optimum (in terms of start-up time) [15]:

$$g_{m,opt} = 4C_L\omega\left(1 + \frac{C_L}{C_p}\right) \tag{2.7}$$

Equation (2.2) suggests that as long as R_N is larger than R_m, the motional current grows infinitely over time. In practical systems, the oscillation amplitude reaches a certain steady-state amplitude $\hat{I}_{m,SS}$. All capacitors in the circuit are discharged when the motional current reaches its peak $\hat{I}_{m,SS}$, and the resistors store no energy, such that all the energy in the circuit is stored in the crystals' motional inductance at this point in time. This means that the total energy stored can be calculated as:

$$E_{crystal} = \frac{1}{2}L_m\hat{I}_{m,ss}^2 \tag{2.8}$$

When the circuit does not store any energy before start-up ($\hat{I}_m(0) = 0$) and assuming the active circuit is ideal and the losses in R_m are negligible, $E_{crystal}$ equals the (theoretical) minimum amount of energy that needs to be fed to the system to start up.

The desired magnitude of $\hat{I}_{m,SS}$ depends on the desired output voltage amplitude, which depends on the desired phase noise performance as well as load capacitance; $I_{m,SS}$ has to be larger when better phase noise is required or if a larger load capacitance is used. This trade-off will be discussed in more detail in Chapter 5.

The method to maintain a certain steady-state amplitude may vary. The stabilization in amplitude can be due to non-linearity, or through an amplitude regulator. In the case of non-linearity, the output amplitude grows exponentially until the active circuit starts to saturate, which reduces the effective negative resistance, reducing the growth rate up to the point where the effective R_N equals R_m [15], for which the oscillation amplitude remains stable. When the output amplitude is controlled by an amplitude regulator, the negative resistance is actively regulated to result in the desired amplitude $\hat{I}_{m,SS}$ [12], [15], [17]. This is often achieved by regulating the bias current of the transconductor.

2.1.4 Fast start-up

While a long start-up time does not result in a large energy consumption *per se*, it does have an influence since start-up energy is the product of start-up *time* and *power.* This is normally a compromise, depending on the target specifications.

While R_m and L_m are crystal parameters that are fixed, $I_m(0)$ and R_N can be influenced to achieve the steady-state amplitude in less time. To speed up the start-up process, the active circuit can be designed to yield a larger R_N during start-up by Negative Resistance Boosting (NRB). This decreases the time constant of the exponential growth of the amplitude. Once steady-state is reached, R_N is reduced to sustain the oscillation.

On the other hand, the initial condition $I_M(0)$ can be increased by pre-energizing the crystal using Energy Injection (EI). If the Energy Injection is very effective, it can be solely used to achieve steady-state, skipping the negative-resistance phase in achieving steady-state. The negative resistance is then only required to sustain the oscillation. In other cases, a negative resistance phase (with or without NRB) is still required to achieve steady-state, these methods can be classified as hybrids. Figure 2.7 shows the start-up process for these different start-up techniques.

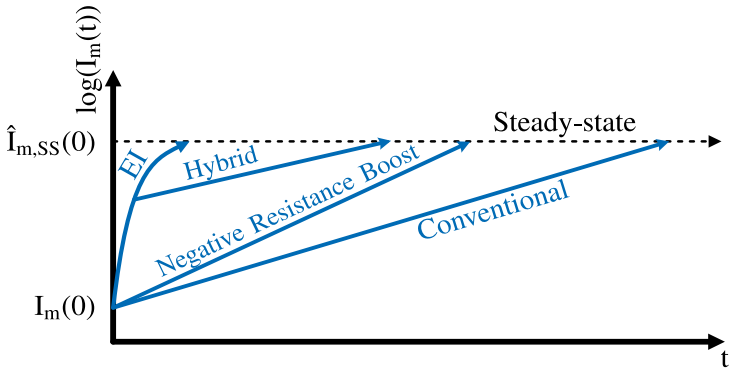


Figure 2.7. Amplitude growth for different start-up techniques.

The subsequent sections discuss the different methods to minimize the start-up time and energy, where attempts to maximize R_N are classified as 'Negative Resistance Boosting' (NRB), and the pre-energization of the crystal by 'Energy Injection' (EI).

2.2 Negative Resistance Boosting

Figure 2.8 shows the concept of negative resistance boosting (NRB), where g_m and C_L (C_{Load}) are variable elements. While C_p and ω are crystal parameters, g_m and C_L can be set by the circuit designer, or varied during the start-up sequence. Finally, the limitation on C_p can be alleviated by canceling it. These methods to influence start-up time and energy will be discussed in the following subsections.

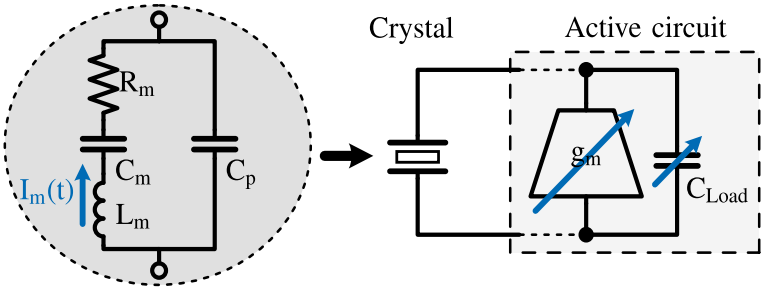


Figure 2.8. Negative Resistance Boosting concept.

2.2.1 Increased transconductance

In conventional crystal oscillators, the negative resistance R_N required to sustain the oscillation in steady-state is much smaller than $R_{N,max}$, as shown in Figure 2.6. Therefore, the transconductance g_m is usually chosen close to $g_{m,min}$ to minimize power consumption, with some margin to allow for PVT variations. From this starting point, increasing g_m increases R_N, as shown in Figure 2.6, and hence decreases start-up time. Note that the increase in g_m only results in an increased R_N as long as $g_m \leq g_{m,opt}$.

The transconductor normally consists of a single stage, using either a single (biased) transistor or an inverter. For these circuits, the increase in g_m can be achieved by increasing the bias current [18], which increases current consumption proportionally to the increase in transconductance, and hence also power consumption. Alternatively, additional transconductance stages can be switched in parallel during start-up [19], which increases both transconductance and power consumption proportionally to the number of parallel stages.

As long as g_m is much smaller than $g_{m,opt}$, R_N scales approximately linearly with g_m. The start-up time constant reduces proportionally with R_N, such that the total energy consumption, which is the product of start-up time and start-up power ($T_{start} \cdot P_{start}$), stays approximately constant. However, as g_m gets close to $g_{m,opt}$, the increase in negative resistance (and hence decrease in start-up time)

does not weigh up against the increased g_m (as shown in Figure 2.6) and hence power consumption, which leads to larger start-up energy. This trade-off of start-up time against energy was noted in [19].

A way to decrease the start-up energy is the reduction of the transconductor power consumption. If a single amplifier stage is used, as shown in Figure 2.9.a., weak inversion operation provides the highest g_m per unit of power. To push the power consumption even lower, the overall transconductance can be increased by putting an (ideal) amplifier with gain A in front of the transconductor stage, as shown in Figure 2.9.b. The overall transconductance then becomes $A \cdot g_m$. If the amplifier power consumption is small enough, i.e., the gain it provides outweighs the increase in power consumption, the overall transconductance per unit power consumption is higher. This can increase g_m and decrease start-up time without the disproportional increase in energy consumption that is found when scaling a single-stage amplifier.

This technique has been applied in crystal oscillator circuits to reduce steady-state power consumption [4], [20], as well as to reduce start-up time and energy [13], [19], [21]–[24].

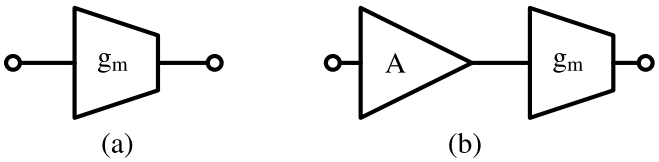


Figure 2.9. g_m boost concept.

The first stage of a cascade of amplifiers usually contributes most to the overall noise. However, (phase) noise performance is not important during start-up or if the amplifier is only used to maintain a low-power mode. In these cases, power and hence energy consumption can be minimized at the expense of noise. If phase noise performance is important, however, the transconductor should be switched to a (conventional) low-noise circuit after the crystal is sufficiently energized.

The bandwidth of the amplifier A is limited, such that it introduces a phase shift that may vary over PVT and which can pull (shift) the oscillation frequency. The amplifier does not have to drive a large capacitive load, and the crystal frequency is much lower than f_{max} in modern CMOS processes. On the other hand, if the phase shift is managed precisely, it can actually boost start-up performance, as will be discussed in Section 2.2.3.

A disadvantage of increasing the transconductance is that with more gain, the amplifier saturates as soon as one of the outputs or internal nodes gets close to the supply voltage V_{DD} as the oscillation is growing. This causes a reduction of the effective transconductance, limiting the effectiveness of the technique. Depending on the boost factor, the effective gm can be below that of a single-stage even before steady-state is reached [13].

2.2.2 Altering load capacitance

For steady-state operation, C_L is fixed and specified by the crystal manufacturer. The load capacitance can be a fixed off-chip capacitor, but can also be an on-chip capacitor bank. During start-up, it may be altered from its nominal value, which can help to increase R_N.

Considering the case that $C_p \ll C_L$, which is typically true, Equation (2.2) can be approximated as:

$$R_N \approx -\frac{g_m}{(2\omega C_L)^2} \tag{2.9}$$

From this equation, it can be seen that a reduction in C_L results in an increase in R_N. Furthermore, the optimum value for g_m is reduced, as shown in Equation (2.3), hence saving power. The increased negative resistance quickly grows the oscillation, and after the desired amplitude is reached, C_L can be ramped up to the specified C_L [18]. Since the output voltage is not only a function of $I_m(t)$, but also C_L, immediately switching to the large load capacitor drops the output voltage. Therefore, C_L is dynamically ramped up, keeping the output voltage constant during the ramp-up process [18].

The improvement using this technique is limited since as C_L is reduced, C_p cannot be neglected anymore. Furthermore, as C_L decreases, $R_{N,max}$ drops to zero, as can be seen in Equation (2.4). This puts a lower bound on the achievable minimum start-up time.

On the other hand, Equation (2.1) shows that the use of a *larger* C_L increases the maximum achievable negative resistance, reducing overall start-up time. This is analyzed in circuit simulations in [25]. The disadvantage, however, is that the required transconductance grows with the increasing C_L, as shown in Equation (2.3), thereby increasing power consumption. For large C_L, Equation (2.4) reduces to:

$$R_{N,max} \approx -\frac{1}{2\omega C_p} \tag{2.10}$$

This shows that the maximum negative resistance, and hence minimum start-up time that can be achieved in this way is ultimately limited by C_p [11]–[13], [19], [23].

2.2.3 Cancellation of parallel capacitance

The previous subsections discussed the change of the design parameters g_m and C_L, showing physical limits to the start-up time due to C_p. To relieve the limit imposed by the crystal C_p, it is possible to (partially) cancel it by the use of an inductor. By placing an inductor in parallel to C_p, and tuning its value so that, at the crystal oscillation frequency, its reactance exactly cancels the reactance of C_p, such that it effectively becomes an open circuit, as shown in Figure 2.10. This assumes that the quality factor of the resulting resonant circuit is infinite. According to Equation (2.4), this allows R_N to go toward infinity and hence realize arbitrarily small start-up times.

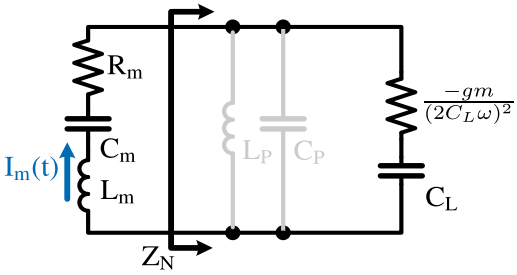


Figure 2.10. Parallel capacitance cancellation.

On-chip physical inductors are not suited for this purpose since the required inductance is in the order of µH's, much more than practically achievable. These inductances can be achieved using off-chip inductors but this increases cost and area. Furthermore, the component spread of both C_p and the inductor itself and the associated tuning requirements limit the use of fixed inductors.

A more attractive solution is the use of a circuit that emulates an inductor, the so-called 'active inductors'. These circuits can be tuned, but consume power and add noise. Noise during start-up is no problem, and if the added power consumption is outweighed by the reduction in start-up time and energy, it can be an attractive solution.

One method is the addition of an explicit active inductor circuit, directly canceling C_p [26]. Adding the inductor effectively adds a resonator to the oscillator circuitry, which may introduce an unwanted oscillation mode. Careful design of the active inductor, limiting its quality factor prevents this [26]. On the other hand, this limits

the equivalent impedance at resonance, which in turn puts a limit on the maximum negative resistance.

Alternatively, the phase delay in a multi-stage amplifier (as discussed in Section 2.2.1) can be exploited to (partially) cancel C_p. If the pre-amplifier stage generates some phase delay, it can be shown that this makes the overall active circuit appear inductive. The phase delay can be the natural bandwidth limitation of the amplifier, or the addition of explicit capacitors, either as capacitive loading or capacitive feed-forward to the internal nodes [13], [21], [23], [24].

Even though canceling C_p theoretically allows infinite R_N, this is difficult to achieve in practice, as it requires an inductance that *exactly* compensates C_p. This is especially difficult over PVT variations as well as variations in the crystals' parasitics. Therefore, a limited R_N is usually chosen, which can be guaranteed over PVT [26]. When using inductive cancellation of C_p, careful tuning of the inductance is required. Firstly, the optimum inductance is dependent on the crystal C_p. Secondly, as R_N gets larger, the tuning requirements become increasingly strict, which makes stability over temperature difficult. The maximum practical R_N is a compromise between start-up time and robustness.

2.2.4 Limitations

R_N has a local maximum when g_m is equal to $g_{m,opt}$, as was shown in Figure 2.6. Since R_N determines the start-up time constant, the start-up time is hence not sensitive to variations in transconductance as long as it is chosen equal to $g_{m,opt}$, as at this point, variation in g_m results in only marginal variation in R_N. However, g_m is often smaller than $g_{m,opt}$ to minimize energy consumption, such that R_N is susceptible to variations in g_m. Furthermore, R_N is sensitive to variations in C_p and C_L, as shown in Equation (2.5), where especially C_p is not necessarily well-controlled.

A further practical challenge is the limited supply voltage, as was briefly discussed in Section 2.2.1. Consider Figure 2.5, as $|Z_N|$ goes toward infinity, the peak crystal voltage $\hat{I}_m \cdot |Z_N|$ also goes toward infinity. This is not possible in practice, as the active circuit will start to saturate or clip when its output voltage is close to the supply voltage, reducing the effective transconductance and hence R_N and therefore $|Z_N|$. Assuming that the active circuit is linear up to the point that the crystal voltage reaches V_{DD}, the maximum motional current that can be achieved without compromising the exponential growth can be calculated as:

$$\hat{I}_{m,max} = \frac{V_{DD}}{|Z_N|} \tag{2.11}$$

As Z_N goes toward infinity, the motional current that can be reached without limiting the exponential growth becomes zero. Setting $\hat{I}_{m,max}$ equal to the required steady-state amplitude $\hat{I}_{m,SS}$, the maximum Z_N for exponential growth can be calculated. It is interesting to note that the voltage applied over the crystal motional branch is lower than V_{DD}, until the exponential growth reaches the supply.

A reduction in R_N can be accepted, and still result in fast and low-energy start-up, as done in [13], [19], [26], where an approximately linear growth is observed once the transconductance stage starts saturating. There may be a point where the boosted resistance becomes less effective than a non-boosted stage during the start-up process. In this case, switching over to a single-stage amplifier stage can be worthwhile [13].

Using a negative-resistance based approach, no frequency selecting or generating components are necessary to let the crystal oscillation grow. The circuit is essentially timing itself through the crystal resonance. Since the crystal parallel capacitance is part of the resonant circuit, it takes no (additional) energy to charge and discharge it, in contrast to the Energy Injection approach that is discussed in the next section.

2.3 Energy Injection

Instead of deriving the timing from the crystal itself, the crystal can be driven by an injection source that generates a periodic waveform, as shown in Figure 2.11, thereby injecting energy in each (half) oscillation cycle.

When the injection source is a current source, the crystal ‘sees’ an infinite load, such that it resonates at its parallel resonance frequency, as discussed in Section 2.1.1. For a fast start-up, as much current as possible must be injected into the crystal (motional branch). The frequency of the current source must equal the parallel resonance frequency, as any other frequency is off-resonance, which would result in slower (and limited) growth of I_m. However, at the parallel resonance frequency, the crystal impedance is highest, which makes it difficult to create a current source that can inject a large current into the crystal.

On the other hand, when a voltage source is used, the voltage over the crystal is forced, such that the motional branch only ‘sees’ the injection voltage. It only

exchanges energy with the source, and not with C_p; the crystal is effectively loaded by a short-circuit and resonates at its series resonance. The crystal should be driven at this series resonance frequency, where its impedance is lowest, for maximum growth of the motional current.

A sinusoidal voltage source could be used as an injection source, but rather than generating sinusoidal voltage, it is simpler to connect the crystal to a fixed voltage in alternating polarity. The highest voltage available is usually the supply voltage V_{DD}, such that the injection waveform is effectively a square wave with amplitude V_{DD}, as shown in Figure 2.12. This square wave contains harmonics, but these are effectively filtered out due to the very high quality factor of quartz crystals (in the order of 100.000), such that the motional current $I_m(t)$ can be assumed to be sinusoidal. It may be worth noting that, in contrast to the negative-resistance based approach, the (peak) voltage over the crystal is equal to the supply voltage during the *entire* start-up sequence.

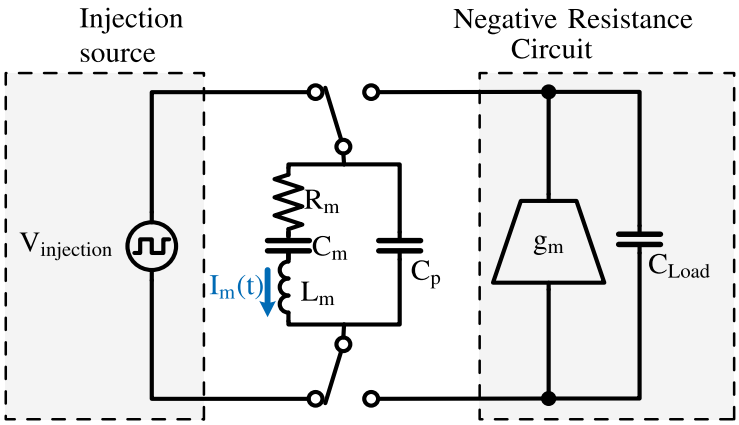


Figure 2.11. Energy injection concept.

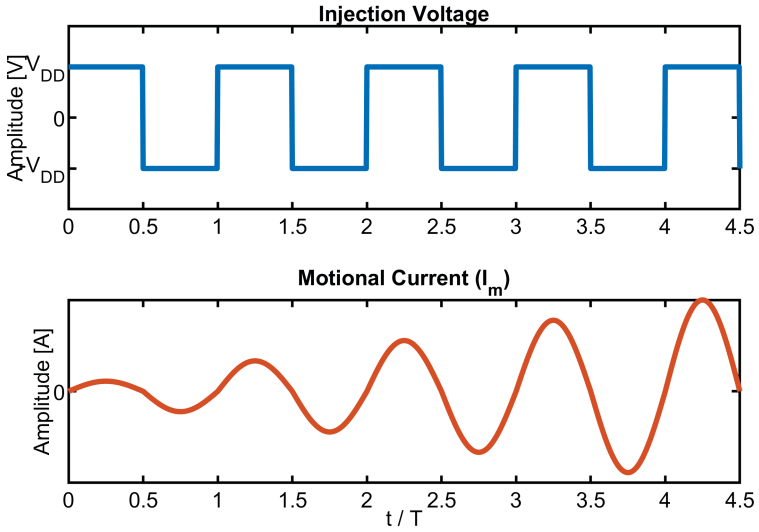


Figure 2.12. Ideal Energy Injection waveforms.

If the crystal losses are negligible ($R_m = 0$), the crystal current envelope grows as:

$$\hat{I}_m(t) = \frac{A}{2L_m}t \tag{2.12}$$

Where A is the amplitude of the fundamental of the injection waveform, as can be calculated through Fourier analysis. The amplitude at the fundamental frequency can be calculated as $A = \frac{4}{\pi}V_{DD}$, which is higher than V_{DD} itself, a property of the Fourier expansion of a square wave.

For long injection times, or if R_m is large, losses in R_m become significant as the amplitude grows, to a point where the oscillation no longer grows. Including R_m, the envelope of the oscillation can be calculated to grow as [19]:

$$\hat{I}_m(t) = \frac{A}{R_m}(1 - e^{-\frac{R_m}{2L_m}t}) \tag{2.13}$$

2.3.1 Injection frequency accuracy

The calculations above assume an injection frequency (and phase) that precisely matches the crystal frequency series resonance frequency. In practical circuits, however, no source can generate a precise frequency since the accurate reference itself - the crystal oscillator - is not started yet, creating a 'chicken-and-egg' problem. Any injection oscillator has worse frequency stability; if it would have equal or better performance, there would be no need for the crystal oscillator.

The injection source is normally an 'injection oscillator' with a low quality-factor, such as RC- or ring oscillators. Their low quality factor ensures that they start up quickly, but due to their PVT sensitivity, they suffer from frequency inaccuracy.

Any deviation in frequency from the crystal series frequency leads to an injection phase that drifts over time, increasing the phase difference between the injection voltage and current, such that the growth rate is reduced. Once the phase difference exceeds 90 degrees, the oscillation is even dampened. Figure 2.13 shows the growth of the envelope of I_m as a function of time for a typical MHz-range crystal, as calculated using the analysis in [26] for a driven damped resonator, for different frequency offsets. This shows the increasingly strict frequency requirements for larger $\hat{I}_{m,SS}$, requiring the injection waveform to be in phase over a longer time. Note that $\hat{I}_{m,SS}$ is dependent on the crystal and application. For the example in Figure 2.13, $\hat{I}_{m,SS}$ is at least in the mA range. To quickly achieve the desired steady-state amplitude, without much variation due to injection accuracy, the injection source has to be accurate within 1000 ppm or better.

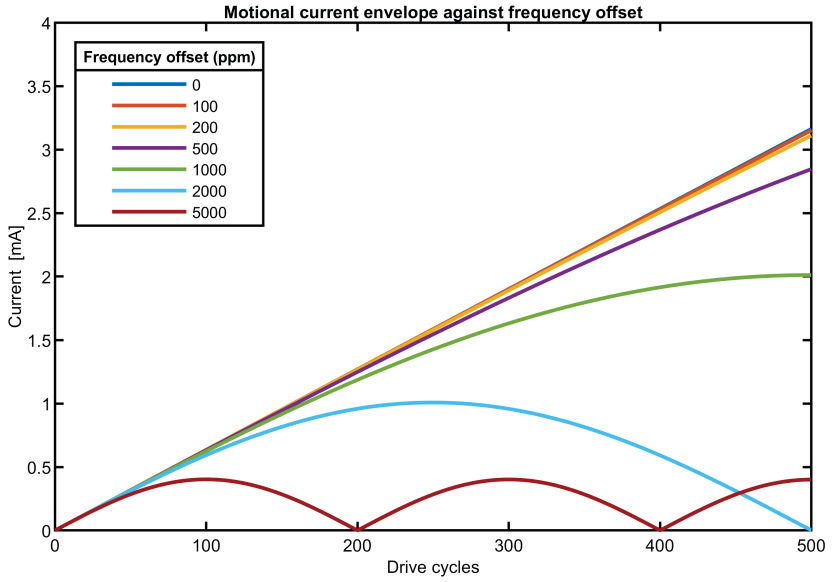


Figure 2.13. Motional current envelope growth with frequency inaccuracy for a typical (tens of) MHz-range crystal.

Injecting up to the required steady-state amplitude requires the least time, but requires a high injection precision, which becomes more strict for higher steady-state amplitudes. When not injecting up to the full steady-state amplitude, the

frequency accuracy requirement is relieved but it becomes necessary to use a negative-resistance circuit to grow the oscillation amplitude to its steady-state value, which adds to the start-up time and energy. The frequency accuracy requirements can be solved or circumvented by various methods, which will be described in the following subsections.

2.3.2 Constant frequency injection

The injection source is usually an on-chip oscillator. As shown in the previous subsection, the injection source itself should at least achieve a 1000 ppm accuracy. Furthermore, its power consumption should be low enough to save power and energy overall. For reference, the (average) power consumption during startup in the state-of-the-art crystal oscillator startup circuits is in the order of a milliwatt. This not only covers the injection oscillator, but the *entire* system, including for example the power required to drive the crystal. As will be discussed in Chapter 4, driving the crystal costs a significant part of the power (and energy) consumption, which means that the power consumption of the injection oscillator itself should be well below a milliwatt to result in a competitive overall start-up.

Achieving low power consumption and high frequency accuracy over a large temperature range is challenging. On-chip LC frequency references can achieve accuracies as low as 1.7 ppm [27] over a large temperature range but require many trim points over temperature. With a single trim, 120 ppm can be achieved [28], which is sufficient for crystal oscillator start-up. Nevertheless, LC oscillators consume several milliwatts or more [27]–[30] due to the limited LC tank quality factor and impedance scalability of on-chip LC tanks. Similarly, references based on thermal diffusivity (TD) can achieve 1000 ppm accuracy but also consume several milliwatts [31], [32]. This high power consumption makes both LC and TD references unattractive for use in crystal oscillator start-up.

In terms of power consumption, ring- or RC-based oscillators [29], [33]–[41] are most suited for crystal oscillator startup. Recent advances have made their accuracy sufficient for use in crystal oscillators. For example, using two-point trim, an accuracy of 200 ppm over temperature, for a power consumption of 142 µW can be achieved [36]. Likewise, 530 ppm for only 34 µW [37]. However, this comes at the cost of complexity, which shows in the need for multiple trim points over temperature, as well as a large chip area consumption. For example, one of the smallest RC references with sufficient accuracy covers 0.06 mm^2 [36], which in itself is more than many state-of-the-art crystal oscillator start-up circuits altogether (Table 3.4 and Table 4.5 list the state-of-the-art).

Applied to crystal oscillators, early attempts use a temperature-compensated ring oscillator as injection oscillator [42], which is stable enough to energize the crystal a bit, even over PVT variations, but is not sufficiently accurate to reach the steady-state amplitude after the injection time. Another work uses a chirped injection source, weakly injecting energy into the crystal, and measuring the voltage response until the crystal resonance is detected. Then, the injection frequency is kept constant and strongly drives the crystal [43]. The achieved detection accuracy limits the achieved frequency accuracy, such that large steady-state amplitudes cannot be achieved, and Negative Resistance Boosting is still required after injection.

Injection at a single frequency, for an infinite amount of time can be represented as a delta-function in the frequency domain. Injecting for a limited time T_{inj} broadens the frequency spectrum, as the Fourier transform of a windowed sine wave is a $sinc$ function with a main lobe width equal to $4\pi/T_{inj}$, as shown in Figure 2.14.

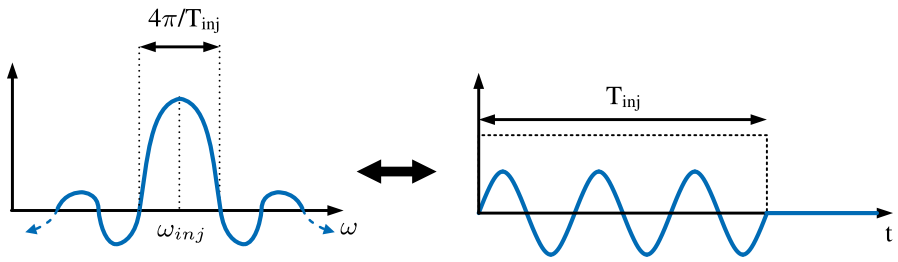


Figure 2.14. Pulse broadening due to limited injection time.

By precisely regulating the injection time, and using a sufficiently precise temperature-compensated ring oscillator, the achieved amplitude after injection can be kept within 10% of the ideal amplitude [44], and timing the injection duration by counting the number of cycles of the ring oscillator. As the $sinc$ shape narrows for longer injection times, achieving larger amplitudes becomes increasingly difficult, which is consistent with the reasoning in Section 2.3.1 as well as Figure 2.13.

2.3.3 Spreading of injection bandwidth

The frequency accuracy requirements can be reduced by accepting some inaccuracy, and deliberately spreading the injection energy over a sufficiently wide bandwidth. If the spread is sufficiently wide, the crystal is always excited at some point, even with variations in the injection frequency over PVT.

The spread in bandwidth can be achieved by chirping the injection frequency. By making sure that the crystal frequency is within the chirp range, even over PVT, there always is an amount of energy injected into the crystal [13], [19].

Alternatively, the injection oscillator can be implemented as a digitally controlled oscillator, which is dithered to spread the injection energy over a bandwidth that covers the crystal bandwidth [2], [22], [26].

Another technique to spread the injection energy is varying the injection time. Lengthening or shortening the injection time, therefore, changes the injection bandwidth, as discussed in the previous section. When temperature drifts, the main lobe can be made wider by changing T_{inj} [21]. The disadvantage is that the main lobe not only becomes wider but also lower, such that the total energy injected for temperatures away from nominal is reduced.

Regardless of the spreading technique, most of the energy is wasted, as it is not within the crystal bandwidth. The energy injected in the crystal is relatively small, such that the motional current after the injection time $I_m(T_{inj})$ is relatively small. Therefore, these techniques are usually complemented by a negative resistance boosted circuit to reach steady-state quickly.

2.3.4 Injection waveform re-alignment

It is difficult to ensure that the injection signal is in-phase over the entire injection time. However, injecting for a short time with some frequency inaccuracy hardly hampers the growth of the oscillation, as shown in Figure 2.13. The oscillation amplitude is still low after a short initial burst, but sufficient to observe the crystal oscillation and use this information to re-align the injection oscillator with the crystal oscillation. Another burst that is in phase with the crystal oscillation can then be applied, which allows further growth of the oscillation amplitude. This process can be repeated an arbitrary number of times until the desired amplitude $\hat{I}_{m,SS}$ is achieved [45].

Alternatively, the low oscillation amplitude after an initial burst can be used to synchronize the injection oscillator by using a PLL [46]. If the frequency accuracy is sufficiently improved, this allows continued energy injection in a longer burst from the now accurate injection oscillator until the desired steady-state amplitude is reached.

The disadvantage is that it takes some time for the injection oscillator to synchronize or re-align, which increases start-up time. Nevertheless, large steady-state amplitudes can be reached by these techniques.

Instead of changing the phase of the injection oscillator itself, [47] proposes to use a multi-phase injection oscillator, and switch to a different phase as the injection phase drifts from the crystal oscillation. Although multi-phase injection signals can be easily generated when using e.g. a ring-oscillator, it is unclear how to detect to which phase should be switched. [47] proposes to ensure that the frequency of the injection oscillator is below the crystal frequency, such that the phase is always incremented. However, it is unclear how to detect when to switch to the next injection phase, unless the exact frequency deviation is known, which was the problem in the first place.

Alternatively, when injecting in multiple bursts, the output amplitude can be measured in between these bursts, continuing injection until the desired steady-state amplitude is reached.

2.3.5 Limitations

In theory, the only parameters that put a lower bound to start-up time are the crystal parameter L_m and the supply voltage V_{DD}, as shown in Equation (2.12). In practice, however, the generation of the injection waveform is a significant challenge. As this waveform has to be precise over PVT, power has to be spent on calibration, spreading, or the re-alignment of the injection waveform.

When injecting energy for a short time, or over a wide bandwidth, only a small amount of energy is injected into the crystal. This requires the motional current amplitude to further grow, then grow using a (boosted) negative resistance circuit, forming a 'hybrid' start-up scheme.

A slight increase in the initial condition $I_m(0)$ can greatly reduce start-up time, as the start-up time using a negative-resistance circuit scales with $\ln(1/I_m(0))$ [11], [19]. This greatly reduces the amount of time that the negative resistance circuit draws power, and hence minimizes start-up energy.

However, the logarithmic dependence on $1/I_m(0)$ causes a large sensitivity for variations in the injected energy when injecting only a relatively small amount of energy, as done in hybrid techniques. Therefore, it must be ensured that the energy injected is constant over PVT.

On the other hand, the minimum start-up time is achieved when directly reaching the steady-state amplitude using energy injection alone. In this case, variations in $I_m(T_{inj})$ are less problematic. After injection, an amplitude error of 10% can typically be tolerated [48], [49].

The injection source is an 'external' component, that has no feedback from the crystal itself. This usually means that it has to be trimmed or calibrated, and depending on the tuning range, this can limit the flexibility to use different crystals. For example, the work in [48] uses 3 separate start-up circuits for 3 different crystal frequencies.

When using Energy Injection, the voltage is forced upon the crystal, with no feedback from the crystal itself. The crystal is loaded with a voltage source that has a low impedance, such that the crystal can be driven at its series resonance. C_p is effectively 'shorted'. However, this also means that the crystal parallel capacitance is charged and discharged by the injection source, as opposed to negative-resistance based circuits, that charge C_p by resonance. Since reaching the steady-state requires at least hundreds of cycles, C_p is charged and discharged at least hundreds of times, this costs a significant amount of energy, as will be further discussed in Chapter 4.

2.4 Comparison

Figure 2.15 compares the state-of-the-art in crystal oscillator start-up, where a distinction is made between Negative Resistance Boosting (NRB), Energy Injection as well as hybrids, which use Negative Resistance Boosting to achieve steady-state after Energy Injection. To normalize for crystal frequency, the x-axis shows the start-up time as the number of crystal cycles.

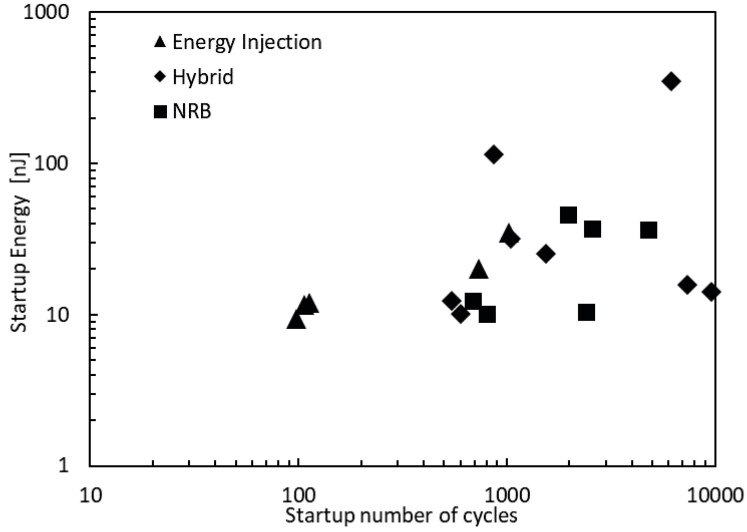


Figure 2.15. Comparison of state-of-the-art start-up techniques.

This comparison shows that even though pure NRB circuits can be among the lowest energy consumption, their start-up time is relatively long. Hybrid techniques are effective in reducing the start-up time. In terms of start-up energy, the hybrid and NRB techniques can be on par with energy injection techniques, despite their relatively long start-up time. However, energy injection seems to achieve the lowest start-up time and energy.

Note that this comparison is not completely fair. Equation (2.8) showed that the (theoretical) minimum start-up energy depends on L_m and $\hat{I}_{m,SS}$, which shows that the start-up energy depends on crystal type and circuit operating conditions. Consider, for example, the energy injection technique that achieves the lowest start-up time [48]. This circuit reaches a relatively low steady-state amplitude (2-3 times lower than others). If this circuit would be able to reach higher steady-state amplitudes, it would cost more time and energy (but still be faster than NRB or hybrid circuits).

These trade-offs, methods of comparison, and an in-depth comparison of different techniques will be further discussed in Chapter 5.

2.5 Conclusion

This chapter discussed the basics of crystal oscillators and shows that the motional branch current is the leading variable to observe to analyze the start-up of crystal oscillators. Quick and efficient start-up can be achieved by one or both of two types of start-up circuits; negative resistance boosting and energy injection.

Section 2.2 discussed the start-up time and energy consumption of NRB techniques. Whereas the crystals' parallel capacitance puts a lower bound on the negative resistance, (inductive) cancellation of C_p, can, in theory, allow arbitrarily fast start-up. Furthermore, the use of multi-stage amplifiers can greatly improve start-up energy by generating the required transconductance in an energy-efficient way. Negative-resistance circuits benefit from self-timing, relying only on the crystal for the timing accuracy, and can be started up very quickly. However, practical limitations in both robustness and supply voltage limit the speed at which the crystal oscillator can be started using NRB techniques.

A different method is energy injection, as discussed in Section 2.3. Energy injection forces the crystal from an external source. If the injection source is sufficiently accurate, this allows the motional current to grow linearly over time. The required

injection accuracy increases as the injection time increases and poses a significant challenge.

The frequency accuracy requirements can be relaxed by only injecting for a short time, and/or spreading the injection energy. However, this typically does not inject sufficient energy to achieve a high steady-state swing. Either a low steady-state amplitude must be accepted, or a negative-resistance based circuit is still required to achieve a large steady-state amplitude, forming a hybrid start-up circuit. If a large amplitude is to be reached by energy injection, the low-amplitude oscillation after a (short) burst can be used to re-align the injection source or improve its frequency accuracy, which allows further injection up to the desired steady-state amplitude.

While both NRB and energy injection show no fundamental limitations in terms of start-up time and energy, a comparison shows that in practice, energy injection techniques achieve the lowest start-up time and energy consumption. A more in-depth comparison between the different techniques will be made in Section 5.1.1.

Chapter 3

Self-timed energy injection

This chapter covers a self-timed injection technique that allows quick and energy-efficient start-up of crystal oscillators.
Sections 3.2 to 3.6 were previously published in the IEEE Journal of Solid-State Circuits [50], and are reproduced in this chapter with minor textual corrections. The conclusion in Section 3.6 has been adapted from [50].

3.1 Introduction

As discussed in Chapter 2, the start-up energy can be low using Negative Resistance Boosting. However, practical constraints limit the speed at which crystal oscillators using this technique can be started. On the other hand, energy injection seems the fastest practical way to start up a crystal oscillator. However, ensuring that the injection waveform as generated by an injection oscillator requires additional effort to ensure that the injection waveform is in-phase with the motional current during the entire injection period, which costs additional overhead in start-up time, power, and energy.

This chapter discusses an energy injection technique that operates without an injection oscillator, to combine the benefits of the self-timing property of negative resistance techniques, with the application of the maximum 'kick' - the supply voltage – as with energy injection. This is achieved by realizing that the motional current is a result of the injection voltage, but for an ideal injection waveform as shown in Figure 3.1, the zero-crossings of the motional current coincide with the zero crossings of the injection voltage. This means that instead of relying on an external injection oscillator to generate the injection voltage, the timing of the injection voltage can be derived by detecting the current and alternating the injection voltage polarity at each zero crossing. The injection timing now is only dependent on the crystal itself, which is why this concept is termed as 'self-timed energy injection'.

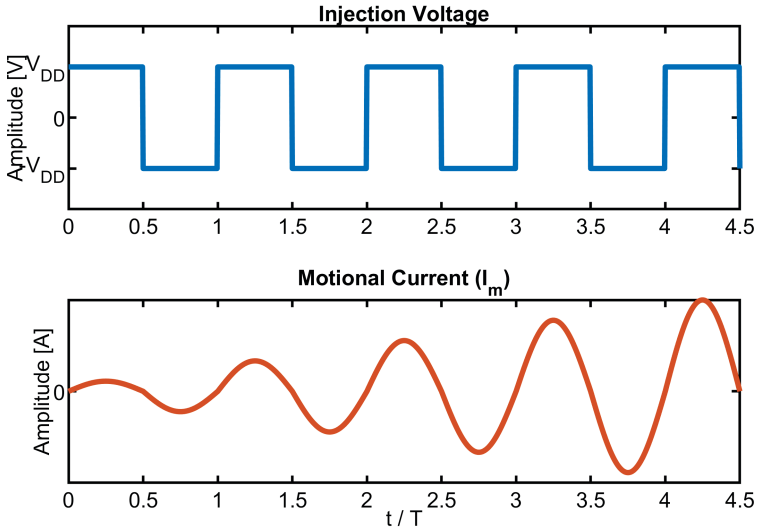


Figure 3.1. Ideal injection waveforms.

Section 3.2 elaborates on the concept and design considerations of self-timed injection. Section 3.3 covers design considerations and Section 3.4 covers the implementation of a prototype. Section discusses 3.5 simulation results. Measurements on the fabricated prototype are discussed in Section 3.6, followed by a conclusion in Section 3.7.

3.2 Concept

The proposed self-timed energy injection relies on measurement of the motional current I_m. To minimize CV^2 losses, there are no load capacitors connected during start-up. It is impossible to directly measure $I_m(t)$ since the motional branch is in parallel with C_p, so any current measured at the crystal terminals could flow in either the motional branch or C_p. This can be overcome by ensuring that no current flows in C_p, such that the current measured at the crystal terminals can only flow through the motional branch. This is achieved by applying (quasi-) constant voltages to the crystal by connecting it in an H-bridge, as shown in Figure 3.2. For a zero switch resistance, the voltage over the crystal settles immediately to $+V_{DD}$ or $-V_{DD}$, respectively. This means that $dV_{C_p}/dt = 0$ (except at the switching instants), meaning that $I_{C_p} = 0$, and hence all current I_m flows through the low-impedance path to the supply. The switch current therefore accurately indicates the zero-crossing of I_m.

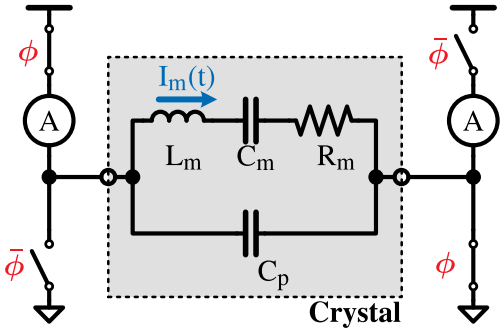


Figure 3.2. Self-timed energy injection concept.

The current measurement can be performed by exploiting the non-zero on-resistance of practical switches. The voltage over a switch in its 'on' state is a measure of the current flowing through it. The use of non-zero switch resistances has some implications that will be further discussed in the next section.

A block diagram of the proposed architecture is shown in Figure 3.3. The switches to ground have a low impedance, while the switches to the supply have a relatively high resistance to increase the current detection sensitivity. As $\hat{I}_m(t)$ is normally very small before start-up, it is maximized by applying a single voltage step, leading to an initial oscillation that is large enough to be detected. Comparators determine the direction of the current through the switches, while only the comparator that is connected to the switch that is 'on' is active. If the output of that comparator toggles, its input voltage has changed sign, meaning that I_m has reversed direction. The switch control block then toggles the switches and waits until the next zero crossing is detected, resulting in current and voltage waveforms similar to Figure 3.1.

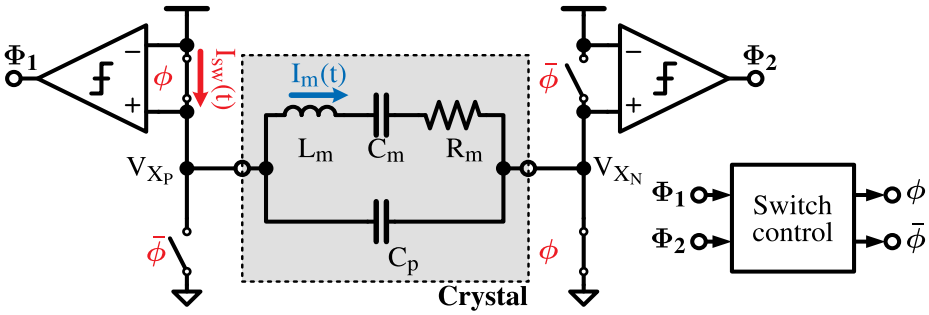


Figure 3.3. Self-timed energy injection implementation using comparators.

3.3 Design considerations

This section covers a few design considerations, such as the switch resistance and required comparator specifications.

3.3.1 Switch resistance

The current sensing sensitivity is critical at the beginning of start-up, where $\hat{I}_m(t)$ is the smallest. A high switch resistance R_{sw} is desired to maximize this sensitivity, resulting in a voltage drop $I_m(t) \cdot R_{sw}$. However, a non-zero switch impedance has two side effects. Firstly, the voltage over the crystal does not immediately settle to $+V_{DD}$ or $-V_{DD}$ due to the RC-time constant of C_p being charged through R_{sw}. Secondly, part of the current $I_m(t)$ flows through C_p and part of it through the switch, such that there is a phase shift between I_m and I_{sw}.

To analyze these effects during a single switch cycle, the circuit can be modeled as shown in Figure 3.4. The motional branch has a high Q-factor, such that it can be approximated as a sinusoidal current source with amplitude $\hat{I}_m(t)$, which increases with each switching cycle. The model includes a parasitic capacitance C_{par}, consisting of parasitics like comparator input capacitance, bond pad capacitance, and PCB trace capacitance. The current through R_{sw} can be separated in the individual contributions due to charging of $C_{tot} = C_p + C_{par}$ and the motional current $I_m(t)$.

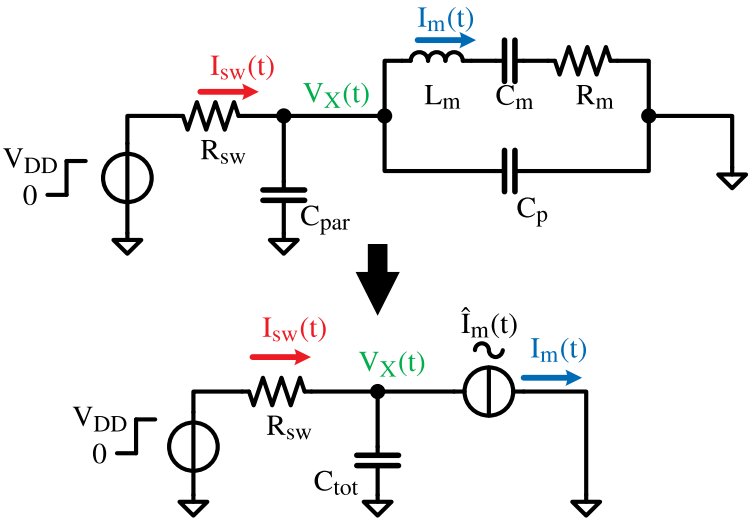


Figure 3.4. Model of the start-up circuit during one switch period.

Charging current

The current through R_{sw} due to charging C_p and C_{par} can be calculated as:

$$I_{sw,charge}(t) = \frac{V_{DD} - V_X(0)}{R_{sw}} e^{-\frac{t}{R_{sw}C_{tot}}} \tag{3.1}$$

In this expression $C_{tot} = C_p + C_{par}$, and $V_X(0)$ is the initial voltage at the crystal terminal. The voltage over C_{par} starts at 0 V, while C_p is initialized to $-V_{DD}$ as a result of charging to V_{DD} in the previous switch state. After switching, C_p and C_{par} share charge, such that the initial voltage $V_X(0)$ can be calculated as:

$$V_X(0) = -V_{dd} \frac{C_p}{C_p + C_{par}} \tag{3.2}$$

Motional branch current

R_{sw} and C_{tot} form an RC filter, which affects the phase and amplitude of the current I_{sw} with respect to I_m. The current through R_{sw} due to the motional current I_m can be calculated as:

$$I_{sw,I_m}(t) = A\, \hat{I}_m(t) \sin(\omega t - \varphi) \tag{3.3}$$

Where:

$$\varphi = \tan^{-1} \frac{1}{\omega R_{sw} C_{tot}}$$

$$A = \frac{1}{\sqrt{1 + (\omega R_{sw} C_{tot})^2}}$$

Total switch current

By superposition, Equations (3.1) and (3.3) can be added to yield the total switch current:

$$I_{sw}(t) = A\, \hat{I}_m(t) \sin(\omega t - \varphi) + \frac{V_{DD} - V_X(0)}{R_{sw}} e^{-\frac{t}{R_{sw}C_{tot}}} \tag{3.4}$$

Figure 3.5 shows the individual contributions, as well as the total switch current $I_{sw}(t)$, over an oscillation period T.

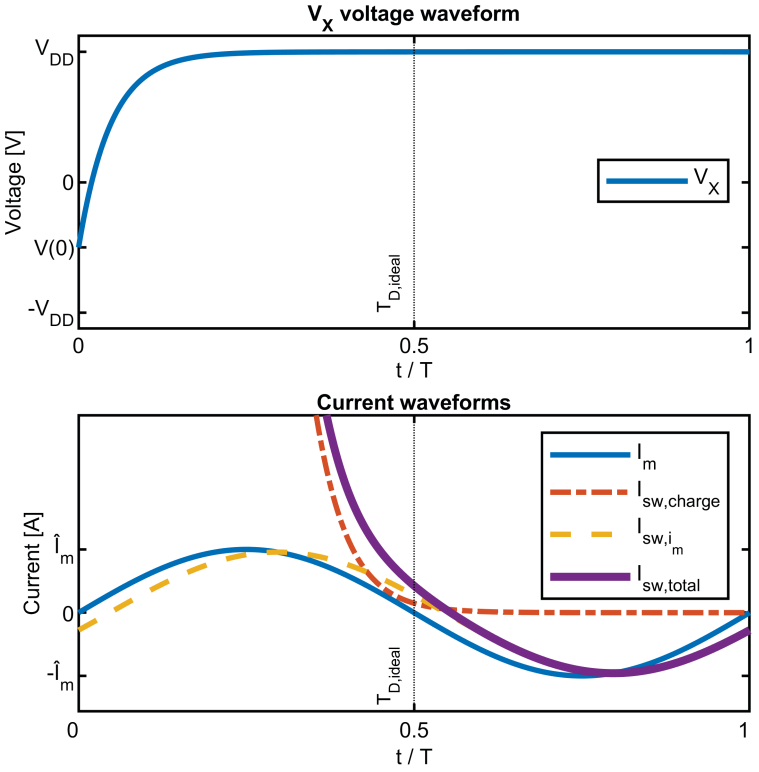


Figure 3.5. Modeled crystal voltage and switch current for a single switching event and (large) non-zero switch resistance ($\tau/T = 0.048$). In actual operation, the circuit would switch again just after $t = T/2$.

Ideally, we would like the comparator to detect the zero crossing of $I_m(t)$, occurring at $t = T/2$. The actual decision is taken when $I_{sw} = 0$, which is later than $t = T/2$ and depending on the switch resistance, as illustrated in Figure 3.6. Furthermore, delay from, for example, the comparator or D flip-flop, increases the time between the ideal switching time and the actual switch time. The latest point in time at which the injection waveform may switch is 90 degrees $(T/4)$ out of phase with I_m, as otherwise the oscillation would be damped instead of amplified. For a comparator delay $T_{D,comp}$, this means that $I_{sw}\left(\frac{3}{4}T - T_{D,comp}\right) < 0$, as illustrated in Figure 3.6. Substitution in (3.4) yields:

$$\frac{1}{\sqrt{1+(\omega R_{sw} C_{tot})^2}}\,\hat{I}_m(\mathrm{t})\,\sin\left(\frac{3}{2}\pi - \tan^{-1}\frac{1}{\omega R_{sw} C_{tot}}\right) + \frac{V_{DD}}{R_{sw}} e^{-\frac{\frac{3}{4}T - T_{D,comp}}{R_{sw} C_{tot}}} < 0 \quad (3.5)$$

This inequality can be solved (numerically) for R to find the maximum switch resistance R_{max}.

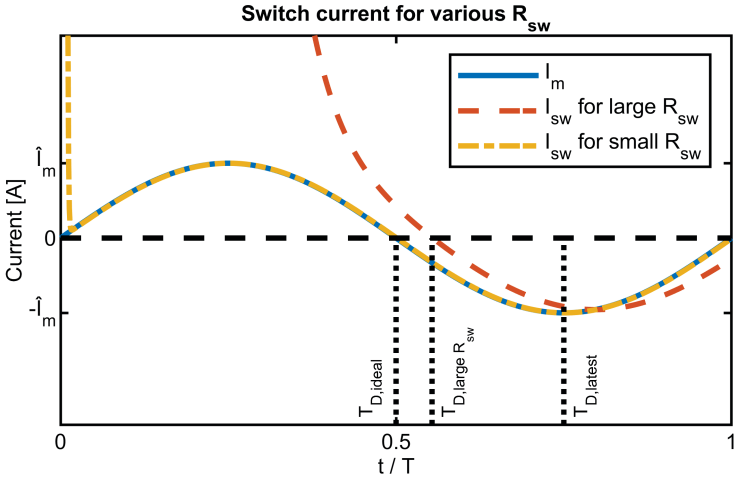


Figure 3.6. Switch current for various switch resistances.

Note that $T_{D,comp}$ is in practice amplitude dependent, and $\hat{I}_m(\mathrm{t})$ is time dependent. However, the first cycle is most critical since the motional current is at its smallest. Each cycle, the amplitude $\hat{I}_m$ grows and the specifications on the comparator and switch resistance become more relaxed. To maximize the initial current, a 'single kick' is given to the crystal by applying a voltage step equal to the supply. The initial current amplitude after this 'single kick' can be found by calculating the step response of an LC circuit to a step with amplitude V_{DD}, resulting in $\hat{I}_m(0) = V_{DD}\sqrt{C_m/L_m}$, which is in the range of 150 nA – 2 µA for typical crystals ranging between 16 MHz to 50 MHz. Substituting in the equation for R_{max} and assuming that the comparator delay is negligible results in a maximum switch resistance that is typically in the order of 1 kΩ, depending on the crystal and the parasitics.

3.3.2 Comparator specifications

Comparator offset results in decisions taken early or late, as illustrated in Figure 3.7. If the offset is positive, the comparator decision is slightly late, while for a negative offset, the decision is taken slightly early. As discussed in Section 3.3.1, the decision is delayed with respect to the ideal decision moment due to the charging of (parasitic) capacitances and comparator delay. Too much delay slows down the start-up process or can even dampen the oscillation. Therefore, we make sure that the decision threshold is always below V_{DD} in the circuit implementation.

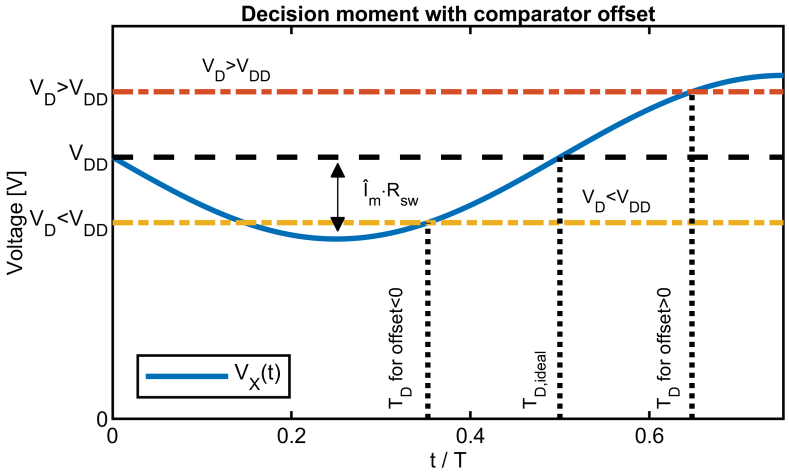


Figure 3.7. Decision moment variation over comparator offset, where V_D is the decision voltage.

With this decision threshold always below the supply, comparator offset will cause a current-referred offset $\frac{|V_{offset}|}{R_{sw}}$, causing early comparator decision. The earliest allowable decision moment is at $t = \frac{T}{4}$. Hence;

$$I_{sw}\left(\frac{T}{4}\right) < \frac{|V_{offset}|}{R_{sw}} \tag{3.6}$$

Using Equation (3.4), this equation can be solved (numerically) for the maximum allowable offset for a given switch resistance. Figure 3.8 shows the allowable offset for different values of comparator delay, for a 50 MHz crystal with $L_m = 1.18\,mH$ and $C_{tot} = 7\,pF$. Furthermore, the allowable switch resistance range is indicated, as calculated from Equation (3.5), showing the design space of offset versus switch resistance that permits the oscillation to start at a frequency that will inject energy into the crystal.

Note that the current-referred offset may be larger than $\hat{I}_m(0)$, but start-up is still achieved as long as the decision moment is after $T/4$. In this case, the circuit can be regarded as a relaxation oscillator. This behavior, due to the RC-charging of C_p, is taken into account in the previous analysis. This means that, as long as the requirements set on offset and switch resistance are fulfilled, energy is injected into the crystal in each cycle such that $\hat{I}_m(\mathrm{t})$ grows.

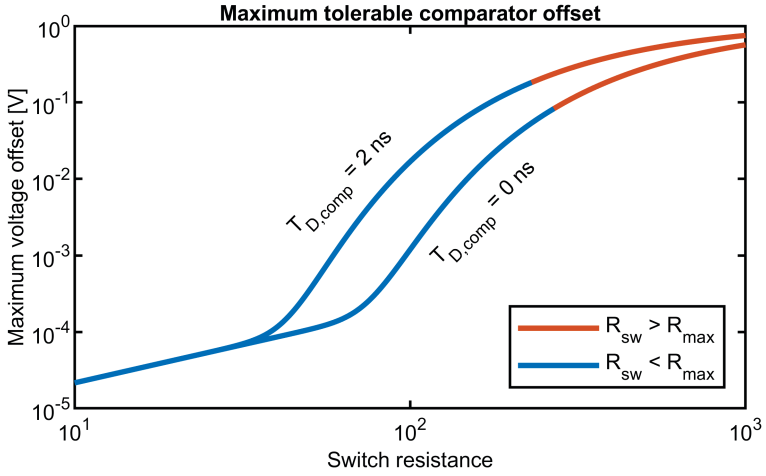


Figure 3.8. Maximum tolerable offset against switch resistance.

3.4 Circuit implementation

A block diagram of the implemented circuit is shown in Figure 3.9. The enable logic block enables the appropriate circuit blocks for start-up or steady-state. During start-up, the offset detection is briefly enabled, after which the start-up circuitry starts injecting energy into the crystal. The 15 pF load capacitor bank consists of 1 pF unit elements to allow various load capacitances and is disconnected during start-up to minimize CV^2 losses.

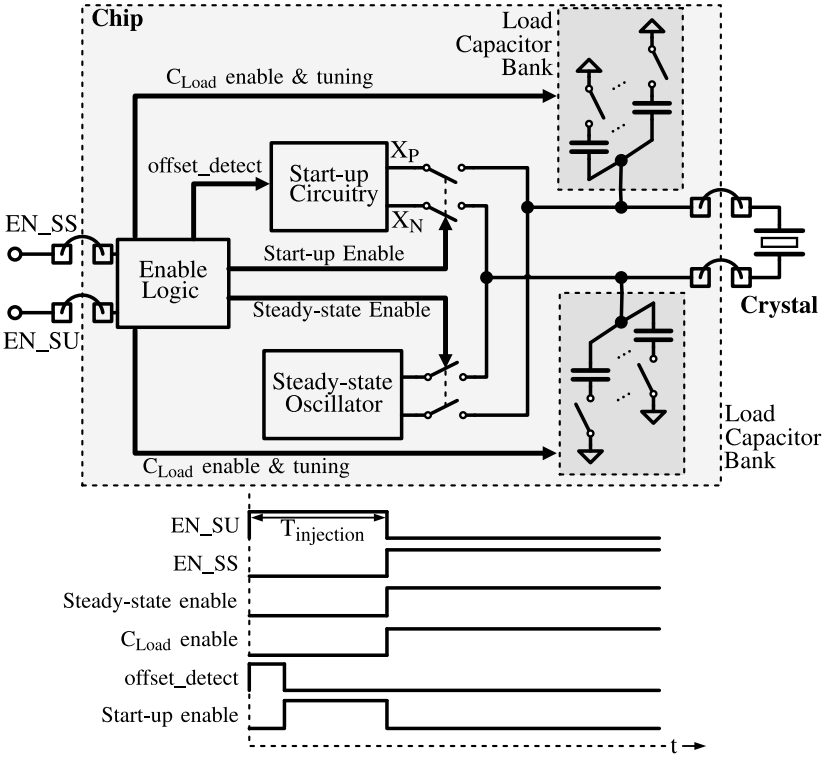


Figure 3.9. Circuit block diagram and timing diagram.

After a pre-determined (externally controlled) start-up time, the start-up control block disables the start-up circuitry. The steady-state oscillator and as well as the load capacitor bank are then enabled by closing the appropriate switches.

3.4.1 Start-up circuit

Figure 3.10 shows the block diagram of the start-up circuitry. Since only one comparator is active at any instant in time, a single comparator is used, with a switch matrix that is controlled by the Switch Control Logic, to connect the appropriate comparator inputs. The Switch Control Logic block consists of static combinational logic. When the start-up circuit is enabled, the D flip-flop toggles every time the comparator detects a zero-crossing. This in turn toggles the H-bridge switches, as well as the comparator inputs, repeating the process until the start-up circuitry is disabled.

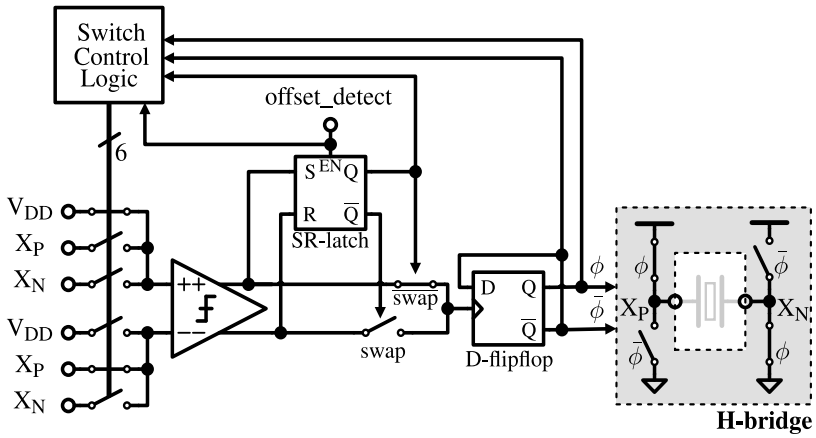


Figure 3.10. Start-up circuit block diagram.

During the first 80ns of each start-up cycle, the comparator offset sign detection is enabled by the enable logic. During this phase, both comparator inputs are connected to V_{DD}. The comparator output, which indicates the sign of the offset, is stored in an SR-latch. This serves as an input for the switch control logic, which swaps the comparator inputs and output when necessary to make sure the decision threshold is always below V_{DD}.

The comparator is implemented as a continuous time (limiting) amplifier, as shown in Figure 3.11. The first differential pair is large to minimize offset and is connected to a symmetric active load. A second differential stage increases the gain and converts to a single-ended output, which is amplified by cascaded inverters generating rail-to-rail outputs.

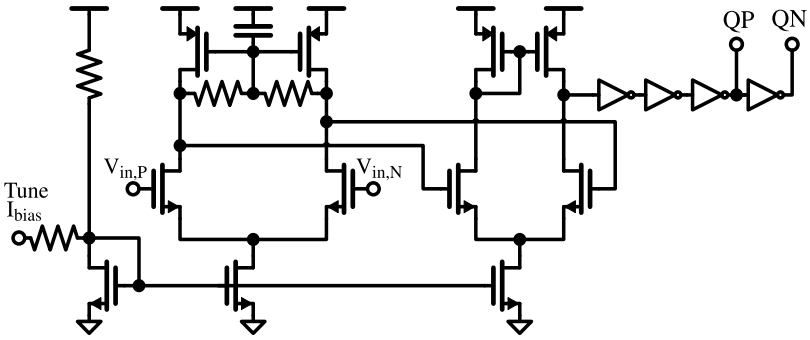


Figure 3.11. Comparator schematic.

The schematic of the H-bridge is shown in Figure 3.12. A low-impedance path to ground is provided by large NMOS switches. The PMOS switches to the supply act as measurement resistors. Their impedance is binarily scalable over a range of

approximately 40 Ω to 1.3 kΩ to accommodate various crystals having different requirements on settling time and detection sensitivity. Self-quenching NMOS switches are connected in parallel to the PMOS switches to quickly pull up the respective crystal nodes to $V_{DD} - V_{TH,N}$ after a switch event. In our current implementation, this allows a reduction in settling time by approximately one-third, while retaining the PMOS switch resistance for current detection sensitivity.

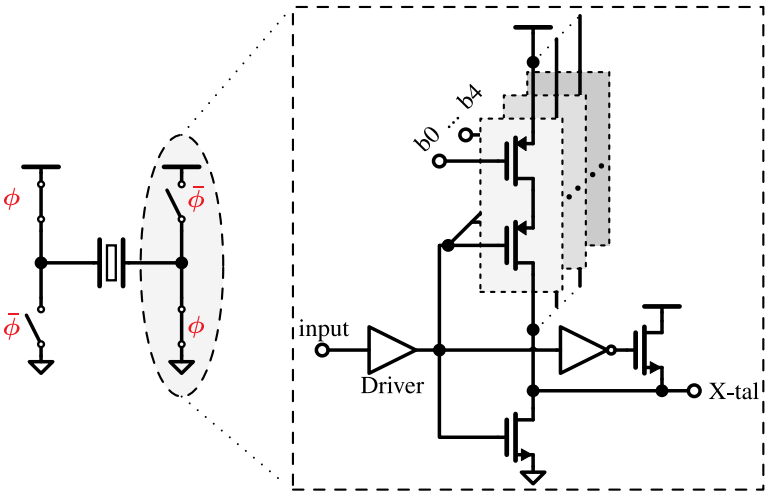


Figure 3.12. H-bridge schematic.

For supply filtering, 55 pF of decoupling capacitance is integrated on-chip. Simulations show that any (supply) ringing due to switching of the H-bridge has damped before the next zero-crossing of $I_m(t)$.

3.4.2 Steady-state oscillator

To demonstrate the transition from start-up to steady-state, a self-biased NMOS oscillator is integrated, as shown in Figure 3.13. There is no amplitude control loop for simplicity. The bias current, however, is externally tunable to accommodate various crystals and to enable manual amplitude control. Binary switches allow coarse tuning, while analog fine-tuning is possible through an external pin. Self-quenched NMOS transistors, triggered by a delay-line as a one-shot, pull the load capacitor voltages to $V_{DD} - V_{th}$ to reduce the settling time of the steady-state oscillator during the transition from start-up to steady-state. The CV^2 energy consumption associated with charging the load capacitors is negligible.

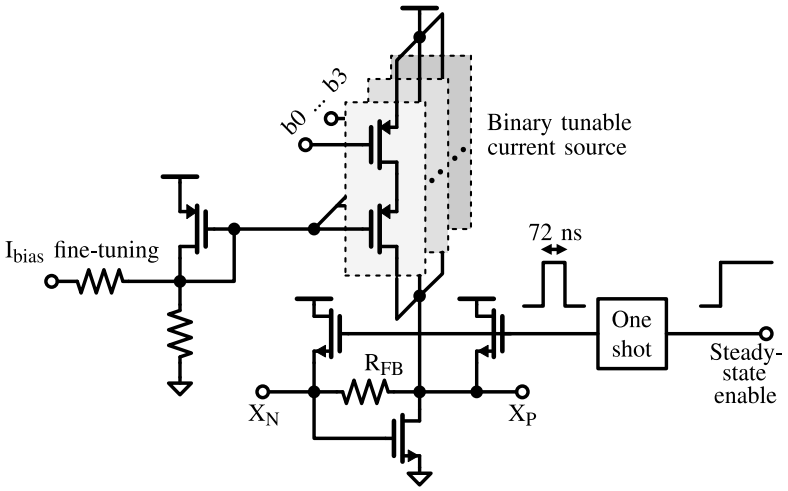


Figure 3.13. Steady-state oscillator schematic.

3.5 Simulation results

The proposed circuit is implemented in a 22nm FD-SOI technology with 0.8V supply voltage. Figure 3.14 shows waveforms for full-chip simulations with a 50 MHz crystal. At $t = 0$, the start-up circuit is activated, linearly increasing $\hat{I}_m$ after a brief offset sign detection phase. Although the initial injection frequency error is large, energy is injected into the crystal during the first few cycles, causing linear growth of $I_m(t)$. If the injection frequency were to be constant, $I_m(t)$ would quickly saturate because the injection phase drifts away from the crystal phase. However, using the proposed technique, the injection phase aligns itself with the crystal oscillation as $\hat{I}_m(\mathrm{t})$ grows. The injection frequency, therefore, converges to the crystal (series) frequency, allowing $I_m(t)$ to keep growing (approximately) linearly. At $t = 3.4\ \mu s$, the start-up circuit is disabled and the steady-state oscillator and load capacitors are enabled. The resonance frequency immediately switches to the parallel resonance frequency as evident from the frequency of $I_m(t)$, while the frequency of the output voltage requires some settling time (approximately 6-7 µs). The simulated time required for the output frequency to settle within 20 ppm is 6.9 µs, mainly due to the DC settling of the steady-state oscillator. The steady-state oscillator has a differential swing of 320 mVpp. The switches that (dis)connect the crystal to the steady-state oscillator and load capacitors have a negligible effect on phase noise performance.

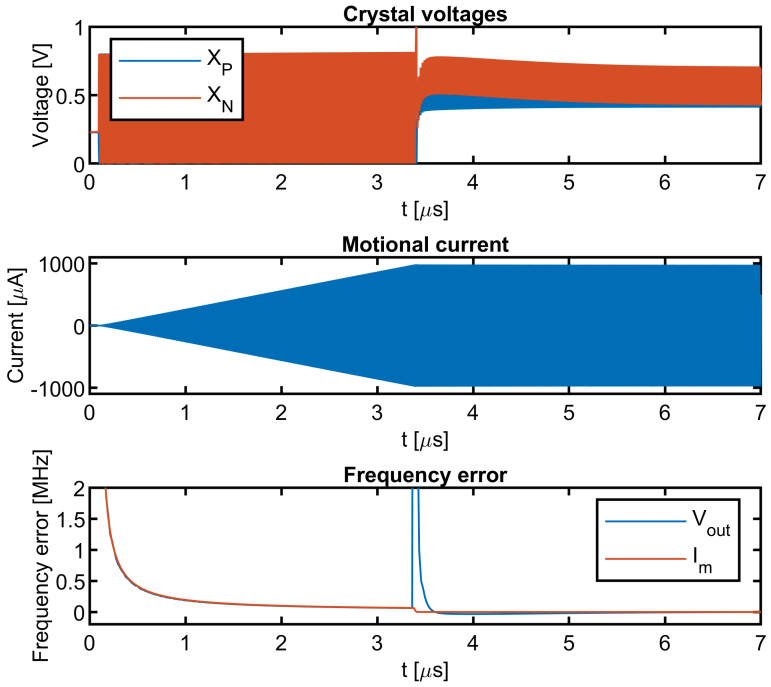


Figure 3.14. Simulated waveforms for a 50 MHz crystal.

Table 3.1 lists the simulated start-up energy breakdown for a 50 MHz crystal, as used in [48]. Most of the energy is consumed by the H-bridge, consisting predominantly of CV^2 losses from (dis)charging its capacitive load C_{tot}, consisting of both crystal C_p and circuit parasitics.

Table 3.1. Simulated start-up energy breakdown for a 50 MHz crystal.

	Energy (nJ)	**% of total energy**
H-bridge	2.32	73%
Comparator	0.49	15%
Logic etc.	0.03	1%
Steady-state oscillator settling	0.33	10%
Total start-up energy	**3.19**	**100%**

3.5.1 PVT variations and mismatch

As discussed in Section 3.3.2, comparator offset is an important factor in start-up time. The simulated comparator 1-σ offset is 0.8 mV. Figure 3.15 shows Monte-Carlo simulation results for local mismatch in the typical process corner, showing the spread in start-up time and energy after injecting energy for 3.4 µs to a 50 MHz crystal, without any calibration or tuning.

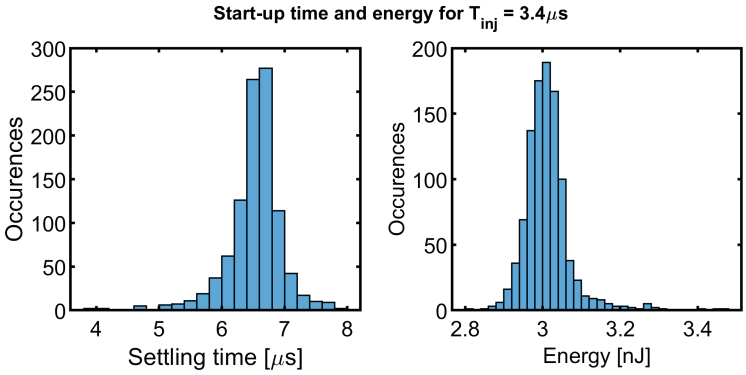


Figure 3.15. Monte Carlo simulation results for a 50 MHz crystal over 1016 points for an injection time of 3.4 µs.

As the steady-state oscillator in the prototype is unregulated, the steady-state amplitude varies greatly over process corners. However, in a practical implementation, the steady-state oscillator would be compensated to have a constant swing over PVT variations. To achieve this swing in the shortest possible time, the injection time could be corrected to yield the nominal steady-state current. Since $\hat{I}_m$ is approximately a linear function of T_{inj}, this could be achieved with a single trim. The additional start-up time due to variation in T_{inj} is listed in Table 3.2. Simulations over extreme process corners confirm that start-up is achieved over process variations, as also shown in Table 3.2. $\hat{I}_m(T_{inj})$ is within +/- 25% of its nominal value after a fixed injection time of 3.4 µs, without any tuning or calibration. The third and fourth column lists the required adjustment in T_{inj} to result in the same steady-state swing and the resulting settling time, respectively. Note that the variation in start-up time is mostly due to the DC settling of the steady-state oscillator.

Table 3.2. Simulated variation over extreme process corners at 20 °C.

Corner	$\hat{I}_m(T_{inj})$ (µA)	T_{start} (µs) (untrimmed)	ΔT_{inj} (µs)	T_{start} (µs) (trimmed)
Nominal	908	6.9	0	6.9
SS	679	12.0	+1.07	10.2
FF	1048	6.3	-0.46	4.6
FS	916	7.3	-0.03	7.3
SF	899	9	0.03	8.8

Simulations show minimal variation over circuit temperature, with $\hat{I}_m(T_{inj})$ varying less than 3% over -40-+85 °C. The settling time, however, varies between 6 to 9.6 µs due to the variation in steady-state oscillator settling. Simulations over supply voltages between 750-850 mV show a variation in $\hat{I}_m(T_{inj})$ ranging from 763 to 1041 µA, and start-up times between 6.9 to 9.4 µs.

Variation of the crystal L_m, just like other injection techniques, has a direct influence on the growth of $I_m(t)$ since its slope varies with $\frac{A}{2L_m}$. Simulations show successful start-up for C_p varying over ±50%, as well as robustness over crystal quality factor, with only 3% variation in $I_m(T_{inj})$ for a 5 times lower quality factor. These large variations in crystal parameters are unlikely to be encountered in practice.

3.6 Measurement results and discussion

The proposed circuit was fabricated in Global Foundries' 22nm FD-SOI CMOS process. A photo of the fabricated test chip is shown in Figure 3.16. The area breakdown is listed in Table 3.3. The output voltages are buffered by off-the-shelf amplifiers (LTC6268) in a unity-gain configuration. Figure 3.17 shows the conventional start-up sequence (without the proposed start-up technique) for a 5x3.2 mm sized 50 MHz crystal from the Abracon ABM3 series. The start-up time is more than 16ms, for an energy consumption exceeding 0.8 µJ. This long time is the result of the oscillator bias current being fixed for the final steady-state swing. The start-up would have been faster with an amplitude control loop.

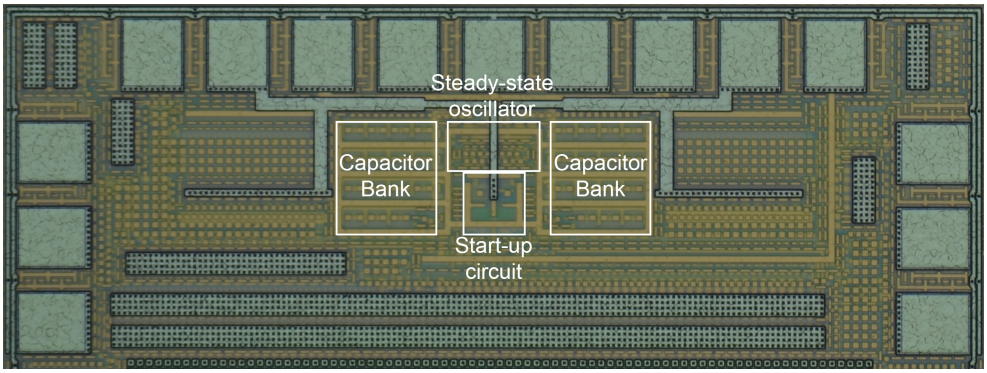


Figure 3.16. Chip photo.

Table 3.3. Area breakdown.

	Area (mm^2)	Fraction of total area
Start-up circuitry	0.0025	12.6%
Steady-state oscillator	0.0033	16.6%
Load capacitor banks	0.0140	70.7%
Total	0.0198	100%

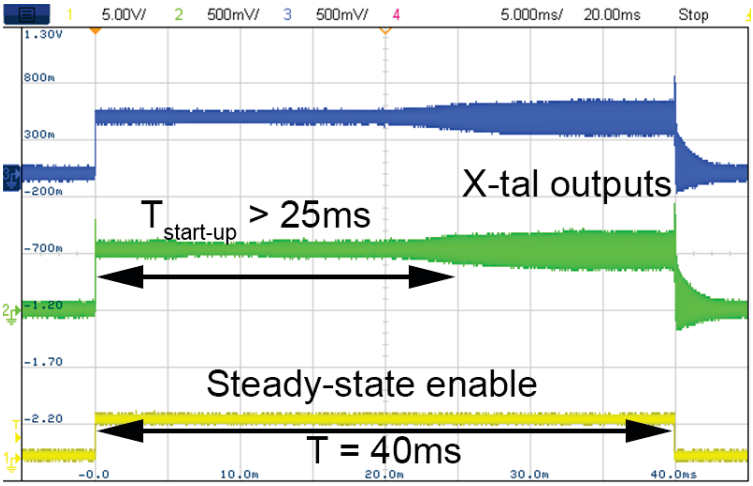


Figure 3.17. Measured output voltages for a 50 MHz crystal in a 5x3.2 mm package, without energy injection.

The optimum injection time depends on the crystal frequency, as well as the desired output swing, which depends on $\hat{I}_m$ and motional inductance, as well as the load capacitance. The injection time is controlled by an external microcontroller, but could easily be integrated on-chip by e.g. counting comparator decisions. The optimum injection time is manually (iteratively) determined once to reach the desired steady-state swing, as in the prototype it is not possible to detect if the steady-state amplitude has been reached during injection. The switch resistance is also determined manually, depending on the crystals' motional inductance and parallel capacitance. The injection time and switch resistance are kept constant in the measurements over voltage and temperature variations. Figure 3.18 shows the start-up transient with the proposed energy injection technique. After an injection time of 3.4 µs, the steady-state oscillator quickly settles to its steady-state amplitude, with a total start-up time of 6 µs.

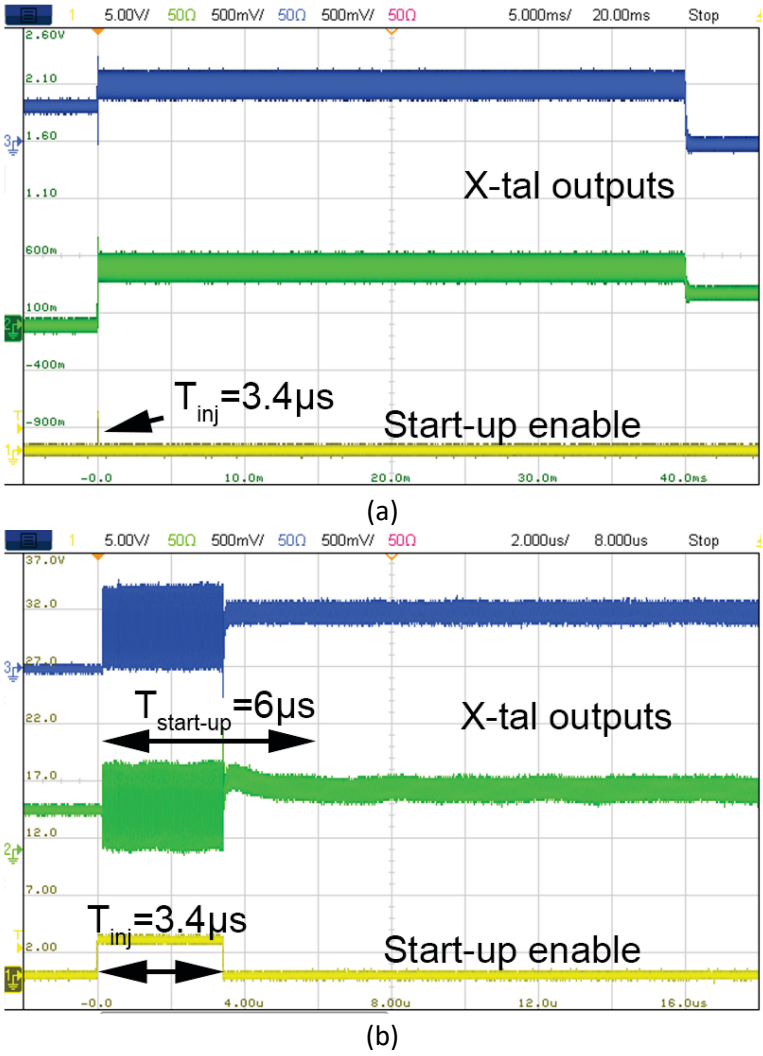


Figure 3.18. (a) Measured output voltages for a 50 MHz crystal in a 5x3.2 mm package, with energy injection, for T_{inj} = 3.4 µs, at T = 20 °C. (b) Zoomed in.

Figure 3.19 shows the measured frequency error during start-up, as measured using a wide (25 MHz) IF bandwidth. The injection frequency settles towards the crystal series resonance frequency during energy injection, and quickly settles towards the parallel resonance frequency after switching to steady-state, causing a frequency step after T_{inj}. Although the initial injection frequency error is large, this happens during such a short time interval that the growth of I_m is not hampered.

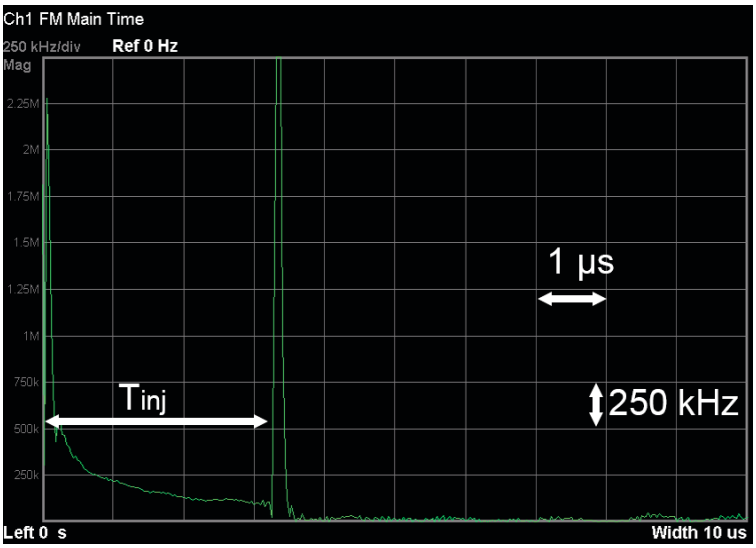


Figure 3.19. Measured frequency error at 20 °C.

As with any energy injection technique, driving the crystal not only excites the crystals' fundamental tone, but other spurious tones as well. These become visible as slight frequency deviations after energy injection until these spurs have damped after 1-2 ms. To show the frequency settling of the fundamental, the center frequency and IF bandwidth in measurement can be chosen such that the spurious tones fall out of band, assuming that a PLL would normally filter out these spurs. Figure 3.20 shows the frequency settling measurement, showing that the frequency has settled within 20 ppm after only 6 µs.

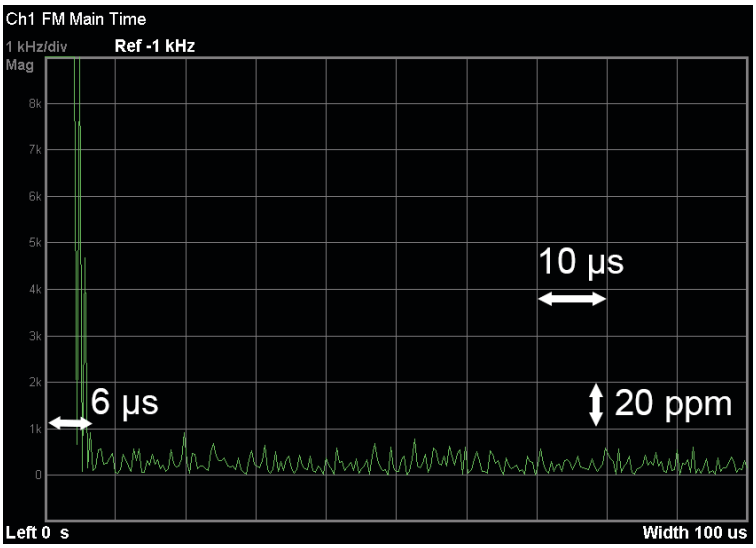


Figure 3.20. Measured frequency settling at 20 °C.

The settling time after T_{inj} is mainly due to the DC settling of the steady-state circuit, and could be improved by reducing R_{fb} (now 190 kΩ) in the steady-state oscillator, at the cost of increased power consumption. This is confirmed by simulation, showing that halving R_{fb} results in a 45% reduction of the settling time. The measured start-up energy is 3.7 nJ, more than 2 orders of magnitude lower than without the proposed injection technique.

Note that for measurement flexibility, the injection duration is externally controlled in the proposed prototype. However, an (initially inaccurate) clock signal is immediately available at the comparator output, which could be used to self-time the start-up circuit, e.g. by counting the number of cycles. An additional oscillator to generate this timing is therefore not necessary. Additionally, this clock could be used for, for example, oarse settling of a PLL or clocking digital circuitry.

Figure 3.21 and Figure 3.22 show the measured start-up time and energy over temperature and voltage, respectively. For both measurements, the injection time is kept constant. The steady-state oscillator bias current is manually adjusted to keep the amplitude constant.

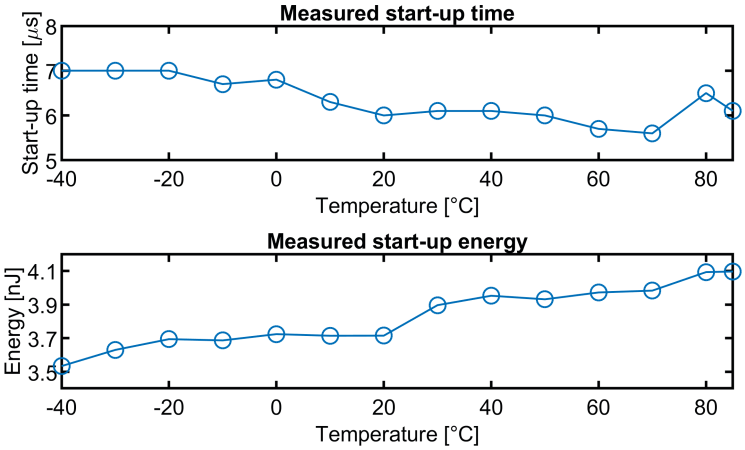


Figure 3.21. Measured start-up time and energy over temperature for T_{inj} = 3.4 µs.

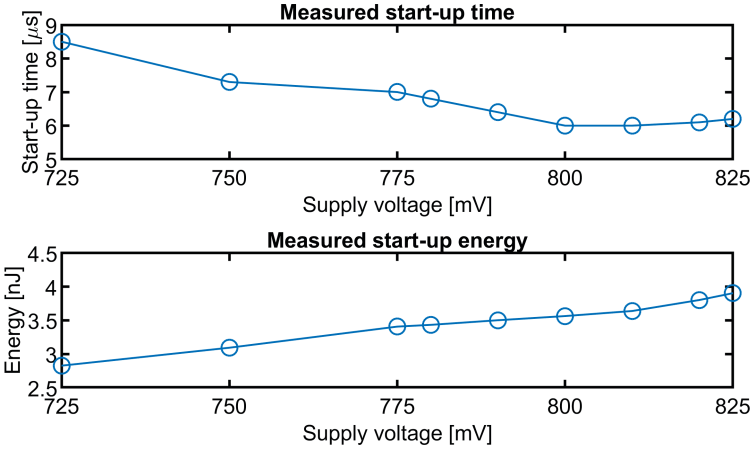


Figure 3.22. Measured start-up time and energy over supply voltage for T_{inj} = 3.4 µs.

Figure 3.23 shows the measured and simulated amplitude just after disabling the start-up circuitry, as a function of T_{inj}. The measured amplitude for long injection times is significantly lower than those of the extracted simulations. The inclusion of additional board parasitics and comparator offset in the simulation did not improve the match, leaving the exact reason for the deviation unknown. Figure 3.24 shows the measured start-up time over switch resistance variation.

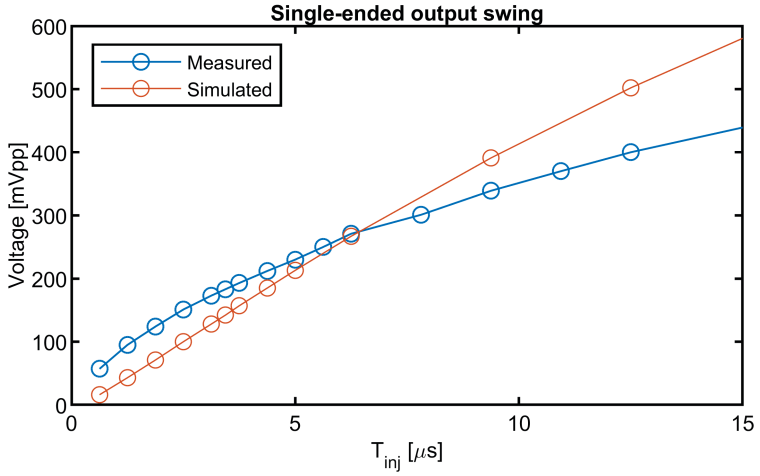


Figure 3.23. Measured and simulated output voltage swing as a function of T_{inj}.

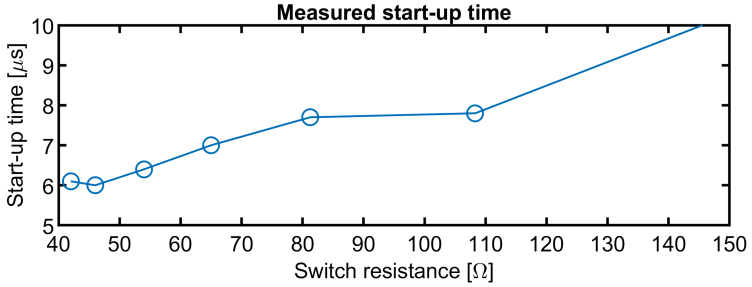


Figure 3.24. Measured start-up time over switch resistance variation for T_{inj} = 3.4 µs.

The measured phase noise is -123 dBc/Hz at a 1 kHz offset. The phase noise can be lowered by increasing the injection time and steady-state bias current, increasing the output swing at the expense of increased (start-up) energy consumption.

3.7 Conclusion

Table 3.4 lists the measured performance, for both a 24 MHz and a 50 MHz crystal, and compares it to the state-of-the-art. A comparison of startup time and startup energy is also graphically displayed in Figure 3.25. Compared to the prior art with the lowest start-up energy [48], which uses energy injection, start-up takes longer due to a lower injection amplitude caused by a lower supply voltage, as well as comparator delay. However, the energy consumption, using identical crystal part numbers, is 2.6 times lower.

Table 3.4. Comparison with prior art.

	JSSC' 16 [19]	TCAS-I' 18 [18]	VLSI' 18 [23]	JSSC' 18 [13]	ISSCC' 16 [2]	ISSCC' 19 [51]	ISSCC' 19 [45]	JSSC' 17 [48]	Chapter 3	
CMOS process (nm)	180	90	65	65	65	65	55	65	22 FD-SOI	
Supply voltage (V)	1.5	1.0	1.2	0.35	1.68	1.0	1.2	1	0.8	
Active area (mm^2)	0.12	0.07	0.005	0.02	0.08	0.07	0.05	0.09	0.02	
Frequency (MHz)	39.25	24	40	24	24	54	32	50	24	50
Load capacitance (pF)	8	10	9	6	6	6	6	9	6	7
Steady-state amplitude (V_{pp})	1.5	N/A	N/A	0.3	N/A	0.7	0.75	0.25	0.32	
Steady-state power consumption (µW)	181	95	141	32	393	198	N/A	195	10	51
Start-up time (µs)	158	200	64	400	64	19	23	1.95	15	6
Temperature range (°C)	-30–125	-40–90	-20–85	-40–90	-40–90	-40–85	-40–140	-40–85	-40–85	
Start-up time variation over temperature	±7%	28%	±10%	8%	±35%	±1%	±11%	10%	N/A	23%
Start-up time (cycles)	6202	4800	2560	9600	1536	1026	736	98	360	300
Start-up Energy (nJ)	349	37†	37	14	25*†	35†	20	9	4.4	3.7
Technique	Chirped energy injection + negative resistance boost	Dynamically adjusted load + gm increase	Negative resistance boost	Negative resistance boost	Dithered energy injection	2-step energy injection	Multi-step energy injection	Precisely timed injection	Self-timed injection	

** Estimated by multiplying steady-state power consumption and start-up time*

† Including clock buffer power

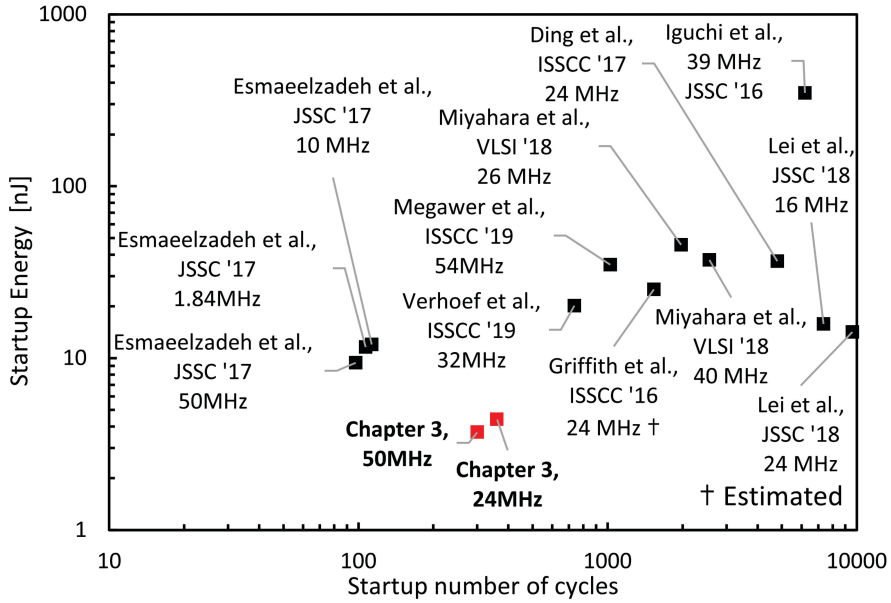


Figure 3.25. Start-up energy versus number of start-up cycles of the state-of-the-art crystal oscillators at the time of publication of [50]. Estimated value obtained by multiplying start-up time with steady-state power.

This chapter presented a self-timed energy injection technique, enabling quick and energy-efficient start-up of crystal oscillators. This is achieved by detecting the zero crossings of the motional branch current of the crystal and using this information to switch the voltage over the crystal. Since the injection waveform is self-timed, the injection frequency automatically matches the crystal frequency. This allows accurate energy injection, without the need for power-hungry frequency injection oscillators or calibration steps. The manufactured prototype achieves a start-up energy of 3.7 nJ. To the authors' best knowledge, this was the lowest start-up energy reported in literature at the time of publication of the article [50].

Chapter 4

Stepwise charging applied to energy injection

This chapter describes the application of step-wise charging to energy injection circuits to lower crystal oscillator start-up energy consumption and presents improvements to the energy injection technique that was presented in Chapter 3. Sections 4.2 to 4.4 were previously published in the IEEE Journal of Solid-State Circuits [52], and are reproduced in this chapter with minor textual corrections. The comparison and conclusions in Sections 4.5 and 4.6 have been adapted from [52].

4.1 Introduction

Regardless of the technique used for energy injection, a large part of the energy is caused by the injection buffers or switches that drive the crystal. In the most energy-efficient implementations in literature, more than 75% of the start-up energy stems from driving the crystal [46], [48], [50](Chapter 3). While a part of this energy is consumed by the switch drivers or actually stored in the oscillation, the majority of this energy is wasted in driving the large capacitive load that consists of e.g. C_L, C_p, and parasitics.

To reduce this overhead, C_{Load} can be disabled during start-up [26], [50]. Furthermore, careful design minimizes the parasitics consisting of e.g. PCB traces, wiring, and ESD protection. Nevertheless, most of the energy is spent (dis)charging the crystal C_p (typically in the order of picofarads), which is charged and discharged at least a couple hundred times during start-up, wasting energy in each switching cycle.

In this chapter we propose to charge and discharge the output load in multiple steps, a technique termed stepwise charging, to significantly reduce the energy

consumed when driving the capacitive load of the crystal. Section 4.2 covers the theory of stepwise charging and its application to crystal oscillator start-up. Section 4.3 covers the integration of the technique with a self-timed injection circuit, as well as improvements to the circuit. Measurements on the manufactured prototype are covered in Section 4.4 and Section 4.5 discusses the results, finally concluded by Section 4.6.

4.2 Crystal oscillator start-up with stepwise charging

To achieve the injection waveforms shown in Figure 3.1, both crystal terminals are alternately connected to the supply voltage and ground, as shown in Figure 4.1.(a). In each switching cycle, energy is injected into the crystals' motional branch, consisting of L_m, C_m and R_m. However, each switching cycle also charges various capacitors, including C_p, C_{Load} and parasitic capacitances from e.g. the PCB, ESD protection, and bond pad capacitances, as illustrated in Figure 4.1.(b).

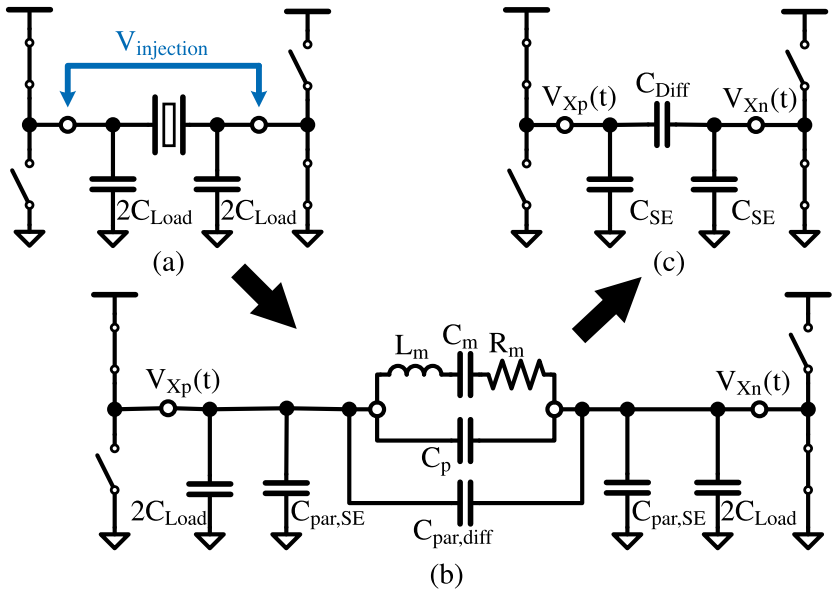


Figure 4.1. (a) H-bridge. (b) Model including parasitic capacitors (c) Equivalent model of capacitors during switching cycle.

This circuit can be simplified by realizing that, from a switching point of view, the motional branch can be seen as an open due to the large inductance of L_m (typically in the mH range). Furthermore, all capacitors can be lumped into two single-ended capacitances C_{SE} to ground at each terminal, as well as a differential capacitance C_{Diff}, as shown in Figure 4.1.(c).

Charging these capacitors costs energy. At every switching cycle (every $\frac{T}{2}$), one of the C_{SE} is discharged and the other is charged to V_{DD}, such that an amount of charge equal to $\Delta Q = C\Delta V = C_{SE}V_{DD}$ is drawn from the supply. Furthermore, C_{Diff} is charged from $-V_{DD}$ to $+V_{DD}$, costing an amount of charge $\Delta Q = C_{Diff}\Delta V$, with $\Delta V = 2V_{DD}$. By adding the individual contributions, the energy delivered by the supply to charge C_{SE} and C_{Diff} in each *half* crystal cycle can be calculated as $E = \Delta Q V_{DD} = \left(C_{SE} + 2C_{Diff}\right)V_{DD}^2$.

4.2.1 Stepwise charging

The energy required to alternately charge and discharge a capacitor can be reduced by stepwise charging [53]. If instead of directly charging a capacitor from 0 to V_{DD}, the capacitor is charged and discharged in N sequential steps of size V_{DD}/N, the energy consumption is reduced from CV^2 to $\frac{CV^2}{N}$. This technique was successfully applied in several fields, including ADCs [54], [55], ultrasonic transceivers [56], touch-screen readout circuits [57], and class-D amplifiers [58].

To understand this technique, consider a capacitor C_L that is periodically charged to V_{DD} and discharged to 0, as shown in Figure 4.2. Before being fully charged to V_{DD}, C_L is sequentially charged through each of the intermediate steps of size $V_{DD}/_N$ from (large) buffer capacitors $C_{buffer,n}$ (with $n = [1\,..\,N-1]$), assuming they are charged to $n\frac{V_{DD}}{N}$. In this case, the supply V_{DD} only has to supply an amount of charge equal to $C_L\Delta V = \frac{C_L V_{DD}}{N}$, which is N times less than if it would be directly charged to V_{DD}, and hence N times less energy.

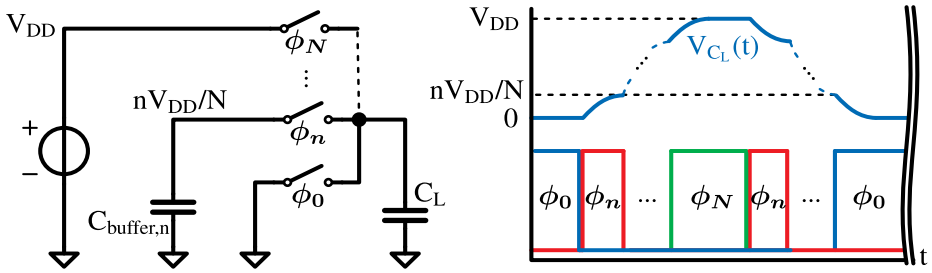


Figure 4.2. Stepwise charging concept.

If $C_{buffer,n}$ is charged to $n\frac{V_{DD}}{N}$, the amount of charge on $C_{buffer,n}$ is balanced over an entire cycle, as a packet of charge equal to $\frac{C_L V_{DD}}{N}$ is *removed* from each $C_{buffer,n}$ every time C_L is *charged*, but the same amount of charge is *added* every time C_L is *discharged*.

When $C_{buffer,n}$ is initially empty, it delivers no charge in the first stepwise *charging* cycle. However, a packet of charge is dumped onto $C_{buffer,n}$ in the *discharge* cycle, thereby increasing the amount of charge stored on $C_{buffer,n}$. In this way, the voltage on $C_{buffer,n}$ ($V_{C_{buffer,n}}$) converges towards $\frac{nV_{DD}}{N}$ with each consecutive cycle in what is essentially a self-stabilizing process [53]. It takes a time in the order of $N(\frac{C_{buffer,n}}{C_L})$ for $V_{C_{buffer,n}}$ to stabilize to $n\frac{V_{DD}}{N}$ [59].

$C_{buffer,n}$ should not be too large, as it would take a long time before $V_{C_{buffer,n}}$ settles towards $\frac{nV_{DD}}{N}$, which would compromise energy saving in the first few cycles. On the other hand, $C_{buffer,n}$ should be large enough ($C_{buffer,n} \gg C_L$) to be able to fully charge C_L to $n\frac{V_{DD}}{N}$ as to save a factor N in energy.

Note that the stepwise charging process requires no additional energy; no net charge is delivered by the supply, except when making the final step to V_{DD} [53]. All energy that is used to charge $C_{buffer,n}$ is recycled from C_L, which energy would otherwise have been wasted by dumping its charge to ground.

4.2.2 Application to crystal oscillator startup

The stepwise charging concept can be applied to crystal oscillators in several ways, since part of the capacitive load is differential and part of it is single-ended, as discussed in the previous section. A few possible implementations of stepwise charging are discussed in this subsection.

2-step charging

Consider the case shown in Figure 4.3.a. where the crystal is (dis)charged in 2 discrete time steps. The crystal node is connected to a voltage $\frac{V_{DD}}{2}$ before it is connected to the supply. Applying the model shown in Figure 4.3.c., the energy to charge C_{SE} can be calculated as $E_{SE} = \frac{C_{SE}V_{DD}^2}{2}$, while C_{Diff} only has to be charged from 0 to V_{DD}. This results in $E_{Diff} = C_{Diff}V_{DD}^2$, saving a factor of 2 compared to the conventional case.

Note that in this case, one of the crystal terminals is charged, while the other is *dis*charged, and C_{Diff} is effectively short-circuited. Therefore, the schematic can be simplified to Figure 4.3.b, shorting the crystal terminals by a single switch and leaving out the buffer capacitors to save switch and capacitor area for the same energy reduction.

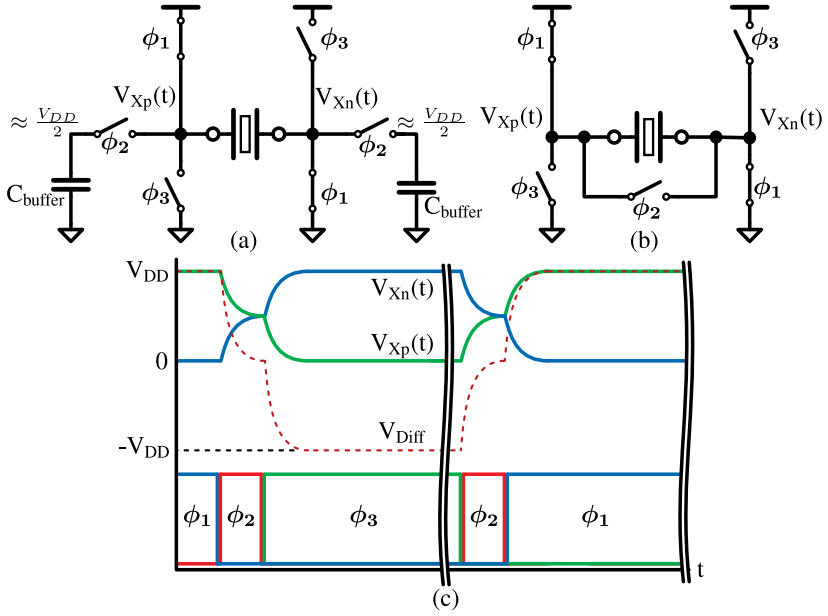


Figure 4.3. (a) 2-step charging. (b) Simplified 2-step charging. (c) Timing diagram.

4-step charging

Although (dis)charging in 2 steps halves the energy consumption, the supply still has to charge C_{Diff} from 0 to V_{DD} in a step equal to V_{DD}. The energy consumption can be further reduced by increasing the number of time-steps to 4, by first charging C_{Diff} to $\frac{V_{DD}}{2}$, as shown in Figure 4.4. C_{SE} still experiences the same voltage steps ΔV, and hence equal energy consumption, but the supply is charging C_{Diff} only from $\frac{V_{DD}}{2}$ to V_{DD}, costing only $E_{Diff} = \frac{C_{Diff}V_{DD}^2}{2}$. Please note that the time that the crystal is connected to C_{buffer} is much shorter than the time that it is connected to V_{DD}.

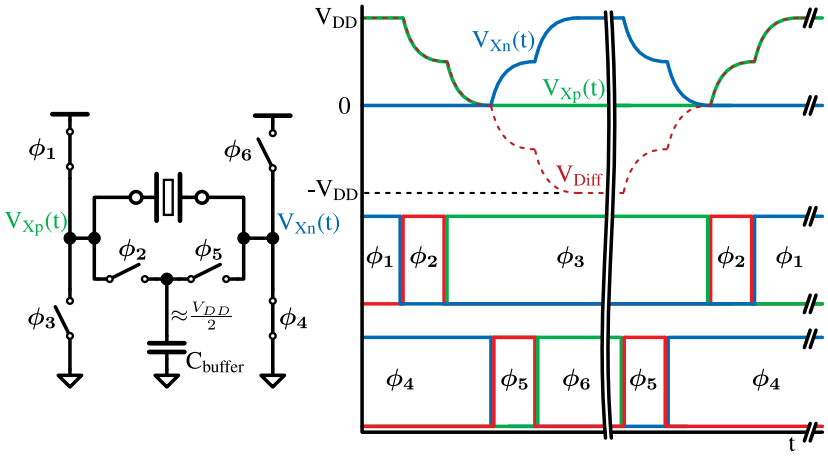


Figure 4.4. 4-step charging schematic and timing diagram.

By using stepwise charging, all energy that is stored in C_{Diff} and C_{SE} is redistributed before making the final step that charges either X_P or X_N towards the supply voltage. A comparison of the theoretical energy consumption using the proposed charging techniques is listed in Table 4.1. Note that the total reduction factor for 4-step charging depends on the ratio C_{SE}/C_{Diff} since a factor of 2 is saved in charging C_{SE} but a factor of 4 in C_{Diff}.

Table 4.1 Energy delivered by supply per ½ cycle.

	C_{Diff}	C_{SE}	Total reduction factor
Conventional	$2C_{Diff}V_{DD}^2$	$C_{SE}V_{DD}^2$	1
2-step charging	$C_{Diff}V_{DD}^2$	$\frac{1}{2}C_{SE}V_{DD}^2$	2
4-step charging	$\frac{1}{2}C_{Diff}V_{DD}^2$	$\frac{1}{2}C_{SE}V_{DD}^2$	2-4

4.3 Prototype circuit implementation

The proposed 4-step injection is integrated into a crystal oscillator circuit as a proof of concept. A block diagram of the start-up circuitry is shown in Figure 4.5. The start-up principle is self-timed injection, where the crystal voltage is reversed every time the motional branch current changes sign [50]. The change of the sign of the crystal current is detected by a comparator that senses the voltage over the bridge switches. At every positive comparator decision, the delay line generates the switch timing for the H-bridge to go through the stepwise charging sequence as described in Section 4.2.2 and shown in Figure 4.4.

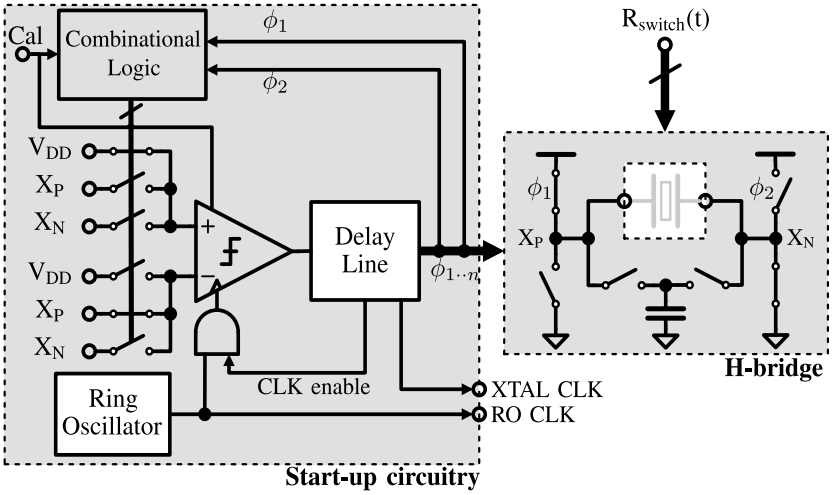


Figure 4.5. Start-up circuit block diagram.

The work in [50] uses a relatively large differential pair to achieve an acceptable offset, which decreases speed and increases power consumption. In this work, we propose to use a discrete-time comparator, running at a much higher (non-critical) clock rate than the crystal frequency. The delay from zero-crossing to comparator output is maximum one comparator clock cycle, which is lower than the delay for the continuous comparator used in [50]. A simple offset calibration scheme is used to reduce the offset, allowing the input differential pair to be relatively small, thereby increasing the energy efficiency of the comparator. A single comparator is used, with combinational logic and switches connecting the appropriate nodes to the comparator inputs. A calibration mode connects both comparator inputs to V_{DD} to allow offset compensation.

The injection timing is governed by the crystal through the zero-crossings of I_m, and not the comparator clock source. Hence, the frequency stability and phase noise requirements on the clock source are very relaxed, as long as it is running at a rate well above the crystal frequency. A simple minimum-sized current-starved ring oscillator (RO) is used, which is tunable between 200 MHz and 2 GHz. This comparator clock is disabled during stepwise charging (and steady-state operation) to save comparator energy and prevent false comparator decisions.

4.3.1 Comparator

The comparator is implemented as a dynamic bias latch-type comparator as shown in Figure 4.6, which offers high speed for a low energy consumption [60]. The comparator does not use any static bias current. Furthermore, by setting the ratio C_D/C_{Tail}, the pre-amplifier is quenched during the comparison time as soon as the

common-mode voltage drop ΔV_D at the pre-amplifier drain nodes D_1 and D_2 triggers the latch stage. This reduces the amount of charge required per comparison to $C_D \Delta V_D$ instead of the conventional $C_D V_{DD}$. The comparator is sized for up to 2 GHz clock speed and 0.3 mV input-referred noise, which is low enough to detect zero-crossings of I_m in the first few cycles of start-up. Comparator noise mainly affects the timing in the first few cycles, when the detected voltage is small due to the small motional current. As the amplitude of the motional current grows, the error due to noise becomes smaller. Since energy is injected over hundreds of cycles, any variation in $\hat{I}_{m,SS}$ due to variation in the initial cycles is small. Comparator noise is dominated by thermal noise as in [60]. (Low frequency) flicker noise is suppressed by the offset calibration that runs at the beginning of each start-up event. Note that any residual low frequency noise components might slightly shift the phase of the injected waveform in the beginning, but this phase error does not accumulate over time.

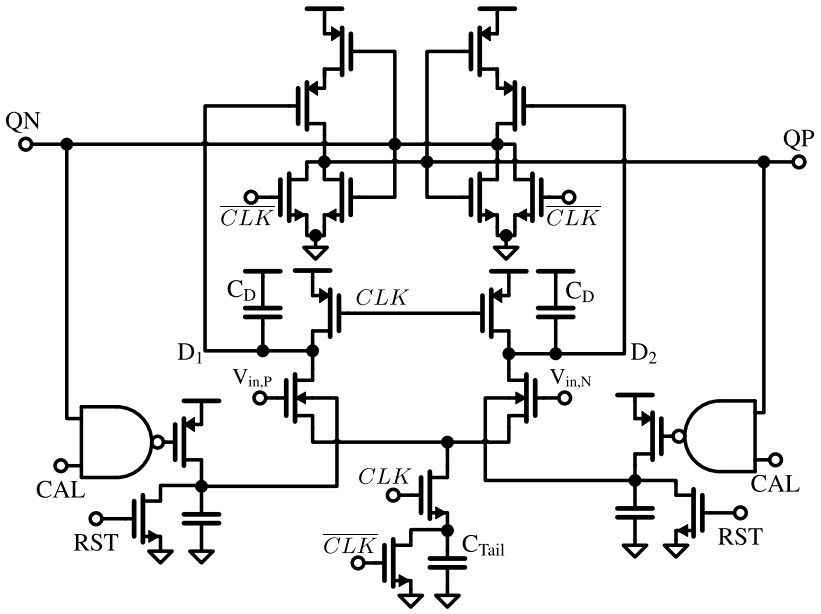


Figure 4.6. Comparator and offset compensation schematic.

By tuning the body potentials of the input differential pair the offset can be reduced [61], [62]. In this work, both comparator inputs are shorted to V_{DD} during calibration, and depending on the comparator output, using a triple-well structure, one of the body potentials is increased, such that the offset converges towards zero. The number of clock cycles for offset calibration is programmable and is set high enough to cancel the expected worst-case offset. The calibration is run every

time the crystal oscillator is started to ensure that the offset is affected by neither temperature variations nor leakage of the capacitors that store the body potential. Monte-Carlo simulation without and with offset cancellation shows a reduction of the 1-σ offset from 7.5 mV to only 72 µV.

4.3.2 Delay line

Figure 4.7 shows the block diagram of the delay line. Each positive comparator decision triggers the D flip-flop, which toggles the bridge output with intermediate stepwise charging. Delay elements consisting of inverters with long channel length generate pulses and delayed signals [54], which are used to generate the non-overlapping timing signals $\emptyset_{1\ldots n}$ for the bridge through combinational logic.

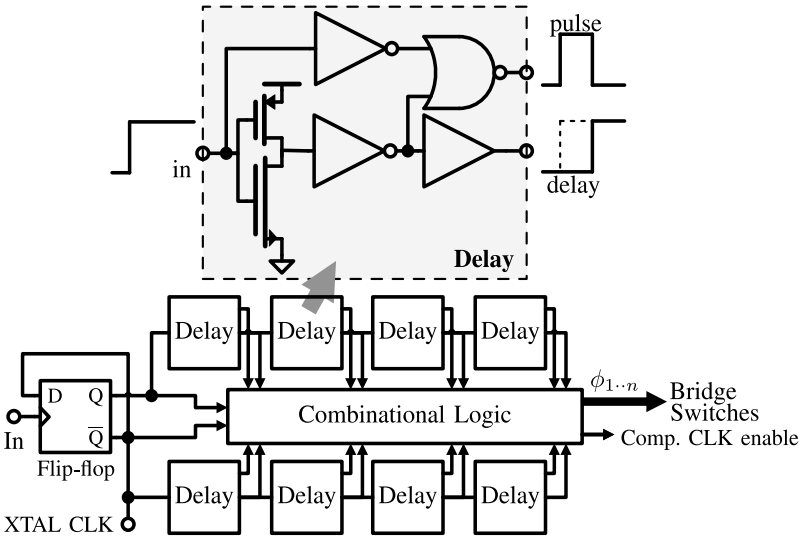


Figure 4.7. Delay line block and timing diagram.

4.3.3 Bridge

Figure 4.8 shows the schematic of the bridge. In addition to the switch timing as shown in Figure 4.4, large switches ('UP Fast Left' and 'UP Fast Right') to V_{DD} are briefly enabled to quickly pull up the crystal nodes before the relatively high-resistance sensing switches take over. These sensing switches are binarily tunable over a range of 18 Ω to 600 Ω and enable measurement of the motional current $I_m(t)$.

The switches that connect the crystal to C_{buffer} are bootstrapped to achieve low switch resistance. The voltage at the crystal node is *lower* than $V_{C_{buffer}}$ (typically ~$V_{DD}/2$) during stepwise *charging*, but *higher* during stepwise *discharging*. If the

switch would be bootstrapped with respect to a fixed terminal this could cause the voltage over the gate oxide to become higher than V_{DD}, which could cause a breakdown of the gate oxide. To prevent this, the stepwise charging switches are implemented as 2 pairs of bootstrapped switches that are bootstrapped with respect to $V_{C_{buffer}}$ and the crystal nodes for the charge and discharge cycle, respectively.

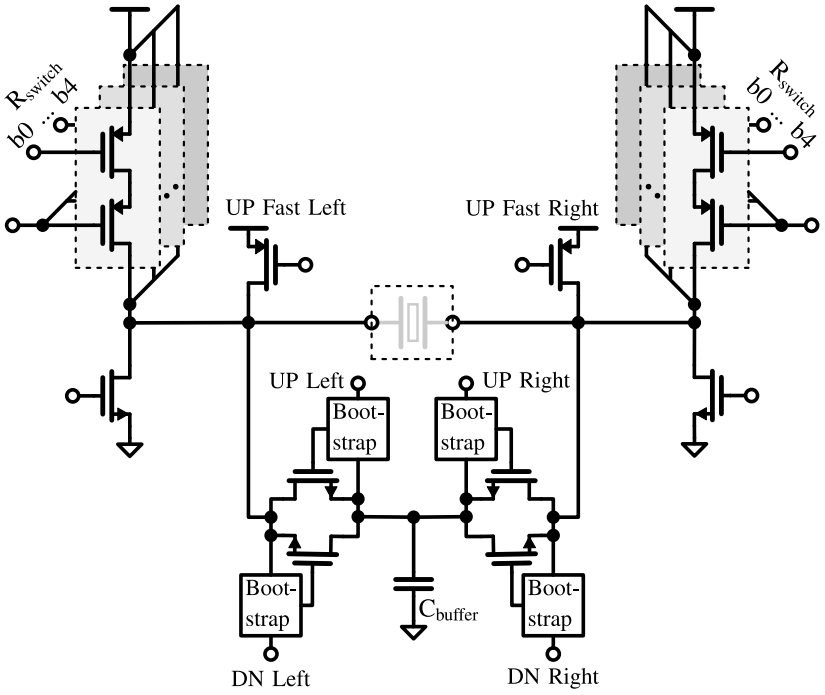


Figure 4.8. Bridge schematic.

The analysis on stepwise charging in Section 4.2.2 assumes full settling of the crystal node when stepwise charging and discharging. This can be achieved with very large switches, which, however, not only require large drivers and hence increased power consumption but also introduce a significant off-state leakage current. This current flows through the measurement resistor, generating an offset for the zero-crossing detection of I_m. This imposed an upper limit on the switch size.

The switch size also influences energy consumption reduction. The theoretical energy reduction calculations presented in the previous subsection assume full settling to the stepwise voltages. Assuming that C_{buffer} is much larger than the capacitive loading ($C_{buffer} \gg C_{Diff}$ and C_{SE}), the intermediate steps settle

exponentially with a time constant $\tau = R_{stepwise}C_{eff}$, where $R_{stepwise}$ is the resistance of the bootstrapped switches and C_{eff} is the effective capacitive load at one of the crystal terminals, consisting of $C_{SE} + C_{Diff}$.

For a settling time t_{step}, when charging from 0 to $\frac{V_{DD}}{2}$, instead of reaching $\frac{V_{DD}}{2}$, only $\frac{V_{DD}}{2}\left(1 - e^{-\frac{t_{step}}{\tau}}\right)$ is reached. More charge is drawn from the supply, and the energy saving is reduced to $0.5\left(1 - e^{-\frac{t_{settle}}{\tau}}\right)$. Suitable values for the settling time are 2-4 time constants [53].

As discussed in Section 4.2.2, C_{buffer} should neither be too large, as it would take a long time before it is charged and energy is saved, nor too small, as it would not be able to fully charge the load. The optimum depends on the number of start-up cycles, output load, and overhead, and can be found by simulation. However, the total energy consumption is only weakly dependent on the size of C_{buffer}, which is implemented as a fixed capacitor of 137 pF in our design. For the 32 MHz crystal, C_{buffer} is charged to 90% of its final value in 20 cycles. MOS and MOM capacitors are stacked on top of each other to minimize chip area. Note that the load capacitor bank can be partially reused for this purpose. MOS leakage discharges C_{buffer} with a time constant of about 17 ms. Because of the relatively long time of inactivity between successive start-up events, this means that C_{buffer} is (almost) completely discharged every time the crystal oscillator is started.

4.3.4 Full-chip overview

A block diagram of the entire chip, as well as a timing diagram of the start-up sequence, is shown in Figure 4.9. A single enable signal starts the crystal oscillator. When this signal (*EN_XO*) is enabled, the Control Logic block resets all timers and enables the ring oscillator. Comparator offset calibration is active for a programmed number of cycles of the ring oscillator, T_{cal}. After this, the self-timed injection start-up circuitry is enabled to inject energy into the crystal. The value of R_{switch} is varied through programmed values during the first 16 cycles of start-up, reducing R_{switch} as the amplitude of the oscillation I_m grows. This alleviates the trade-off between current detection sensitivity and delay encountered in [50]. After a programmed number of cycles of the crystal, as counted from *CLK_XTAL*, the steady-state oscillator is enabled.

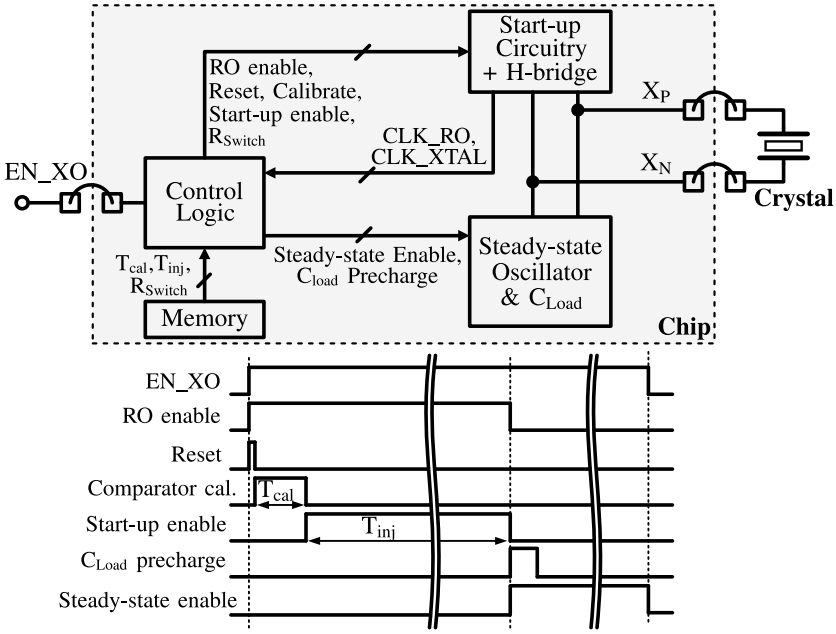


Figure 4.9. Circuit block diagram and timing diagram.

The steady-state oscillator core is a Pierce oscillator, as shown in Figure 4.10. Switches enable the bias current and (dis)connect the oscillator core to the crystal. The 31 pF load capacitor bank consists of 1 pF unit elements to accommodate crystals with various load capacitances. To reduce the time required to (dis)charge the load capacitors, the output nodes are briefly connected to C_{buffer} to quickly charge these nodes to approximately $\frac{V_{DD}}{2}$ when the steady-state oscillator is enabled.

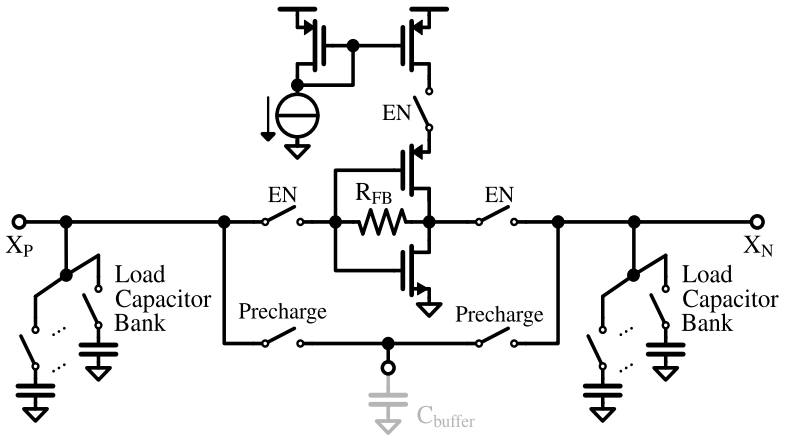


Figure 4.10. Steady-state oscillator schematic.

4.3.5 Simulation results

Figure 4.11 shows transient simulation results for a 32 MHz crystal, showing swift settling to steady-state after injecting energy for 400 programmed cycles. Full-chip transient noise simulations over 100 different noise seeds show a worst-case variation of $\hat{I}_m(T_{inj})$ within 3.1% of its nominal value, with a 1-σ of 1.1%. This shows that neither comparator noise, nor other noise sources significantly affect the start-up process. Monte-Carlo simulation over mismatch shows a variation of $\hat{I}_m(T_{inj})$ with σ=1.4% and a worst-case deviation less than 5%, which demonstrates robustness against mismatch. Simulations over process corners show, without changing any settings, less than 15% variation of $\hat{I}_m(T_{inj})$.

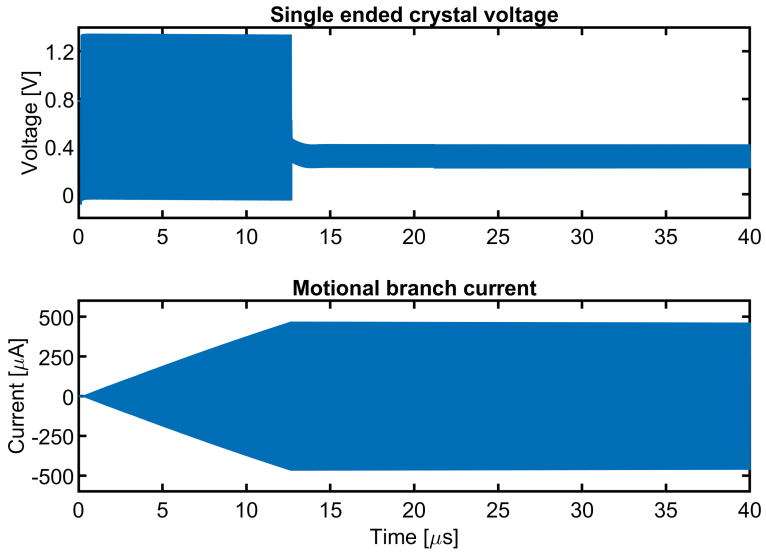


Figure 4.11. Simulated waveforms for a 32 MHz crystal, injecting for 400 cycles.

Table 4.2 shows the simulated energy breakdown, with and without stepwise charging. To simulate the case without stepwise charging, the delay line is modified to skip stepwise charging. The rest of the circuitry is identical and includes the proposed improvements to self-timed injection. The contribution of the bridge energy to the total energy consumption is divided into three parts. Firstly, the overhead of switch drivers and bootstrap circuits. Secondly, the energy that is stored in the crystal, calculated as $\frac{1}{2}L_m\hat{I}_m^2$, and lastly, the energy required to drive the capacitive load.

Table 4.2. Simulated energy breakdown for a 32 MHz crystal for 400 drive cycles.

	w/o stepwise charging	Stepwise charging	
		Same T_{inj}	Same Amplitude
T_{inj} **(us)**	10.36	10.36	12.66
Bridge (nJ)	7.98	4.63	5.99
Switch drivers + bootstrap (nJ)	0.20	0.48	0.59
Crystal ($\hat{I}_m$) (nJ)	1.35	0.91	1.35
Capacitive load (nJ)	6.43	3.24	4.05
Startup circuits (nJ)	1.63	1.65	2.01
Total (nJ)	9.61	6.28	8.00

For an equal number of drive cycles, the capacitive losses are reduced by a factor >2. However, the amplitude at the fundamental frequency of the injection waveform is lower than the $\frac{4}{\pi}V_{DD}$ due to the time required for stepwise charging. Therefore, for the same T_{inj}, the reached amplitude and crystal energy are lower when using stepwise charging compared to conventional injection. A larger number of drive cycles is required, to reach the same amplitude, as shown in the third column of Table 4.2. The increased injection time costs additional energy in start-up circuitry as well as more cycles of driving the capacitive load. Nonetheless, the overall energy consumption is lower when using stepwise charging. Combined with the other proposed techniques, this results in a low start-up energy consumption. This work aims for minimum start-up energy and therefore implements the 4-step charging technique. If chip area is of importance, the 2-step charging technique that was proposed in 4.2.2 can be used instead, at the expense of saving less energy.

4.4 Measurement results

Figure 4.12 shows a photo of the prototype, as fabricated in a 65nm CMOS process. The chip was wire bonded to a QFN package and clamped to a PCB, on which the crystal voltages are buffered by off-the-shelf amplifiers (LTC6268) in a unity-gain configuration. The circuit was tested with various crystals in the range of 24 MHz to 50 MHz in various package sizes, showing reliable start-up. The presented measurements are performed using a 24 MHz (TXC 7V-24.000MAAE-T), a 32 MHz crystal (Murata XRCGB32M000F2P00R0), and two different 50 MHz crystals (Abracon ABM3-50.000MHZ-D2Y-F-T and TXC 7M-50.000MAHV-T), respectively.

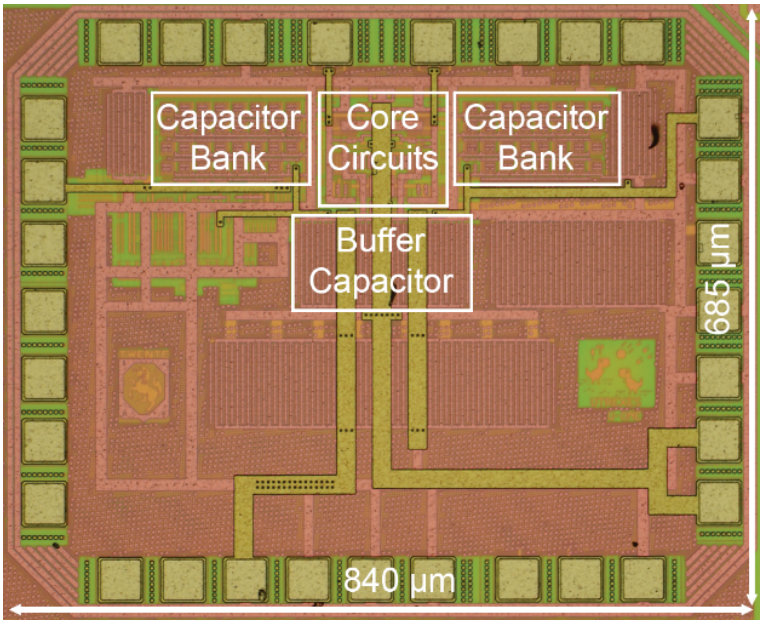


Figure 4.12. Chip photo.

Figure 4.13 shows the measured start-up transient for the 32 MHz crystal in a 2x1.6 mm package. At $t = 0$, the oscillator enable signal is triggered, and after a brief comparator calibration time of approximately 130ns energy injection starts. After the programmed 400 drive cycles, the oscillator quickly settles to its steady state.

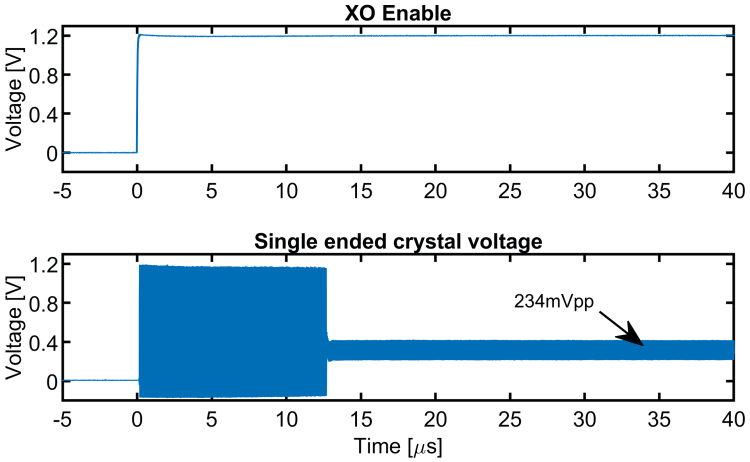
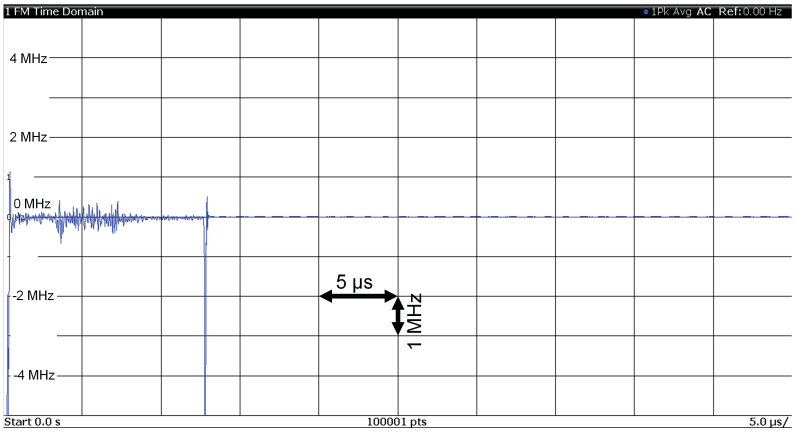


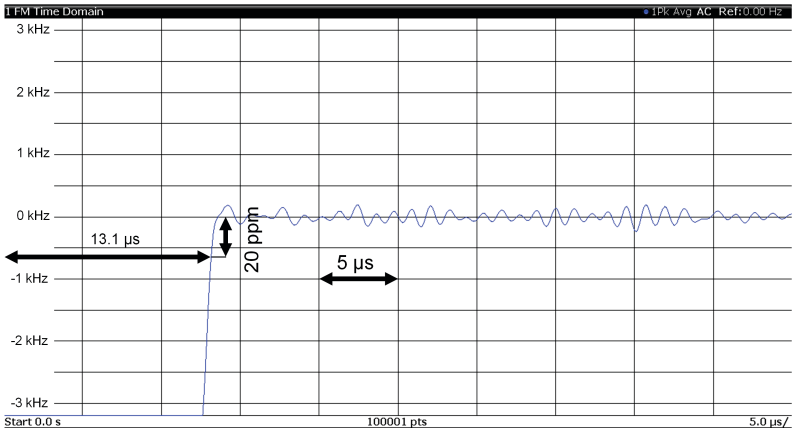
Figure 4.13. Measured single-ended output for a 32 MHz crystal, injecting for 400 cycles at T = 20 °C.

Figure 4.14.(a) shows the measured frequency settling, showing frequency variations around the fundamental frequency due to comparator noise during injection. Nevertheless, the frequency converges towards the crystal frequency as the amplitude grows. As with any injection technique, slight frequency variations are visible after switching to steady-state, caused by excitation of the crystal spurious tones during injection. Assuming that a PLL would normally filter out these spurs, the frequency settling of the fundamental tone can be measured by choosing the center frequency and demodulation bandwidth such that the spurious tones fall out of band. This measurement is shown in Figure 4.14.(b), showing quick settling to a frequency error of less than 20 ppm.

Figure 4.15 shows the measured performance as a function of the number of programmed drive cycles for a few crystals, showing increased amplitude and improved phase noise, at a cost of increased energy consumption. Crystals in larger packages generally have a lower L_m [2], but a larger C_p. A lower L_m implies a larger slope $d\hat{I}_m(t)/dt$, and the required injection time to reach a given steady-state motional current $\hat{I}_{m.SS}$ scales proportional with L_m [48]. Larger crystals, therefore, require a shorter injection time compared to smaller crystals, thereby reducing start-up time. On the other hand, the increased C_p implies a larger energy consumption per injection cycle. To reach an equal output amplitude, however, the overall start-up energy is lower due to the reduced injection time. Since a fixed delay is used for the generation of the stepwise charging pulses, the effective phase shift of the injection waveform is larger for higher frequency crystals. Hence, the growth in amplitude drops off faster for the 50 MHz crystal, while the amplitude growth of the 24 MHz crystal is closer to linear.



(a)



(b)

Figure 4.14. Measured frequency settling for a 32 MHz crystal, for 400 drive cycles at T = 20 °C. (a) Coarse frequency scale. (b) Fine frequency scale.

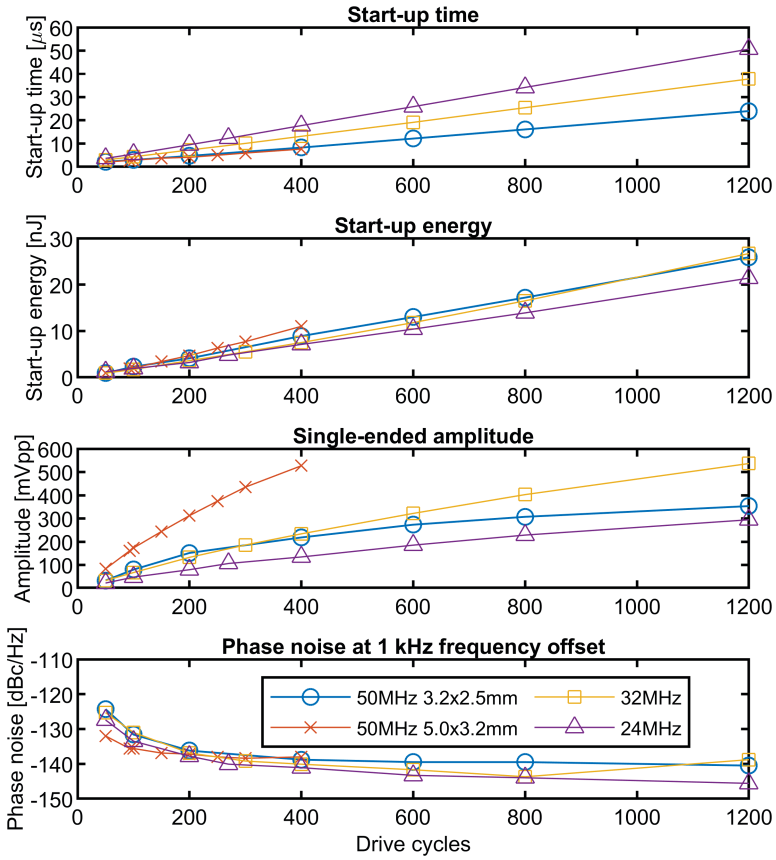


Figure 4.15. Measured start-up time and energy as well as steady-state amplitude and phase noise against number of drive cycles at 20 °C.

Figure 4.16 shows the measured start-up time and energy over temperature variations, where the settings are kept constant, except for the data points at 60 °C and higher, for which the switch resistance setting is lowered to achieve a reliable start-up.

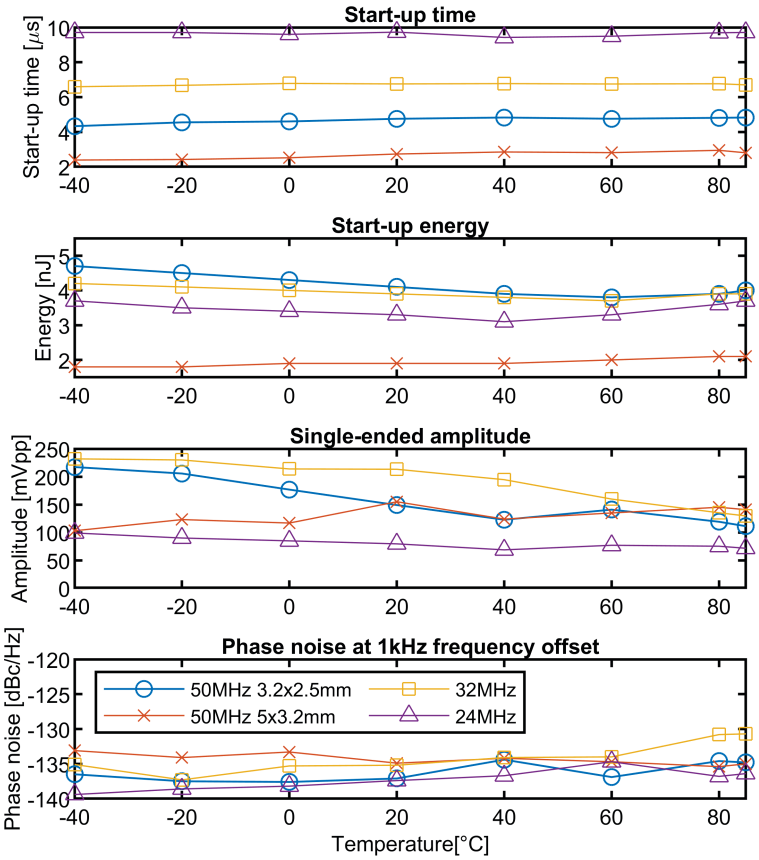


Figure 4.16. Measured start-up time and energy as well as steady-state amplitude and phase noise over temperature, for an injection time of 200 cycles (93 for the 50 MHz 5x3.2 mm crystal).

The measured energy breakdown is listed in Table 4.3, where E_{bridge} is the energy consumed by the bridge, and E_{aux} comprises the energy consumption by all other blocks (start-up circuitry, RO, enable logic, etc.). The number of drive cycles was set to 400 to allow comparison to the simulation results in Table 4.2. To demonstrate robustness over samples, four different dies were tested using identical settings, except for the number of drive cycles, which was set to 200. Table 4.4 lists the measured performance, showing a marginal variation between samples. The spread originates mostly from the steady-state settling time. To demonstrate robustness against RO frequency, performance is measured over RO bias current as shown in Figure 4.17.

Table 4.3. Measured energy breakdown for different crystals for 400 drive cycles.

Crystal (MHz)	$E_{start-up}$ (nJ)	E_{bridge} (nJ)	E_{aux} (nJ)
24	4.1	3.5	0.6
32	7.1	5.3	1.8
50	7.5	5.5	2.0

Table 4.4. Performance over samples for a 32 MHz crystal for 200 drive cycles.

Sample	T_{start} (µs)	$E_{start-up}$ (nJ)	Single-ended amplitude (mVpp)	Phase noise @ 1kHz (dBc/Hz)
1	7.0	3.6	128	-139.5
2	7.2	3.5	133	-139.9
3	7.1	3.6	129	-139.4
4	7.0	3.7	125	-139.4

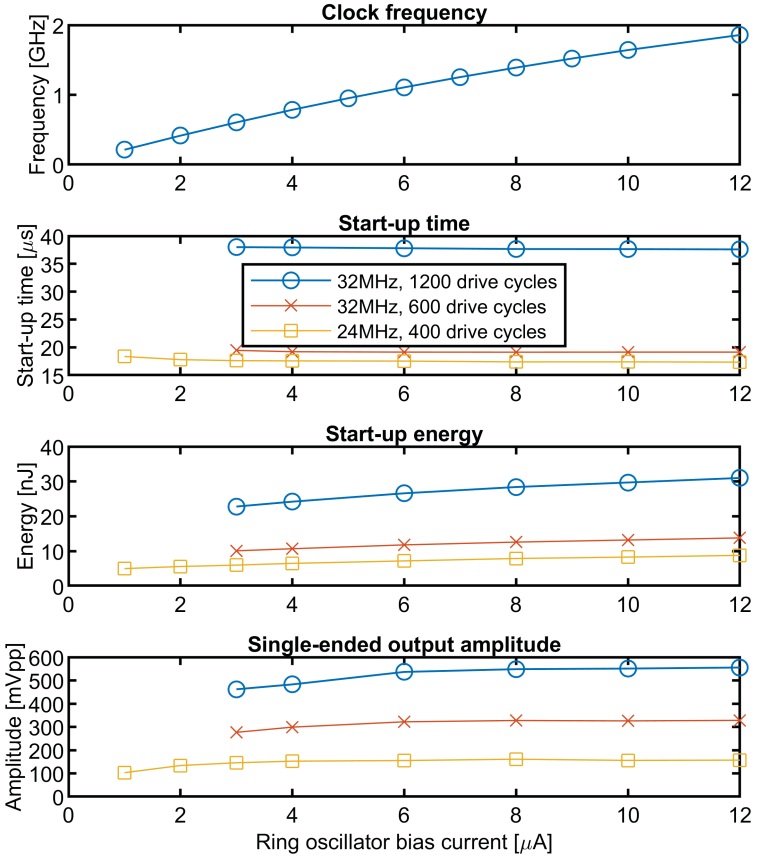


Figure 4.17. Measured performance against ring oscillator bias current at 20 °C.

4.5 Comparison

A fair comparison between different start-up techniques is difficult since the start-up energy is dependent on the number of drive cycles, which in turn depends on the steady-state swing, L_m, C_L and injection amplitude. To enable fair comparison with the state-of-the-art, the prototype was tested using the same crystal as in [48], [50] (50 MHz). [50] used a 7 pF C_L compared to 9 pF in [48], which resulted in a $\frac{9}{7}$ times higher steady-state amplitude compared to [19], while start-up was not affected since C_L is disconnected during start-up. In this Chapter, we used the same C_L and output amplitude as Chapter 3 ([50]) in the measurements on the 50 MHz 5x3.2 mm crystal. Although the chip in this Chapter uses 65nm technology, with a 1.5x higher supply voltage than in Chapter 3([50]), which used 22nm technology, start-up is more than 2x faster and requires almost 2x less energy.

Table 4.5 compares the proposed work with the state-of-the-art. Figure 4.18 compares the start-up time and energy of crystal oscillators having low start-up time (<1000 cycles) and energy (<100 nJ). The measurement results from the chip presented in this Chapter are among the lowest start-up times, for the lowest energy consumption.

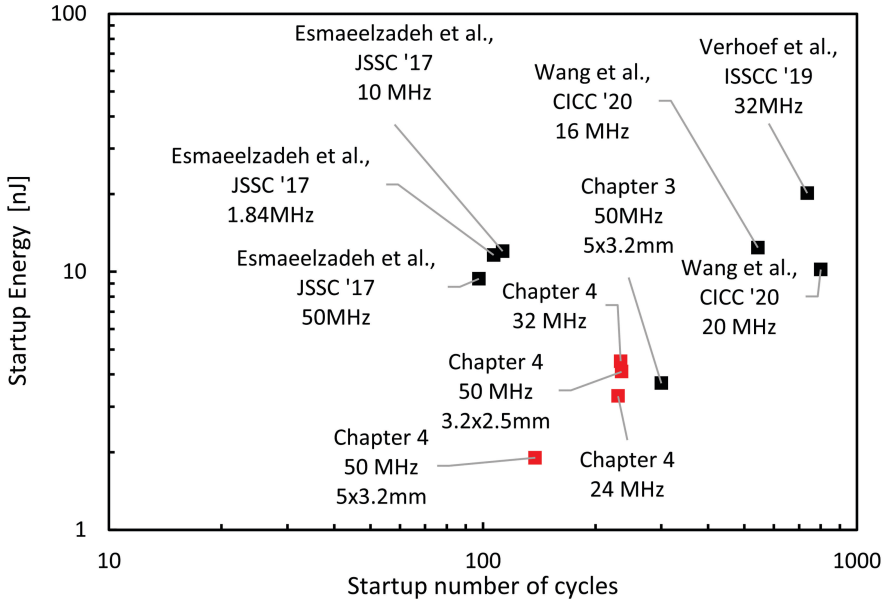


Figure 4.18. Start-up energy versus start-up time of the state-of-the-art.

Table 4.5. Comparison with prior art.

	JSSC' 19 [46]	ISSCC' 19 [45]	JSSC' 18 [48]	ESSCIRC' 19 [24]	CICC' 20 [21]	Chapter 3	Chapter 4			
CMOS process (nm)	65	55	65	65	65	22 FD-SOI	65			
Supply voltage (V)	1.0	1.2	1	1.2	1.2	0.8	1.15	1.2	1.2	1.2
Active area (mm^2)	0.07	0.05	0.09	0.006	0.046	0.02	0.07			
Frequency (MHz)	54	32	50	16	20	50	24	32	50	50
Package size (mm)	N/A	N/A	5.0x3.2	N/A	N/A	5.0x3.2	3.2x2.5	2.0x1.6	3.2x2.5	5.0x3.2
Load capacitance (pF)	6	6	9	8	4	7	12	6	8	7
Differential steady-state amplitude (Vpp)	0.7	0.75	0.25	0.6	N/A	0.32	0.16	0.26	0.30	0.32
Steady-state power consumption (µW)	198	N/A	195	70	169	51	19	70	36	32
Phase noise at 1 kHz offset (dBc/Hz)	-139.5	N/A	N/A	N/A	-146.6 @ 10kHz	-123	-137.4	-136.9	-136.2	-135.5
Start-up time (µs)	19	23	1.95	150	30	6	9.7	7.2	4.7	2.8
Temperature range (°C)	-40–85	-40–140	-40–85	N/A	-20–100	-40–85	-40–85			
Start-up time variation over temperature	±1%	±11%	10%	N/A	N/A	23%	3.1%	2.8%	10.3%	18.9%
Start-up time (cycles)	1026	736	98	2400	600	300	233	230	235	138
Start-up Energy (nJ)	35‡	20	9.4	10.5	11.1	3.7	3.3	3.6	4.1	1.9
Technique	2-step energy injection	Synchronized energy injection	Precisely timed injection	Negative resistance boost (NRB)	NRB + DPW injection	Self-timed injection	Self-timed injection + stepwise charging			

‡ *Including clock buffer power*

4.6 Conclusion

This chapter presented several techniques to reduce the start-up energy of crystal oscillators using energy injection. By using the concept of stepwise charging, the energy consumption associated with (dis)charging the capacitive load is reduced. Additionally, the self-timed energy injection technique is improved by the use of a discrete-time, dynamic-bias comparator. This reduces energy consumption and injection delay, and allows a simple offset calibration scheme to be applied. Furthermore, the self-timed control logic with dynamic switch resistance relaxes the speed-accuracy trade-off. Together, these techniques enable energy-efficient generation of the injection signal in self-timed injection. The manufactured proof-of-concept achieves state-of-the-art performance, starting up in just 2.8 µs for only 1.9 nJ.

Chapter 5

Discussion

This chapter provides additional insight into the design space of (self-timed) injection circuits as well as insights toward a fair comparison of crystal oscillator start-up circuits.

Chapters 3 and 4 presented novel techniques to quickly start up crystal oscillators for low energy consumption. While these two chips achieve state-of-the-art performance, they are general proofs of concepts, which can be further optimized for an application. Therefore, it is useful to reflect on how the different design elements affect start-up time and energy, and how they can be optimized for the intended application, which can have widely varying requirements regarding crystal type, IC process, phase noise requirements, and start-up time and energy.

Some design elements are specific for self-timed injection, such as the comparator and bridge implementations. Section 5.1 reflects upon these design considerations and the realizations from Chapters 3 and 4, which provides additional insight into the design space of self-timed injection circuits.

On the other hand, design parameters such as the crystal parameters, supply voltage, and steady-state amplitude are usually set at a system level (considering a crystal oscillator with its start-up circuitry as a system). Section 5.2 reflects on these system-level parameters. These considerations are not limited to self-timed injection but apply to energy injection systems in general.

To make a fair comparison, the chips in Chapters 3 and 4 were (partially) tested with identical crystals and parameters. Comparison among different publications, however, is difficult due to the due to the vastly different parameters and conditions, as mentioned in Section 2.4. Section 5.3 aims towards a (more) fair comparison between the different ways to start up crystal oscillators that were described in Sections 2.2 and 2.3, as well as the techniques proposed in Chapters

3 and 4, by using the insights from Sections 5.1 and 5.2. Finally, this chapter is wrapped up by a conclusion in Section 5.4.

5.1 Implementation of self-timed injection circuits

Chapters 3 and 4 covered the implementation of two self-timed injection circuits, showing quick start-up and low energy consumption. This is achieved by starting up in as few cycles as possible while minimizing the amount of energy spent in each individual injection cycle.

To minimize the number of injection cycles, the growth rate of the motional current must be maximized, for which the generation of a precise injection signal is key. As discussed in Chapters 3 and 4, phase shift and delays in the self-timed injection circuit affect the amplitude and phase of the injection waveform, which in turn affects the growth rate of I_m. On the other hand, the amount of energy spent in each cycle can be minimized by reducing the energy spent driving the crystal, as well as minimizing the energy spent in control circuits.

Subsection 5.1.1 elaborates on phase shift and effective injection amplitude affect the growth rate of I_m, and provides an overview of where errors originate. Sections 5.1.2 and 5.1.3 in turn show how these errors can be mitigated, and reflect on the energy consumption.

5.1.1 Phase shift and injection amplitude in self-timed injection

Consider an ideal injection waveform, which is in phase with the motional current and immediately switches polarity between $\pm V_{DD}$ at each zero-crossing of $I_m(t)$. This results in a theoretical rate of growth of the motional current of $A/2L_m$, where A is $4V_{DD}/\pi$ for a square wave.

In open-loop energy injection, any phase error in the injection waveform accumulates, since there is no feedback from the crystal. As the phase error accumulates, the growth rate reduces, and can even become negative, as shown in Figure 2.13.

In self-timed injection, however, each cycle is used as feedback, which prevents the accumulation of phase shifts. Nevertheless, a phase shift between the motional current and the injection waveform still exists, as discussed in Sections 3.3 and 4.4. This, together with a reduction of the effective injection amplitude A, reduces the growth rate $I_m(t)$ compared to the theoretical maximum. This increases the required injection time, which not only increases start-up time but also increases start-up energy consumption.

To understand how phase shift affects the rate of growth, it is instructive to observe the difference between an ideally timed single injection cycle compared to a phase-shifted injection cycle, as shown in Figure 5.1. This figure shows $I_m(t)$ for a certain (non-zero) initial condition. This is the case after an 'initial kick', but also holds for each subsequent injection cycle.

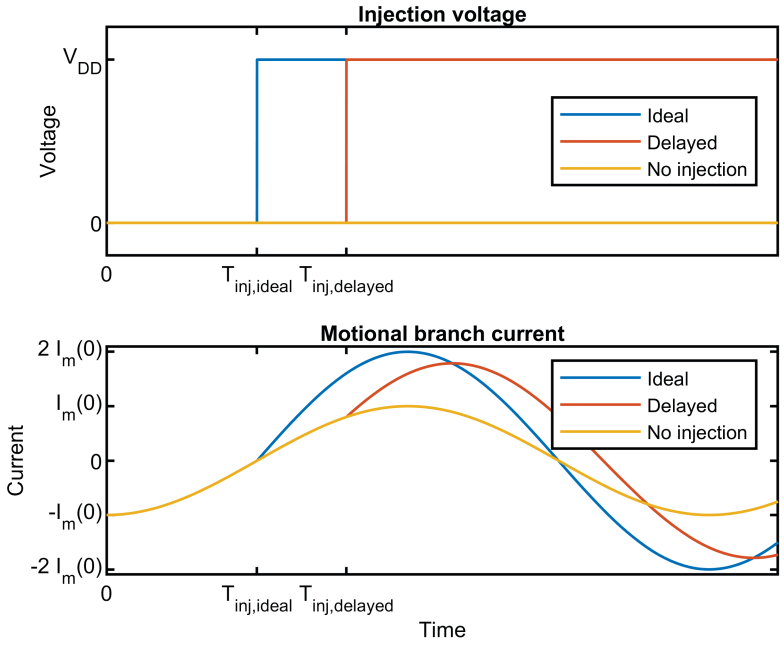


Figure 5.1. Simulated phase shift of the motional current as a result of phase shift in injection waveform.

A voltage step is applied at different moments in time. Firstly, it is applied at the time of zero crossing of I_m, as would be the case with ideal injection ($I_{m,ideal}$). This results in a motional current that remains in phase with the initial motional current, but at a higher amplitude. Secondly, a voltage step is applied with some delay (or phase shift), resulting in $I_{m,delayed}$. Compared to the 'ideal injection' case, the amplitude after the injection cycle has grown, but not as much as in the ideal case. Furthermore, the phase has shifted, as can be observed by the shifted zero-crossing after injection.

Figure 5.2 shows a flow chart of the simplified self-timed injection process. The loop describes the basic self-timed injection cycle. Starting from a certain current I_m, a switch current I_{sw} is sensed. This current is converted to the voltage V_{sw} over the switch resistance, which is fed as an input to the comparator, which in turn

takes a decision Q_{comp} whenever a zero-crossing is detected. This triggers the toggling of the bridge, to apply an injection voltage V_{inj} to the crystal, that – if all works well – increases the motional current amplitude $\hat{I}_m$, after which the process is repeated.

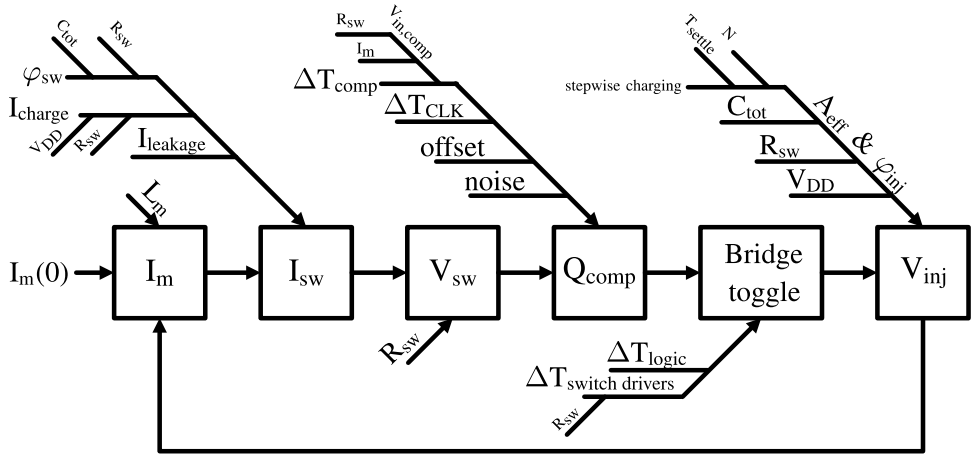


Figure 5.2. Flowchart of the (simplified) injection cycle, with factors that affect injection phase-shift and/or amplitude.

Figure 5.2 also shows the (most important) factors that influence the injection timing and/or injection amplitude, thereby affecting the injection amplitude and/or phase. The entire cycle can be explained as follows:

The initial current $I_m(0)$, the injection voltage V_{inj}, together with the motional inductance L_m yields a motional current I_m. For the conversion from I_m to I_{sw}, the phase shift (depending on C_{tot} and R_{sw}) and I_{charge} influence I_{sw}, as discussed in Section 3.3.1. Furthermore, the bridge switch leakage $I_{leakage}$ affects the phase shift, as will be discussed in Section 5.1.2.

The conversion from I_{sw} to V_{sw} only depends on the switch resistance R_{sw}. Parasitic capacitances are taken into account in C_{tot}, and any inductance is negligible due to the short on-chip trace lengths.

The comparator's decision Q_{comp} depends on the decision speed of the comparator. One of the factors that influences this is the propagation delay ΔT_{comp}, which depends on the comparator input voltage, which in turn depends on I_m and R_{sw}. In case of a clocked comparator, the delay between the zero-crossing of the comparator input and the next clock edge, ΔT_{CLK}, is also a factor

for the comparator decision. Furthermore, both offset and noise can cause an early or late decision, affecting phase shift.

The delay in the toggling of the bridge is affected by the propagation delays of the logic (ΔT_{logic}) and switch drivers ($\Delta T_{switch\ drivers}$). Finally, the effective amplitude A_{eff} and phase φ_{inj} of V_{inj} are dependent on the supply voltage V_{DD}, R_{sw}, C_{tot} as well as the stepwise charging sequence, which depends on the number of steps N and settling time per step T_{settle}.

Not all parameters are independent of each other. For example, C_{tot} affects both the injection waveform and the switch current phase and R_{sw} even affects almost all of the steps in the injection process.

A few of these parameters are (more-or-less) fixed system-level specifications, such as the supply voltage V_{DD} and the crystal parameters L_m and C_p (which governs C_{tot}), and will be discussed in Section 5.2. The other parameters can be chosen by the designer of a self-timed injection system and will be discussed in the next subsections.

5.1.2 Bridge design

The goal of the bridge is to apply the injection voltage over the crystal. In its simplest form – the basic self-timed injection concept in Figure 3.2 - the bridge consists of just 4 switches. The switches to ground have a low resistance, and have a minimal influence on the design. On the other hand, there is only one pair of switches towards the supply in the self-timed injection concept, but as shown in Chapters 3 and 4, the number of switches is increased to implement 'fast charging' and/or stepwise charging in practical realizations.

The implementation and sizing of these switches affect the injection amplitude and phase. Firstly, the bridge switches affect the detection delay between the zero crossings of I_m and the zero- crossings of I_{sw} that the comparator detects. Secondly, when the bridge toggles, the bridge design affects the shape of the injection waveform, through the switch topology and sizing, the stepwise charging sequence, and total capacitance C_{tot}.

Detection delay

Due to the bridge, the zero-crossings of the comparator input voltage are delayed compared to the zero-crossings of I_m. As analyzed in Section 3.3.1, this detection delay stems from the (residual) charging current through the bridge switches, as well as the phase shift in the motional branch current due to R_{sw} and C_{tot}. Even if the circuit is otherwise ideal, this phase shift causes a detection delay between the

ideal and realized (change in) V_{inj} towards $\pm V_{DD}$, and reduces the growth of I_m, as shown in Figure 5.1. In the next subsections, the analysis is further discussed and extended with a switch leakage term.

Charging current

As analyzed in Section 3.3.1, the (residual) charging current delays the detected zero-crossing. This analysis assumes a fixed switch resistance, which poses a trade-off between detection sensitivity and charging current. Note that this is a 'large signal' effect, due to the voltage step that is applied. Quickly charging to V_{DD}, and only selecting the high-R switch afterward breaks this trade-off, as implemented in Section 3.4.1. This also helps to maximize the injection amplitude as will be discussed later. Nevertheless, a residual charging current remains, since full settling is not achieved.

Leakage

The off-state leakage of the bridge switches is another factor that influences the time difference between the zero crossings of I_m and I_{sw}. This can be understood by extending the model in Figure 3.4 with the (large) switches to ground, as well as the switches to the intermediate voltages (in case of step-wise charging) in off-state, as shown in Figure 5.3.a.

The voltage over these switches is approximately constant before the desired detection moment, as V_X has settled to approximately V_{DD}, while the ground and the intermediate voltages are constant. This means that - at a given temperature - the leakage current just before the decision moment is approximately constant. The leakage current contributions of each switch can therefore be added, resulting in the model shown in Figure 5.3.b.

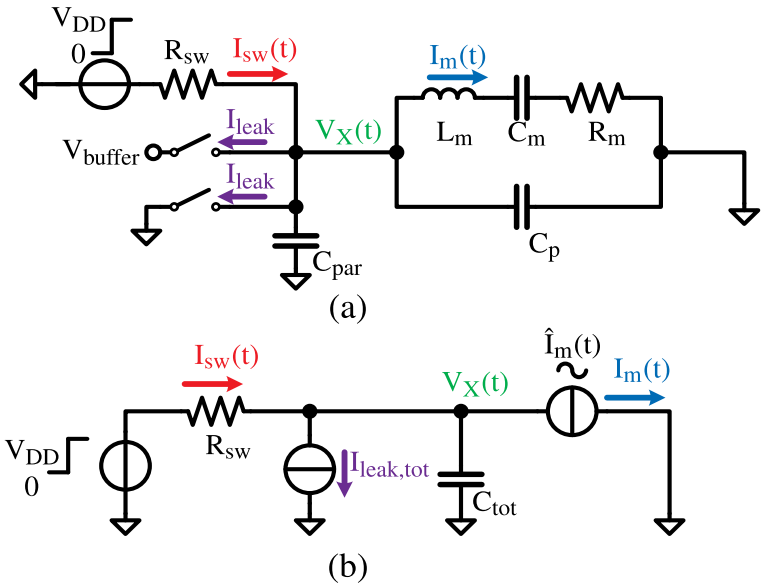


Figure 5.3. (a) Single-side model. (b) Leakage model.

The total leakage current $I_{leak,tot}$ adds an additional (approximately constant) term to Equation (3.4). Following the same procedure as discussed in 3.3.2, this term can be taken to the right-hand side in Equation (3.6), from which it becomes clear that the effect is similar to comparator offset, resulting in a delayed decision moment.

The switch leakage current can be decreased by increasing the length L of the MOSFET switches, as was applied in both proposed prototypes. Extending the switch length should be done with care since the width of the switches needs to be increased as well to keep the on-resistance constant. This increases the switch area ($W \cdot L$), which not only increases the gate capacitance and hence drive power but also increases the parasitic drain capacitance. This capacitance adds to the capacitance at the crystal nodes, adding to C_{tot}, and hence influencing the decision moment as well, as analyzed in Section 3.3.1. Hence, leakage puts an upper limit on the switch size, both through switch width and length.

Motional branch current

Another cause of detection delay is the phase shift φ_{sw} due to the RC filter that is formed by the switch resistance R_{sw} in combination with the capacitive loading C_{tot}, as analyzed in Section 3.3.1. Note that, as opposed to the charging current, the filtering effect is rather a small-signal effect. Both effects show as separate terms in Equation (3.4). Minimizing the parasitic capacitance helps to minimize the

phase shift due to 'filtering'. However, it can never be completely eliminated since the crystal C_p is always part of C_{tot}. On the other hand, reducing R_{sw} helps to minimize phase shift, but a relatively high R_{sw} is required to retain comparator sensitivity.

Similar to the charging current, the trade-off can be alleviated by using a dynamic (variable) switch resistance as implemented in Chapter 4, allowing effective growth in the first cycles, albeit not at the maximum rate. After the first few cycles, the effect of RC filtering is reduced by switching to a lower resistance, which increases the motional current growth rate.

Injection waveform

Once the decision to toggle the bridge is made, the bridge applies a waveform V_{inj} over the crystal. The waveform depends on how the bridge is implemented, but its shape, amplitude, and phase have a direct influence on the rate of growth of I_m. To show how the shape of the waveform itself affects both the injection amplitude and phase, Figure 5.4 shows the ideal $I_m(t)$ for ideal and practical waveforms, for a single injection cycle. The 'ideal' injection waveform is a square wave, shown as V_{ideal}. The basic concept of self-timed injection with a fixed resistance to charge and detect I_m is shown is shown as V_{RC}. Also shown is the waveform using 'fast charging', V_{fast}, as implemented in Chapter 3. Figure 5.4 also shows the conceptual stepwise charging waveforms for 2- and 4-step charging (as discussed in Section 4.2.2) as V_{2-step} and V_{4-step}, respectively.

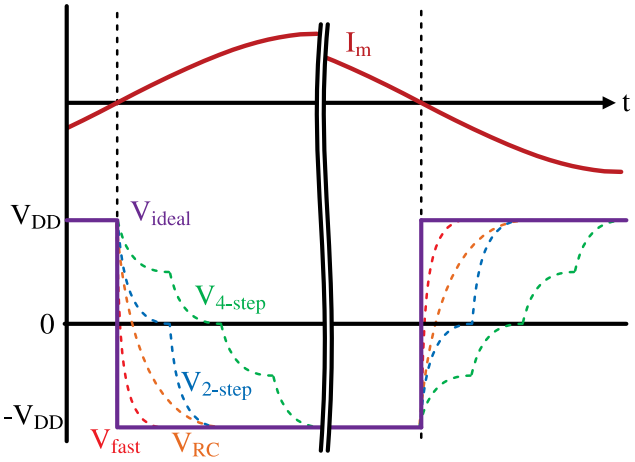


Figure 5.4. Injection waveforms for different charging methods.

The effective amplitude of the injection waveform A_{eff} can be calculated using the Fourier transform. However, by visual inspection, it already becomes clear that the energy in the practical waveforms is lower than the ideal square wave, as the area under the waveform is lower than in V_{ideal}. Furthermore, by observing the zero-crossings, it becomes clear that the phase of the practical injection waveforms is shifted with respect to $I_m(t)$.

Fast charging

The trade-off between a low resistance for injection amplitude maximization and high resistance for detection sensitivity can be alleviated by 'fast charging', shown as V_{fast}. This quickly brings the voltage over the crystal to either $+V_{DD}$ or $-V_{DD}$. If this is done fast enough ($t_{charge} \ll \frac{1}{f_{crystal}}$), the crystal voltage resembles the 'ideal' injection waveform. This was implemented in two different ways, described in Sections 3.4.1 and 4.3.3.

In Chapter 3 a relatively large, self-quenching NMOS switch, is used. This solution is simple but has the disadvantage that once the crystal voltage goes toward V_{DD}, the effective resistance lowering drops. In Chapter 4, charging the crystal nodes was done as part of the step-wise sequence. The delay line that generates the step-wise charging steps is used to quickly charge up to V_{DD} before selecting a higher resistance for detection. This approach is more complex, but easily integrated as part of step-wise charging.

In both cases, the trade-off is alleviated, but the switch resistances cannot be made arbitrarily low to eliminate it. Decreasing the switch on-resistance by increasing the switch width W causes a proportional increase in switch drive power, as the switch gate area increases with W. However, the switch driver power is only a small portion of the total power consumption in the realizations, as shown in Table 4.2. Rather, for the implementation in Chapter 4, the limitations in parasitic capacitance and off-state leakage that affect the detection delay (as discussed earlier) constrain the switch sizing.

Stepwise charging

Stepwise charging can be used to decrease the energy associated with driving the capacitive load. In theory, the number of steps N can be increased to infinity to reduce the energy needed for charging the capacitive load. However, the stepwise charging sequence takes time, which reduces the effective injection amplitude and introduces phase shift, as shown in Figure 5.4. Note that this is the case despite starting the step-wise charging cycle at the 'ideal' point of time; the phase shift originates from the time required to reach $\pm V_{DD}$.

The injection waveform phase shift increases, and the effective injection amplitude decreases when the entire stepwise charging sequence takes more time. The duration of the step-wise charging sequence depends on the number of steps N, as well as the duration of each step, T_{settle}. If the steps could be made arbitrarily short, N could be increased to save more energy, and the injection waveform would resemble the ideal one. However, the switch resistance cannot be made arbitrarily low due to switch leakage and the required switch driver power.

With a non-zero switch resistance, some time T_{settle} is required to settle toward each of the (intermediate) voltage levels. This not only affects the injection amplitude. The duration of each individual step also determines (together with R_{switch} and the (effective) capacitance C_{tot}) how closely the crystal voltage settles towards the intermediate voltage levels, which impacts the efficiency of stepwise charging. Allowing a very large time to settle allows the largest energy saving *per cycle*, but decreases the rate of growth of I_m, such that the overall start-up time and hence energy can become larger. This forms a compromise between step-wise charging effectiveness and maximizing the effective injection waveform amplitude.

In the realization in Chapter 4, T_{settle} is designed to be roughly 2-4 times the time constant of each charging step, $\tau = R_{stepwise}C_{eff}$, where $R_{stepwise}$ is defined as the resistance of the switches that perform the stepwise charging steps. This varies between 2-4, depending on the crystal that is used, since C_{eff} depends on the crystal parameters. Nevertheless, the crystal nodes settle to at least 85% of their final value at each stepwise charging step, such that the impact on step-wise charging effectiveness is marginal.

The selection of the number of steps N goes hand-in-hand with the design of the stepwise charging sequence. Furthermore, the overhead in the generation of the switch timing costs an increasing amount of time to go through the charging steps and increases switch driver power. Furthermore, this adds more switches, which adds to the parasitic capacitance and leakage, and the requires more capacitors to store the N intermediate voltages, adding to the circuit area.

For large N, the energy reduction is outweighed by the increased overhead and reduced growth rate of the motional current. Through simulation, 4-step charging was determined as optimum in terms of start-up energy consumption for the realization in Chapter 4. It should be noted, however, that simulations showed that 2-step charging achieved lower start-up times, for a significantly lower area consumption, but at higher energy consumption. It is expected that for more

advanced technology nodes (note that Chapter 4 was realized in 65nm CMOS) that offer better switches, this trade-off shifts towards higher N.

The phase shift due to the step-wise charging cycle could be compensated by setting the decision moment slightly 'early', ideally by a fixed time offset. Deciding before the actual event, however, is rather difficult to achieve because it requires a non-causal system. Instead, it could be triggered before the zero crossing of I_m, at a negative value. This can be achieved using a 'negative' comparator offset, as used in Chapter 3, but rather in a controlled fashion instead of the 'negative offset' being a result of PVT variations.

5.1.3 Comparator and logic

Another key element in self-timed injection is the 'digital' circuitry, consisting of the comparator, logic, and switch drivers.

Comparator noise

The comparator is designed such that the influence on the detection of I_m from its (input referred) noise is negligible, as discussed in Chapter 3. However, the continuous-time comparator consumes a large amount of power to achieve this. The use of a dynamic comparator is more energy-efficient, as was shown in Chapter 4. Nevertheless, the start-up circuitry - to which comparator energy consumption is one of the main contributors - remains a significant contribution to the overall start-up energy, as shown in Table 4.2.

The comparator noise specifications are relaxed as the motional current grows. This means that comparator energy consumption could be further reduced. This can be achieved by switching over to a secondary, low(er) performance comparator. Alternatively, a single comparator can be adapted in situ. Using the dynamic comparator that is used in Chapter 4 this can, for example, be achieved by switching to lower tail- and drain capacitances after the initial start-up cycles. This sacrifices noise performance (and increases speed), but energy is saved by decreasing the amount of charge that is dumped and replenished at each clock cycle.

Comparator offset

A further cause of phase shift is comparator offset, as discussed in Section 3.3.2. Comparator (voltage) offset effectively manifests as a current-referred offset in I_m, through R_{sw}, causing an early or late decision as explained in Section 3.3.2. While this can be solved by selecting a large R_{sw}, this has multiple drawbacks, as discussed in the section on bridge design. Instead, the comparator should be designed for a suitably low offset.

The comparator used in Chapter 3 required large transistors to achieve this, which negatively impacted speed and power consumption. Any residual offset was used advantageously to create a 'negative' delay that (partially) compensated delays from other sources. However, this solution is not very robust, since the offset varies over PVT. This was improved in Chapter 4, where the trade-off between energy, speed, and offset is de-coupled by calibrating the comparator, for a negligible energy and speed penalty. This allows a negligible delay due to comparator offset.

Comparator delay

Another factor that influences overall delay is the delay of the comparator, meaning the delay between a zero-crossing at the input of the comparator to the time that the comparator output toggles. In the case of a time-continuous measurement of the switch current, as done in Chapter 3, this is purely the comparator propagation delay. In the discrete-time implementation in Chapter 4, this is the comparator clock-to-Q delay, but also the clocking; the decision is only made *next* clock cycle after the zero-crossing (assuming no offset and memory effects). In the realization in Chapter 4, however, the clock speed is high enough that this effect is negligible.

It is worth noting that the comparator propagation delay is amplitude-dependent since a larger input voltage usually leads to a faster decision. Since the dV_{in}/dt at and around the comparator decision moment is larger when $\hat{I}_m$ is larger, the overall phase shift becomes smaller as I_m builds up. In the measurements of Chapters 3 and 4, this shows as the injection frequency not being constant over T_{inj}, with the deviation reducing as $\hat{I}_m$ grows.

Logic and switch driver propagation delay

Apart from comparator delay, the logic and switch drivers also introduce delay. There is also a dependency on switch size, since larger switches may need a larger fan-out of the switch drivers than smaller switches. Since the power consumption is small compared to the overall power consumption, they can be optimized for speed. In Chapter 4 this was achieved by minimizing the delay in the path from comparator output to the bridge switches, by both minimizing the number of gates in the critical path and applying an appropriate fan-out throughout the logic path. Furthermore, technology scaling is advantageous for both energy consumption and speed.

5.2 System-level trade-offs

Assuming that a crystal oscillator system consists of (at least) a steady-state oscillator and a start-up mechanism, several parameters affect the design of such a system. Among these parameters are the supply voltage, crystal selection, and steady-state amplitude. These trade-offs affect the steady-state oscillator but also have a direct influence on the start-up time and energy.

The next subsections will cover these parameters, showing how they affect the start-up time and energy of crystal oscillators. This does not only provide insight into the design of self-timed injection circuits, but these trade-offs apply to energy injection techniques in general, which will serve to compare different energy injection techniques in Section 5.3.

To compare different influences, a distinction is made between different energy consumption contributions. The total energy consumption can be split up in three factors. Firstly, the energy to drive the capacitive load $E_{capactive}$. Secondly, the overhead energy $E_{overhead}$, which is applicable for energy injection systems in general, but in the case of self-timed injection comprises the comparator, control logic, delay line, et cetera. Finally, the main objective of energy injection; the energy that is stored in the crystal $E_{crystal}$.

5.2.1 Supply voltage

The supply voltage has a great effect on the performance of start-up circuits. The supply voltage can be lowered to reduce power consumption, but this reduction can also be a necessity for reliability in more advanced (scaled) technology nodes since core transistors in these nodes normally have a lower maximum supply voltage. A reduced supply affects energy injection circuits in multiple ways.

Firstly, the injection amplitude is reduced, and the injection time has to be increased since $T_{inj} = \frac{\pi L_m}{2V_{DD}} \hat{I}_{m,SS}$. This not only increases start-up time but also requires more cycles of driving the crystal. Since most of the energy consumption stems from driving the crystal load, as discussed in Section 4.1, this would increase the overall energy consumption. However, the losses *per cycle* actually *decrease* quadratically with decreasing supply voltage, since CV_{DD}^2/N is reduced, as discussed in Section 4.2.1. To calculate the overall effect, the total number of charge and discharge cycles during start-up can be defined as $M = 2 \cdot T_{inj} \cdot f_{crystal}$. The total energy spent driving the capacitive load is M times the loss per cycle, resulting in:

$$E_{capacitive} = M \cdot \frac{CV_{DD}^2}{N} \tag{5.1}$$

Substituting $M = 2 \cdot T_{inj} \cdot f_{crystal}$ and $T_{inj} = \frac{\pi L_m}{2V_{DD}} \hat{I}_{m,SS}$ yields:

$$E_{capacitive} = \frac{\pi L_m \hat{I}_{m,SS} \cdot f_{crystal} \cdot C \cdot V_{DD}}{N} \tag{5.2}$$

This shows that the overall energy consumption for driving the capacitive load scales proportionally with V_{DD}. Hence, lowering the supply voltage can be an effective way to reduce start-up energy consumption, albeit at the cost of an increased start-up time. Note that this only takes start-up into account, and assumes that steady-state performance is not affected by the supply voltage change.

Apart from the energy from driving the load, the power consumption of digital circuits, such as the control logic and switch drivers reduces by reducing the supply voltage. However, their speed also reduces, such that additional measures are required, which can cost extra power consumption. For example, in self-timed energy injection, the 'initial kick' at the beginning of start-up, calculated as $\hat{I}_m(0) = V_{DD}\sqrt{C_m/L_m}$, is reduced. This initial motional current has to be detectable, meaning that the requirements on the comparator noise and offset become tougher as the supply voltage decreases. This means that more current has to be spent on the comparator. In practice, however, this contribution to overall energy consumption is usually relatively small.

5.2.2 Crystal parameters

As evident from measurement results in Chapters 3 and 4, the choice of the crystal can greatly affect start-up time and energy. This is due to the wide range of crystals parameters, in frequency, L_m, C_m, C_p and C_L. The selection of a crystal type depends on many factors, such as cost, physical size, requirements in phase noise, frequency stability, and shock and vibration resistance, many of which fall outside the scope of this thesis. Crystal oscillator start-up time and energy can be significant factors in the selection of a crystal. This subsection aims to give insight into these crystal parameters and how they affect start-up time and energy as this becomes increasingly important in practical applications.

Motional resistance

The motional resistance R_m affects the crystals' Q-factor, which is important for phase noise and energy consumption in steady-state. However, it is of little importance during start-up, since the motional resistance is usually high enough

not to limit the growth of I_m [45], [63], nor burn a significant energy amount of energy in R_m during start-up.

Motional inductance and capacitance

The crystal resonant frequency is determined by the physical thickness of the crystal blank. With the thickness set by the desired frequency, the motional capacitance (and shunt capacitance) are proportional to the electrode area, while the motional inductance (and resistance) are inversely proportional to the electrode area [64]–[66]. Intuitively, this can be understood by impedance scaling. Consider a crystal with a certain C_m, L_m, R_m and C_p. Putting 2 of these crystals in parallel results in 2x higher motional capacitance and parallel capacitance, but 2x lower motional inductance and resistance.

Smaller crystals can fit in a smaller package. When cut for the same frequency, smaller crystals have a higher motional inductance and lower motional capacitance. While crystals with small blanks could be fitted to larger packages, in general, there is an inverse correlation between package size and motional inductance. To illustrate this, the author performed measurements on three different 50 MHz crystals in various package sizes using a Keysight E5061B Network Analyzer. The results are listed in Table 5.1, confirming the trend that crystals in smaller packages have a higher motional inductance.

Table 5.1. 50 MHz crystal parameters against package size.

Crystal series	**TXC 8Y**	**TXC 7M**	**Abracon ABM3**
Package size [mm]	2.0x1.6	3.2x2.5	5.0x3.2
$\boldsymbol{L_m}$ **[mH]**	3.30	2.00	1.07
$\boldsymbol{C_m}$ **[fF]**	3.07	5.07	9.47

An increased motional inductance has several effects when applied to self-timed energy injection. Firstly, it reduces the initial current that scales with $\sqrt{C_m/L_m}$, as was discussed in Section 3.3.1. This toughens the requirements on comparator offset and noise. Secondly, an increase in motional inductance leads to a decrease in C_p, as explained earlier. However, since C_L is normally much larger than C_p, most of the motional current flows into C_L, such that (for a given $\hat{I}_{m,SS}$) any change in C_p does not lead to a significant change in output voltage amplitude. However, due to the increase in L_m, the injection time needs to be increased to achieve an equal steady-state amplitude, since $T_{inj} = \frac{2L_m}{A}\hat{I}_{m,SS}$. This shows a proportional increase in injection time with motional inductance, which directly affects start-up time and energy.

The energy required to drive the capacitive load, $E_{capacitive}$, scales proportionally with L_m as shown in Equation (5.6), since a longer injection time requires more cycles to drive the (capacitive) load. Furthermore, with a longer on-time of the controlling circuitry (e.g. comparator and control logic), it also leads to higher overhead energy consumption $E_{overhead}$, which can be calculated as:

$$E_{overhead} = P_{on} T_{inj} \tag{5.3}$$

Where P_{on} is the (average) power consumption of the control circuitry. Substituting $T_{inj} = \frac{2L_m}{A} \hat{I}_{m,SS}$ results in:

$$E_{overhead} = P_{on} \frac{2L_m}{A} \hat{I}_{m,SS} \tag{5.4}$$

Another consequence of a larger L_m is that the energy stored in the crystal $E_{crystal}$ becomes larger (assuming the steady-state amplitude remains equal) since it can be calculated as:

$$E_{crystal} = \frac{1}{2} L_m \hat{I}_{m,SS}{}^2 \tag{5.5}$$

All contributions to the overall energy consumption above scale linearly with L_m. Hence, a small L_m is desirable to minimize start-up time and energy, which favors large crystals in large packages. However, crystals in larger packages have larger parasitics and parallel capacitance, as will be discussed later.

Alternatively, crystals of different materials than the usual quartz, such as langasite, could be used. These crystals can have a lower motional inductance, but also a much lower Q-factor [67].

Parallel capacitance

An important factor that influences start-up time and energy is C_p. Similar to L_m and C_m, C_p is largely determined by the parallel plate capacitor that is formed by the crystal electrodes, and hence scales with package size. A further contribution to C_p is the package (parasitic) capacitance.

When using energy injection to start up the oscillator, the repeated (dis)charging of C_p contributes to energy consumption, as it forms a differential load capacitance, as discussed in Section 4.2. Crystals with a smaller physical size have a smaller C_p, which is beneficial, and step-wise charging helps to reduce the energy consumption driving this (differential) load, as demonstrated in Chapter 4.

A further (second-order) effect that affects the injection waveform timing is the phase-shift of the detected voltage due to C_p, as was discussed in Section 5.1.1.

Proper selection of R_{sw} reduces this effect, and dynamic switch resistance minimizes this after the first few injection cycles.

For minimum start-up time and energy, a small C_p is favorable, which can be achieved by selecting a crystal in a small package. However, the increased L_m that comes with the smaller package can easily offset this advantage, as evident from the start-up time and energy measurements on the 50 MHz crystals in Chapter 4.

Load capacitance
The load capacitance C_L also affects start-up time and energy. While C_L is not a *physical* property of the crystal, it is part of the crystal specifications. The crystal is trimmed to achieve a specified frequency for a specified external capacitance C_L. This means that two crystals of the same frequency can have similar values for L_m and C_m, but be trimmed for a different C_L. Fine-tuning of C_L allows trimming of the resonance frequency, where crystals with a large C_L are more robust to variations in capacitance, but have a lower tuning range. The crystal selection usually comes from system-level requirements and falls outside the scope of this thesis.

From the perspective of start-up time and energy, however - all else being equal - an increase in C_L requires a proportional increase in $\hat{I}_{m,SS}$ to obtain an equal output swing, as shown in Equation (5.1). The increased $\hat{I}_{m,SS}$ requires a longer injection time and hence increases start-up time and energy. If these crystals have the same $\hat{I}_{m,SS}$, the start-up energy is the same, but in steady-state, the output voltage amplitude is different due to the different C_L, as was discussed in Section 5.1.3.

If C_L would be connected to the circuit during start-up, this would compromise energy consumption and toughens the requirements on switch resistance and comparator specifications, as discussed in Section 3.3. C_L is disconnected during startup in the chips presented in this thesis.

5.2.3 Steady-state amplitude

Another factor that allows for design freedom is the steady-state amplitude of the crystal oscillator. On a system level, the injection time is not a specification or requirement but rather follows from the phase noise performance in steady-state, which sets the requirements on the steady-state amplitude $\hat{V}_{out,SS}$. A large steady-state amplitude is desirable to obtain low phase-noise, since a larger amplitude increases the signal-to-noise ratio [15], [68]. A larger steady-state (voltage) amplitude requires a larger motional current amplitude, which in turn requires a longer injection time. Hence, as observed in measurements over various T_{inj} in

Chapters 3 and 4, as well as other work [45], the steady-state amplitude has a large impact on start-up time and energy.

Another consideration is the loading of the crystal oscillator. Many applications require a rail-to-rail clock signal, for example, to drive mixer switches or clock digital circuitry. Amplification of the crystal oscillator output is required to achieve this. The lower the crystal output amplitude, the more amplification is required, with its associated added noise and power consumption. This suggests that a high crystal oscillator output amplitude is desirable. However, the oscillation amplitude should be low enough to avoid excessive aging of the crystal resonator [15] and low enough to avoid non-linear effects that detriment performance [12], apart from the increased start-up time and energy consumption.

While the selection of steady-state amplitude lies outside the scope of this thesis as it greatly depends on system specifications, this subsection aims to give insight into the trade-offs between start-up time and start-up energy against steady-state amplitude.

In steady-state, the output voltage $\hat{V}_{out,SS}$ of the crystal oscillator is determined by $\hat{I}_{m,SS}$ which is converted to a voltage through C_L in parallel with C_p. Considering that C_L in steady-state is usually much larger than C_p, the output voltage amplitude approximately equals:

$$\hat{V}_{out,SS} \approx \frac{\hat{I}_{m,SS}}{\omega C_L} \tag{5.6}$$

Assuming that a certain crystal is chosen, ω and C_L are fixed through the crystal properties. The remaining degree of freedom to vary the output amplitude is then $\hat{I}_{m,SS}$.

Energy injection puts energy into the series branch of the crystal to inject up to the required steady-state current swing, where the current ideally equals:

$$\hat{I}_{m,SS} = \frac{A}{2L_m} T_{inj} \tag{5.7}$$

Equation (5.1) shows a linear relationship between $\hat{I}_{m,SS}$ and T_{inj}. The energy in the crystal $E_{crystal}$ can then be calculated using Equation (5.5). This energy is delivered by the supply. In an ideal case, all energy that is delivered by the supply is stored in the crystal, such that the start-up energy consumption grows quadratically with steady-state amplitude (and injection time).

However, the energy that is spent in overhead, such as comparator and logic power consumption, driving the capacitive load, etcetera scales *linearly* with T_{inj}, and

hence $\hat{I}_{m,SS}$. The total energy consumption is the sum of the energy in the crystal and all other sources; the first scales quadratically with T_{inj}, the latter linearly with T_{inj}. Therefore, the relation between energy consumption and output amplitude is actually somewhere between linear and quadratic.

Figure 5.5 shows the calculated contributions from crystal energy and overhead energy over the number of drive cycles, for the chip from Chapter 4. This shows linearly increasing overhead losses, while the crystal energy does not increase quadratically because $\hat{I}_{m,SS}$ does not grow linear with T_{inj} due to the (amplitude-dependent) phase shift between I_m and V_{inj}. This non-ideality complicates the analysis above.

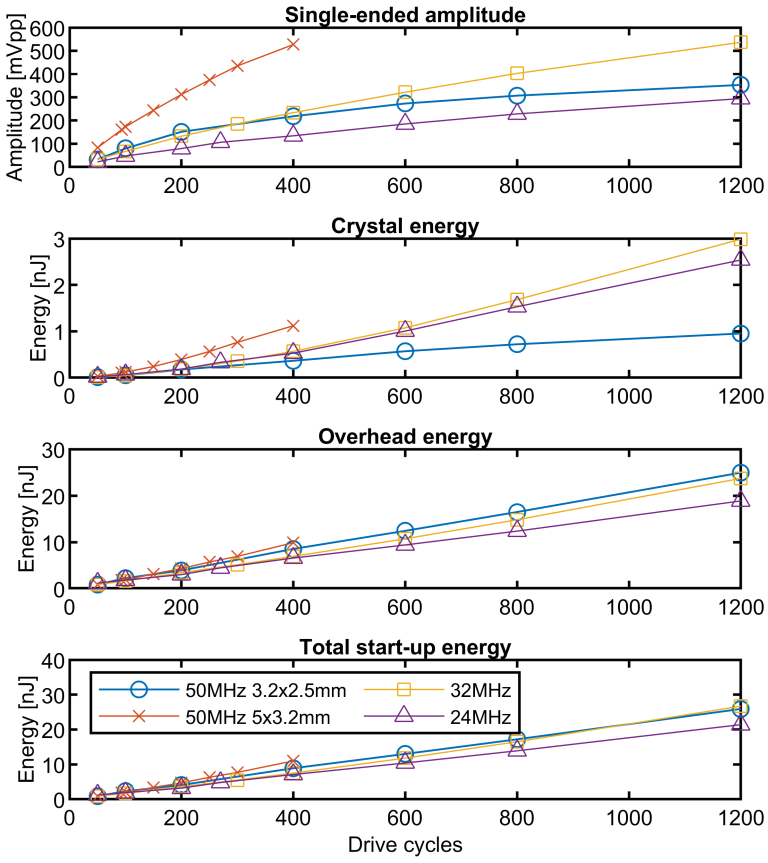


Figure 5.5. Calculated crystal energy and overhead energy for the chip presented in Chapter 4.

Figure 5.6 shows the measured energy consumption as a function of measured output amplitude. This figure shows a rapid increase in energy consumption. For each of the measurements, a 2nd order polynomial fit is made, of which the equations are shown in the legend. For the 3.2x2.5 mm 50 MHz crystal, the fit is rather poor, which can be attributed to the saturation in amplitude (as was shown in Figure 5.5) causing a disproportional increase in energy consumption to achieve larger steady-state amplitudes. The dashed line shows the fitted polynomial without the last 3 data points. The fitted equations show a quadratic and a linear term, partly due to the crystal energy growing quadratically amplitude, and partly due to the non-linear growth of amplitude against drive cycles, which causes a 'more than linear' energy consumption.

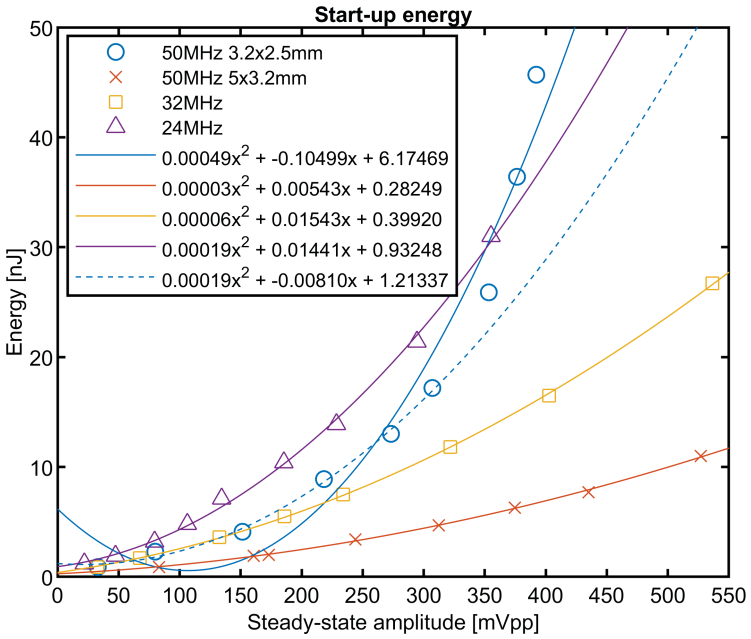


Figure 5.6. Start-up energy consumption as a function of achieved steady-state amplitude.

5.2.4 Design parameter sensitivity

Table 5.2 lists the dependence of various circuit parameters as discussed in the previous subsections on start-up time and start-up energy. For start-up time it is assumed that the overall start-up time is dominated by the injection time T_{inj}. The energy is split up in firstly; the energy to drive the capacitive load, secondly; the energy that is stored in the crystal itself, and lastly; the overhead energy, consisting of start-up circuitry.

Note that this overview assumes that T_{inj} is adjusted for the change, and all other boundary conditions remain equal, such as frequency, output amplitude, et cetera. For example, for an increase in C_L, $I_{m,ss}$ has to increase to keep the output amplitude constant, which in turn requires an increase in T_{inj}. This means that the energy to drive the capacitive loading also increases, even though C_L is not connected during start-up.

Table 5.2. Influence of design parameters.

	Start-up time	Start-up energy		
Parameter	T_{inj}	**Capacitive load**	**Crystal**	**Overhead**
Supply voltage (V_{DD})	$\propto \frac{1}{V_{DD}}$	$\propto V_{DD}$	$\equiv$	$\propto \frac{1}{V_{DD}}^{\ddagger}$
Motional inductance (L_m)	$\propto L_m$	$\propto L_m$	$\propto L_m$	$\propto L_m$
Parallel capacitance (C_p)	$\cong^{*}$	$\propto C_p^{\S}$	$\equiv$	$\cong^{\dagger}$
Load capacitance (C_L)	$\propto C_L$	$\propto C_L^{\S}$	$\propto C_L^2$	$\propto C_L$
Steady-state amplitude ($\hat{V}_{out,SS}$)	$\propto \hat{V}_{out,SS}$	$\propto \hat{V}_{out,SS}$	$\propto \hat{V}_{out,SS}^2$	$\propto \hat{V}_{out,SS}$

[*] Dependence is a second-order effect. Remains approximately equal.

[†] Assuming that T_{inj} remains equal.

[‡] Assuming that only T_{inj} changes. Not considering power consumption change of logic, comparator, etc.

[§] Assuming that C_L is disconnected during start-up.

As discussed in the previous subsections, these dependencies are much more complex in practical implementations, requiring circuit simulations and/or measurements to design and verify a self-timed injection circuit. Nevertheless, this overview can serve as a guideline in design.

5.3 Comparison between techniques

The chips in Chapters 3 and 4 were (partially) tested with identical crystals and parameters, allowing a fair comparison between these chips. However, as briefly discussed in Section 2.4, the vastly different parameters and conditions among different publications make a fair comparison hard to make.

This section aims to provide insight towards a comparison between different ways to start up crystal oscillators, as described in Sections 2.2 and 2.3, as well as the techniques proposed in Chapters 3 and 4, using the insight of the previous section on influence on start-up time and energy.

5.3.1 Supply voltage

The selection for the optimum supply voltage is a compromise between start-up time and start-up energy. The optimum depends on the requirements on start-up time and energy, technology, and crystal.

For energy injection methods, the largest part of the energy consumption are the losses associated with the capacitive load, as was shown in Chapter 4. As discussed in Section 5.2.1, these losses scale approximately linearly with the supply V_{DD}. It is therefore instructive to compare $E_{start-up}$ against V_{DD} for different publications, as shown in Figure 5.7.

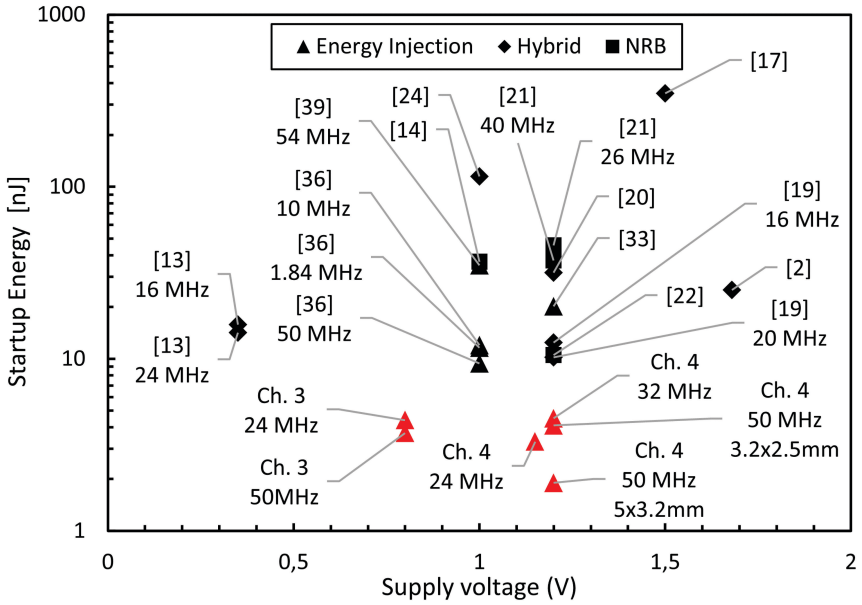


Figure 5.7. Start-up energy against supply voltage.

Although there is a general trend that lower energy consumption is achieved with lower supply voltages, there is insufficient data to draw hard conclusions. Not only do the other circuit parameters greatly vary; different crystals are used and the steady-state amplitude is neglected in this figure.

5.3.2 Steady-state amplitude & crystal parameters

The previous subsection showed that supply voltage for the state-of-the-art can vary, but generally is in the same order of magnitude (around 1V). Parameters that vary much more are the steady-state amplitude, as well as crystal parameters, which can have a variation of a factor over 5x between different publications.

An important parameter in determining the steady-state amplitude is the crystal load capacitance. Similar crystals, but trimmed for different load capacitances, achieve similar motional current amplitude for identical injection times. However, the steady-state voltage amplitude is different due to the difference in load capacitance, as was discussed in Section 5.2.3, such that comparing steady-state *voltage* amplitude is not fair.

A fairer comparison could be comparing steady-state *current*, which is irrespective of C_L. However, this is not easily achieved. Firstly, I_m is not directly measurable. Secondly, the achieved current for a given injection time depends greatly on L_m, which makes the comparison among different crystals difficult. Lastly, comparing $I_{m,SS}$ does not give a fair comparison in terms of start-up energy, as was discussed in Section 5.2.3.

Figure 5.8 shows start-up energy against the achieved steady-state amplitude. The trend for a larger start-up energy consumption for a larger steady-state swing is clear. However, the differences in crystal parameters, especially C_L and L_m are not visible in this figure. Crystals with a larger load capacitance or motional inductance require more energy to achieve the same output swing as crystals with smaller values.

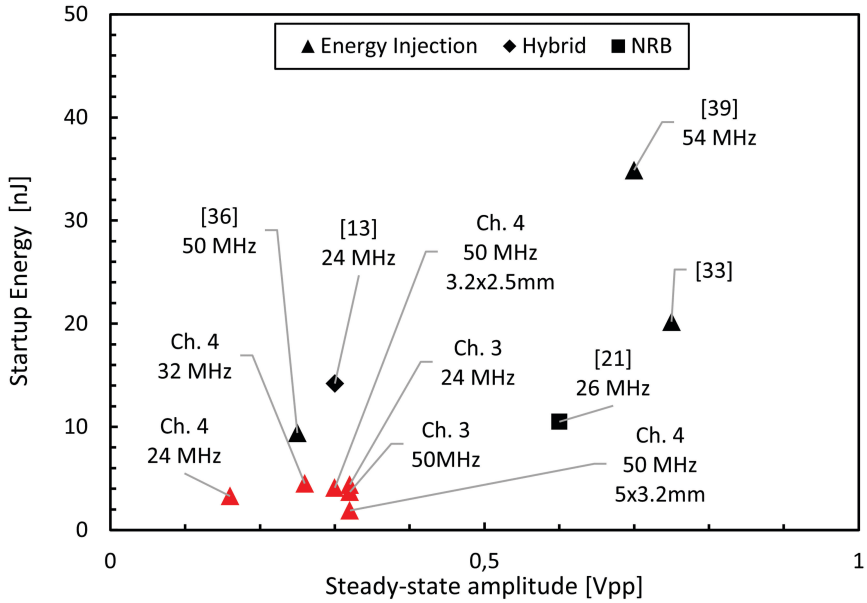


Figure 5.8. Start-up energy against steady-state amplitude. The results from Chapters 3 and 4 of this thesis are marked Ch. 3 and Ch. 4 respectively.

These crystal parameters, or even crystal type, are often not shown in papers. A fair comparison is only possible when the same crystals *and* similar conditions (steady-state amplitude) are used. For a few works, sufficient data was available to make a more detailed comparison to the realizations of Chapters 3 and 4.

Table 5.3 lists measurements on a 24 MHz crystal with the same part number as in [13], and for a comparable amplitude. The chip from Chapter 3 achieves a similar amplitude but a much lower start-up time & energy. In the results from Chapter 4, the correct load capacitance was used (12 pF as opposed to 6 pF). Since this results in a $\frac{6}{12}$ times lower steady-state amplitude compared to the other entries, the data for *half* the output amplitude was used.

Table 5.3. Comparison of [13] and the chips from Chapters 3 and 4.

	Lei et al. JSSC '18 [13]	**Chapter 3**	**Chapter 4**
Supply voltage (V)	0.5	0.8	1.15
Load capacitance (pF)	6	6	12
Amplitude (mV_{pp})	300	320	160
Start-up time (µs)	400	15	9.7
Start-up energy (nJ)	14	4.4	3.3

Table 5.4 shows measured data from the chip of Chapter 4, using the same 32 MHz crystal type as Verhoef et al. [45]. Since [45] also shows results over a range of drive cycles, a comparison can be made for different amplitudes. It is clear that the work from Chapter 4 requires more cycles of driving the crystal to achieve a certain amplitude, yet the start-up time is similar. This is partially due to the regular interruption of the injection cycle to synchronize the injection source in [45], and partially because frequency settling after injection is quicker in the work from Chapter 4. Despite the larger number of drive cycles, the work from Chapter 4 is more energy efficient due to the application of stepwise charging, as well as the full disconnection of C_L, whereas in [45] a minimum C_L of 9 pF (single-ended) is always connected.

Table 5.4. Comparison of [45] and the chip from Chapter 4.

	Verhoef et al. ISSCC '19 [45]		**Chapter 4**	
Supply voltage (V)	1.2		1.2	
Amplitude [mV_{pp}]	750	260	750	260
Drive cycles	290	≈100	731	196
Injection time [µs]	9.1	≈3.1	22.8	6.1
Start-up time [µs]	23	N/A	23.3	7.2
Start-up energy [nJ]	20.2	≈8	14.9	3.3

Table 5.5 compares results for identical 50 MHz crystals. As discussed in Section 4.5, the output amplitude was adapted for the difference in C_{Load} compared to Esmaeelzadeh et al. [48] to enable a fair comparison. It is clear that the work from Chapter 4 requires a longer time to start up, but is still more energy efficient.

Table 5.5. Comparison of [48] and the chips from Chapters 3 and 4.

	Esmaeelzadeh et al. JSSC '18 [48]	**Chapter 3**	**Chapter 4**
Supply voltage (V)	1	0.8	1.2
Load capacitance (pF)	9	7	7
Amplitude (mV_{pp})	0.25	0.32	0.32
Start-up time [µs]	1.95	6	2.8
Start-up energy [nJ]	9.4	3.7	1.9

Figure 5.9 shows a graphical overview of the work, using equal crystals and comparable conditions, as discussed in this section.

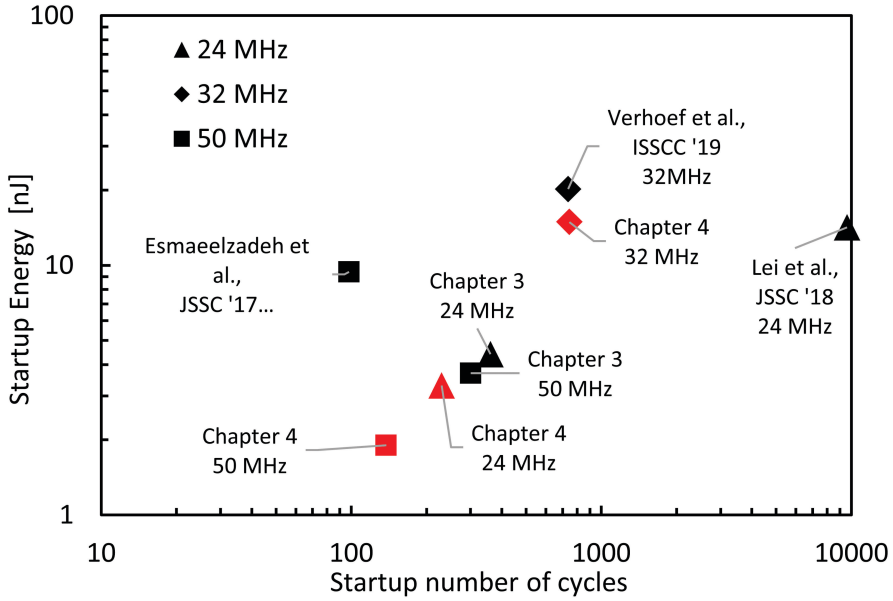


Figure 5.9 Comparison using equal crystals and comparable conditions.

5.3.3 Efficiency

In search for a fair metric that removes the dependency from circuit-level parameters such as the supply voltage or crystal parameters, the idea grew to assess the quality of the different circuits by their energy efficiency. Assuming that the crystal oscillation has completely stopped before start-up, there is no energy stored in the crystal. On the other hand, the circuit stores an amount of energy $E_{crystal} = \frac{1}{2} L_m \hat{I}_{m,ss}^2$ in steady-state, as shown in Equation (2.8). This is the absolute minimum energy that needs to be put in the system, as this energy has to be injected by the start-up circuitry. In practical circuits, however, the start-up energy is larger, as additional energy is spent in driving the crystal and generating the injection waveform.

Then, we can define the start-up efficiency as the ratio of energy in the crystal against the total energy spent for start-up:

$$\mu_{start-up} = \frac{E_{crystal}}{E_{start-up}} \cdot 100\% \tag{5.8}$$

Where $E_{crystal}$ is the energy stored in the crystal, and $E_{start-up}$ is the total start-up energy. This allows a comparison of the achieved start-up energy relative to the (theoretical) minimum start-up energy.

It is easy to determine the (peak) motional current $\hat{I}_m$ in order to calculate the energy stored in the crystal in simulation. In measurements, however, the crystal motional current cannot be measured directly. Still, the crystal energy can be calculated using the crystal parameters and output voltage amplitude.

Figure 5.10 shows the calculated crystal energy and efficiency from measurements of the chip that was proposed in Chapter 4. The achieved efficiency is highly dependent on the crystal that is used. Also, longer injection times result in higher efficiency. If the crystal amplitude would be linear with the number of drive cycles, the crystal energy would grow quadratically. However, due to the 'saturation' of the output amplitude with a large number of drive cycles, the crystal energy grows only (approximately) linearly. For larger numbers of drive cycles, the efficiency saturates, towards a value that strongly depends on the crystal. On the other hand, for small numbers of drive cycles and hence amplitude, the crystal energy goes towards zero, while the start-up circuitry itself, as well as driving the capacitive load still costs energy, such that the efficiency drops towards zero.

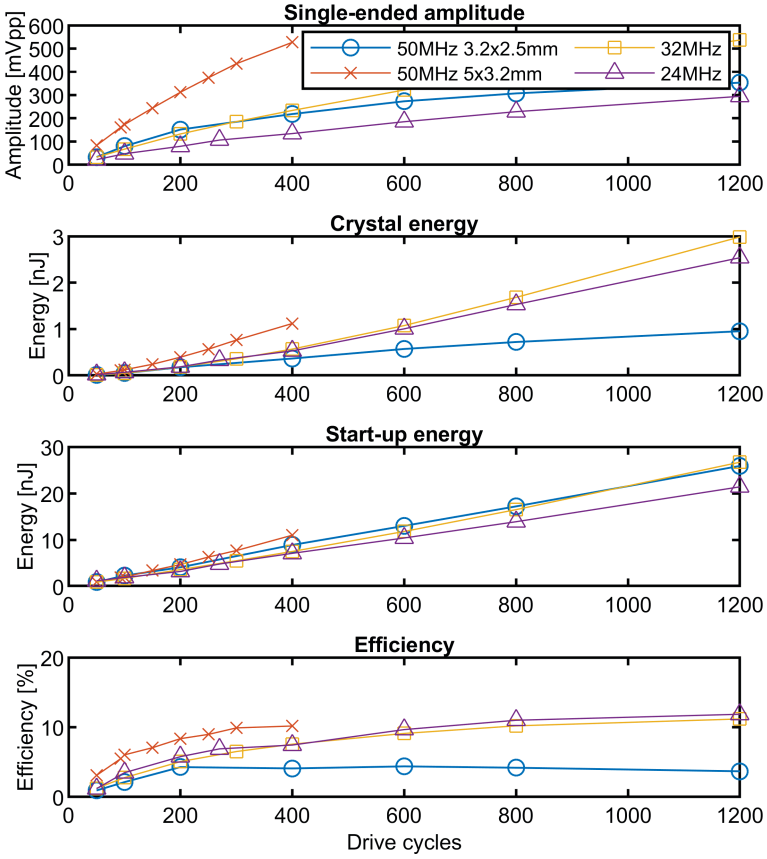


Figure 5.10. Calculated crystal energy and efficiency for the chip presented in Chapter 4.

In literature, there is not always sufficient information to calculate this, as the crystal parameters and/or output amplitude are not always reported. Table 5.6 lists the calculated efficiency for recent work in crystal oscillator start-up techniques, for those where sufficient information is available. Note that, for the results from this thesis, the table lists the efficiency for a (differential) output amplitude of 320 mVpp. In reality, the efficiency varies over drive cycles and hence output amplitude, as was shown in Figure 5.10.

Table 5.6. Calculated efficiency.

	[24]	[13]	[19]	[26]	[45]	[46]	[48]	Ch.3†	Ch.4†
Start-up time (µs)	150	400	158	18	23	19	1.95	6	2.8
Crystal energy (nJ)	2.66	0.15	1.95	2.82	0.96	1.51	0.13	0.1	0.1
Start-up energy (nJ)	10.5	14.2	349	115	20.2	34.9	9	3.7	1.9
Efficiency (%)	25	1.1	0.56	2.5	4.8	4.3	1.5	2.8	5.5
Technique	NRB	Hybrid	Hybrid	Hybrid	E.I.	E.I.	E.I.	E.I.	E.I.

† 50 MHz, 5x3.2 MM CRYSTAL

The pure NRB technique in [24] achieves remarkably high efficiency. This can partly be attributed to the relatively high motional inductance, which means that for a given motional current and hence output amplitude, a relatively large amount of energy is stored in the crystal. Furthermore, [24] appears to calculate the start-up energy by multiplying steady-state power consumption with the start-up time, which likely results in an under-estimation of start-up energy, and hence over-estimation of efficiency, as crossbar currents through the inverter stages are larger during start-up than in steady-state, since the PMOS and NMOS are never completely off for small swings. This last observation likely also explains the low efficiency of the Hybrid energy injection techniques. Interestingly, the hybrid techniques show a lower efficiency than Energy Injection techniques.

Efficiency as a metric has clear limitations. The efficiency is not necessarily constant for a given technique, neither in theory, as was discussed in Section 5.2.3, nor in practice, as shown in Figure 5.10. Nevertheless, it provides insight into how much (or little) energy actually is actually 'useful', and shows that improvement is possible.

5.4 Conclusion

This chapter provided insight into the design considerations for energy injection systems in general, as well as a comparison between different implementations.

Section 5.1 reflected on the specific design considerations and limitations of self-timed injection, with a focus on one of the main challenges in energy injection; the generation of an accurate injection waveform. The injection amplitude and phase depend on several non-idealities and design variables, which stem from the main elements; the bridge and the comparator together with the control logic, for which the design considerations were elaborated.

On a broader perspective, Section 5.2 covered the influence of supply voltage, crystal selection, and steady-state amplitude on start-up time and energy are

covered. These insights on system-level parameters are applicable for self-timed injection systems, but also energy injection in general.

Based on this knowledge, Section 5.3 discussed and compared different implementations by their supply voltage and steady-state amplitude. Furthermore, the start-up efficiency is introduced as a metric to compare crystal oscillator start-up circuits. These comparisons show that, with the broad variation in boundary conditions, it is difficult to fairly assess different techniques and realizations. This shows that for a fair comparison, equal crystals and test conditions should be used.

Chapter 6

Conclusion

This chapter summarizes this thesis and provides perspectives for future work.

6.1 Summary and conclusions

Chapter 1 introduced the research goal by showing the necessity for quick and energy-efficient start-up of crystal oscillators in energy-efficient (wireless) communication systems.

Chapter 2 provided an overview of current start-up techniques. Firstly, the fundamentals of crystal oscillators were covered. This includes modelling of the crystal as well as the negative-resistance based active circuits that sustain but conventionally also start up the oscillation, where the start-up is normally rather slow.

This chapter also covered recent advances in crystal oscillator start-up, which not only lowers their start-up time but - more importantly - also their start-up energy. The different techniques are classified into two distinct techniques; negative-resistance based circuits and energy injection based circuits. Negative-resistance-boosting (NRB) based circuits increase negative resistance by either increasing the transconductance, altering the load capacitance, and/or canceling the crystal parallel capacitance. While especially canceling the crystal parallel capacitance can theoretically result in extremely low start-up times, it cannot be achieved in practice due to limitations in supply voltage and robustness against PVT variations.

On the other hand, in energy injection techniques the crystal is energized from an auxiliary injection source. This enables rapid start-up, provided that the injection waveform is in-phase with the crystal oscillation during the entire injection duration. This poses very strict requirements on the injection source since its frequency needs to be accurate over the entire PVT range. Furthermore, a

significant amount of energy is required to drive the capacitive load that the crystal poses.

A comparison of realized circuits shows that energy injection systems start up faster than NRB circuits. In terms of energy consumption, however, they are on par with the best NRB and hybrid circuits, which combine EI and NRB techniques. The comparison also shows that a one-to-one comparison of start-up energy does not make for a truly fair comparison due to significant differences in steady-state amplitude.

Chapter 3 introduced a new method to generate the injection signal to solve the requirement for an accurate injection source. Instead of relying on an auxiliary injection source, the injection timing is generated from the crystal oscillation itself, thereby realizing 'self-timed' injection.

The basic concept of self-timed injection relies on (indirect) measurement of the crystal motional current, and switching the injection voltage at its zero-crossings. An H-bridge applies the supply voltage over the crystal in either the positive or negative polarity. By feeding the voltage over the bridge switches to a comparator, the direction of the current flowing into the crystal is detected, which approximates the crystal motional current, provided that the switch resistance is sufficiently low. The comparator output then drives, via combinatory logic, the H-bridge switches to repeatedly alternate the polarity of the voltage over the crystal. This realizes energy injection, similar to the techniques shown in Chapter 2, but instead of deriving the injection timing from an 'open loop' auxiliary source, the timing is derived from the crystal itself.

Chapter 3 also discussed the design of self-timed injection circuits, as well as the design space for the switch resistance and comparator offset. Furthermore, a prototype implementation is discussed, in which the comparator offset is minimized, and by detecting the sign of the comparator offset any residual offset is used advantageously. Circuit simulations and measurements on the fabricated prototype show robustness against crystal type and PVT and show state-of-the-art performance in terms of start-up time and energy consumption.

Chapter 4 described the application of step-wise charging to injection circuits to reduce the main source of energy consumption in energy injection circuits; (dis)charging the capacitive load. Instead of dumping the energy that is stored in the crystal parallel capacitance every time it is discharged, a part of this energy is stored and re-used by step-wise charging. This reduces the amount of charge that

the power supply has to deliver in each cycle, thereby reducing overall start-up energy.

A model for the capacitive load was introduced, which consists of the load capacitance, the crystal parallel capacitance, and parasitics. This model is used to analyze the energy consumption due to the single-ended and differential contributions to the total capacitance. Furthermore, several step-wise charging architectures are proposed, which reduce the theoretical energy consumption driving the capacitive load by a factor of 2-4, depending on the architecture and the ratio between differential and single-ended capacitances. Although step-wise charging could be applied to any energy injection technique, its feasibility is demonstrated by implementing the proposed 4-step charging method in the start-up technique that achieved the lowest start-up energy at the time of development; the self-timed injection that was introduced in Chapter 3.

Not only the energy to drive the capacitive load is reduced, the energy consumption of the other circuit blocks is lowered as well. Furthermore, the overall robustness is improved by refining the self-timed energy injection method. The use of a dynamic comparator allows for a low power consumption, which is minimized by preventing the full discharge of its drain capacitors at each clock cycle. The trade-off of comparator offset against speed and energy is alleviated by implementing a simple offset calibration scheme. Furthermore, the trade-off between sensitivity and quick charging of the crystal nodes is broken by a switch resistance that varies over the start-up sequence, and autonomy is improved by extending the control logic to automatically switch to the steady-state mode after counting a programmable amount of injection cycles.

Measurements on the manufactured prototype, using the same crystals as in Chapter 3, show a reduction of both start-up time and energy, as well as increased robustness against crystal types and PVT variations compared to the prototype from Chapter 3. Furthermore, the proposed chip improves upon the state-of-the-art in terms of start-up energy.

Chapter 5 covered additional design considerations for self-timed injection circuits regarding their main challenges; maximizing the injection amplitude and minimizing the phase shift between motional current and injection voltage. The origins and mitigation of phase shifts in the self-timed injection cycle are identified. Considerations and mitigations for the bridge design, including step-wise charging and switch resistance, as well as the design and requirements on the comparator and logic, were also discussed.

Furthermore, system-level considerations that influence the design of a crystal oscillator start-up circuit were covered. These lead to a design parameter sensitivity that gives insight into how supply voltage, crystal parameters, and steady-state amplitude affect start-up time and energy.

Finally, the work discussed in Chapter 2, as well as the proposed chips covered in Chapters 3 and 4, were compared by their supply voltage, steady-state amplitude, and crystal parameters. Additionally, start-up energy efficiency is introduced as an additional metric to compare crystal oscillator start-up circuits, in an effort towards a fair metric for comparing crystal oscillator start-up circuits. Although, using the metrics covered in this chapter, the various data can be compared under certain assumptions and conditions, it also shows that equal or at least similar conditions are required to fairly compare different designs.

In all, the research goal of this research was to quickly start up crystal oscillators, for as little energy as possible. To achieve this, this thesis presented self-timed injection, as well as the application of step-wise charging to crystal oscillators. Although the start-up efficiency shows that start-up energy consumption is still far from its theoretical minimum, the proposed techniques - when compared to other energy injection methods - achieve competitive start-up times and significantly lower start-up energy.

6.2 Future perspectives

Knowing that constant efforts are being made to render crystal oscillators superfluous, crystal oscillators will very likely at some point be replaced by cheaper, less area-consuming alternatives such as LC oscillators. This makes it hard to predict the future of crystal oscillators and their start-up circuits. However, with the vast number of applications for crystal oscillators, they will likely see continued use, at least in the near future. This motivates further research in the start-up of crystal oscillators.

The most straightforward recommendations and research directions regard the implementation of the presented self-timed injection circuits. Firstly, their start-up time is longer than the theoretical minimum due to delay in the self-timed injection cycle. This means that more start-up cycles are required than strictly needed, which adds to the overall start-up energy. Further reduction of the delay could be achieved by triggering slightly before, instead of at the motional current zero crossings. This creates a ‘negative delay’ that can compensate for the overall delay in the loop. This can be a fixed delay, but it could also involve a mechanism to

detect the optimum amount of 'negative delay'. Reduction of the delay due to (dis)charging of the crystal parallel capacitance can be achieved by extending the time range in which the switch resistance is varied.

Otherwise, technology scaling helps, as the logic circuits become faster and more energy efficient. Furthermore, smaller technology nodes enable bridge switches with lower parasitic capacitance and lower on-resistance. This allows a faster step-wise charging sequence and hence improved efficiency. Even without significant design changes, implementation of the circuit proposed in Chapter 4 in a more modern technology node than the 65nm CMOS that was used for the prototype will certainly result in lower start-up times and lower energy consumption.

Additionally, the robustness of the switch resistance settings against PVT can be optimized. This can, for example, be done during a calibration cycle that finds the optimum switch resistance settings automatically, instead of inserting these parameters manually as done in the presented prototypes. Furthermore, temperature compensation of the switch resistances can reduce the variability over temperature. This can be achieved by adapting the switch resistance, depending on temperature. Basic temperature compensation of the ring oscillator can also reduce its frequency variation over temperature, which in turn will reduce the variation in comparator clock rate, and hence variations in energy consumption.

While the required time and energy for offset compensation of the comparator are relatively low, they can be further reduced. For example, for the comparator in Chapter 4, the offset compensation is completely reset every time the start-up circuit is enabled. Instead of forgetting the previously calibrated value, the offset compensation parameters (i.e., differential pair body potentials) can be stored and used as a starting point for offset calibration in the next start-up event. This can help to shorten the calibration cycle, saving some energy.

Regarding chip area, it is recommended to re-use the load capacitors for the stepwise charging buffer capacitors, instead of using distinct capacitors for both functions. This would save a significant amount of chip area.

Additional research is recommended to investigate the use of different resonator types. These could be different quartz crystals with smaller physical sizes, but with associated larger motional inductance. The increased motional inductance means that more injection cycles are needed to achieve a certain output amplitude, meaning that the start-up time is longer, such that the injection signal must be accurate for a longer time. Here, self-timed injection could be beneficial compared

to open-loop injection, since the phase error does not accumulate over time. However, additional research is required to achieve the increased sensitivity requirements that come with these crystals. Furthermore, the application of self-timed injection and/or self-timed injection to non-quartz resonators could be explored. These could be, for example, applications that use (high-Q) MEMS resonators as frequency references or sensors.

A different research direction is the crystal spurs. Any crystal has spurious responses, which can be at the harmonics, but also spurious tones close to the fundamental (in terms of frequency), which can even shift over temperature. Exciting the crystal with a square wave for a limited time, as done in all energy injection techniques, 'broadens' the injection spectrum. This means that not only the crystal fundamental is excited, but nearby spurs could also be excited. Their quality factor is normally lower than the fundamental, but it takes some time after injection for the oscillations to dampen. Depending on the PLL implementation (e.g., loop bandwidth) and the actual spurious responses of the crystal, this may or may not be a problem. Additional research on the severity of these spurs is recommended.

On a broader perspective, the general trend in circuit design, in which purely analog circuits shift towards switching and/or digitally assisted circuits, is also visible in crystal oscillator start-up circuits. This applies to recent publications on MHz-range crystal start-up circuits, as well as kHz-range (steady-state) crystal oscillators, and will likely start to see use in MHz-range steady-state crystal oscillators as well.

Another perspective is the growing use of (direct) feedback from the crystal itself, instead of open-loop injection. Current examples periodically use the crystal oscillator to calibrate the injection source, detect the crystal resonance frequency by a sweep and measuring the crystal response, or (as proposed in this thesis) use feedback from the crystal at every (half) injection cycle. Other methods to directly use information from the crystal itself ('closed loop') will likely emerge. This can be beneficial for start-up, but when combined with switching techniques can also benefit the steady-state oscillator. Furthermore, instead of regarding the crystal oscillator as a separate building block, it could be further integrated into the entire system. The crystal oscillator could for example be closely integrated with the PLL, where information from previous PLL activity can be used to set start-up parameters, and while the crystal oscillator is starting, its output could already be used for (coarse) PLL settling.

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- **J. B. Lechevallier**, R. A. R. van der Zee, and B. Nauta, "Fast & Energy Efficient Start-Up of Crystal Oscillators by Self-Timed Energy Injection," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3107–3117, Nov. 2019.

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