3D SELF-ALIGNED FABRICATION OF SUSPENDED NANOWIRES BY CRYSTALLOGRAPHIC NANOLITHOGRAPHY

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ABSTRACT

Known templating procedures mostly create out-of-plane nanowires where individual connections at both ends are complicated. Here we introduce a templating procedure for wafer scale fabrication of in-plane nanowires. The template fabrication process employs two simple interference lithography masking patterns and relies on self-aligned crystallographic processing. In-plane nanowires with diameters down to 10 nm can be fabricated wafer scale through this 3D templating procedure. As a first demonstration arrays of suspended silicon nitride wires have been created.

KEYWORDS

Corner lithography, nanowires, templating, 3D, silicon crystal

INTRODUCTION

Templated nanowire growth is a relative old technique, initially based on track-etched membranes [1] as well as anodic aluminum oxide (AAO) porous membranes [2]. Nanowires are typically oriented out-of-plane and connecting both ends is challenging. Typical diameters are at least tens of nm. Several procedures have been developed for *silicon* in-plane nanowires, typically using (advanced) lithography and silicon-on-insulator (SOI) substrates for defining the wire thickness and for release etching through oxide dissolution [3, 4]. Here we introduce an in-plane templating procedure with nm accuracy over the complete wafer for standard p-type silicon substrates, yielding nanowires in the 10 nm diameter range. More in detail, convex corner lithography [5, 6], an emerging self-aligned nanopatterning technique, is employed to create nano-cavities at the apex of silicon wedges [6]. Essential steps have been added to this basic scheme to create a template for suspended nanowires of ~100 nm length, and to create a strategy for controlled release etching. The complete procedure has been tested by creating arrays of suspended silicon nitride nanowires.

EXPERIMENTAL

Approach

Fig. 1 shows the basic steps for the template formation. Initial wedges are formed from a line pattern in silicon nitride, used as a hard mask for anisotropic etching of the (100)-silicon substrate, followed by LOCOS and another anisotropic silicon etching step [7]. Cavities are formed by "convex corner lithography" combined with anisotropic etching [6]. Nanowires are then formed in the cavities through "irreversible processing", i.e. conformal deposition of silicon nitride in confined space followed by isotropic etching (Fig. 2). This isotropic etching is performed through planar windows which are defined in a hard mask, as to define the finite length of the nanowires and their suspension. The hard mask stack consists of amorphous silicon on top of silicon nitride in which the pattern is created through interference lithography (DTL: displacement Talbot lithography). The same masking apertures are used to expose the silicon side walls. Exposed silicon is then etched in KOH to release the nanowires (fig. 2).

Details of template cavity fabrication

Boron doped (100) oriented silicon (Si) wafers (5-10 Ω cm, 100mm diameter, 525 µm thick, one-side polished, Okmetic, Finland) are used to fabricate wafer scale wedges combining DTL with reactive ion etching and anisotropic wet-chemical etching. Stoichiometric silicon nitride (Si_3N_4) is used as a hard mask for anisotropic etching of Si to form V-grooves followed by local-oxidation-of-silicon (LOCOS), stripping of Si_3N_4, and anisotropic etching of Si to form wedges, as shown in fig. (1a). Subsequently, low temperature (800°C steam) thermal oxidation is performed to grow SiO_2, as shown in fig. 1b. Timed isotropic thinning of SiO_2 is performed in 1% hydrofluoric acid (HF) to only expose the apices or the convex corners, shown in fig. 1c. Finally, the exposed apices are etched selectively in tetramethylammonium hydroxide (TMAH) to form cavities with free standing SiO_2 flaps, as shown in Fig. 1d [6].

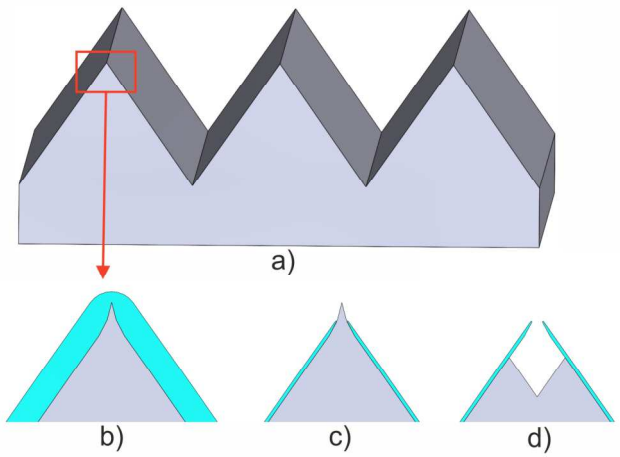

Figure 1: Process flow for template cavity fabrication. Starting from the silicon wedge array (a), a low temperature thermal oxidation follows (b), then HF thinning of SiO_2 (c) and finally TMAH etching of silicon (d). Adapted from [6] with permission.

Details of suspended nanowire formation

The substrate containing the wedge based cavities were standard pre-furnace cleaned by means of fuming 99% nitric acid (HNO_3) (2x 5 min) and boiling 69% HNO_3 (10 min). Low pressure chemical vapor deposition (LPCVD; Tempress horizontal diffusion system, type TS6604, 800℃, 200 mTorr, 22 sccm SiH_2Cl_2, 66 sccm NH_3, 17 min) was carried out to conformally grow 13.1 ± 0.1 nm Si_3N_4 to embed the cavities. Next, amorphous silicon (a-Si) of 14.3 ± 0.8 nm was conformally deposited using LPCVD (Tempress horizontal diffusion system, 550 ℃, 250 mTorr, 50 sccm SiH4, 6min 30s) to serve as a hard mask for patterning Si_3N_4. Next, a Si_3N_4 layer of 12.4 ± 0.2 nm was conformally deposited using LPCVD to be used as a hard mask for a-Si patterning. Subsequently, ~200 nm bottom anti-reflective coating (BARC, Barli-II) was spin coated at 3000 rpm for 45s followed by pre-exposure bake at 185℃ for 60s. Then ~160 nm positive-tone photo-resist (PFI:88, 1:1 PFI: PGMEA (propylene glycol monomethyl ether acetate – Sumitomo Chemical Co., Ltd.) was spin coated at 4000 rpm for 45s followed by pre-exposure bake at 90℃ for 60s. An advanced interference lithography technique DTL (PhableR 100C, Eulitha, Switzerland) was carried out. A phase-shift mask with gratings featuring a pitch of 500nm was aligned perpendicular to the substrate of nano- wedges. The photoresist was exposed at a wavelength of 375 nm with an intensity of 0.98 mW cm^{-2} for 75s at a Talbot distance of 3 µm and a gap spacing of ~65 µm. After DTL, the substrate was post-exposure baked at 110℃ for 60s followed by resist development in TMAH (OPD4252, Arch Chemicals) solution for 60s (substrate submerged two times for 30s in separate beakers). Next, the photoresist pattern was transferred into the BARC layer using a conductively coupled plasma RIE system (25W, 50 mTorr, 50 sccm N_2, 6 min 50s; TEtske home-built system). Prior to RIE, the chamber was pre-cleaned by wiping it with organic solvent, followed by oxygen plasma cleaning for 10 min (100W, 50mTorr, 50 sccm O_2). The etching was timed as such that the BARC layer was removed only from the apex of the nanowedges to expose Si_3N_4 layer whereas the concave corners were still protected. Next, the Si_3N_4 layer was etched for 60s in the same RIE chamber (25W, 10 mTorr, 25 sccm CHF_3, 5 sccm O_2; Tetske home-built system) to expose the a-Si layer, as shown in fig. 2a. The photoresist and BARC layer were stripped using an oxygen plasma (TePla 300) for 45 min, followed by 10 min Piranha cleaning (mixture (95 °C) of sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in a volumetric ratio of 3:1). Next, the substrate was etched in 1% HF at room temperature for 60s to remove native oxide from the surface of the exposed a-Si. The substrate was then placed in 20 wt.% potassium hydroxide (KOH) solution at 21℃ to selectively etch a-Si for 40s, as shown in fig. 2b. After KOH, the substrate was cleaned for 20 min to remove alkali-residue in RCA-2 (mixture (80 °C) of 36% hydrochloric acid (HCl), 31% hydrogen-peroxide (H_2O_2) and demineralized water (DI water) in a volumetric ratio of 1:1:5). Next, the substrate was etched in 1% HF at room temperature for 20s to remove native oxide on top of the exposed Si_3N_4 layer. The substrate was then placed in a solution of 85 wt.% H_3PO_4 at 140°C to isotropically thin the Si_3N_4 layer at a pre-determined etch-rate of 2.0 nm/min. The substrate was timed for 7 min to leave the Si_3N_4 layer only in the cavities, shown in Figure 2c. Next, the exposed SiO_2 layer was etched in 1% HF at room temperature for 30s followed by etching of Si in 20% KOH at 21 °C for 8 min 30s to release the Si_3N_4 nanowires. The substrate was then carefully freeze dried to not damage the suspended Si_3N_4 nanowires. The freeze drying process includes rinsing in isopropanol and cyclohexane followed by freeze drying at -7 °C under a nitrogen flow.

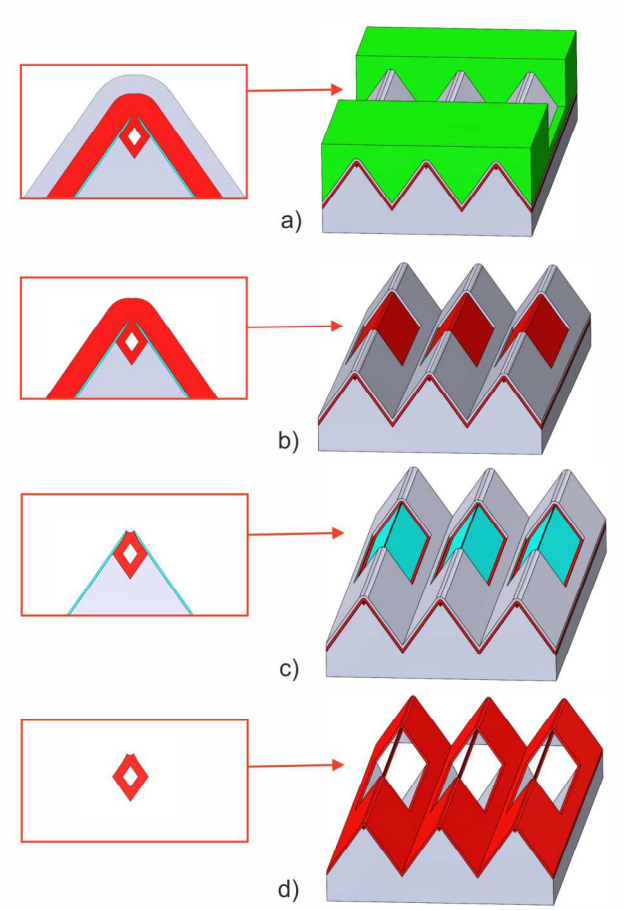

Figure 2: Process flow for finite length nanowire creation and release. a) After patterning the a-Si hard mask in 20% KOH, the silicon nitride is thinned in H_3PO_4 solution (b) -> c)). After HF removal of the SiO_2 stop layer, the exposed silicon is etched in 20% KOH at room temperature, followed by rinsing and freeze dying (d).

RESULTS AND DISCUSSIONS

The windows for removing silicon from underneath the nanowires by anisotropic etching, , are created by a hard mask layer stack composed of Si_3N_4/a-Si /Si_3N_4. Post to DTL and RIE (of BARC) the top layer of Si_3N_4, which is 12.4 nm thick, is opened with RIE. Via openings in this Si_3N_4 film, the underlying a-Si is selectively etched (patterned) using KOH. Post to cleaning steps, the bottom layer of Si_3N_4 (14.3 nm thick) is isotropically thinned, such that only in the cavities Si_3N_4 remained (i.e. non-suspended Si_3N_4-nanowires), followed by KOH-etching. By

performing this sequence, the complete top layer of Si_3N_4 is removed during the HF thinning step, whereas the a-Si film and bulk-Si underneath the Si_3N_4-nanowires are removed during the KOH-step. Thus, the hard mask applied for realizing suspended Si_3N_4-nanowires in designated windows is a stack of three films, of which the top layer Si_3N_4 (deposited after a-Si) has to be thinner than the bottom layer Si_3N_4 (deposited at first).

Fig. 3 shows a TEM cross section of the templates after conformal filling with silicon nitride. The silicon oxide used for the convex corner lithography initially was grown at a thickness of about 8 nm on the {111}-planes (far away from the apex), of which about 2 nm remained after the HF etching employed to expose the silicon at the apex. As this is close to the minimum thickness for this procedure, the 6 nm slit at the apex is the lower limit for this material system and procedure. The cavity width is 12 nm and was determined to be rather uniform at five positions across the wafer [6]: 12.0 ± 0.5 nm (±1 SD_N).

Fig. 4 shows SEM images and drawings illustrating the release at different times in the etching process. The top row illustrates when the hard masks are just opened and after 2.5 min of KOH etching (20% KOH, 21 °C). The middle shows the result of 5 min anisotropic etching of silicon is not enough because the template is still connected to the bottom of the nanowire. The bottom row shows the result after 8.5 min anisotropic etching of the template to create a cavity, yielding suspended Si_3N_4 nanowires.

Fig. 5 shows SEM images of fabricated suspended nanowires. The wires are about 10 nm in diameter and have a length slightly over 100 nm. Currently, the estimated yield is about 40%. The main loss of wires occurs in the final freeze drying release step, which has to be further optimized for the small scale of the nanowires.

CONCLUSIONS AND OUTLOOK

We have demonstrated the template formation of suspended nanowires with diameters close to 10 nm in a wafer scale process. The current procedure has now been demonstrated for silicon nitride wires and needs further optimization to increase the yield. It is expected that the presented method will enable wafer scale in-plane nanowire formation for a wide variety of materials including metals, semiconductors and piezoelectric ceramics.

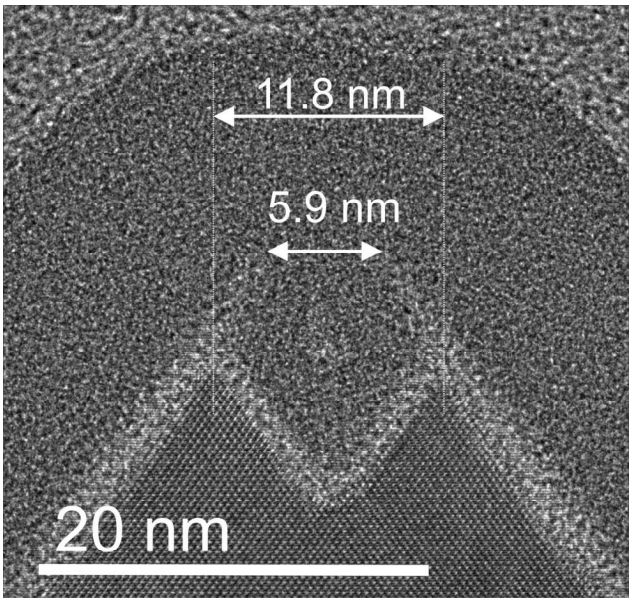

Figure 3: TEM image of a cross-slice of the nanowire template, showing the 12 nm wide cavity and the 6 nm top gap. The remaining thickness of free-standing silicon oxide flaps is about 2 nm.

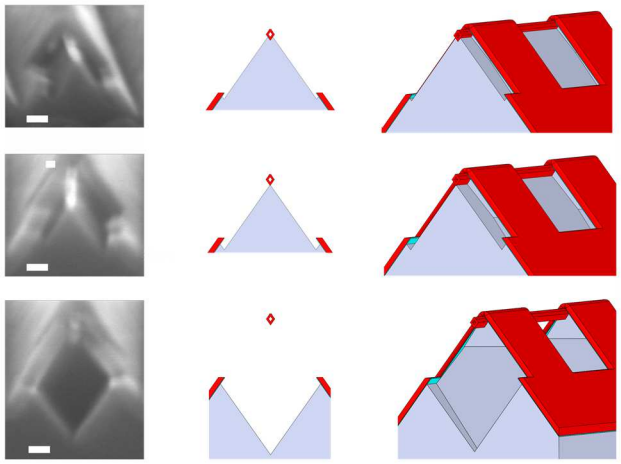

Figure 4: SEM photos and drawings illustrating the release etching at different stages. Top row: The hard masks have just been opened; Middle row: The silicon template still connects to the bottom side of the nanowires; Bottom row: A silicon cavity bound by slow etching crystal planes has formed beneath the nanowire, resulting in a suspended nanowire. Scale bars are 20 nm.

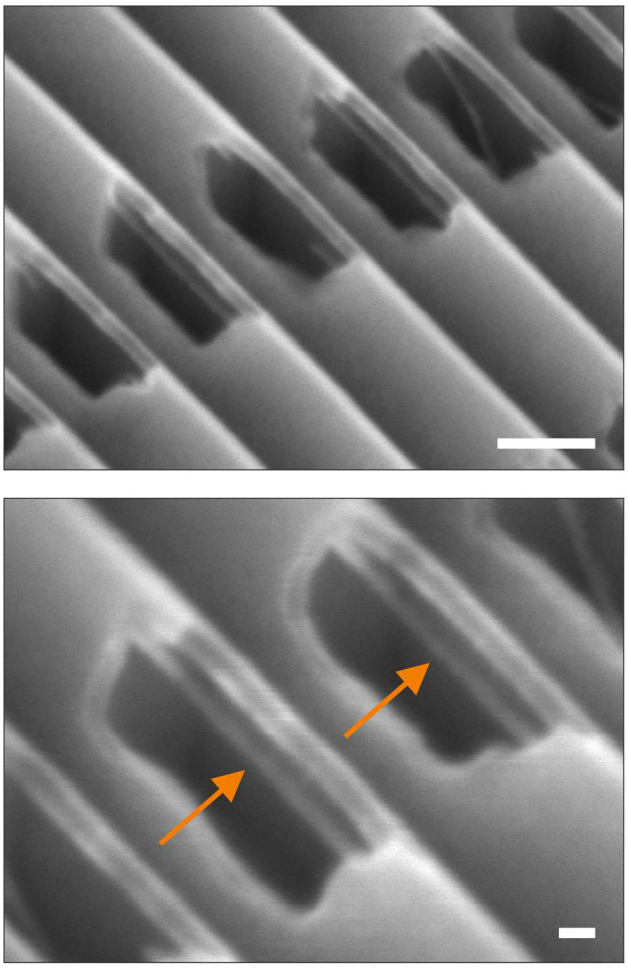

Figure 5: SEM photos showing finally produced suspended nanowires. Scale bars are 100 nm and 20 nm, respectively. It is noted that some suspended nanowires in the top image have collapsed during freeze drying.

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