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The influence of technology variation on ggNMOSTs and SCRs against CDM ESD stress

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Abstract

In this paper we present a systematic study on the effect of process and layout variation for grounded-gate NMOSTs and LVTSCRs in a 0.18μm technology under negative non-socketed Charged Device Model (CDM) stress. Failure Analysis of the stressed devices was done using Scanning Electron Microscopy (SEM). A comparison of the CDM test results with those of ggNMOSTs in various other technologies is also presented. It is shown that the CDM robustness of ggNMOSTs increases with technology scaling and that the performance of LVTSCRs can be as good as that of ggNMOSTs under CDM stresses.

1. Introduction

An Electrostatic Discharge (ESD) where the charge stored in a device discharges to the ground through one of its pins is known as Charged Device Model (CDM). CDM pulses have a very short rise time and pulse width of ~ 500 ps. and very large current amplitudes ~10A. On one hand with downscaling of the IC dimensions, especially the thinning down of gate-oxide thickness, and increased complexity in the circuit network, the ICs have become more sensitive to CDM kind of ESD events. Whereas on the other hand the increased usage of automated handlers in the advanced processing techniques has increased the probability of ICs facing CDM kind of ESD [1].

Most often the CDM failure is attributed either due to the delay in the switching of the protection device during stress or due to improper designing which can result in voltage build up within the internal nodes of an IC. In this paper we deal only with the behavior of protection devices under CDM stress.

This paper shows the influence of design and process variations on grounded-gate NMOS transistors (ggNMOSTs), in technology nodes from 0.5μm down to 0.18μm. We have also studied the behavior of Low Voltage Triggered Silicon Controlled Rectifiers (LVTSCRs) in 0.18μm technology node, under CDM stress. Failure analysis of the stressed devices was done using a Scanning Electron Microscope (SEM). The results of this analysis are presented in Section 3. The test results of the ggNMOSTs in the 0.18 μm technology are discussed with respect to relevant layout

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parameters in the following sections. In section 4.3 the influence of technology variation on the ggNMOSTs is investigated. Lastly the CDM performance of the LVTSCRs with various cathode to anode spacings (C-A) are discussed.

2. Experiment and measurements

The cross-section of the ggNMOST is shown in figure 1, indicating the relevant layout parameters. Devices with several gate-widths (25-100 μm), gate-lengths (0.18-6 μm) and silicide blocked drain extensions (0-8 μm) were available. Similar structures have been used for other technologies.

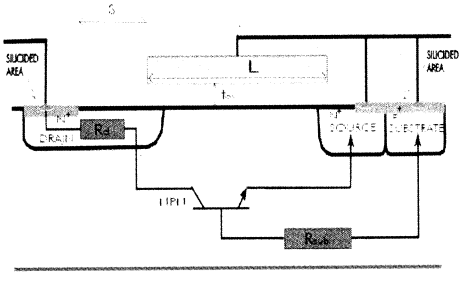

Figure 1: The layout of ggNMOST with its various layout parameters and the parasitic bipolar transistor

The second protection device studied was the LVTSCRs in the 0.18μm technology. Figure 2 shows the cross-section of the SCR structure indicating the Cathode to Anode spacing,. which is an important design parameter for SCRs.

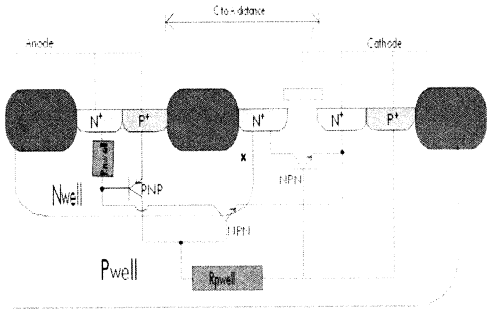

Figure 2: The layout of LVTSCR with the various bipolar transistors which are activated during ESD stress.

All the devices were subjected to negative non-socketed CDM tests [4], which typically is the most critical stress mode. In this test method the IC is placed in a dead bug position (with pins facing up) on a metal plate which is charged to the desired value. Each pin of the IC is then discharged by touching it with a grounded probe. The devices were thus step stressed from 200V until 3000V with 100V increments with one zap per stress level. After each stress, the devices were tested for electrical failure. This was done in two steps. First as a continuity test a forward current of 1μA was forced through the device and the voltage drop across the drain-source V_{cont} was measured. Then the drain-source current I_{leak}, was measured at the maximum operational voltage of the device $V_{max} = V_{op} + 10\%V_{op}$. For undamaged devices this current, generally known as the leakage current, should be very small in the order of few ns. A careful study of the current and voltage values was made and three types of failures namely soft fails, opens and shorts were identified, as illustrated in figure 3. The failure criteria used are:

- open fail: I_{leak}<0.05μA and V_{cont} >500mV
- short fail: I_{leak} >1μA and V_{cont} <10mV
- soft fail: consistent leakage current increase beyond 0.1μA, while V_{cont} 10mV

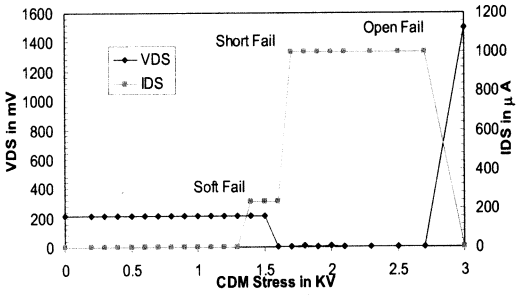

Figure 3: The leakage current I_{leak} and Voltage V_{cont} after each stress level showing the onset of different kind of failures.

In general we cannot find all these three failure modes occurring in each device, e.g. a device may exhibit a short fail without showing a soft fail. The failed devices where then subjected to SEM study to see the actual physical failure. For most devices we eventually get an open fail as shown in figure 3. This failure mode is ignored in the discussions below, as it is irrelevant for design engineering of the protection structures.

3. Failure Analysis

The pictures of the physical failure give a clear insight into the cause for the failure. There is a clear correlation between the electrical failure and the physical failure. All SEM pictures, except for figure 4, were taken after the sample had been deprocessed to the silicon surface. This is the reason why the metal layers are found in figure 4 alone. Figure 4 shows a transistor after an open fail. Clearly the whole device and part of its environment have completely been blown away by the extreme energy densities that occur during such high level stresses. Typically this failure mode is only observed for stress levels that have no practical relevance.

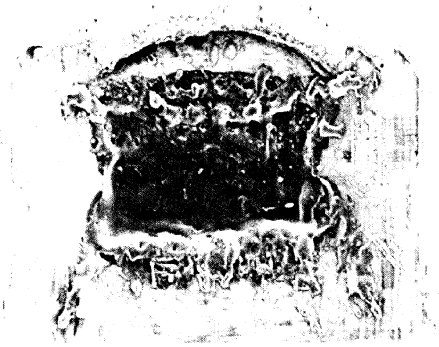

Figure 4: The SEM picture showing a ggNMOSt after a CDM stress of 3KV.

The SEM picture of the device, which showed a soft fail, is shown in figure 5. In figure 5 we see needle shaped silicide melts extending from the drain to the source. During electrical measurements this device showed a small increase in its leakage current.
We could observe some damage near the gate-oxide, see figure 6. This damage can be mistaken for the gate-oxide damage that is often observed within the protected circuit. Careful observation indicates that it is the silicon under the gate between the source and drain that has melted. Because of the high local currents the silicon became so hot that the silicon had melted and damaged the whole gate region.

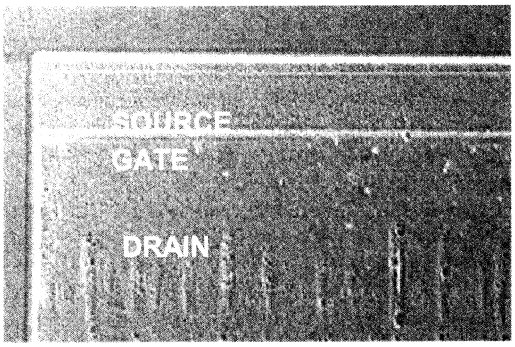

Figure 5: SEM picture of a ggNMOST showing a soft failure.

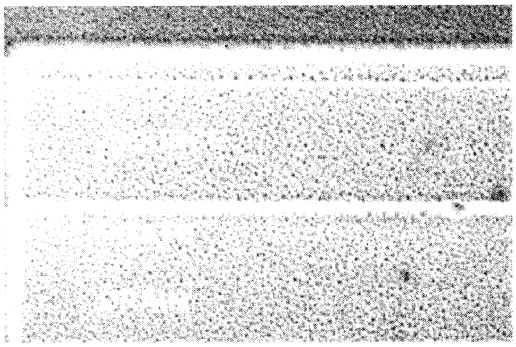

Figure 6: SEM picture of a ggNMOST showing a short failure.

Sometimes we observe high current density filaments as shown in figure 7. This typically happens near the failure level when the current gets localized instead of spreading uniformly throughout the width of the device. Before failure, the current distribution was uniform in this structure, as will be shown in the next section. Figure7 is the SEM picture of a ggNMOST of width 100μm and with silicide block of 6μm. Although the CDM failure is mainly attributed to the slow triggering of the devices, the thermal effects also play some role. Hence while simulating CDM failures thermal effects should not be neglected completely.

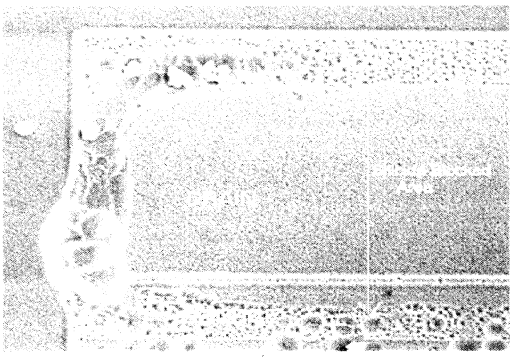

Figure 7: SEM picture of a ggNMOST showing a short failure.

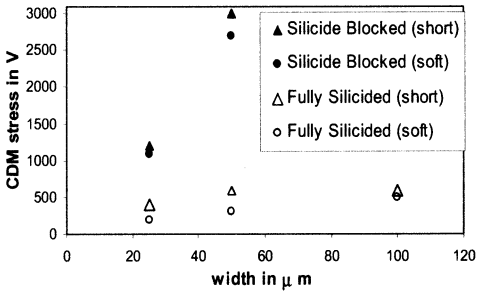

Figure 8: The effect of width variation on CDM robustness for silicide protected (solid markers) and fully silicided (open markers) process on 0.18 μm process, with L=0.18μm.

4. Discussion of results

4.1. ggNMOST Width (W) scaling

Figure 8 shows the soft and hard (short) failure levels of ggNMOSTs with L = 0.18μm as a function of device width. Figure 8 also shows the effect of adding a silicide block of 6μm, as indicated in the figure 1. It is clear from the figure that for smaller W, the CDM failure level reduces. The fully silicided devices fail at very low CDM stress levels and do not scale with W. With silicide blocking the devices have better CDM performance and show a linear W-dependence. The ggNMOSTs with W=100 μm did not fail due to practical limits on maximum stress levels. This scaling with W indicates that the flow of ESD current is uniform through out the device.

For silicide blocked devices, the area which is blocked acts like a ballast resistance. This ensures uniform distribution of ESD current along the whole width of the device and also helps in forcing the current into the substrate region below the drain and avoids current crowding at the drain junction close to the gate edge. For fully silicided devices uniform conduction of ESD current is not obtained, and hence the robustness is almost independent of the device width.

4.2. ggNMOST Length (L) scaling

From figure 9 it is evident that devices with smaller channel lengths show good CDM robustness. This is in agreement with previously obtained results [3]. Under a negative CDM stress a parasitic lateral bipolar, shown in figure 1 gets switched on (npn=source-substrate-drain) and safely grounds the ESD current. The transit time of this device plays an important role in the CDM failure level. A bipolar transistor with a base width of 1 μm has a base transit time of approximately 150 ps [5]. The CDM rise time is in the order of 250 ps. Thus ggNMOSTs that are longer than 1 μm are expected to have poor CDM robustness, since the device will not turn on in time to shunt the current. Shorter devices thus will have increasingly better performance, as is observed in figure 9.

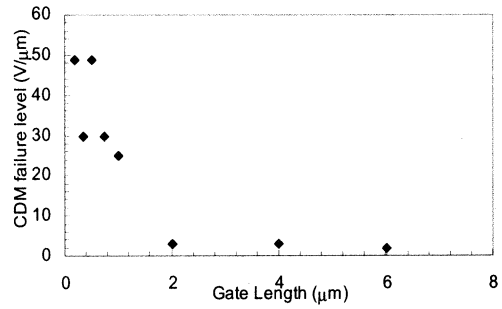

Figure 9: Influence of gate length on CDM robustness of ggNMOSTs in 0.18 μm technology.

4.3. Influence of technology variation

Figure 10 shows the influence of electrical gate length Leff on the CDM failure threshold, for ggNMOSTs with silicide blocking in various technologies. The dashed line indicates the soft failure while the dotted line indicates hard failure (short). Note that the CDM performance scales linearly with 1/Leff, which is in line with the results of 0.18μm technology. For channel lengths longer than 2μm from different technologies their failure levels coincide. This confirms the fact that the transit time of the device plays a major role in deciding the switching speed of the device. We also find that all the technologies show poor and non-scaling behavior for fully silicided ggNMOSTs.

With the downscaling of technologies the vulnerability (sensitivity) of the circuits to CDM stress has increased. But the good part of it is that it has increased the switching capabilities of the protection devices. This would mean that we can build more efficient protection devices, which can withstand with the scaling down of technology, in our case devices which can withstand CDM stress of 50V/μm for the 0.18μm technology node. This is just the first step. Proper distribution of these protection devices within the circuit is very much important to achieve CDM robustness for the entire IC.

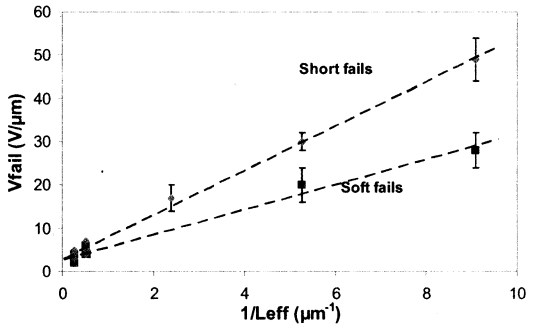

Figure 10: The variation of CDM performance with 1/Leff of the ggNMOSt in various technologies. For 1/Leff > 2μm^{-1} the failure level is taken from the smallest transistor of the respective technology.

4.2. Silicon Controlled Rectifier (SCR).

Figure 11 shows the CDM performance of LVTSCR as a function of its cathode to anode (C-A) spacing, see figure 2. Note that the best CDM performance is obtained for smaller C-A values. It is known that the holding voltage is affected by the C-A

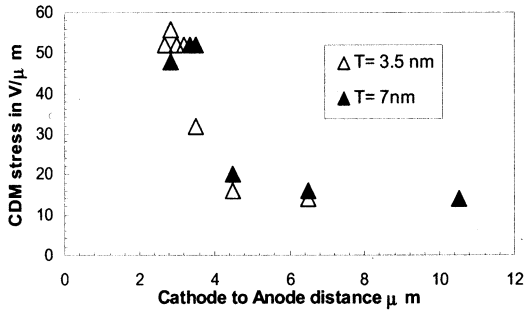

Figure 11: Effect of cathode to anode distance variation on the CDM performance of the LVTSCRs, with thin and thick gate-oxide ggNMOSts. T=thickness of the gate-oxide.

distance [6]. Generally the CDM robustness decreases and latch-up immunity must be kept in mind while designing these structures. Figure 11 also shows the effect of the oxide thickness of the ggNMOST integrated in the LVTSCR. Thin and thick gate oxide is available to accommodate different supply voltages in this technology. Note that the results of both the LVTSCRs (with two different types of ggNMOST) coincide. This indicates that the role of the ggNMOST, is only to help in the triggering of the SCR. After that the behavior is fully determined by the nature of the two bipolar transistors, figure 2. Note that the maximum obtained performance is 50 V/μm, which is equal to the best results for ggNMOSTs in the same technology. For longer spacings the performance level saturates at approximately 10 V/μm, which is significantly higher than the saturation level for long ggNMOSTs.

5. Conclusions

We have studied the influence of process and layout variations on ggNMOSTs for several technologies. FA done on the samples show several types of failures and most of them being thermal failures. This indicates that thermal effects play a significant role even under CDM stress condition. For all technologies considered, it was found that silicide blocking is necessary to obtain linear width scaling. For best robustness the shortest device in the technology should be chosen. For all technologies ggNMOSTs longer than 1μm show very poor CDM robustness. The maximum obtained robustness increases with technology scaling to 50 V/μm for the

0.18 μm technology node. For LVTSCRs in this technology node the same maximum robustness is obtained. The performance of the LVTSCRs decreases with increasing anode to cathode spacing.

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