



# ECIO 2022

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4<sup>th</sup> May – 6<sup>th</sup> May

Milan, Italy

23<sup>rd</sup> European Conference on  
Integrated Optics



**POLITECNICO**  
MILANO 1863



# A Universal 20-mode Quantum Photonic Processor

(Student paper)

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**Universal, phase-stable, reconfigurable quantum photonic processors enable manipulation of photonic quantum states and are one of the main components of photonic quantum computers in various architectures. In this paper, we report the realization of the largest quantum photonic processor to date.**

**Keywords:** *quantum, reconfigurable photonics, silicon nitride*

## INTRODUCTION

With the recent experimental results demonstrating a quantum advantage<sup>1,2</sup>, photonics has become one of the most attractive approaches to quantum computing. The strengths of photonics as quantum computing platform are, for example, its inherent low decoherence due to the weak interaction of quantum states of light with their environment and the operation at room temperature. Photonic quantum computing can also exploit the high maturity of existing classical integrated photonics technologies making it a scalable and phase-stable approach to large-scale quantum computing.

Quantum computational models based on photonics range from non-universal approaches, such as Boson Sampling<sup>3</sup>, which forms the basis of the recent quantum advantage experiments<sup>1,2</sup>, to universal ones based on a variety of different encodings<sup>4-6</sup>. Applications of non-universal photonic quantum computing have been proposed, such as quantum chemistry<sup>7,8</sup> and graph properties<sup>9</sup>.

A quantum photonic processor<sup>7,10-12</sup>, or linear optical interferometer, is one of the essential components of photonic quantum computing and is the main player in applications such as quantum neural networks<sup>13</sup>, quantum metrology<sup>14</sup>, PUFs<sup>15</sup>, witnesses of bosonic interference<sup>16,17</sup> and for benchmarking multi-photon light sources<sup>18,19</sup>.

Of the available integrated platforms, silicon nitride (Si<sub>3</sub>N<sub>4</sub>) is the most promising platform for photonic quantum computing. It provides an optimal combination of low loss and high optical mode confinement<sup>20</sup>, enabling the scaling up of low-loss fully-reconfigurable linear optical interferometers for quantum computing and information processing.

In this paper, we present the largest universal quantum photonic processor to date, with 20 input/output modes. Our processor is based on silicon nitride waveguides. The device has losses of 2.9 dB/mode and enables arbitrary linear optical transformations, making it compatible with all linear optical models of quantum computation. We validate the processor performances over more than 1000 experiments showing high-fidelity operations.

## RESULTS

Our 20-mode quantum photonic processor consists of three parts: the Si<sub>3</sub>N<sub>4</sub> photonic chip, the peripheral system which includes the control electronics, and the dedicated control software<sup>12</sup>.

The Si<sub>3</sub>N<sub>4</sub> photonic chip (Fig. 1a) contains a total of 380 thermo-optic tunable elements, arranged in a universal square interferometer<sup>21</sup> where the unit cell comprises a tunable beam splitter (TBS) followed by a phase shifter (PS). Propagation losses as low as 0.07 dB/cm at 1562 nm are measured across the entire photonic chip, obtained by a higher-temperature annealing process compared to our previous chip<sup>12</sup>. The peripheral system comprises the control electronics and an active cooling module. The thermo-optic tunable elements can be switched at kHz rate<sup>20</sup>, setting the limit for the switching speed between different configurations of the processor. To precisely control the temperature of the photonic chip, it is actively cooled. The cooling module consists of a Peltier element attached

to a water-cooling module providing a maximum heat reduction rate of 200 W. The dedicated control software performs both the decomposition of any unitary matrix transformation into the phase settings of each unit cell and their assignment to the corresponding tunable elements. The control software takes also into account the imperfections of the processor, such as crosstalk of individual tunable elements and compensates for those.

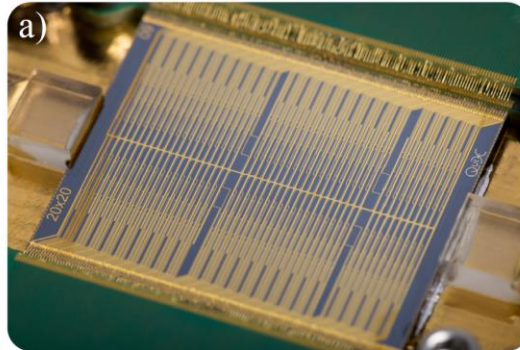


Figure 1 Photograph of the 20-mode processor chip  $22 \times 30$  mm. The chip is optically packaged to an input/output fiber array and it is wire-bonded to the control PCB enabling the addressing of each individual tunable element.

The characterization of the 380 tunable elements shows that they all have a phase tuning range exceeding  $2\pi$ , allowing for full control of the unitary transformation implemented within the interferometer. The insertion loss of the photonic processor is measured to be  $2.9 \pm 0.2$  dB: this is the overall loss experienced by light going in and out of the processor, from input to output fiber, through all the tunable MZIs and phase shifters. Coupling losses are measured at 0.9 dB/facet, which is derived from measuring the insertion loss on the on-chip alignment loops, i.e., paths consisting of a very short length section with negligible propagation loss which therefore only have fiber-to-chip coupling losses.

We verify the reconfigurability and control of the processor by generating and implementing 190 permutation and 1000 Haar-random matrices on the device. For each input mode of each matrix, the output intensity distribution is measured, from which a fidelity measure  $F = \frac{1}{20} (|U^+| \cdot |U_{exp}|)$  of the unitary optical transformations on the input light is determined. We obtain fidelities as high as  $F = (99.5 \pm 0.2)\%$  and  $F = (97.4 \pm 0.5)\%$  for the permutations and the Haar-random transformations, respectively (see also Fig.2 a and b).

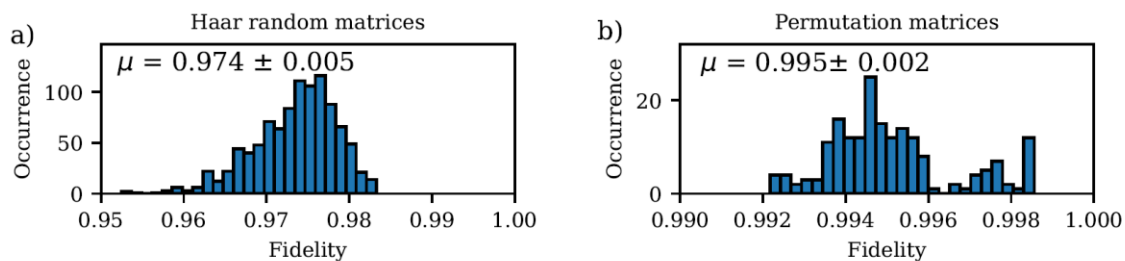


Figure 2 Distribution of the measured amplitude fidelities for, respectively, 1000 Haar-random matrices (a) of average fidelity  $(97.4 \pm 0.5)\%$  and for 190 Permutation matrices (b) of average fidelity  $(99.5 \pm 0.2)\%$ .

Measuring the visibility of quantum interference<sup>22</sup> at every location on the processor provides quantum validation of the device. The photons are then injected into pairs of input modes are routed to interfere at each on-chip TBS, set to a 50:50 splitting ratio. The output modes are connected to superconducting nanowire single-photon detectors (SNSPDs), whose coincidence rate is measured using a standard time-tagger. To route the two photons to every on-chip TBS, and to the connected outputs, the entire interferometer is used. TBSs are set to full reflection or transmission to create optical paths, which contain no intersections other than the TBS of interest. The spatial distribution of the 190 HOM visibilities over the rows and columns of the network, as shown in Fig. 3, is quite random, confirming that there are no systematic errors within the processor. Furthermore, the visibility of the HOM interference appears to be limited by the quality of the source used for the characterization.

In conclusion, we have demonstrated a record universal quantum photonic processor with 20 input/output modes, which is the largest processor to date. Thanks to its low loss and high-fidelity operations, it locates itself at the top of all ever demonstrated universal quantum photonic processors.

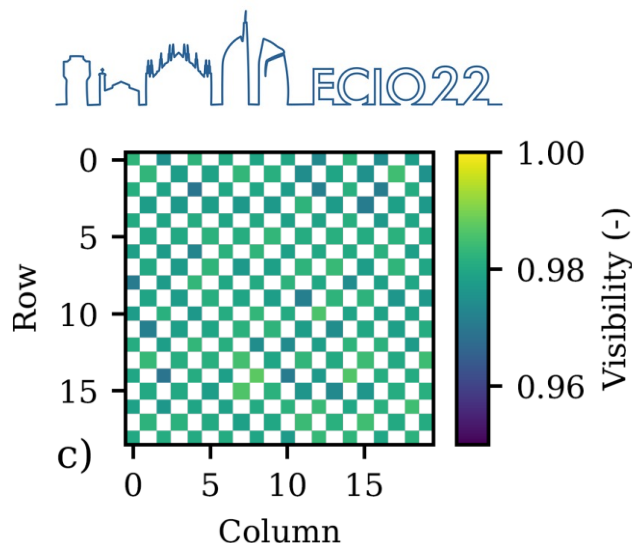


Figure 3 HOM visibilities of all TBS for each network row and column. The checkerboard pattern reflects the alternating pairwise coupling of neighbouring channels as layed out in Fig. 1b.

Acknowledgements: Funding is acknowledged from the Nederlandse Organisatie voor Wetenschappelijk Onderzoek (NWO) via QuantERA QUOMPLEX (Grant No. 680.91.037), NWA (Grant No.40017607), and Veni (grant No. 016.Veni.192.121).

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