Recovery of Hot-Carrier Degraded nMOSFETs

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Recovery of Hot-Carrier Degraded nMOSFETs

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Abstract

Nowadays, computer chips are used in all kinds of industries and applications, from communication, transport to health care, and are an important part of our daily lives. The building brick of every computer chip is the transistor, where advancements in transistor technology have led to smaller and faster chips than ever before. Transistors are so important and omnipresent that they are indispensable for keeping our society running.

However, since transistors are getting smaller and smaller and the operation requirements become more severe, computer chips get more susceptible to damage. This results in reduced functionality and ultimately may lead to the failure of the whole computer chip and electronics. Generally, the manufacturers of electronics aim for transistors to function within the specifications for at least ten years. Earlier research had a focus on preventing transistor degradation, or at least minimizing loss in functionality by optimizing material properties, the fabrication process and in some cases the device or chip architecture.

In addition, when it is possible to (partially) repair the transistors, the damage is either prevented/reduced or the defects created in the transistor may be removed completely, resulting in limited and ideally no loss in functionality. Current lifetime predictions do not take repair into account and the possibility of healing a transistor may lead to a device that has a longer operating lifetime, operates at a higher speed and is generally more reliable.

The transistor most commonly used, is the MOSFET (Metal-Oxide-Semiconductor Field-Effect-Transistor), where the manufacturer aims to have as few defects present in the device as possible to optimize both the lifetime and operation use. During fabrication, the gate dielectric (the oxide in MOSFET, in this thesis SiO_2) is deposited on top of a semiconductor substrate (in this thesis Si). Not all Si atoms at the Si/SiO_2-interface can make a bond with atoms in the gate oxide, leading to dangling bonds. Since these dangling bonds can act as a charge trap and may distort various operation parameters, an anneal step in an hydrogen ambient is performed during the fabrication process to passivate the dangling bonds with hydrogen.

Due to hot-carrier injection, the leading degradation mechanism in MOSFETs that takes place during operation, hydrogen start to dissociate at the Si/SiO_2-interface, leaving behind defects. This thesis investigates how to repair these hydrogen-related defects, accelerate the recovery process and go back to the initial, fresh state of a device. In a product, the hydrogen that is present in the chip due to the various processing steps can be used to recover the operation

induced damage. In this thesis we also investigate the impact of supplying extra hydrogen at various pressures, an effect that mimics the impact of packaging chips in a H-rich environment.

Generally, the recovery of hot-carrier induced damage depends on the amount of hydrogen present for repassivation, the anneal time and anneal temperature. Experiments done in this thesis showed that recovery takes place at temperatures lower than those during fabrication and that an external supply of hydrogen will enhance the recovery rate, even at low pressures (mbar). More recovery was achieved when the hydrogen ambient pressure was increased. Furthermore, other material considerations, such as a capping layer on top of the device that may act like a diffusion barrier, influence the effective recovery rate.

The recovery seems to fit reasonably well with an earlier model of hydrogen passivation proposed by Stesmans, in which the passivation rate at the Si/SiO_2-interface can be described in terms of anneal time, anneal temperature, hydrogen concentration in the device and some material/technology specific parameters. However, experiments showed that Stesmans' model does not show the whole picture. Subsequent cycles of partial degradation/recovery may lead to a different energy distribution in Si-H bonds, making the recovery of each degradation/recovery cycle different.

Furthermore, hot-carrier injection may also lead to oxide traps. It was found that hydrogen-related defects tend to recover faster/more easily than oxide-related defects. As a consequence, this finding may lead to that after multiple partial degradation/recovery cycles, damage can be attributed more and more to oxide-related traps, where the recovery process behaves according to a different mechanism.

One of the earlier solutions to minimize degradation during the stress phase was to use deuterium instead of hydrogen as a passivation species. These silicon-deuterium bonds at the Si/SiO_2-interface are more resilient to hot-carrier stress, which will result in an increased lifetime for the transistor. Experiments described in this thesis suggest that this is only the case for the first degradation cycle. The recovery step may use a combination of hydrogen and deuterium to repassivate the bonds, making the device look more and more like hydrogen passivated devices after subsequent degradation/recovery cycles.

In conclusion, the recovery rate of a hot-carrier degraded transistor is influenced by various parameters like temperature and hydrogen concentration. Various tests have been performed as a first step on the road to a device that can repair itself. However, to induce healing in commercial chips, some of the requirements are that the recovery enhancements should be done internally (no external supply) and at the operation temperature, so that it would not damage the other internal structures of the chip. This would make a self-healing chip viable, that can recover at normal operating temperatures, ultimately leading to a more reliable and potentially faster device.

Samenvatting

Computerchips worden tegenwoordig gebruikt in allerlei industrieën en toepassingen, van communicatie, transport tot gezondheidszorg. Ze zijn een belangrijk onderdeel van ons dagelijks leven. De bouwsteen van elke computerchip is de transistor, waar technologische ontwikkelingen in de transistor hebben geleid tot kleinere en snellere chips dan ooit tevoren. Transistors zijn tegenwoordig zo belangrijk en alomtegenwoordig dat ze onmisbaar zijn om onze samenleving draaiende te houden.

Omdat transistors steeds kleiner worden en er meer van ze wordt gevraagd, zijn ze ook kwetsbaarder geworden voor beschadigingen. Uiteindelijk kan dit leiden tot het uitvallen van de hele computerchip en hierop volgend, de elektronica. Fabrikanten van elektronica streven ernaar om een levensduur van tenminste 10 jaar te garanderen. Een belangrijk onderdeel van ontwikkelingen op het gebied van transistors is het voorkomen danwel minimaliseren van beschadigen in transistors.

Wanneer het mogelijk is om de transistors te repareren en beschadigingen of defecten te verwijderen, dan zou een transistor weer als nieuw zijn. De mogelijkheid om een transistor te repareren kan leiden tot een computerchip dat een langere levensduur heeft, met een hogere snelheid werkt en over het algemeen betrouwbaarder werkt.

De MOSFET (Metaal-Oxide-Halfgeleider Veld-Effect-Transistor) is de meest gebruikte transistor, waarbij de fabrikant een chip met zo min mogelijk defecten probeert op te leveren, om de levensduur en het gebruik van de chip te optimaliseren. Een van de problemen die zich kan voordoen tijdens de fabricage van een MOSFET, wanneer het gatediëlektricum (het oxide in de MOSFET, in dit proefschrift SiO_2) wordt gedeponeerd bovenop het halfgeleidersubstraat (in dit proefschrift Si): niet alle Si-atomen in het Si/SiO_2-grensvlak kunnen een binding maken met atomen in het gateoxide, wat leidt tot halfgebonden Si-atomen. Aangezien deze halfgebonden bindingen als een ladingsval kunnen dienstdoen, kunnen ze de transistorparameters verstoren en is het nodig om een na-verhittings stap uit te voeren om de halfgebonden bindingen te binden (passiveren) met waterstof.

Hete-ladingsdrager injectie, een van de degradatiemechanismes die tijdens gebruik kan plaatsvinden, kan ertoe leiden dat het waterstof begint los te laten van de Si-atomen, waardoor Si-defecten worden geïntroduceerd. In dit proefschrift wordt onderzocht hoe deze waterstof gerelateerde defecten kunnen worden hesteld, hoe het herstelproces kan worden versneld en hoe de

transistor terug kan gaan naar de oorspronkelijke staat. Voor het herstelproces kan waterstof worden gebruikt dat al in de gate-stack aanwezig is vanwege verschillende fabricageprocessen waarbij waterstof betrokken is.

In het algemeen is het herstelproces afhankelijk van de aanwezige waterstof en van de temperatuur. Experimenten die in dit proefschrift zijn beschreven, hebben aangetoond dat herstel plaatsvindt bij temperaturen die lager zijn dan tijdens fabricage en dat een externe toevoer van waterstof de herstelsnelheid zal verhogen, zelfs bij kleine hoeveelheden. Een groter herstel werd geobserveerd, wanneer de waterstofomgevingsdruk werd verhoogd. Bovendien kunnen andere materiaaloverwegingen, zoals een afdeklaag bovenop de transistor die dienst kan doen als een diffusiebarrière, van invloed zijn op de effectieve herstelsnelheid.

Het herstelproces lijkt goed te kunnen worden beschreven met behulp van een eerder, door Stesmans voorgesteld, model van waterstofpassivering. Experimenten toonden echter ook aan dat het model van Stesmans niet alles beschrijft. Opeenvolgende cycli van gedeeltelijke degradatie/herstel kunnen leiden tot een andere energieverdeling in Si-H-bindingen, waardoor het herstel van elke degradatie/herstelcyclus anders is.

Bovendien kan de injectie van hete-ladings dragers leiden tot oxidedefecten. Experimenten lieten zien dat waterstofgerelateerde defecten zich sneller en gemakkelijker laten herstellen dan oxidegerelateerde defecten. Dit suggereert dat na meerdere gedeeltelijke degradatie/herstelcycli, de schade in de transistor meer en meer kan worden toegeschreven aan oxidegerelateerde defecten, waar het herstelproces zich gedraagt volgens een ander mechanisme dan voor waterstofgerelateerde defecten.

Een van de eerdere oplossingen om degradatie tijdens de stressfase tot een minimum te beperken, was het gebruik van deuterium in plaats van waterstof als passiveringsmiddel. Deze waterstofisotoop is beter bestand tegen stress door hete-ladingsdragers en de transistor heeft een langere levensduur. Experimenten in dit proefschrift hebben aangetoond dat dit alleen het geval is voor de eerste degradatiecyclus. Bij de herstelstap wordt een combinatie van waterstof en deuterium gebruikt om de bindingen opnieuw te passiveren, waardoor de transistor na opvolgende degradatie/herstelcycli steeds meer op een waterstofgepassiveerde transistor gaat lijken.

De conclusie kan worden getrokken dat de herstelsnelheid wordt beïnvloed door verschillende electrische parameters zoals temperatuur en waterstofconcentratie. Door middel van verschillende experimenten is de eerste stap gezet naar een transistor die zichzelf kan repareren. Om het herstelproces in commerciële chips uit te voeren, moeten de reparaties echter intern worden uitgevoerd (geen externe waterstoftoevoer) en bij lagere temperaturen die de rest van de chip niet beschadigen. Als dit te verenigen is in transistors, dan zou een zelfherstellende chip mogelijk zijn, die kan herstellen bij normale operatietemperaturen, wat uiteindelijk leidt tot een betrouwbaardere computerchip.

Contents

CHAPTER 1

Introduction

The evolution in microprocessors and transistors technology has led to many changes in society and a world that cannot be envisioned without the use of transistors. From the mundane, like a coffee machine, to the growing field of computer-assisted, completely autonomous driving cars, transistors have become more and more ubiquitous and an important tool to make everything in society work.

Just as any other tool that is used, microprocessors can get damaged and break down over time. The durability of transistors is determined by how often and under what conditions they are used. Generally, the manufacturer aims for an expected lifetime of around $\sim$10 years of continuous operation, *e.g.* see [1]. The lifetime will be reduced if they are used more than expected or if more is asked of them than expected (*e.g.* overclocking, more extreme operation conditions).

Earlier research has focussed to minimize the number of defects in transistor devices during the fabrication process, where the aim is to have as small a risk as possible to breakdown [2, 3]. Although the number of defects is minimized during fabrication, failure and breakdown can take place before the expected end-of-life is reached. Right after fabrication, devices may show a higher failure rate (infant or early end-of-life failures), which may be explained by material variations introduced during the fabrication processes. Most devices with infant failures can be eliminated right after fabrication if a testing phase is used (burn-in), wherein devices susceptible to early stress are identified and removed before they are sold commercially.

Random failures can take place in a device during its useful lifetime and these failures tend to have a constant failure rate. Lastly, over time, intrinsic degradation mechanisms start to take place, which lead to wear-out failure. The different stages of failure mechanisms are shown in Figure 1.1, where the shape of the cumulative failure can be described by the so-called Bathtub curve [3].

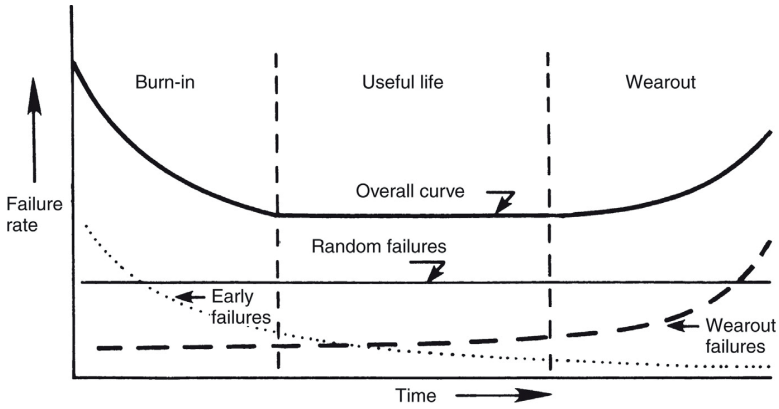

Figure 1.1: Bathtub curve to describe failure rates in general (including transistors). Image by [3].

The various degradation mechanisms will lead to structural changes at device level and may lead to oxide breakdown. *E.g.* Hot-Carrier Injection (HCI), Bias Temperature Instability (BTI), Stress-Induced Leakage Current (SILC) and Time-Dependent Dielectric Breakdown (TDDB) [4]. SILC and TDDB may lead to various oxygen-related defects in the gate dielectric, which may subsequently lead to soft or hard breakdown. The degradation mechanisms related to the topic of this thesis, HCI and BTI, could cause hydrogen related defects at the Si/SiO_2-interface between the substrate and the gate dielectric as well as defects in the gate dielectric (oxide related traps, (de-)charging). These kinds of degradation mechanisms are responsible for the wearout defects of Figure 1.1.

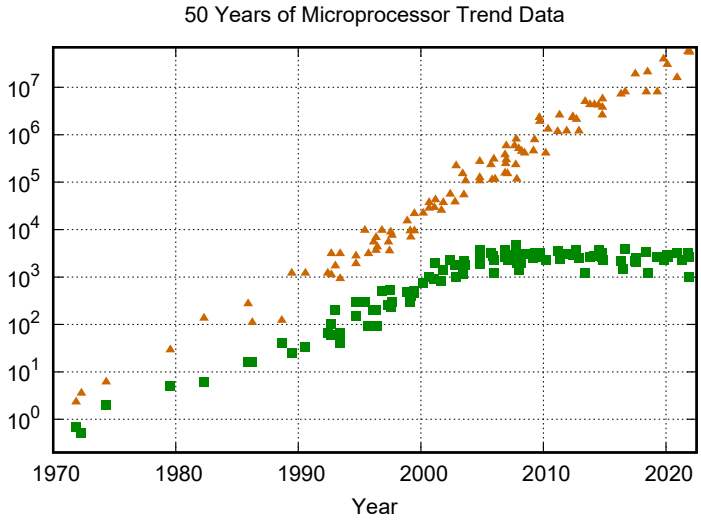

Figure 1.2: The trend of various microprocessor components/parameters over time. Transistors (thousands) is in orange and Processor Frequency (MHz) is in Green. Image by Karl Rupp [5].

The evolution of transistors moves to smaller and faster devices, which tend to go hand in hand with a higher susceptibility to degradation mechanisms. Due to the necessity of balancing fast, small and reliable microprocessors, some parameters that define microprocessors have started to flatten out over time, see Figure 1.2. Degradation and the creation of new defects are then at a manageable level during its operational life. Completely circumventing degradation is however not possible.

When something breaks down, from coffee machines to cars, it is often possible to repair them and extend their lifetime. Similarly, research in different fields has been done to investigate self-repair and self-healing in certain materials, *e.g.* concrete and polymers [6, 7], extending the time to failure. Similar to microelectronics, when defects in transistors can be repaired, whether completely or partially, it would be beneficial for both the lifetime and the performance of a device. Depending on how and how often the repair step can be executed, certain physical limitations due degradation mechanisms may diminish, can be ignored if different degradation mechanisms take over the leading role in lifetime predictions, or will completely disappear. This would lower the wearout failures of Figure 1.1, lowering the failure curve and it would eventually lead to a self-healing transistor.

Problem Statement

The main objective of this thesis is the investigation of various methods to induce and enhance the recovery rate of hydrogen-related defects at the Si/SiO_2-interface in devices, that have been electrically degraded by hot-carrier injection. This is done in the pursuit of creating a self-healing device [8] that has an infinite (or at least extended) lifespan due to various recovery mechanisms that remove/repair hydrogen-related defects.

Recovery in a single transistor using an external source would lead to practical problems when it is scaled up to 10^9s of transistors that are present in a single microprocessor (Figure 1.2). Ideally, a transistor can be made that has all the materials and recovery mechanisms present internally and no outside material or recovery method needs to be applied to the device to repair the damage. In this thesis, various experiments have been done to investigate what has a positive or negative influence on the recovery rate of hot-carrier degraded devices.

Thesis Outline

In **Chapter 2**, *Device Characteristics and Characterization*, the basic operations of a MOSFET device and the various methods of parameter extraction are discussed. The threshold voltage, linear drain current, transconductance and subthreshold voltage are determined using IV-measurements. The charge-pumping method and how it can be used to determine the interface defect concentration will be explained. Lastly, some considerations that had to be

taken into account due to constraints of the experimental setup will be mentioned as well as the influence of temperature on the measurement process.

In **Chapter 3**, *The Role of Hydrogen*, the role of hydrogen in the device and at the Si/SiO_2 interface will be discussed. Furthermore, the various ways fabrication materials may affect the hydrogen concentration and transport will be addressed.

In **Chapter 4**, *Degradation*, the theoretical background of various degradation mechanisms that may take place will be discussed. The main focus in this thesis is degradation by hot-carrier injection which will be discussed most extensively. Other degradation mechanisms that may affect the devices under study will also be addressed. *I.e.* BTI, which may also take place when a device is stressed under the used HCI stress conditions, as well as some oxygen-related defects, which may have similarities with degradation caused by SILC and TDDB. Another topic addressed in this chapter is annealing and exposure to plasma, which might have a positive influence on the recovery rate but can also induce degradation in the device under certain circumstances.

In **Chapter 5**, *Enhancing Recovery*, recovery of hot-carrier induced degradation is discussed in combination with various methods and conditions that may affect the recovery rate. Various experiments have been done to investigate the effect of bias during recovery, exposure to light, gate length, cooling rate after anneal, anneal temperature and various ambients (Hydrogen, Nitrogen, Plasma). The main anneal temperature of interest was around $T_a = 150 - 200$ °C, the temperature where roughly 50% recovery takes place within a reasonable timescale (maximum of $\sim$2 weeks). This way, both the positive and negative influence on the recovery rate can be investigated.

In **Chapter 6**, *Recovery: Fast versus Slow Traps*, the degradation and recovery behavior of hydrogen-related interface defects in combination with other (oxygen-related) bulk defects are discussed. Hot-carrier injection was used to induce degradation, and recovery was induced by annealing in air on a thermochuck.

In **Chapter 7**, *Influence of the Stress Phase on the Stress/Recovery Cycles*, the isotope effect and the effect of multiple degradation/recovery cycles will be discussed. Experiments have been done to investigate what happens during the recovery phase of a deuterium-passivated device and if the frequency of degradation/recovery cycles, *i.e.* the time per cycle, influences on the cumulative lifetime of a device.

The final conclusions and recommendations will be given in **Chapter 8**.

CHAPTER 2

Device Characteristics and Characterization

This chapter provides an overview of the theoretical background of the MOSFET and the various characterization techniques that have been used to identify the role of hydrogen in the reliability of a device. In 1959 Mohamed M. Atalla and Dawon Kahng manufactured the first metal-oxide-semiconductor field-effect transistor (MOSFET) [9] by combining the growth of a metal gate on top of a silicon dioxide layer on a silicon (semiconductor) substrate with two *pn*-junctions. Earlier contributors to variants of the FET (*e.g.* Lilienfeld) had difficulty with the fabrication of a good quality semiconductor and interface. However, improvements in crystalline silicon and the thermally grown oxide layer on top ensured that the number of defects at the Si/SiO_2-interface reduced significantly, enough to ensure the fabrication of a reliable transistor.

Since the silicon substrate is crystalline and the gate oxide is amorphous, not all defects can be removed at the interface and a significant number of dangling bonds will still be present. The number of dangling bonds reduced even further in the next generations of MOSFET, after an anneal in hydrogen forming gas was introduced, which passivated more of the dangling bonds at the interface, see Chapter 3. Figure 2.1 shows the schematic representation of a four-terminal MOSFET device, with the four terminals: bulk/substrate, source, drain and the gate.

2.1 Current-Voltage Behavior

This section describes the IV-behavior of a MOSFET, specifically an nMOSFET. A short overview will be given on how to characterize a MOSFET [2, 10] and acquire the parameters of interest to investigate the reliability of a device.

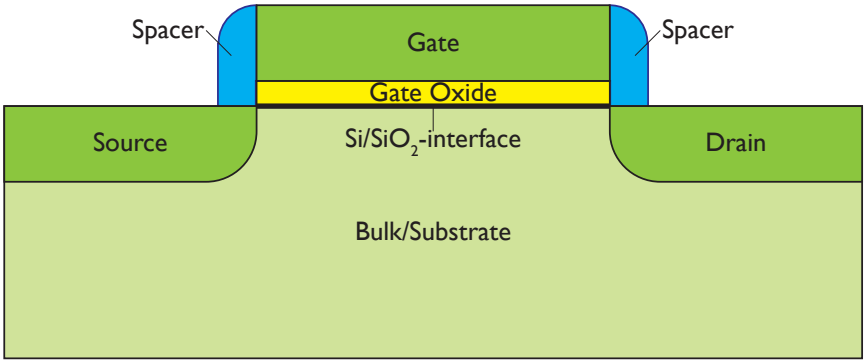

Figure 2.1: Schematic cross-section of a MOSFET.

2.1.1 Device

When a MOSFET is turned on and current flows from the source to the drain, there are two main operation regimes. When the gate-source voltage (V_{gs}) is increased, minority charge carriers will be introduced in the bulk and the MOSFET moves via depletion to weak inversion and eventually strong inversion. The current behavior is shown in Figure 2.2 on a linear and logarithmic scale for both regimes, separated by a transition regime where the device goes from weak into strong inversion. The transition occurs when V_{gs} becomes higher than the threshold voltage (V_t). The strong inversion regime can be in the linear or saturation regime, depending on the applied drain-source bias [2, 10--12].

Subthreshold regime

The subthreshold regime is the weak inversion regime, where the applied gate-source voltage is not sufficient to induce strong inversion ($V_{gs} < V_t$). The left side of Figure 2.2 shows the subthreshold regime, where the drain current, I_d, increases as a function of V_{gs}. The drain current depends exponentially on the gate-source voltage and can be described by the equation:[13, 14]

$$I_d = \frac{\mu W}{L}(C_{ox} + C_{dep} + C_{it})(\frac{k_b T_m}{q})^2 \times \exp\left(\frac{C_{ox}}{C_{ox} + C_{dep} + C_{it}} \frac{q(V_{gs} - V_{t,0})}{k_b T_m}\right)\left(1 - \exp(-\frac{qV_{ds}}{k_b T_m})\right). \quad (2.1)$$

where V_{t0} is the threshold voltage when there is no drain-source and bulk-source bias ($V_{ds} = V_{bs} = 0$), μ is the charge carrier mobility, T_m is the measurement temperature, C_{ox} is the oxide capacitance per unit area, C_{it} is the fast interface defects capacitance per unit area and C_{dep} is the capacitance of the depletion layer per unit area defined by:

$$C_{dep} = \sqrt{\frac{\kappa_{Si} q N_A}{2(\phi_s - V_{bs})}}, \quad (2.2)$$

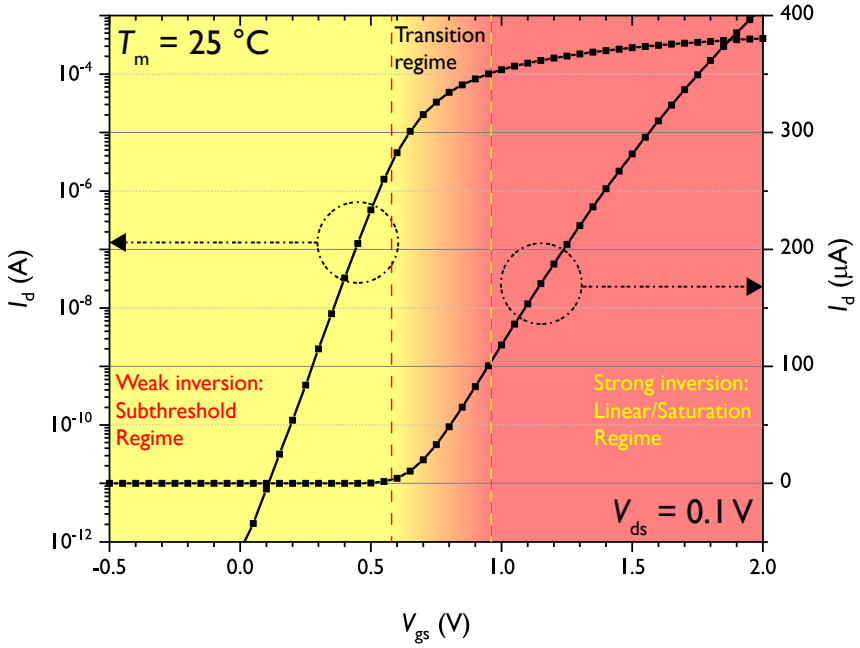

Figure 2.2: A typical IV-curve of an nMOSFET in the linear regime on linear (right) and logarithmic scale (left). The color schemes indicate the transition from weak inversion (yellow) to strong inversion (red) ($W_g = 10.0$ µm, $L_g = 0.5$ µm and $t_{ox} = 7$ nm).

where N_a is the acceptor doping in the channel region, ϕ_s is the surface potential and κ_{Si} is the dielectric constant of silicon. Equation 2.1 gives a good quantitative description of the drain current in the subthreshold regime, however, it will not be completely accurate. Due to various effects, there may be a deviation, *e.g.* μ is not constant and will change if a higher V_{gs} is used due to charge carrier collision with the Si/SiO_2-interface by the changing transversal electric field [15].

Subthreshold Swing

The subthreshold swing (SS) can be defined in the subthreshold regime. It indicates the increase in V_{gs} needed to increase I_d one order of magnitude in the subthreshold regime, *i.e.* how easily a device can be turned on/off. At room temperature, the subthreshold swing will be in the order of $SS = 70 - 100$ mV/dec. Using Equation 2.1, the subthreshold swing can be described by [16]:

$$\begin{aligned} SS &= \ln(10)\frac{k_b T}{q}\left(1 + \frac{C_s + C_{it}}{C_{ox}}\right); \\ &= \ln(10)\frac{k_b T}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right), \end{aligned} \tag{2.3}$$

where it is assumed that the capacitance in the channel per surface area (C_s) can be neglected in the depletion regime. In this thesis, the subthreshold swing

is extracted from the IV-curves by taking two I_d values in the subthreshold regime:

$$SS = \frac{\Delta V_{gs}}{\Delta \log(I_d)} = \frac{V_{gs,high} - V_{gs,low}}{\log(I_{high}(V_{gs,high})) - \log(I_{low}(V_{gs,low}))}. \tag{2.4}$$

Linear regime

The linear regime (right in Figure 2.2) is when the drain-source voltage is $V_{ds} < V_{gs} - V_t$. Under this condition, it is assumed that the charge in the channel is uniformly distributed, where the total charge in the channel is defined as:

$$Q_{channel} = C_{ox}(V_{gs} - V_t), \tag{2.5}$$

where C_{ox} depends on the gate thickness, t_{ox} and the dielectric constant in the gate oxide, κ_{ox} via:

$$C_{ox} = \frac{\kappa_{ox}}{t_{ox}}. \tag{2.6}$$

The total current at the drain can then be calculated by:

$$I_d = Q_{channel} W_g \mu \mathcal{E}_{ds}. \tag{2.7}$$

Using the lateral electric field in the channel between the source and drain ($\mathcal{E}_{ds} = V_{ds}/L_g$) and average potential ($\frac{V_{ds}}{2}$), the drain current in the linear regime can be described as:

$$I_d = \mu \frac{W}{L} C_{ox} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}. \tag{2.8}$$

Equation 2.8 is valid under small V_{ds} conditions ($V_{ds} < V_{gs} - V_t$) and a long channel MOSFET shows a linear dependence on V_{gs}, where a higher V_{gs} result in a higher electron concentration and a higher V_{ds} in a higher lateral field.

Saturation regime

When the drain-source voltage is increased while keeping $V_{gs} - V_t$ constant, Equation 2.8 changes. When the V_{ds} is increased above a certain level ($V_{ds} = V_{ds,sat}$), the gate-source voltage is not sufficient enough to induce strong inversion in the channel near the drain. The effective channel length is based on the distance between the source and the point where strong inversion cannot be induced anymore: pinch-off. Since Equation 2.8 is based on the channel length, the effective channel length decreases ($L_{g,eff} < L_g$). Between the pinch-off point and the drain a region in depletion is induced, where the charge carriers do not gain a higher group velocity above the saturation voltage, regardless of the lateral electric field. The drain-source voltage or the saturation voltage where pinch off takes place is defined as:

$$V_{ds,sat} = V_{gs} - V_t. \tag{2.9}$$

Saturation of the drain current results in a drain current of: $I_{d,sat} = I_{d,lin}(V_{ds} = V_{ds,sat})$. Combining Equation 2.9 and Equation 2.8, the drain current in the saturation regime can be found (Equation 2.11).

The drain current in the two post threshold regimes can be summarized in the Square Law Model for MOSFET drain current as:

$$I_d = \mu C_{ox} \frac{W_g}{L_g}(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} \qquad |V_{gs} > V_t; V_t, V_{ds} < V_{ds,sat}; \tag{2.10}$$

$$I_d = \mu C_{ox} \frac{W_g}{2L_{g,eff}}(V_{gs} - V_t)^2 \qquad |V_{gs} > V_t; V_t, V_{ds} > V_{ds,sat}. \tag{2.11}$$

All parameters and the characterization from the IV-curve are summarized in Figure 2.3, where the points, SS_{min} and SS_{max}, used to calculate the subthreshold swing are shown in red (Equation 2.4), and how the point of $g_{m,max}$ (Figure 2.4) is used to find the threshold voltage using the extraction from the linear regime method.

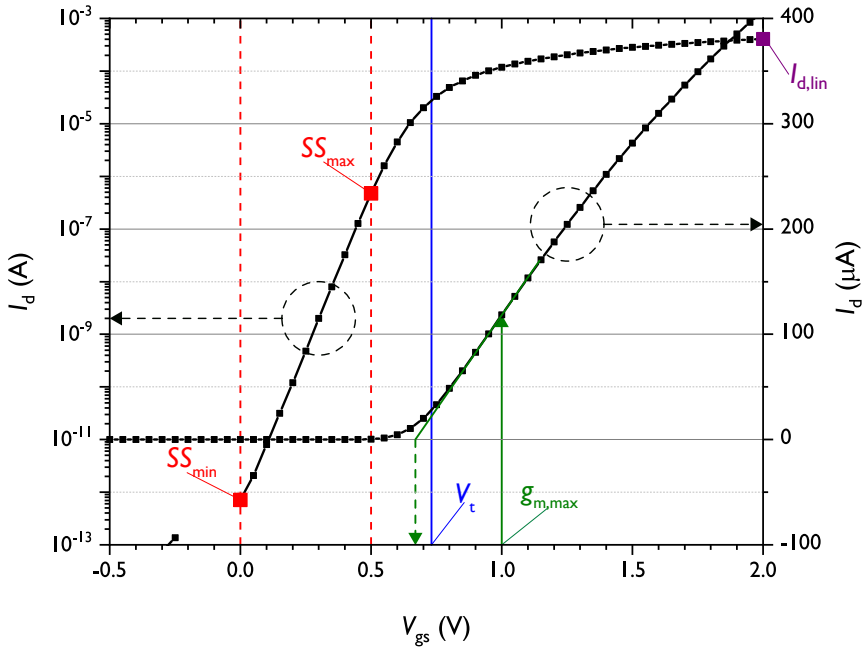

Figure 2.3: IV-behavior on log and linear scale to determine the subthreshold swing (red), the linear drain current at $V_{gs} = 2.0$ V (purple), the threshold voltage (blue) using the position of the maximum transconductance (green).

Transconductance

To measure the threshold voltage in this thesis, the extraction from the linear regime (ELR) method is used, which uses the point of maximum transconductance in the IV-curve. The transconductance or mutual conductance, g_m is used as a measure for the relation between the flux of charge carriers in the

channel and the gate-source voltage. The transconductance for long-channel devices can be calculated by taking the derivative of the drain current, or the derivation of Equation 2.8 and Equation 2.11 to V_{gs}:

$$g_m = \frac{\partial I_{d,lin}}{\partial V_{gs}} = \mu \frac{W_g}{L_g} C_{ox} V_{ds} \quad \text{|Linear Regime;} \tag{2.12}$$

$$= \frac{\partial I_{d,sat}}{\partial V_{gs}} = \mu \frac{W_g}{L_{g,eff}} C_{ox} (V_{gs} - V_t) \quad \text{|Saturation Regime.} \tag{2.13}$$

Equation 2.12 and Equation 2.13 describe the transconductance in different regimes, but assumes that the various parameters do not change in the transition regime [17]. Figure 2.4 shows the transconductance from Figure 2.2 as a function of V_{gs}. The maximum transconductance of this device can here be found at $V_{gs} = 1$ V, $g_{m,max} \approx 350$ µA/V.

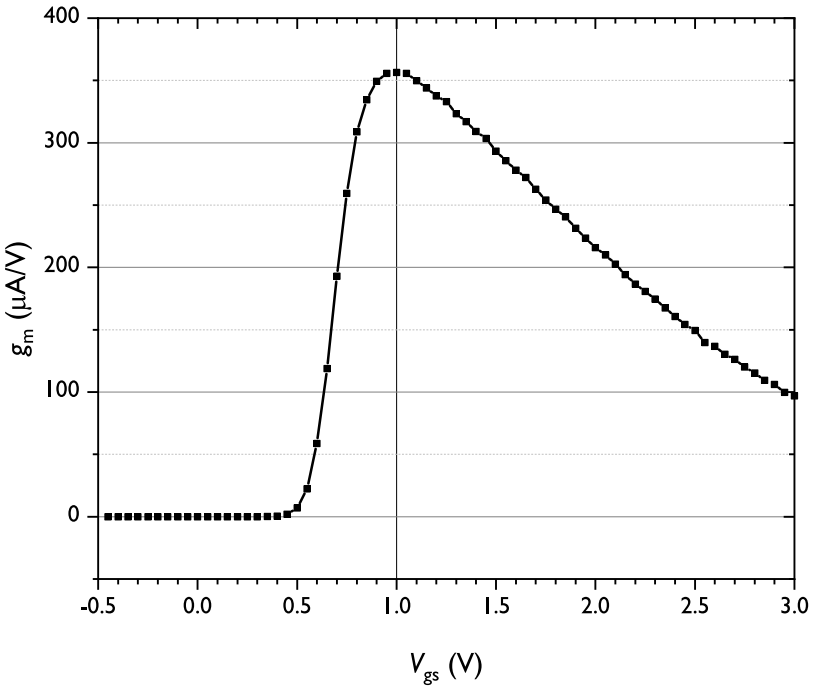

Figure 2.4: The transconductance g_m as a function of the gate-source voltage of Figure 2.2.

Since various threshold voltage extraction methods result in different V_t values (even if the same dataset/transistor is used) [18], only one extraction method is used in this thesis (ELR) [18]. The extraction method uses the linear extrapolation from the I_d-V_{gs} curve from the point of maximum transconductance ($g_{m,max}$) to the intercept with the V_{gs} axis (where $I_d = 0$). Combining Equation 2.8 and Equation 2.12, V_t can then be found by subtracting $\frac{V_{ds}}{2}$ from the found V_{gs} of the intercept.

Threshold voltage

The threshold voltage is the parameter that denotes the transition regime, or when a device goes from weak into strong inversion and the device is turned on [2]. When a bulk-source bias, V_{bs} is applied (the depletion region would change) and the effect of the difference in work function or the contribution of fixed oxide charges to V_t are taken into account, the general equation for the threshold voltage can be found:

$$V_t = V_{fb} + 2\phi_b + \frac{\sqrt{2q\kappa_{Si}N_s(2\phi_b + V_{bs})}}{C_{ox}}, \tag{2.14}$$

where the bulk potential is denoted by ϕ_b. To compensate for potential oxide charge, the flat band voltage, V_{fb}, is included, which is defined as:

$$V_{fb} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot} + Q_{it}}{C_{ox}}, \tag{2.15}$$

where ϕ_{ms} is the work function difference between the metal and the silicon, Q_f is the total fixed charge in the gate oxide, Q_m is the total mobile charge in the gate oxide, Q_{ot} is the total charge due to the oxide/border traps and Q_{it} is the total charge due to the interface states.

2.1.2 Temperature Dependency

The IV-behavior of a MOSFET is strongly affected by the measurement temperature, T_m [19]. Figure 2.5 shows the IV-curves of a fresh, undegraded device measured at different temperatures. When the various parameters are extracted, a temperature-dependent shift can be observed (see *e.g.* Equation 2.3 and Equation 2.1).

Figure 2.6 shows the temperature dependence of the various parameters. A higher T_a will cause a negative shift in ΔV_t, Δg_m and $\Delta I_{d,lin}$ and a positive ΔSS. When these parameters are compared to the values after degradation and recovery at different temperatures, the measurement temperature has to be taken into account. *I.e.* the shift of the parameters due to T_m competes with the shift due to degradation or recovery.

2.1.3 Degradation

Degradation (recovery) of a device will increase (decrease) in the subthreshold swing (Equation 2.3) and is indicative of the number of interface defects that are created (recovered). Similarly, degradation (recovery) will result in a decrease (increase) of the transconductance in the linear regime (Equation 2.12). Similar to the transconductance, the drain current (Equation 2.8 and Equation 2.11) in subthreshold, linear and saturation regime will decrease (increase) due to degradation (recovery).

Since the threshold voltage calculated by the ELR method uses the maximum slope of the I_d-V_{gs} curve, the curve will deviate when the transconductance and

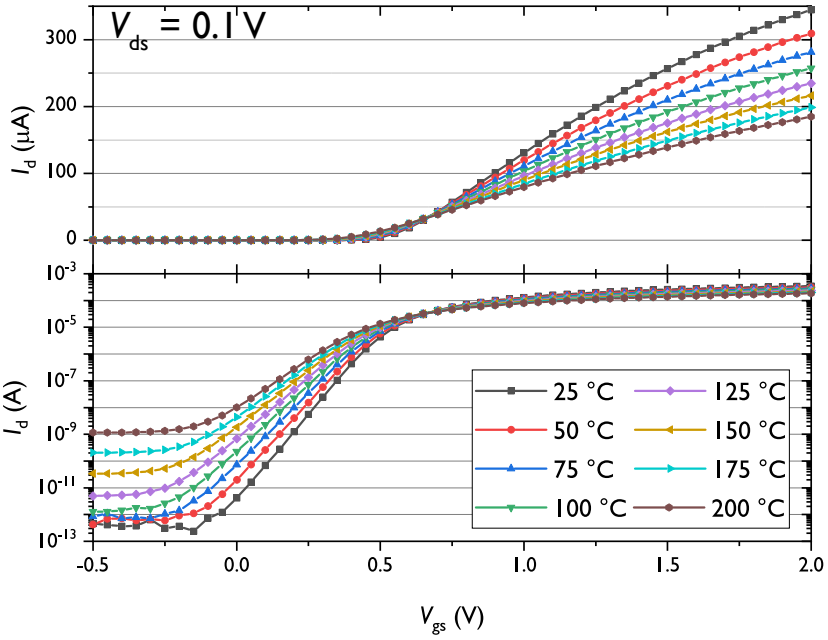

Figure 2.5: The *IV*-behavior of a fresh, undegraded device as the function of the measurement temperature on linear (top) and logarithmic (bottom) scale.

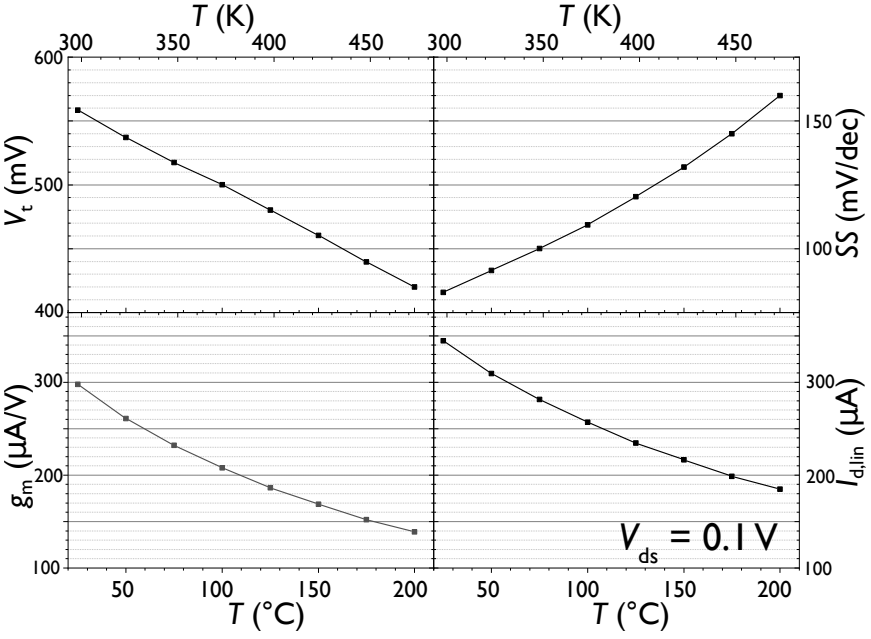

Figure 2.6: The dependence of V_t (top-left), SS (top-right), $g_{m,max}$ (bottom-left) and $I_{d,lin}$ (bottom-right) as a function of T_m.

the drain current start to shift due to degradation (recovery). As a consequence, the threshold voltage is strongly influenced by defects and mobility degradation due to an increase in coulomb scattering [20], inducing a positive (negative) shift when degradation (recovery) takes place. Furthermore, when due to degradation mechanisms more interface defects are introduced, the various regimes in the IV-curve start to shift, the various parameters values will shift, which may eventually lead to device/circuit breakdown.

Although some variability in the shift in V_t [21] exists after degradation by HCI and BTI, the shift in the threshold voltage is directly related to the introduction of new interface defects, when is assumed that the other defects of Equation 2.15 do not play a significant role:

$$\Delta V_t = \Delta V_{t,it} = -\frac{\Delta Q_{it}}{C_{ox}} \rightarrow \tag{2.16}$$

$$\Delta N_{it} \propto \Delta V_t. \tag{2.17}$$

The shift in the threshold voltage is related to the number of created/recovered interface defects according to Equation 2.17. Although the threshold voltage (and other parameters) are indicative of the number of hydrogen-related interface defects (as described above), trapped charges, bulk (oxide) defects (ΔN_{ot}) and other defects may influence the measurement and distort the (calculated) number of interface defects. This raises the question of whether this relation can be used and will be further experimentally investigated in Chapter 6. The charge-pumping method can be used to only measure interface states and will be discussed in the next section.

2.2 Charge Pumping

An easy approach to characterize a device was described in Section 2.1, however, the method does not differentiate easily between different defects (Equation 2.15). A more direct approach to measure the defect density at the interface (N_{it}) accurately is the charge-pumping (CP) method, which correlates the substrate current directly to the interface defects.

2.2.1 Theory

The CP-method was first proposed in 1969 by Brugler and Jespers as a method to relate the number of defects at the Si/SiO_2-interface to the current measured at the substrate [22]. Groeseneken *et al.* published in 1984 a paper with the theoretical explanation and background of the process [23], making the CP-method a reliable, direct and easy method to measure the interface defect density.

The method consists of applying voltage pulses to the gate and switching the MOSFET between inversion and accumulation. During inversion, minority carriers (electrons for nMOS) will flow from the source and drain into the channel region. Some of these charge carriers get trapped in defects at the interface. When the device is then pulsed back from inversion into accumulation, the mobile charges will drift back to the source and drain, while the trapped charges will recombine with the majority carriers (holes for nMOS) [23]. This leads to a net (dc) current towards the channel, which can be measured at the substrate. The CP process and experimental setup are schematically visualized in Figure 2.7. When the device is in inversion ($V_{g,h} > V_t$, blue) minority carriers are injected in the channel from the source and drain and get trapped in defects. When the device is pulsed into accumulation ($V_{g,l} < V_{fb}$, red), majority carriers recombine with the trapped charges, resulting in the bulk current.

Assuming that all interface defects will act as a recombination center for the charge carriers and that the remaining minority carriers will flow back into the source and drain, the total charge attributed to the CP-method, Q_{cp}, is defined as:

$$Q_{cp} = A_g \cdot q \int D_{it}(E)\mathrm{d}E, \tag{2.18}$$

where A_g is the gate area of the MOSFET ($A_g = W_g \cdot L_g$), q is the elementary charge and D_{it} is the interface defect density per unit area at energy level E. Note: in this equation it is assumed that other types of defect do not play a role, see Equation 2.26.

The three main CP-methods are **Method A**: the constant voltage amplitude method, **Method B**: the constant voltage base ($V_{g,l}$) method ($V_{g,l}$ always in accumulation) and **Method C**: the constant voltage top ($V_{g,h}$) method ($V_{g,h}$ always in inversion).

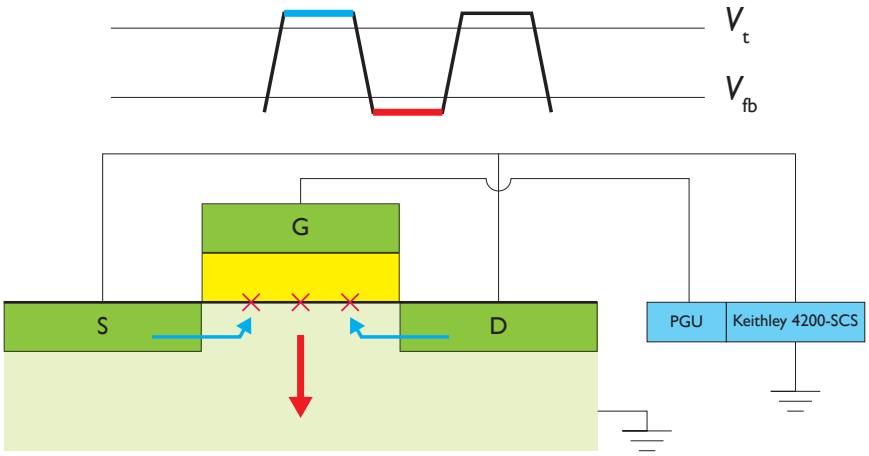

Figure 2.7: Summary of the CP method. Blue: $V_{g,h}$ is above V_t and minority charge carriers are injected into the MOSFET from the source and the drain. Red: $V_{g,l}$ is below V_{fb}. The majority charge carriers recombine with the trapped charges resulting in a current proportional to the number of defects that can be measured at the substrate.

Method A is shown in Figure 2.8 as a function of $V_{g,l}$, where the pulse amplitude V_a is kept constant. At the left (right), $V_{g,l}$ is low (high) enough to keep the substrate in accumulation (inversion) over the whole V_a, so no change takes place when the pulse switches from high to low or vice versa (*a* and *e*). When $V_{g,l}$ is lower than V_{fb} and $V_{g,h}$ is higher than V_t, the device shifts between complete accumulation and inversion. Minority carriers are created and are trapped in the interface defects during the inversion phase. During accumulation, majority carriers will arrive at the interface and recombine with the trapped minority carriers, resulting in a substrate current (I_{cp}), where the maximum current is at *c*.

The CP current depends proportional to the number of defects that can act as a charge trap and recombination center at the interface, N_{it}. Using Equation 2.18, the direct relation between I_{cp}, the frequency of pulses (f_{cp}) and the interface defect density can be found:

$$N_{it} = \frac{I_{cp}}{f_{cp} \cdot A_g \cdot q}. \tag{2.19}$$

The IV-behavior of **Method B** and **Method C** are shown in Figure 2.9. Maximum I_{cp} of **Method B** occurs when $V_{g,h} > V_t$. Maximum I_{cp} of **Method C** occurs when $V_{g,l} < V_{fb}$. Both methods have some advantages compared to **Method A**, *e.g.* information on bandgap and the spatial distribution of defects, [24] or information on defects in a high-κ dielectric [25, 26], however, both methods assume that $I_{cp,max}$ saturates. Constraints due to non-localized defect generation/repair of multiple defects (oxide) (see Section 4), I_{cp} does not saturate under the experimental conditions in this thesis. Under the assumption that the spatial location of the interface defects is not the main focus of this

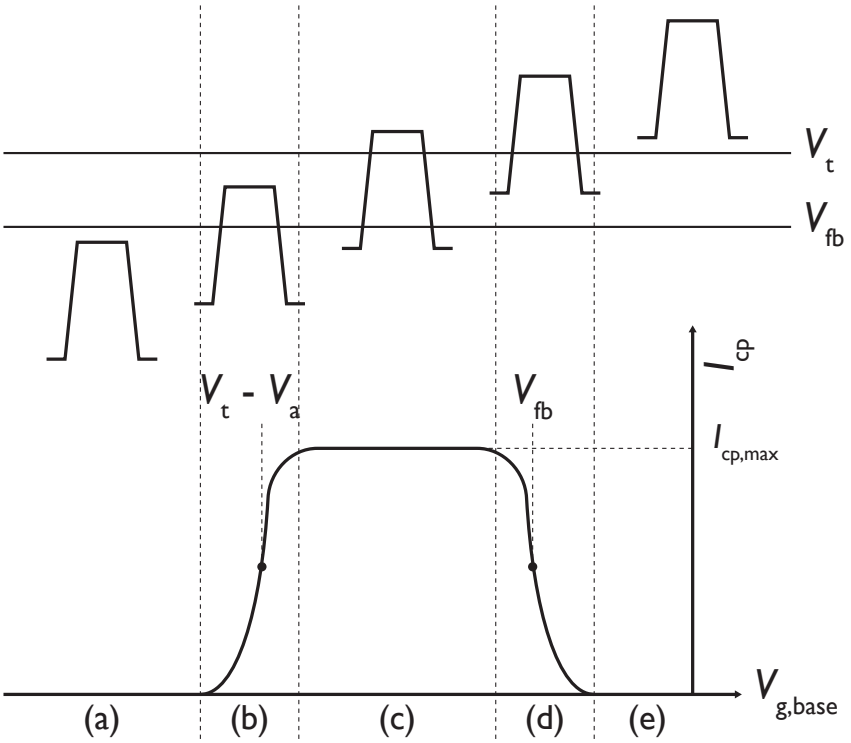

Figure 2.8: Charge pumping current due to the voltage pulse applied to the gate. When the device is pulsed between accumulation and inversion (c), a current proportional to the number of defects that can act as a recombination center can be measured. Image based on [23]

thesis, but the total degradation, and oxide defects are distinguished using the CP-frequency (see Section 2.2.3), **Method A** is chosen in this thesis for data analysis purposes to compare the levels of degradation/recovery of various devices. Note that a combination of **Method A** with **Method B** or **Method C** will result in more extensive approximations on the recovery behavior of interface and oxide traps.

2.2.2 Charge (de-)trapping

The trapping time of charge carriers in the defects can be described by the Shockley-Read-Hall model [27, 28], where the time constants for capture and emission of charge carriers can be described by [22]:

$$\tau_c = \frac{1}{\sigma_{e/h} \nu_{th} n_s}, \tag{2.20}$$

where $\sigma_{e/h}$ is the capture cross section of electrons/holes, n_s is the surface concentration of minority/majority carriers and ν_{th} is the thermal velocity of

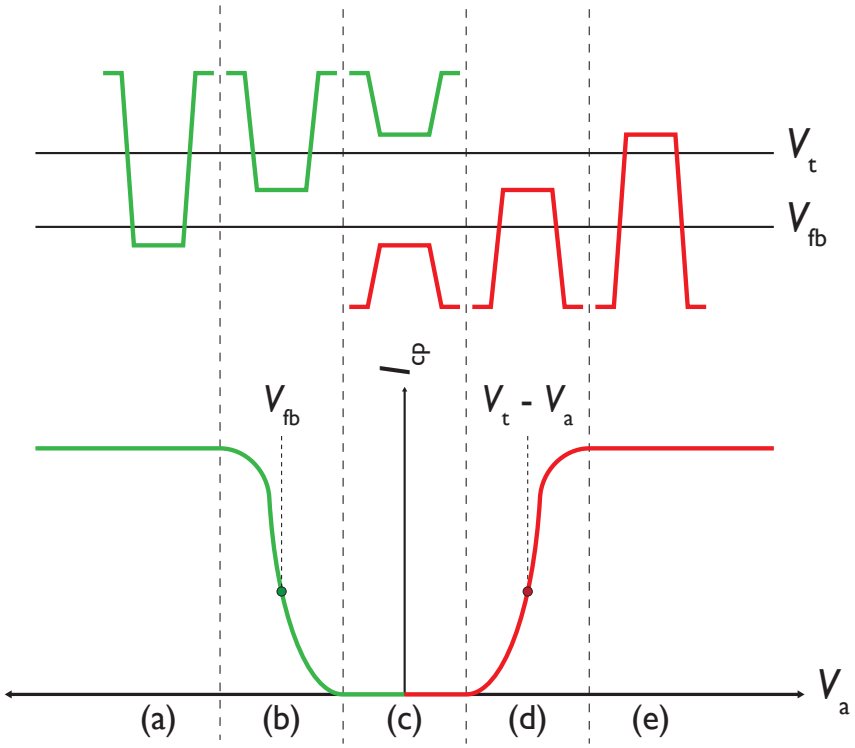

Figure 2.9: Charge pumping current due to the pulse applied to the gate. When a device switches between accumulation and inversion *(c)*, a current proportional to the number of defects that can act as a recombination center can be measured (*(a)* and *(e)*).

the charge carriers defined as:

$$\nu_{\mathrm{th}} = \sqrt{\frac{3k_{\mathrm{b}}T}{m_{\mathrm{n}}}}, \tag{2.21}$$

where m_{n} is the effective mass of an electron. To contribute to the CP current, the defects need to trap the charge carriers for sufficient time. Due to thermal emission, traps that are too close to the valence or conduction band will de-trap immediately when the voltage pulse moves the Fermi level below $E_{\mathrm{em,h}}$ or above $E_{\mathrm{em,e}}$ and do not contribute to I_{cp}. The energy levels between which defects can act as a recombination center and contribute to I_{cp}, are defined by:

$$E_{\mathrm{em,e}} = E_{\mathrm{i}} - k_{\mathrm{b}}T\ln\left(\nu_{\mathrm{th}}\sigma_{\mathrm{e}}n_{\mathrm{i}}t_{\mathrm{em,e}} + \exp\left(\frac{E_{\mathrm{i}} - E_{\mathrm{f,inv}}}{k_{\mathrm{b}}T}\right)\right); \tag{2.22}$$

$$E_{\mathrm{em,h}} = E_{\mathrm{i}} - k_{\mathrm{b}}T\ln\left(\nu_{\mathrm{th}}\sigma_{\mathrm{h}}n_{\mathrm{i}}t_{\mathrm{em,h}} + \exp\left(\frac{E_{\mathrm{i}} - E_{\mathrm{f,acc}}}{k_{\mathrm{b}}T}\right)\right), \tag{2.23}$$

where n_{i} is the intrinsic carrier density, $t_{\mathrm{em,e/h}}$ is the emission time for electrons and holes when the device is in a non-steady state after pulsing the device. The

emission times are defined as:

$$t_{em,e} = \frac{|V_{fb} - V_t|}{V_a} t_f; \tag{2.24}$$

$$t_{em,h} = \frac{|V_{fb} - V_t|}{V_a} t_r, \tag{2.25}$$

where $t_{r/f}$ are the rise and fall time of the voltage pulse applied to the gate. The total period of one pulse is defined by the pulse frequency via $T_p = \frac{1}{f_{cp}}$. When the device switches from accumulation into inversion, the time from V_{fb} to V_t is the hole emission time ($t_{em,h}$). Similarly, when a device switches from inversion into accumulation, the electron emission time is $t_{em,e}$ [29]. The various parameters of the waveform are visualized in Figure 2.10.

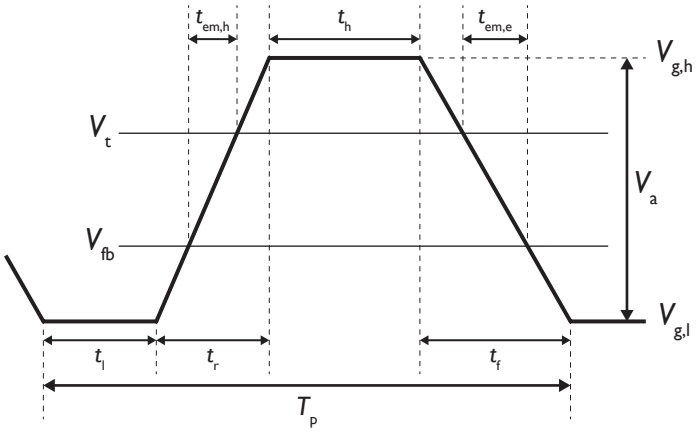

Figure 2.10: Voltage pulse to the gate during the charge pumping measurement. Image based on [30].

Geometric Component

The gate length affects how far the charge carriers have to travel before reaching a recombination center [31]. If during switching the pulse (from inversion to accumulation) and the rise/fall time (see Figure 2.10) is not sufficient to ensure that all untrapped minority charge carriers flow back to the source or drain, they may recombine with the majority carriers. This results in a parasitic component to the I_{cp}: the geometric component [32] ($I_{cp,gc}$). This mainly occurs in older generations of devices with larger gate dimensions and when $W \ll L$, the geometric component can usually be neglected [22, 23].

Since ΔI_{cp} due to degradation/recovery is of interest (instead of I_{cp}), the same $t_{r/f}$ is used for different frequencies and the devices are small enough, $I_{cp,gc}$ should be negligible. For the experiments in this thesis $t_{r/f} = 10$ ns is used for all frequencies and device areas. Because the rise and fall time are chosen to be identical over all frequencies, $\frac{t_{r/f}}{T_p}$ will increase for higher frequencies, however, this will have a negligible effect even at the highest used frequency of

$f_{cp} = 3$ MHz, since the rise/fall times will be at most $\approx 6\%$ of the total period time.

2.2.3 Frequency Dependency

When the devices are pulsed with a higher frequency, the amount of total recombinations that can take place increases, increasing the total charge pumping current according to Equation 2.19. When I_{cp} acquired at different frequencies is compared, the charge per cycle needs to be compared, or $\frac{I_{cp}}{f_{cp}}$, relating the measurement to Equation 2.18. Since the CP-current consists of the contribution from all recombination centers ($I_{cp,rc}$), interface traps and border/oxide traps, the CP current can be described as:

$$I_{cp} = I_{cp,rc} = I_{cp,it} + I_{cp,ot}. \tag{2.26}$$

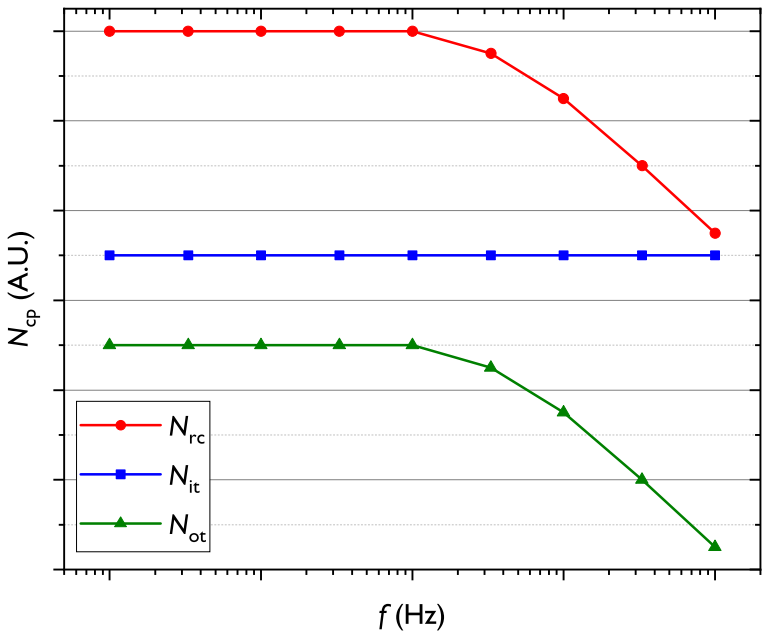

Figure 2.11: Schematic visualization of the N_{cp} dependency in arbitrary units on N_{it} and N_{ot}.

A higher pulse frequency will result in less time per pulse spent in accumulation or inversion. Traps with lower trap/emission constants do not have enough time to ensure recombination of minority and majority charge carriers, mainly if the traps reside further away from the channel, *i.e.* deeper in the gate oxide, *e.g.* oxygen-related border traps [30]. This frequency dependency is responsible for the behavior schematically visualized in Figure 2.11 when both shallow interface defects and deeper oxide traps are present. The number of

defects that can act as a recombination center and contribute to I_{cp} will drop when the frequency is high enough. At lower frequencies both the $I_{cp,it}$ (blue) and $I_{cp,ot}$ (green) contribute to I_{cp} (red). At higher frequencies ($f_{cp} \geq$ 1 MHz) $I_{cp,ot}$ drops [33], while the decrease in $I_{cp,it}$ is negligible and $I_{cp,it}$ is in line with $I_{cp,rc}$.

When the defect density is calculated according to Equation 2.19, N_{rc} consists of two terms, N_{it} and the oxide trap defect density, N_{ot}. In this thesis Equation 2.19 is thus changed to:

$$N_{rc} = N_{it} + N_{ot} = \frac{I_{cp}}{q \cdot A_g \cdot f_{cp}}, \tag{2.27}$$

where N_{rc} is the density of defects that can act as a recombination center [34, 35]. At higher frequencies, when the contribution due to N_{ot} has dropped and N_{rc} starts to approach $\approx N_{it}$.

2.2.4 Temperature Dependency

Using Section 2.2.1, Section 2.2.3 and Section 2.2.2, the general equation for the charge pumping current is described as [23]:

$$I_{cp} = 2q\overline{D_{it}} f A_g k_b T \left(\ln\left(v_{th} n_i \sqrt{\sigma_n \sigma_p}\right) + \ln\left(\frac{|V_{fb} - V_t|}{|V_a|} \sqrt{t_f t_r} \right) \right). \tag{2.28}$$

In addition, the emission time of trapped charges in defects is strongly dependent on the temperature [23, 36, 37] and can be described by:

$$t_{em,e/h} \propto \exp\left(\frac{E_b}{k_b T}\right). \tag{2.29}$$

Charge carriers will de-trap faster from defects at a higher temperature, before they can recombine and contribute to I_{cp}, resulting in a lower I_{cp}. Figure 2.12 shows the temperature dependency of both Equation 2.28 and Equation 2.29 on temperature, where a decrease is measured in I_{cp} of an undegraded device when the measurement temperature is increased from $T_m = 25\ ^\circ\text{C}$ to $T_m = 85\ ^\circ\text{C}$.

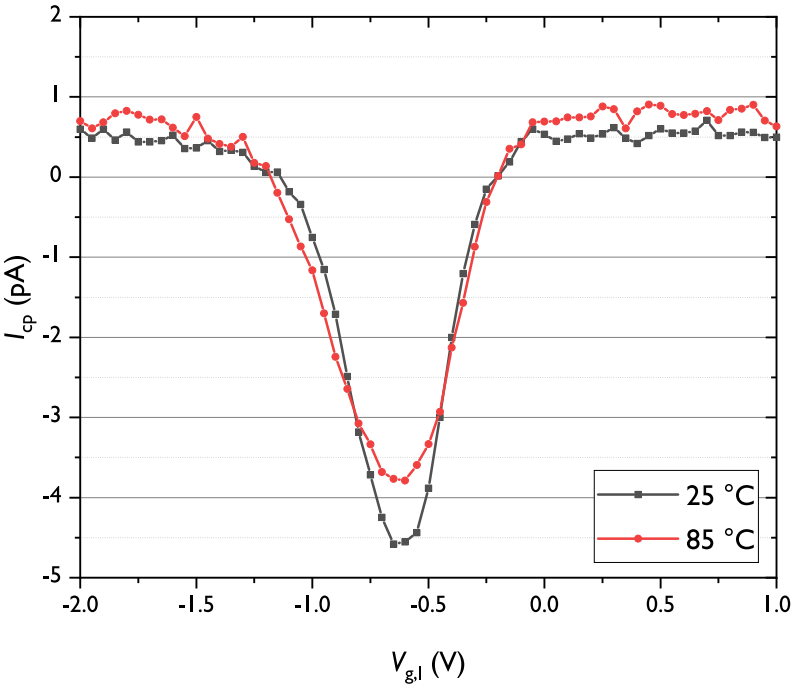

Figure 2.12: Charge pumping current as a function of gate-source voltage at the bottom of the pulse ($V_{g,l}$), measured at $f_{cp} = 30$ kHz of a fresh device measured at two different measurement temperatures.

2.3 Measurement process

To measure the effect of annealing on the recovery rate of the electrically degraded devices, various measurement methods were used in this thesis. Usually, a 5-step method (MSM(AM)-method) is used:

1) **M**easurement of a fresh, undegraded device
2) **S**tressing of the device
3) **M**easurement of the degraded device
4) **A**nneal or recovery step is performed on the device
5) **M**easurement of the recovered device

Step 1: Measures the non-offset value of the device as reference (*i.e.* $V_t(t_s = 0)$).
Step 2: Induces a parameter shift as a function of the stress time (*e.g.* $\Delta V_t(t_s)$).
Step 3: Measures the maximum parameter shift and the maximum degradation.
Step 4: Enables recovery by applying a temperature treatment, possibly in combination with a bias or an ambient.
Step 5: Measures the device again to observe how much recovery (if any) was induced.

Variations of the MSM(AM)-method used in this thesis are shown in Figure 2.13. Method A consists of several anneal/recovery cycles on the same device, where each subsequent anneal is at a higher temperature ($T_n > T_3 > T_2 > T_1$), under the assumption that negligible recovery takes place at room temperature. Each anneal results in more recovery due to a longer cumulative t_a, but mainly due to a higher T_a (*e.g.* Equation 3.13). Method B is used to investigate the recovery as a function of the anneal time (t_a) at a specific anneal temperature (T_a). Method C shows several stress-recovery cycles at the same anneal temperature, where each anneal step (partially) recovers the induced damage during the stress phase. Using this method, the effect of multiple stress/recovery cycles can be investigated, in line with a (hypothetical) real, commercially viable device, since individual transistors will not be used continuously. Furthermore, if a device recovers completely, each cycle should be identical, stress- and recovery-wise.

Depending on the anneal conditions (*i.e.* temperature, ambient gas, applied bias, etc.), complete recovery may not be induced. An anneal temperature of roughly $T_a = 150 - 200$ °C results in roughly 40-60% of recovery after one hour of annealing (Chapter 5). A positive or negative effect on the recovery rate by *e.g.* ambient can be observed, when this temperature range is used, *i.e.* you can see a higher a lower percentage of recovery. An improved recovery rate results in more recovery at a lower anneal temperature within the same anneal time and an improved lifetime.

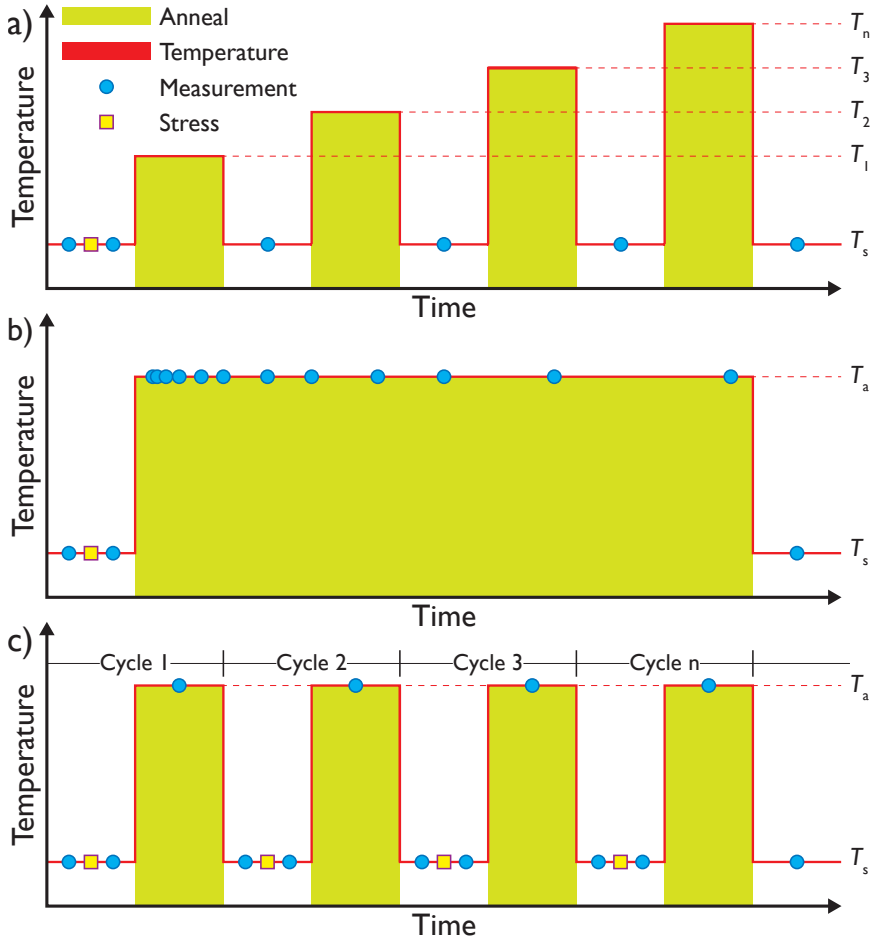

Figure 2.13: The measurement processes to investigate recovery. Method a): the device is stressed at T_s and then annealed at increasing higher temperatures. Method b): the device is stressed at T_s and the recovery is measured as a function of t_a at T_a. Method c): different cycles of stress-recovery are performed. The device is measured after each stress and recovery cycle.

2.4 Considerations for the Experimental Setup

2.4.1 Probe station

In this thesis, characterization was done on three different probe stations (Probeshield PM300ps, Karl Suss PM8 and Microtech model 11000), where a Keithley 4200-SCS with PreAmps was used to measure IV-behavior and I_{cp}. A Keithley 4225-PMU was used to generate the voltage pulses to the gate during the CP-measurements.

CP characterization with a frequency that is too low in combination with a small device (small A_g) and/or a small defect density will result in a I_{cp} too small to distinguish it from the background noise. Since the contribution to I_{cp}

attributed to noise is constant, the signal-to-noise ratio has a $\frac{1}{f_{cp}}$ dependence (combination of Equation 2.19 and Equation 2.26 where a noise component $I_{cp,noise}$ is included), a minimum frequency of $f_{cp} = 5$ kHz is chosen to ensure that the noise contribution is negligible over all gate areas and degradation levels. Figure 2.14 shows a typical I_{cp}-curve at two different frequencies. The charge per cycle is compared and the influence of noise starts to have an effect on I_{cp} when $f_{cp} = 5$ kHz. The offset in the y-axis (current due to measurement $T_m > 0$ K) becomes smaller at a higher frequency, since the contribution per cycle will diminish. The offset is taken into account before the defect density according to Equation 2.19 is calculated. The current is measured via the drain contact to minimize noise [31, 38], resulting in an inversion of Figure 2.8.

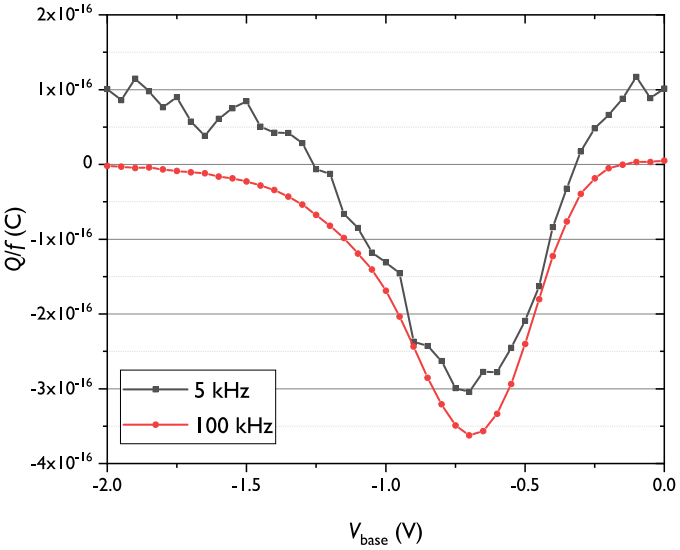

Figure 2.14: The I_{cp} current measured via the drain contact at $f_{cp} = 5$ kHz and f_{cp} =100 kHz.

2.4.2 Thermochuck

Two different thermochuck heating systems were used (ATT Systems m300 on the Probeshield PM300ps and Temptronic Corporation TPO 3200 A-3300-2 on the Microtech model 11000). The temperature of the chuck (T_{chuck}) is measured in the chuck, where a combination of electric (Joule) heating and a cooling liquid is used to stabilize the temperature. The temperature range of the thermochucks are 25 °C $< T <$ 200 °C and were done in air.

Probe needles are removed from the bond pads during the temperature step, to prevent stress due to thermal expansion. Subjecting an unstressed device to this temperature profile did not result in a measurable change in V_t, after being cooled down back to room temperature, suggesting that within the temperature scale of the thermochuck no thermal degradation takes.

Since the wafer/chip is positioned on top of the chuck and the temperature is measured inside the chuck, the device needs some time to adopt the temperature of T_{chuck}. Since all parameters/measurements are affected by the temperature of the device, this results in a time-dependent shift in the parameters until the device has reached the temperature of the chuck.

Figure 2.15 shows the ΔV_t of a fresh, undegraded device as a function of time after the thermochuck reached the anneal temperature (T_a). The V_t measurements conducted in the first $t_a \approx 300$ s after a temperature step from the previous anneal temperature, have an offset by this delay effect. This information is used to correct the data to get the temperature-dependent recovery, independent of the temperature delay effect.

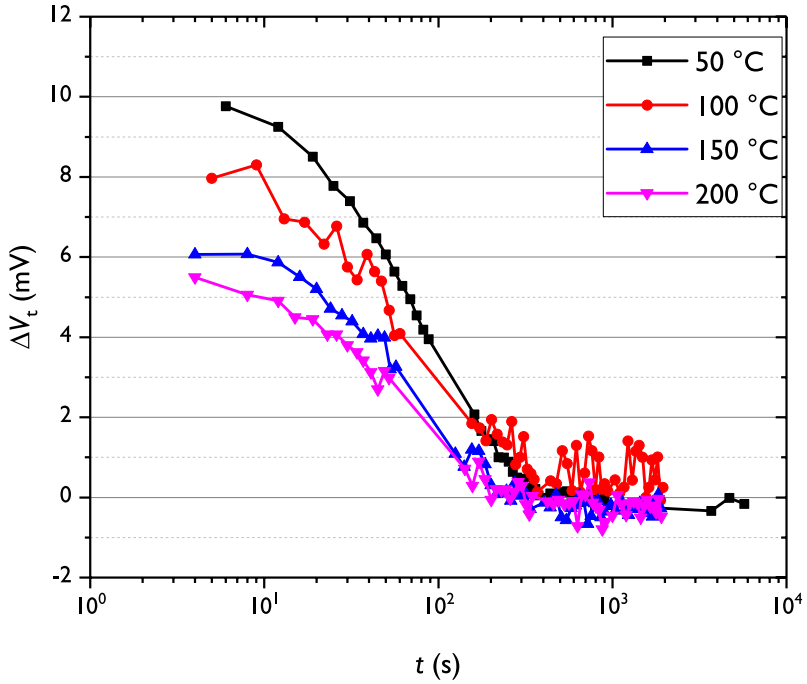

Figure 2.15: The shift in V_t of a fresh device as a function of time at various thermochuck temperatures. The threshold voltage settles after approximately $t_a = 300$ s, indicating the time needed for the device to adopt the temperature of the thermochuck. The reference point ($\Delta V_t = 0$ mV is set at the average settled value.

Annealing a device with a thermochuck is a bulky method that cannot be translated to a system embedded into the package, however, it gives a good indication of the various physical temperature-dependent processes taking place during recovery.

Due to the temperature ramp rate from $T_a = 25$ °C to $T_a = 200$ °C and cooldown back to room temperature, it can take more than 20 minutes between setting a temperature and reaching said temperature. This will cause unsystematic errors, especially for experiments focused on short-term annealing

effects (*e.g.* BTI), making the system more appropriate for the study of long-term effects of degradation and recovery (HCI), in line with the main point of interest of this thesis. It would be necessary to introduce an alternative heating system (*e.g.* [36]) to study the short-term effects of degradation and recovery.

2.5 Summary and Conclusion

The two main methods for characterization in this thesis to study degradation and recovery are the current-voltage measurement and the charge-pumping method. IV-measurements give a fast indication of the (type of) degradation, while the charge pumping method results in more direct qualitative data. Table 2.1 shows how degradation, recovery and an increase in temperature affect the various parameters of the nMOS devices studied in this thesis. In this thesis, the interplay between the various effects is investigated.

Effect	V_t	$g_{m,max}$	$I_{d,lin}$	SS	I_{cp}
Degradation	$+\Delta V_t$	$-\Delta g_{m,max}$	$-\Delta I_{d,lin}$	$+\Delta SS$	$+\Delta I_{cp}$
Recovery	$-\Delta V_t$	$+\Delta g_{m,max}$	$+\Delta I_{d,lin}$	$-\Delta SS$	$-\Delta I_{cp}$
Temperature	$-\Delta V_t$	$-\Delta g_{m,max}$	$-\Delta I_{d,lin}$	$+\Delta SS$	$-\Delta I_{cp}$

Table 2.1: The different effects of mechanisms on the various parameters of an nMOSFET. The temperature row indicates an increase in measurement temperature.

CHAPTER 3

The Role of Hydrogen

This chapter provides an overview of the theoretical background of the gate oxide in a MOSFET and the role hydrogen plays in the fabrication of a MOSFET. Hydrogen can have both a negative influence (Chapter 4) and a positive influence (Chapter 5) on the reliability of the device.

3.1 Introduction

In 1959, Dawon Kahng and Mohamed Atalla [9] reported a reliable method to grow a SiO_2-layer on top of a silicon substrate and that it could be used as a reliable gate dielectric. During the fabrication of a MOSFET, an amorphous oxide layer is grown on top of a silicon substrate using the 'wet'-method (using H_2O) or using the 'dry'-method of thermal oxidation (using O_2). The gate dielectric of contemporary devices uses materials with a high dielectric constant, *e.g.* HfO_2, Si_3N_4 for enhanced performance. However, due to lower stability of high-κ materials on top of the silicon substrate, a small SiO_2 layer is still necessary to accommodate the growth, even in the modern technologies [39].

Since the creation of a small SiO_2-based interfacial layer between HfO_2 and the silicon substrate layer is used to fabricate a reliable interface, the gate dielectric is the combination of both materials. The higher dielectric constant, κ, of HfO_2 ($\kappa_{HfO_2} = 25$) compared to SiO_2 ($\kappa_{SiO_2} = 3.9$), allows for a physically thicker insulator, which ensures that less leakage due to tunneling takes place in the gate oxide while having the same Equivalent Oxide Thickness (EOT):

$$\mathrm{EOT} = t_{\mathrm{ox},SiO_2} + \mathrm{EOT}(t_{\mathrm{ox},HfO_2}); \tag{3.1}$$

$$= t_{\mathrm{ox},SiO_2} + \frac{3.9}{\kappa_{HfO_2}} \cdot t_{\mathrm{ox},HfO_2}. \tag{3.2}$$

The total EOT is thus the sum of the EOT of both dielectric layers in the gate oxide[40]. Since contemporary devices use both high-κ materials and SiO_2 for their dielectric, the research in the reliability of Si/SiO_2 interfaces is

important and relevant for improving the total lifetime of devices.

3.2 Hydrogen Passivation

When amorphous SiO_2 is grown on top of a Si-substrate, not all Si- atoms at the Si/SiO_2-interface can bond properly with the Si- or O- atoms of the oxide, resulting in dangling bonds. The trivalent Si-atoms at the Si/SiO_2-interface with a non-bonding orbital electron are generally called P_b-centers [41], even though it denotes only one configuration of the silicon atom (*e.g.* $P_{b,0}$, $P_{b,1}$-centers.

During the operation of a MOSFET, these dangling bonds can act as an amphoteric charge trap for the charge carriers, inducing a positive or negative shift in the various device parameters which leads to inaccurate devices or creates a large error margin in the parameters. The interface defect density, N_{it} is in the order of 10^{9-11} cm^{-2} and with a surface silicon atom density of 10^{15} cm^{-2} it means that roughly 1 in every 10^{4-6} silicon atoms is not properly bonded [42]. Besides dangling bonds at the interface due to an incomplete bond with the gate oxide, incomplete bonds may arise within the gate oxide: border or bulk traps, both of which are oxide-defects. Border traps are oxide defects close to the channel and may have a strong influence on electrical parameters [43], *e.g.* V_t, see Equation 2.15. Bulk defects will be deeper in the gate oxide and will have a smaller effect on these electrical parameters.

To reduce the number of defects, a Post Metal/Oxide Anneal (PMA or POA) is done after the oxide growth. The device is annealed at a temperature in the range of $T_a = 400–600\ ^\circ C$ in a hydrogen ambient or hydrogen plasma, resulting in the passivation of dangling bonds at the interface and in the gate dielectric. The gate oxide processing step has a strong influence on the device and its lifetime [44].

Figure 3.1 is a schematic representation of the different defects at or near the Si/SiO_2 interface before (**B, E**) and after passivation with hydrogen (**A, C** & **D**). Note that the amorphous SiO_2 is here schematically shown in a crystalline manner to visualize the defects more clearly. The right part indicates that the interface is not 'smooth', which may introduce more kinds of defects. If another material is used in addition (*e.g.* HfO_2), another interface may appear where interface defects can be introduced [26].

Various methods are used to introduce hydrogen in the device for the hydrogenation process. Hydrogen plasma is used during solar cell fabrication for passivation to reduce the recombination of charge carriers at the Si/SiO_2-interface [45, 46]. Beneficial effects are also reported for dielectrics exposed to NH_3 plasma[16], where the passivation of dangling bonds at/near the HfO_2/MoS_2 interface is reported. For MOSFET devices, the PMA step is usually done in an ambient of hydrogen forming gas, however, passivation may also take place if hydrogen is already present in the device due to some other process. *E.g.* the concentration of hydrogen may be enhanced by using wet oxidation (hydrogen

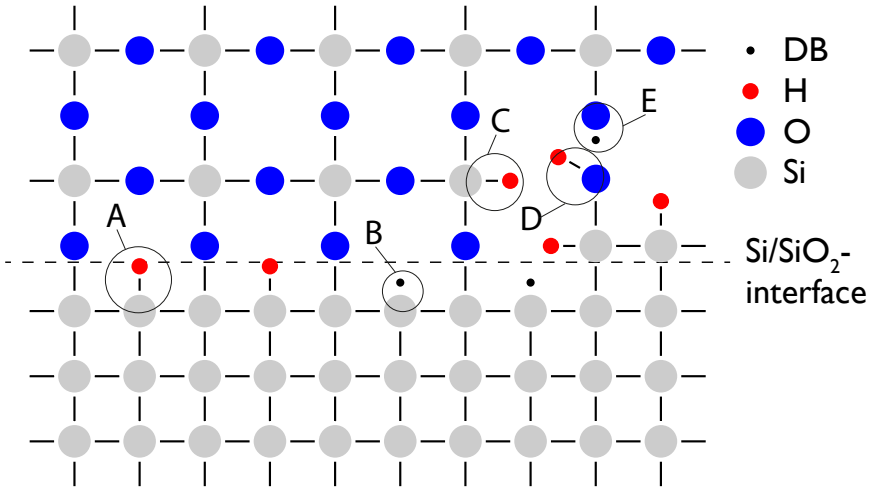

Figure 3.1: Schematic of the Si/SiO_2-interface. Hydrogen is used to passivate the dangling bonds (**B**) to create Si-H bonds (**A**). Due to the fabrication process, dangling bonds are introduced in the gate oxide (**E**), which can also be passivated by hydrogen, introducing Si-H bonds (**C**) or O-H bonds (**D**) in the gate oxide.

coming from H_2O) or if a hydrogen-rich Si_3N_4 layer is deposited on top of your device. Furthermore, hydrogen may be introduced using Ion Implantation (II), which may be used to overcome a diffusion barrier (see Section 3.3.3. Kamgar *et al.* reported that the maximum hydrogen concentration can be found near the interface, improving the chance of passivation, and that the gate oxide keeps its integrity and reliability regardless of the II process [47].

In addition to interface defect passivation, hydrogen may react with oxygen dangling bonds in the gate oxide [48], however, the O-H bonds tend to break easier compared to a Si-O bond [49]. As a consequence, hydrogen may enhance the chance of oxide breakdown, where hydrogen may attach to a strained Si-O bond and form a Si-OH bond [50]. Furthermore, hydrogen in high-κ contemporary devices may bond with Si and Hf over oxygen atoms, indicating that the presence of hydrogen may exacerbate oxide-related defects [51, 52]. Even though hydrogen may react with oxide defects, or even passivate the dopants in the silicon [53], the main focus of this thesis will be on the hydrogen-related interface defects. The recovery of oxide-related traps may be (partially) explained by structural reordering of the gate oxide material, reversing the oxide trap to a normal Si-O bond, unrelated to hydrogen.

Besides a positive influence on the passivation of dangling bonds, hydrogen may also hurt the lifetime of a device [54]. For instance, it is reported that extra hydrogen in the packaging of a device may induce depassivation of Si-H bonds at the Si/SiO_2-interface [55]. The concentration of hydrogen in the device/packaging will lead to an equilibrium between passivated bonds and dangling bonds at the interface, which depends on the concentration of

hydrogen and the temperature [56, 57].

3.2.1 Reaction Process

The passivation of a dangling bond with hydrogen can be described by a reaction with atomic or molecular hydrogen. Brower found the kinetics of the passivation of P_b-centers with H^0 or H_2 to be thermally activated with a single reaction barrier of around $E_b \sim 1.66$ eV [58]. Earlier work [58, 59] on the passivation of P_b centers by a thermal anneal in a hydrogen ambient modeled the passivation via a kinetic model that depends on the introduction of molecular or atomic hydrogen, according to:

$$P_b + H \xrightarrow{k_f} P_bH; \tag{3.3}$$

$$P_b + H_2 \xrightarrow{k_f} P_bH + H, \tag{3.4}$$

where k_f is the forward reaction rate. Depassivation or dissociation of hydrogen due to degradation follows the reverse reaction, according to:

$$P_bH \xrightarrow{k_r} P_b + H; \tag{3.5}$$

$$P_bH + H \xrightarrow{k_r} P_b + H_2. \tag{3.6}$$

Equation 3.4 and Equation 3.5 result in atomic hydrogen, affecting both the passivation and depassivation rate of Equation 3.3 and Equation 3.6. Passivation of one defect may lead to (de-)passivation of another Si-H bond. Although atomic hydrogen may have a positive or negative effect on the reliability of a device [60, 61] and play a role in the (de-)passivation of P_b centers [62], it is highly reactive and unlikely to reach the Si/SiO_2-interface without reacting with the rest of the gate oxide or with another hydrogen atom (creating H_2) [63]. It is assumed in this thesis that passivation is the most likely to be described in terms of H_2 (Equation 3.4 and Equation 3.6) and that other hydrogen species are less relevant. There are however, some models, where various hydrogen species play a role in the gate dielectric to describe BTI degradation, which will be discussed in Section 4.3.1 or hydrogen plasma that results in depassivation, which will be discussed in Section 4.6.

The forward and reverse reaction rate (k_f, k_r) depend via an Arrhenius dependency on the anneal temperature and their specific activation energy according to:

$$k_f = k_{f,0}\exp\left(-\frac{E_{a,f}}{k_b T_a}\right); \tag{3.7}$$

$$k_r = k_{r,0}\exp\left(-\frac{E_{a,r}}{k_b T_a}\right). \tag{3.8}$$

It was proposed that the passivation rate depends on the concentration of available P_b-centers and the concentration of molecular hydrogen at the

Si/SiO_2-interface, resulting in a first-order time dependence of the number of interface defects:

$$\frac{d[P_b]}{dt} = -k_f[H_2][P_b]; \tag{3.9}$$

$$\frac{d[P_b]}{dt} = k_r[HP_b] = k_r(N_0 - P_b). \tag{3.10}$$

Brower assumed that due to the high diffusion constant of H_2 in the gate oxide, it could be assumed that the concentration $[H_2]$ at the interface is similar to the concentration in the rest of the dielectric (reaction limited process instead of diffusion-limited). Solving Equation (3.9), a time-dependent interface defect density formula of Equation (3.11) can be achieved. Similarly, the time dependence of passivated defects can be found.

$$[P_b] = N_0 \exp(-k_f[H_2]t_a); \tag{3.11}$$

$$[P_b] = N_0\Big(1 - \exp(k_r t_a)\Big), \tag{3.12}$$

where $N_0 = [P_b] + [P_bH]$ is the maximum number of defects, passivated and not passivated.

3.2.2 Generalized Simple Thermal (GST) model

Brower assumed that the activation energy for the forward ($E_{a,f}$) and reverse ($E_{a,r}$) reaction are well defined, however, electron-spin resonance experiments suggested that P_b-centers follow a configurational distribution, where the position of a Si atom with dangling bonds varies slightly from atom to atom [64]. This variation is reflected in the various Si-H bond energies, affecting Equation 3.11. Stesmans solved this [64--66] by proposing that the mean activation energy ($\bar{E}_a$) follows a Gaussian distribution with a standard deviation of σ_{E_a}. This General Simple Thermal (GST) model of passivation describes the passivation rate, where an integration over all possible activation energies is done:

$$\frac{[P_b]}{N_0} = \frac{1}{\sqrt{2\pi}\sigma_{E_{a,f}}} \int \exp\left(-\frac{(\epsilon - E_{a,f})^2}{2\sigma^2_{E_{a,f}}}\right) \times \exp\left(-k_{f,0}[H_2]t_a \exp(-\frac{\epsilon}{k_b T_a})\right) d\epsilon. \tag{3.13}$$

This model describes the passivation rate during fabrication fairly well if only passivation takes place. It was noted by Wilkinson and Elliman [67] that at the same time dissociation of Si-H bonds may take place and that the passivation will go to an equilibrium between passivation and depassivation. It was proposed that the dissociation energy of the Si-H bonds follows a similar Gaussian distribution. Combining a similar dissociation behavior of Brower *et al.* with Equation 3.13, Wilkinson proposed that the passivation equation becomes [67]:

$$\begin{aligned}\frac{[P_b]}{N_0} = &\frac{1}{\sqrt{2\pi}\sigma_{E_{a,r}}\sigma_{E_{a,f}}} \int\int \exp\left(-\frac{(\epsilon_r - E_{a,r})^2}{2\sigma^2_{E_{a,r}}} - \frac{(\epsilon_f - E_{a,f})^2}{2\sigma^2_{E_{a,f}}}\right) \\ &\times \frac{1}{k_r + k_f[H_2]}\left(k_r + k_f[H_2]\exp\left(-(k_r + k_f[H_2])t_a\right)\right) \\ &\times d\epsilon_r d\epsilon_f.\end{aligned} \tag{3.14}$$

3.3 Hydrogen Transport

Hydrogen is introduced in the device during the fabrication step by exposure to a hydrogen (or hydrogen-related, *e.g.* NH_3) ambient. Hydrogen is needed during the passivation step, however, hydrogen transport may have a negative influence on the gate dielectric and may introduce new defects [52, 68]. Generally, the flux of a species can be described by a diffusion, J_{diff}, and a drift, J_{drift}, related component [42, 69, 70]:

$$J = J_{diff} + J_{drift}. \tag{3.15}$$

3.3.1 Hydrogen Diffusion

Diffusion is observed along a concentration gradient, where the species flow down from the concentration gradient [42, 70]. This flow is described by the first Fick's law, which describes a one-dimensional flow by:

$$J_{\text{diff}} = -D\frac{\mathrm{d}N}{\mathrm{d}x}, \tag{3.16}$$

where J_{diff} is the flux of the species diffusing ($\text{cm}^{-2}\ \text{s}^{-1}$) and N is the concentration (cm^{-3}). The diffusion constant (D, in cm^2/s) is material-specific and affected by various conditions, *e.g.* defects will lower the diffusion rate of hydrogen. The diffusion constant depends on the temperature via an Arrhenius dependency:

$$D = D_0 \exp\left(-\frac{E_\text{a}}{k_\text{b}T}\right), \tag{3.17}$$

where in general a higher temperature will have a higher diffusion rate. *I.e.* hydrogen will reach the P_b-centers faster at higher temperatures. Differently charged particles (H^+, H^0 and H^-) will also have different diffusion constants and will behave differently in n- or p-doped silicon [71].

The diffusion rate of Equation 3.16 also depends on the supply of the diffusion material. A (semi-)infinite supply, *e.g.* exposure to a hydrogen ambient, uses the complementary error function (erfc) to describe the diffusion rate of the doping material N as a function of time, t, and the location, x:

$$N(x,t) = N_0 \text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right). \tag{3.18}$$

The concentration of infinite supply is given by N_0. Diffusion from a limited supply (*i.e.* the total diffusion material stays the same) will have a lower concentration of the material at the source for longer diffusion times, moving deeper in the device. The concentration is described by:

$$N(x,t) = \frac{n_\text{tot}}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right), \tag{3.19}$$

where n_tot is the total number of atoms of the diffusion species present.

3.3.2 Hydrogen Drift

Diffusion is omnidirectional and depends on the concentration gradient of the diffusion material. An electric field may direct ions in the gate oxide, where it is reported that the drift of mobile protons could be used, where they maintain their charge [72--74]. The protons move from one interface to the other in the gate dielectric due to the applied electric field, *i.e.* applying a positive bias to the gate ensures the drift of H^+ towards the Si-SiO_2 interface [75], a negative bias to the gate/gate oxide interface. The protons appear to hold their charge and react with the bridging oxygen of a Si-O-Si bond near the interface [72], preventing other protons to move through the interface into the substrate. It

was proposed to use the movement of stable, consistent charges in the gate oxide as a type of non-volatile memory [72, 73]. This raises the question of whether it is possible to have a normal concentration of hydrogen (ions) in the gate oxide which may be directed actively towards the interface and dangling bonds using an electric field ϵ, increasing the local hydrogen concentration, where the flux of hydrogen ions is described by:

$$J_{\text{drift}} \propto \mu \cdot \epsilon. \tag{3.20}$$

Although H_2 is the most stable hydrogen species in the gate oxide, more hydrogen-related species, as the before mentioned H^+, may influence the passivation rate. Stesmans' model and its variations currently assume that the passivation rate depends only on the concentration of molecular hydrogen at the Si/SiO_2-interface via diffusion. If proton drift affects local concentrations, it raises the question of whether Stesmans' model needs to be extended and incorporate other hydrogen-related species in combination of the electric field to predict the recovery rate.

3.3.3 Hydrogen Barriers

The diffusion rate (Equation 3.16) depends on the material and diffusion constant. Hydrogen moves more easily through Si and SiO_2 (larger D-coefficient) than through Si_3N_4 [76]. Effectively, a nitride layer acts as a diffusion barrier for hydrogen, where it prevents hydrogen from leaving[77] or reaching certain parts of the device [78]. Similarly, other materials *e.g.* titanium [68, 79, 80] may be used as a diffusion barrier. In general the diffusion rate of hydrogen in Si, SiO_2 and Si_3N_4 can be summarized as:

$$D_{Si_3N_4} \ll D_{Si} < D_{SiO_2}. \tag{3.21}$$

Although diffusion barriers are commonly used to confine the movement of hydrogen, the doping of silicon or proton absorption at the interface [81] may also act as an (ion) barrier.

A diffusion barrier prevents hydrogen from leaving the device over time and ensures a stable hydrogen presence in the device. A silicon nitride layer deposited in combination with hydrogen (*e.g.* NH_3) may contain a high hydrogen concentration. Over time, the hydrogen may diffuse slowly (due to the low diffusion constant) to surrounding areas with a lower concentration of hydrogen [82]. This would result in a slow desorption rate, that stays constant for a long time. This raises the question if a diffusion barrier can be used as a constant hydrogen source and enhance the recovery rate, besides only confining the movement of hydrogen. This is however not part of the research discussed in this thesis.

3.3.4 Hydrogen Concentration

The passivation rate of P_b-centers at the Si/SiO_2-interface depends on the concentration of hydrogen at the interface, see Equation 3.13. In modern CMOS

technologies, there will always be hydrogen present in the gate stack due to the various fabrication processes that involve hydrogen [83]. This is however a limited supply of hydrogen. An external hydrogen source, *e.g.* exposure to a hydrogen ambient, may introduce a (semi-)infinite supply of hydrogen. The maximum concentration is then defined by the maximum solubility of hydrogen in the device. Although the various materials in a device may have a different hydrogen solubility depending on the material properties [84, 85], structure or damage [86], the solubility can generally be described via an Arrhenius dependency:

$$S_{\text{eff}} = S_0 \exp(-\frac{E_a}{k_b T}), \tag{3.22}$$

where S_0 is the material-specific solubility constant. A higher temperature will lead to a higher solubility and a higher concentration of hydrogen that can act as a passivation species.

When the hydrogen concentration in the device is larger than outside, out-diffusion takes place, which becomes significant at temperatures $T > 500$ °C [87, 88], suggesting that at the lower (operating) temperatures the hydrogen concentration is stable.

3.4 Summary and Conclusion

Hydrogen plays an important role during fabrication in passivating dangling bonds at the Si/SiO_2-interface. The temperature has a strong influence on the passivation rate, where a higher temperature generally favors a higher diffusion rate of hydrogen towards the interface defects, a higher solubility of hydrogen in the device itself and ultimately a higher passivation rate. Passivation during the post-metal anneal step during fabrication is usually performed at an anneal temperature of $T_a \approx 400$ °C, where sufficient passivation takes place within a reasonable time frame. The main findings from this chapter are:

- The passivation rate during device fabrication can be reasonably well described Stesmans' Generalized Simple Thermal model, however, it only takes H_2 into account as a passivation species.
- The concentration of hydrogen at the Si/SiO_2-interface depends on a combination of the supply of hydrogen itself, the maximum (material-specific) solubility of hydrogen in the device and the transport (diffusion/drift) of hydrogen towards the interface.

The passivation of P_b-centers using hydrogen creates Si-H bonds and enhances the performance of a device. When hydrogen dissociates from this bond, a dangling bond is created and the performance of the device will deteriorate. The next chapter will discuss how various degradation mechanisms may affect the interface, and how it may lead to eventual end-of-life of the device.

CHAPTER 4

Degradation

4.1 Introduction

This chapter provides an overview of the degradation mechanisms in a MOSFET of interest in this thesis. Different degradation mechanisms affect different parts of the device, where the main focus in this thesis is on the hydrogen-related interface defects, specifically long-term, unrecoverable, permanent damage: **B** in Figure 3.1 [89, 90] on page 29. At room temperature, hydrogen-related defects are mainly introduced by HCI. However, more degradation mechanisms may take place simultaneously that could have similar degradation physics and the mechanisms that enhance the recovery rate of hydrogen-related may affect other, non-hydrogen-related defects introduced by these degradation mechanisms. Hot-carrier injection (HCI), bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), stress-induced leakage current (SILC), plasma-induced degradation (PID) and thermal degradation will cause structural changes in the gate oxide and near the Si/SiO_2 interface [91, 92] and are discussed in this chapter.

Figure 4.1 shows the degradation of an nMOS device, where the cumulative stress time (t_s) by HCI induced a shift to the right in this specific case. The introduction of new interface/oxide defects and the charging of defects results in a shift in the various parameters of the device (see Chapter 2). The shift in a parameter (*e.g.* V_t) at stress time t_s, is defined by:

$$\Delta V_t(t_s) = V_t(t_s) - V_t(0), \tag{4.1}$$

where $V_t(0)$ is the threshold voltage of a fresh, undegraded device. Immediately after the stress phase ends, some recovery/relaxation can take place, which has to be taken into account in degradation models to predict the effective degradation level. Although some recovery/relaxation is reported for older generation HCI degraded devices [93], fast and significant recovery is known to occur after BTI, making it more difficult to model the lifetime accurately.

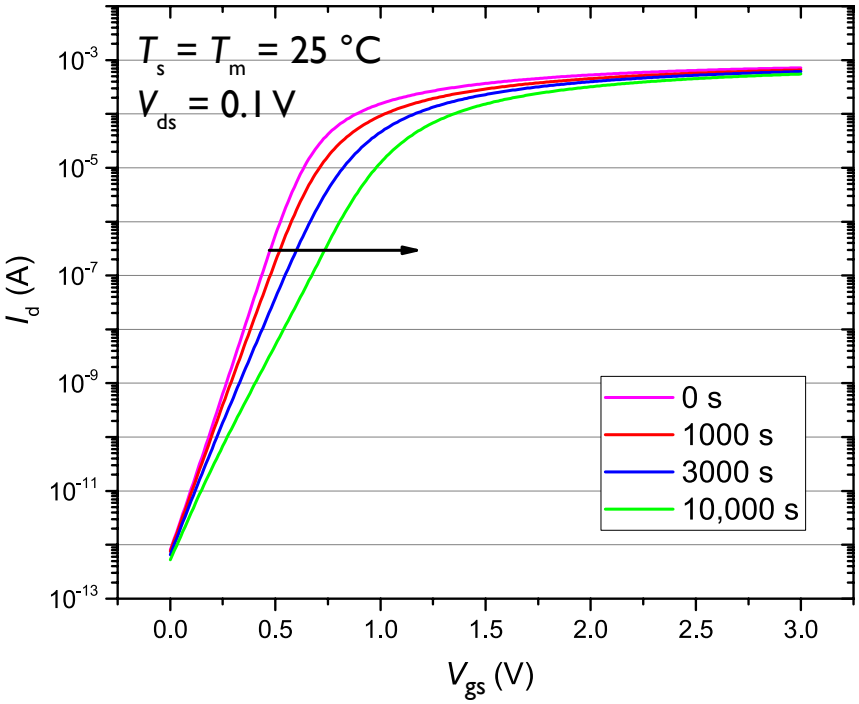

Figure 4.1: I_d-V_{gs} curve after various stress times of HCI ($W = 10.0$ µm, $L = 0.35$ µm and $t_{ox} = 7.0$ nm). Stress was applied at $V_{ds} = 4.5$ V, $V_{gs} = 2.1$ V.

Contemporary devices may have a high-κ dielectric in addition to a Si/SiO_2 interface (see Chapter 3), which results in an extra interface (*e.g.* SiO_2/HfO_2 interface) and extra hydrogen-related interface degradation [94]. Similarly, BTI may take place during HCI, where the short-term relaxation/recovery component of BTI may distort the measured recovery attributed to the recovery of hot-carrier induced damage.

In this thesis, the role of hydrogen on the reliability is investigated, and to minimize other effects this thesis mainly uses MOSFETs where the gate oxide only consists of SiO_2, has a gate area with sufficient silicon-hydrogen bonds ($L_g > 0.2$ µm, $W_g > 1$ µm) for sufficient statistics and the physics of the interface is well defined. The devices under study are stressed at room temperature by HCI, and it is verified that the degradation and shift in parameters do not show significant relaxation or recovery due to some BTI-related component.

4.2 Hot-Carrier Injection (HCI)

In this thesis, the main degradation mechanism under study is hot-carrier injection which causes hot-carrier degradation or damage (HCD). Charge carriers are accelerated in the channel due to a lateral electric field between the source and drain, where they gain enough energy to become 'hot-carriers'. A charge

carrier becomes 'hot' when the kinetic energy is high enough so that the effective temperature is higher than the lattice temperature (T_L). The hot-carriers may rupture a Si-H bond at the interface, creating more P_b-centers and a shift in various device parameters, see Figure 4.1 [95].

HCI mainly leads to the creation of interface defects, however, new oxide traps may also be introduced, in combination with the charging of existing traps due to (de-)trapping of charge carriers [96]. The kinetic energy of the hot-carriers due to the electric field is the highest near the drain, resulting in degradation at the interface and gate oxide localized near the drain [97]. Furthermore, it becomes more likely at higher temperatures for the hot-carriers in long-channel devices to lose energy via optical phonon scattering, so they induce less damage [98, 99].

Hot-carrier injection takes place under various conditions, where the most common are: Channel Hot-Electron (CHE) injection, Substrate Hot-Electron (SHE) injection, Drain-Avalanche Hot-Electron (DAHC) injection and Secondary Generated Hot-Electron (SGHE) [100, 101]. summarized in Figure 4.2.

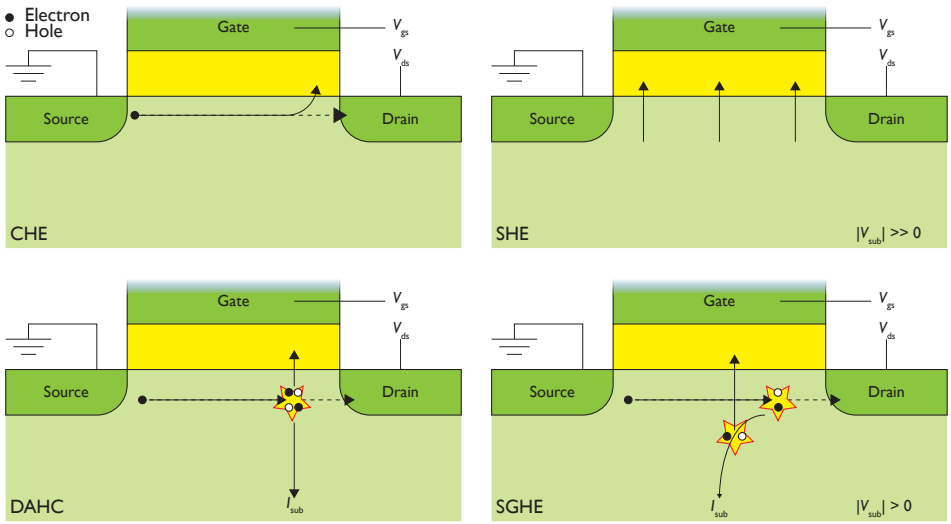

Figure 4.2: Schematic visualization of CHE, SHE, DAHC and SGHE induced degradation. Based on [102]

CHE injection occurs when $V_{gs} \approx V_{ds}$. Charge carriers are accelerated in the channel and get injected into the gate oxide due to the gate-source bias. When the kinetic energy is high enough, it may break the Si-H bond, creating a new interface defect. Devices of previous generations had a lateral electric field large enough for the charge carrier to gain sufficient energy to dissociate the bond by the collision of one particle with the Si-H bond, *i.e.* the Lucky-Electron Model [103--105]. Newer technologies have a smaller drain-source bias, reducing the kinetic energy per charge carrier and multiple charge carriers colliding with the Si-H bond are needed to induce dissociation [95].

SHE injection takes place when a large bias is applied to the substrate

of the device ($|V_{bs}| \gg 0$). The electric field will accelerate charge carriers in the substrate (electrons for nMOS, holes for pMOS), which may collide with the Si-H bonds at the Si/SiO_2-interface, resulting in dissociation via a single or multiple particle collision. When a drain-source bias is present during the degradation phase, the degradation will be localized near the drain in this injection method [106].

DAHC injection occurs when charge carriers are accelerated in the channel and through impact ionization (II) near the drain at the pinch-off point, *i.e.* electron or hole emission, an electron-hole pair is created, where the minority carrier gets injected into the gate oxide. Due to the vertical electric field, this results in a charge injection into the gate oxide and substrate or bulk current (I_{sub} or I_b), according to Figure 4.2. The amount of charge injected into the gate, is proportional to I_{sub}, making it a good indicator to find a drain-source and gate-source bias where maximum degradation due to DAHC takes place ($V_{gs} \approx \frac{V_{ds}}{2}$). Figure 4.3 shows the bulk current as a function of the gate-source voltage for $V_{ds} = 3.5/4.0$ V of an nMOS device, where$|I_{sub}|$ is maximum at $V_{gs} = 1.575/1.75$. In this thesis, DAHC is the main method to induce HCD (Hot-Carrier Degradation) and the corresponding V_{gs} and V_{ds} are found in a similar way for all devices under study. For the experiments done in this thesis, the initial conditions for maximum DAHC degradation are used for the whole stress cycle. DAHC is the most efficient to introduce degradation for devices used in this thesis, devices with a smaller gate length will show more degradation using CHE.

Lastly, SGHE injection occurs when in addition to the creation of electron-hole pairs by impact ionization (similar to DAHC), a strong substrate bias is applied to the device (similar to SHE). The substrate bias creates a vertical electric field that will accelerate secondary carriers and drive the charge carriers towards the gate oxide, where they can get injected [107].

4.2.1 Lucky-Electron Model

The first model to describe HCI in a theoretical framework was proposed by Hu *et al.* in 1979 [103]. The lucky-electron model (LEM) was proposed, where an electron has gained sufficient energy in the lateral electric field (ε) to overcome the potential of the Si/SiO_2 interface, dissociate hydrogen and create an interface defect. Hu determined that the critical energy to create an interface defect is $\phi_{it} \approx 3.7$ eV [104], suggesting that only the electrons in the Electron Energy Distribution Function (EEDF) with sufficient energy contribute to degradation (≥ 3.7 eV). The probability that an accelerated electron will travel a distance d in the channel before a collision where it can lose its energy, is defined by:

$$P(d) = \exp(\frac{-d}{\lambda}), \tag{4.2}$$

where λ is the mean free path of the electron in the device. According to LEM, an increase in lattice temperature will increase the number of phonons, decrease the mean free path and subsequently the damage due to HCI. Using

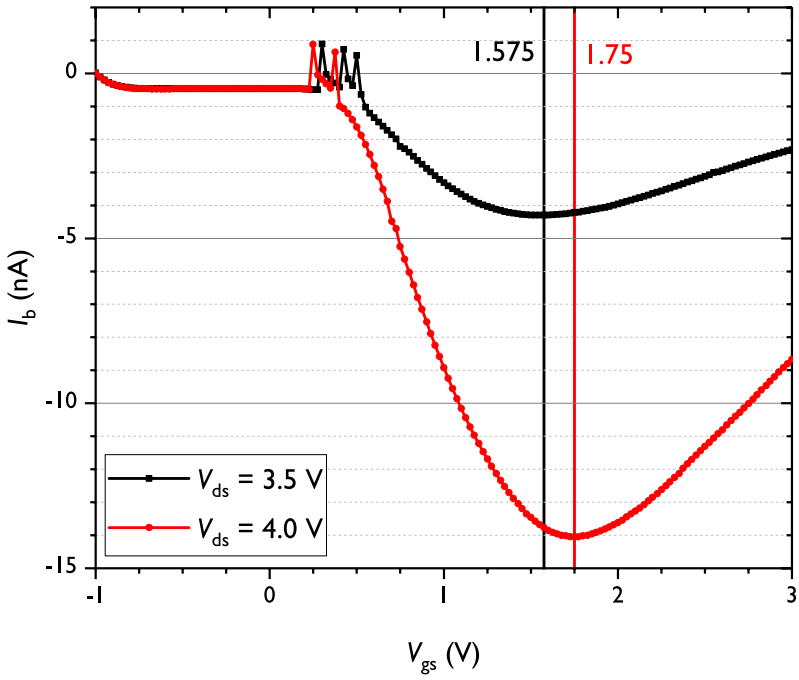

Figure 4.3: Bulk current as a function of the gate-source voltage. Insets shows two different drain-source voltages. $|I_{b,max}|$ occurs at around $V_{gs} < \frac{V_{ds}}{2}$

the energy (E) gained in the lateral electric field ($E = qd\varepsilon$), the electron energy distribution function can be given by:

$$f(E) = P(E) = \exp(-\frac{E}{q\lambda\varepsilon}). \tag{4.3}$$

The EEDF of the hot electrons has a similar distribution to a thermal energy distribution [108], which gives an effective temperature (T_{eff}) higher than the lattice temperature (hence the name "Hot-Carriers"), determined as:

$$T_{eff} = \frac{q\lambda\varepsilon}{k_b}. \tag{4.4}$$

The total current drain current I_d relates to the total current flow of hot-carriers of at least energy ϕ_i that can induce degradation via: $I_d \exp\left(-\frac{\phi_i}{q\lambda E}\right)$.

Using this charge carrier flow, the change in interface defect density can be found as a function of stress time (t_s, n) [104]:

$$\Delta N_{it} \propto \left(t_s \frac{I_d}{W_g} \exp(-\frac{\phi_{it}}{q\lambda\varepsilon})\right)^n. \tag{4.5}$$

HCI in older generations of devices could be described by LEM, however, it simplifies the physical processes and interactions that take place. Charge carriers may not lose all energy upon collision and since charge carrier-phonon collision

is the dominant collision and energy transfer mechanism, the change in energy is limited to the optical phonon energy ($E = 63$ meV in silicon) [109]. Furthermore, LEM assumes that a drain-source bias of at least 3.7 V is necessary to overcome the interface barrier and induce degradation, contradicting degradation that takes place at smaller biases [110].

4.2.2 Multiple Vibrational Excitation Model

The lucky-electron model assumes that only carriers with sufficient energy are responsible for introducing defects and that carriers with insufficient energy do not contribute to bond dissociation. However, Hess *et al.* [110--113] proposed an HCD model that uses single-particle (SP) and multiple particle (MP) collisions in combination with the distribution function of carrier energy.

The Si-H bonds at the interface are modeled as a truncated harmonic oscillator, where the different vibrational modes of the bond can get excited to higher levels due to the interaction with a single (SP) or various (low energy) charge carriers (MP). When the bond is excited to the highest excitation, the Si-H bond will break, leading to depassivation with a probability P_{dep}. Figure 4.4 shows the bond-breaking mechanism of both processes.

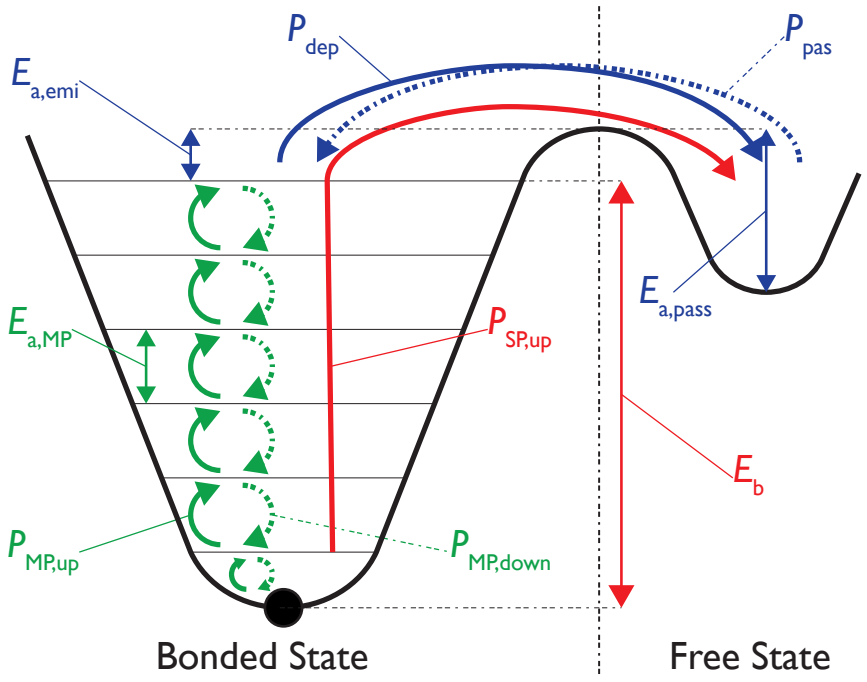

Figure 4.4: Schematic visualization of the energy states of a Si-H bond and the bond-breaking process by single or multiple particles. Image based on [108, 114]

A single charge carrier with sufficient energy ($\geq E_{a,sp}$) will interact with the bond and will bring it into an anti-bonding state, after which the dissociation of the hydrogen at the Si/SiO_2-interface can take place similarly to LEM. The

total Si-H dissociation rate can then be described via an acceleration factor or acceleration integral [113]:

$$R_{\mathrm{sp}} \sim \int_{E_{\mathrm{a,sp}}}^{\infty} \Phi(E) P(E) \sigma(E) \mathrm{d}E, \tag{4.6}$$

where $\Phi(E)$ is charge carrier flux with sufficient energy ($E_{\mathrm{a,sp}}$), σ is the bond dissociation cross section and $P(E)$ is the desorption probability. When multiple particle collisions take place, the probability of going from one energy level to the next can be described by:

$$P_{\mathrm{mp,up}} \sim \int_{E_{\mathrm{th}}}^{\infty} I(E) \sigma_{\mathrm{emi}}(E) \left(1 - f_{\mathrm{ph}}(E + \hbar\omega)\right) \mathrm{d}E; \tag{4.7}$$

$$P_{\mathrm{mp,down}} \sim \int_{E_{\mathrm{th}}}^{\infty} I(E) \sigma_{\mathrm{ab}}(E) \left(1 - f_{\mathrm{ph}}(E - \hbar\omega)\right) \mathrm{d}E, \tag{4.8}$$

where is $I(E)$ the flux of charge carriers colliding with the Si-H bond, $\sigma_{\mathrm{emi/ab}}$ is the capture cross section for phonon emission/absorption, f_{ph} is the number for level occupation and the energy difference between two levels is described by $\hbar\omega$. The total Si-H dissociation rate due to MP is described by:

$$R_{\mathrm{mp}} = \left(\frac{E_{\mathrm{b}}}{\hbar\omega} + 1\right) \left(P_{\mathrm{mp,down}} + \exp\left(-\frac{\hbar\omega}{k_{\mathrm{b}} T_{\mathrm{L}}}\right)\right) \left(\frac{P_{\mathrm{mp,up}} + \omega_{\mathrm{e}}}{P_{\mathrm{mp,down}} + \exp(\hbar\omega / k_{\mathrm{b}} T_{\mathrm{L}})}\right)^{-\frac{E_{\mathrm{b}}}{\hbar\omega}}, \tag{4.9}$$

where T_{L} is the lattice temperature and E_{b} is the energy of the last bonded state, the reciprocal lifetime of a phonon is described by $\omega_{\mathrm{e}} = \frac{1}{\tau_{\mathrm{p}}}$, which defines the decay from one energy state to a lower energy state. The phonon lifetime also explains the difference in degradation level of deuterium passivated interface states compared to hydrogen passivated interface states [110] (see Section 7), where the energy of a Si-D bond decays more easily to a lower level than a Si-H bond.

Rewriting Equation 4.7 and Equation 4.8 and linked to the drain current via [112], the probability of going up/down an energy level are described by:

$$P_{\mathrm{mp,up}} = I_{\mathrm{d}} f_{\mathrm{v}} + \omega_{\mathrm{e}}; \tag{4.10}$$

$$P_{\mathrm{mp,down}} = I_{\mathrm{d}} f_{\mathrm{v}} + \omega_{\mathrm{e}} \exp(-\frac{\hbar\omega}{k_{\mathrm{b}} T_{\mathrm{L}}}), \tag{4.11}$$

where f_{v} is the fraction of electrons that induce an excitation from one level to the next. The total dissociation rate can then be defined via the drain current and the i levels in the truncated harmonic oscillator system:

$$R = \sum_{i=1}^{N_1} \left[\frac{P_{\mathrm{mp,d}}}{P_{\mathrm{mp,u}}}\right] A^{\mathrm{i}} I_{\mathrm{d}} f_{\mathrm{d}}. \tag{4.12}$$

The fraction of electrons that induce an emission to a lower level is defined by f_d and the empirically found factor A between the various energy levels. The total amount of interface states created according to this model is the cumulative contributions of both SP and MP:

$$\Delta N_{it} = \Delta N_{it,sp} + \Delta N_{it,mp}. \tag{4.13}$$

The model uses defects at the microscopic level to describe degradation by HCI, but it does not extrapolate them to device level, introducing an error margin in lifetime predictions. In addition, TCAD device simulations done by Penzin [115] used a simplification of the influence of lower energy/cold charge carriers, resulting in a larger error margin of the influence of these charge carriers on the MVE process [108].

4.2.3 Energy-Driven Model

The third model to described HCD is the energy-driven model by Rauch and La Rosa [116--118]. At lower drain-source voltages ($V_{ds} < 3$ V) and gate lengths, the field-driven lucky-electron model of Section 4.2.1 predicts that no significant degradation can take place. However, experiments confirmed that HCI [116] still induces degradation in MOSFET devices under these conditions. Due to Electron-Electron Scattering (EES), two energetic charge carriers will scatter and some energy transfer takes place, where one carrier can gain energy. This will change the EEDF, introducing more charge carriers in the high-energy regime. It is reported that at lower drain-source potential ($V_{ds} < 3$ V), EES will be the dominant force in the high energy tail population of the charge carrier EEDF and will be one of the driving forces of HCI induced degradation in low-voltage devices [119, 120].

The rate of impact ionization in the device is proportional to the formation of new interface defects and can be described by[109, 118]:

$$Rate = \int f(E)\sigma(E)\mathrm{d}E, \tag{4.14}$$

where f is the electron energy distribution function and σ is the interaction cross section. The rate will have a maximum at one or more points, which correspond to the energies that dominate the hot-carrier rate. This happens when:

$$\frac{\mathrm{d}\ \ln(f(E))}{\mathrm{d}E} = -\frac{\mathrm{d}\ \ln(\sigma(E))}{\mathrm{d}E}. \tag{4.15}$$

The model explains the dominant energy to be controlled by points of high curvature ('knee points') of $\ln(f)$ or $\ln(\sigma)$, where the main difference with LEM is that LEM assumes $\ln(\sigma)$ to be the driving force of the dominant energy and the energy-driven model assumes $\ln(f)$ to be the reason. Furthermore, the localized degradation of $N_{it}(x)$ is taken into account and the model uses only the cumulative formation of new interface defects for lifetime predictions, ignoring other possible mechanisms that affect the device parameters.

4.2.4 Bravaix Model

Bravaix *et al.* proposed a degradation model that combines the multi vibrational excitation model of Section 4.2.2 and the energy-driven aspect of Section 4.2.3 [121]. The model assumes that degradation due to SP, MP or EES are independent of each other [122] and are explained by three stress regimes. In the first HCD stress regime, the applied bias is sufficient for the electrons to gain enough energy for the SP process. This regime consists of a low flux of charge carriers (I_d) of high energy, similar to the LEM of Section 4.2.1. The second stress regime occurs at lower applied biases and multiple charge carrier collisions are needed to induce dissociation of the Si-H bond, similar to the MVE model. In the last stress regime, when V_{ds} and I_d are moderate, electrons with insufficient energy gain energy due to EES [90, 121, 123] and induce dissociation.

The dissociation rate of Si-H bonds can be linked to the total predicted device lifetime (τ) by the lifetime of the various independent breaking mechanisms[123]:

$$R_{it} = \frac{1}{\tau} = \sum_i \frac{1}{\tau_i}. \tag{4.16}$$

The lifetime of each of the stress regimes is described by:

$$\frac{1}{\tau_{sp}} = C_{sp}\frac{I_d}{W} \cdot \left(\frac{I_s}{I_d}\right)^m; \tag{4.17}$$

$$\frac{1}{\tau_{mp}} = C_{mp}(V_{ds} - \hbar\omega)^{1/2} \cdot \left(\frac{I_s}{W}\right)^{E_B/\hbar\omega} \cdot e^{E_{emi}/k_b T_L}; \tag{4.18}$$

$$\approx C_{mp}(V_{ds}^{1/2} \cdot \frac{I_d}{W})^{E_B/\hbar\omega}; \tag{4.19}$$

$$\frac{1}{\tau_{EES}} = C_{EES}\left(\frac{I_d}{W}\right)^2 \cdot \left(\frac{I_b}{I_d}\right)^m, \tag{4.20}$$

where $C_{sp,mp,EES}$ are technology-dependent constants. Depending on the technology, device dimensions and stress conditions, one device might be more susceptible to one over the other processes. However, under normal stress conditions, all processes take place simultaneously [120]. The total device lifetime (τ_d) is found by combining Equation 4.17, Equation 4.19 and Equation 4.20 [108] with some weighting factor (K_{sp}, K_{mp} and K_{EES}):

$$\frac{1}{\tau_d} = \frac{K_{sp}}{\tau_{sp}} + \frac{K_{mp}}{\tau_{mp}} + \frac{K_{EES}}{\tau_{EES}}. \tag{4.21}$$

Combining the dissociation rate of all processes, the mixed mode dissociation rate, R_{mm}, can be found and relates to the interface defect density using some technology specific parameter (c) via [120]:

$$\Delta N_{it} = -N_0 \exp(-c\sqrt{R_{mm} t_s}). \tag{4.22}$$

This model uses physical mechanisms (SP, MP, EES) to described hot-carrier degradation, but it assumes that the three processes are completely independent of each other. However, newly introduced interface defects can act as a charge trap and change the EEDF and the scattering mechanisms. This affects the SP and MP degradation mechanisms, distorting the total predicted damage.

4.2.5 Vienna Model

The Vienna model looks into the degradation and physics of single defects and scale them up to device level [95, 124]. The model assumes that since both electrons and holes affect the degradation rate, the EEDF is expanded to an Energy Distribution Function (EDF), in combination with the MVE model of Section 4.2.2. Furthermore, it is assumed that EES plays a minor, negligible role in the lifetime prediction of scaled devices (100s of nm), but becomes more significant in ultra scaled devices (10s of nm) [108, 125].

Impact Ionization may introduce secondary charge carriers that induce dissociation, and are taken into account [95]. Similar to Equation 4.6, the Vienna model uses the SP and MP bond-breaking mechanisms due to either electrons or holes, where the rate can be described according to a charge carrier acceleration integral:

$$Rate_{\mathrm{sp/mp}} = \int_{E_{\mathrm{th}}}^{\infty} f(E)g(E)\sigma_{\mathrm{sp/mp}}(E)v(E)\mathrm{d}E, \tag{4.23}$$

where f is the EDF of the charge carriers, g is the density of states, v is the charge carrier velocity and the capture cross section is defined by σ. Since both electrons and holes can induce SP degradation with an attempt frequency of ν_{sp}, the bond-breaking rate R_{sp} due to the SP mechanism can be defined by:

$$R^{\mathrm{e/h}}_{\mathrm{sp/mp}} = \nu^{\mathrm{e/h}}_{\mathrm{sp/mp}} I^{\mathrm{e/h}}_{\mathrm{sp/mp}}. \tag{4.24}$$

Similar to Equation 4.22, the time-dependent interface defect creation due SP is determined by:

$$N_{\mathrm{sp}}(t_{\mathrm{s}}) = N_0 \left(1 - \exp(-(R^{\mathrm{e}}_{\mathrm{sp}} + R^{\mathrm{h}}_{\mathrm{sp}})t_{\mathrm{s}})\right), \tag{4.25}$$

where N_0 is the interface density of available bonds to break of an undamaged device. The rates of dissociation and passivation depends on the temperature via an Arrhenius dependency:

$$R_{\mathrm{mp}} = \nu_{\mathrm{mp,act}} \exp(-\frac{E_{\mathrm{emi}}}{k_{\mathrm{b}} T_{\mathrm{L}}}); \tag{4.26}$$

$$P_{\mathrm{mp}} = \nu_{\mathrm{mp,pass}} \exp(-\frac{E_{\mathrm{pass}}}{k_{\mathrm{b}} T_{\mathrm{L}}}), \tag{4.27}$$

where ν_{mp} is the attempt frequency of MP dissociation. The time-dependent amount of interface defects due to MP is determined as:

$$N_{\mathrm{mp}}(t_{\mathrm{s}}) = N_0 \sqrt{\frac{R_{\mathrm{mp}}}{P_{\mathrm{mp}}} \left(\frac{P_{\mathrm{u}}}{P_{\mathrm{d}}}\right)^{N_1} (1 - \exp(R_{\mathrm{mp}} t_{\mathrm{s}}))}. \tag{4.28}$$

The chance of going up/down in an MVE level ($P_{\mathrm{u/d}}$) is similar to Equation 4.7 and Equation 4.8, but with the addition of holes induced degradation. The total

amount of newly created interface defects can be found similar to Equation 4.13, but in addition, a probability for each mechanism (due to competing behavior between SP and MP) is added.

The model describes the rate at which charge carriers react with the Si-H bonds at the interface reasonably well for long-channel devices, where a higher stress will lead to more degradation due to a more pronounced EDF at high energy for holes (pMOS) and electrons (nMOS). Newer models are further expanded to include quantum–chemistry formulation using their wavefunctions to give a physically meaningful interpretation, which for further reading are referred to [125, 126, 126--129]

4.3 Bias Temperature Instability (BTI)

This thesis investigates the reliability of hydrogen-related defects at the Si/SiO_2-interface, mainly introduced by HCI. Bias Temperature Instability (BTI) also affects device reliability significantly under operation conditions, especially at higher temperatures. BTI may introduce similar defects as HCD and depending on the stress conditions, this may even occur simultaneously [126]. BTI is induced when a gate-source bias is applied to the device, where a positive (negative) bias will induce PBTI (NBTI), *i.e.* during normal nMOS (pMOS) device operation. The creation of interface and oxide defects in combination with the charging of the defects is reported due to BTI and investigated for some time [130, 131], however, there is still some debate about which defect-creation process is the main contributor to the degradation [132, 133].

Since recovery after HCD (*i.e.* decharging, passivation) may follow similar mechanisms as recovery after BTI, a short overview of BTI will be given. The Reaction-Diffusion model explains BTI in terms of the dissociation and diffusion of hydrogen from the Si/SiO_2 interface and the creation of new interface defects, while the Defect-Centric model assumes that the charging of oxide defects can describe BTI degradation more accurately [134].

Although there are some reports of local variation in the degradation due to BTI [135], but generally BTI is observed to induce uniformly distributed degradation over the whole channel, so that the concentration of defects due to BTI, N_{BTI}, can be described by: $N_{BTI}(x) = C = N_{BTI}$, where x is the distance in the channel and C some constant value. Besides the gate-source voltage, the dissociation rate of hydrogen is affected by temperature. Dissociation takes place at a higher rate at higher stress temperatures (T_s), whereas HCI induces more degradation at lower T_s (for long channel MOSFETs) [136]. In this thesis, a stress temperature of $T_s = 25$ °C is usually used. Degradation due to BTI is negligible at this temperature and it is assumed and experimentally verified that most degradation can be attributed to HCI.

When V_{gs} is removed and the BTI stress phase ends, a strong relaxation effect starts to take place [136, 137]. Since the relaxation phase starts at the moment the stress phase stops and most relaxation takes place within the first microseconds, the threshold voltage and other device parameters measured with the traditional I_d-V_{gs} characterization method, do not yield the maximum ΔV_t due to BTI. To circumvent the relaxation effect, various fast measuring methods were developed, *e.g.* the on-the-fly (OTF) characterization [138] measures V_t around $V_{gs,str}$, to not interrupt the stress phase. However, these fast measuring methods have its own considerations [139]. Since this thesis mainly has a focus on the recovery of long-term (hydrogen-related) defects due to HCI, the characterization technique of Chapter 2 is used, where any BTI-specific short-term effects will remain undetected.

4.3.1 Reaction and Diffusion Model (R&D Model)

The first version of the Reaction and Diffusion model was proposed by Jeppson and Svensson [140] to describe the creation of interface traps, N_{it} and later expanded by Alam *et al.* [141--143] to describe BTI degradation. The R&D model assumes that the degradation process is a hydrogen diffusion-limited process, where the emphasis is placed on the (de-)passivation of interface traps. The first models assumed that atomic hydrogen depassivate from the interface and diffuse away in a one-dimensional manner from the interface. Later versions include molecular hydrogen and a component related to oxide traps to model BTI degradation [144].

The R&D model uses the role of hydrogen in the gate oxide to describe both degradation and the (short-term) relaxation. Although there are some questions to what degree hydrogen is responsible to both degradation and recovery in a small time frame, similar mechanisms may play a role during the recovery of hydrogen-related defects after HCD and can be considered for the transport behavior of hydrogen in the gate oxide, similar to Section 3.3.

The change in the interface defect density concentration by atomic hydrogen ([H]) is described by:

$$\frac{\mathrm{d}N_{it}}{\mathrm{d}t} = k_f(N_0 - N_{it}) - k_r N_{it}[H]. \tag{4.29}$$

The number of interface states is small at the beginning and the depassivation rate depends on the forward (k_f) and reverse reaction rate (k_r) and the total possible bonds that can depassivate (N_0) by:

$$\frac{\mathrm{d}N_{it}}{\mathrm{d}t} \approx k_f N_0. \tag{4.30}$$

This results in a time-dependent interface defect density of:

$$N_{it}(t_s) = k_f N_0 t_s. \tag{4.31}$$

Later, when the forward and reverse reaction rate in Equation 4.29 are roughly equal:

$$k_f N_0 \approx k_r N_H(x = 0) N_{it}; \tag{4.32}$$

$$N_H(x = 0) = N_{it}, \tag{4.33}$$

which results in a time-independent interface defect density of:

$$N_{it} \approx \sqrt{\frac{k_f N_0}{k_r}}. \tag{4.34}$$

Initially, hydrogen diffusion away from the interface will have a limiting influence on the interface defect creation rate. Since the hydrogen diffusion distance is defined by $x = \sqrt{D_H t}$, the time-dependent interface defect density can be rewritten as:

$$N_{it} \approx \sqrt{\frac{k_f N_0}{k_r}} (D_H t)^{\frac{1}{4}}, \tag{4.35}$$

where is assumed that the hydrogen did not diffuse through the whole oxide layer ($x < t_{ox}$), indicating that this regime can only be observed in thick oxides. When the hydrogen reaches the gate/gate oxide interface and diffuses into the polysilicon gate, it will diffuse away from the gate oxide, lowering the effective N_H. This will result in the interface defect density being described as:

$$N_{it} \approx \sqrt{\frac{k_f N_0}{k_r}} \sqrt{D_H t_s}. \tag{4.36}$$

When all possible Si-H bonds that could have been broken are broken and steady-state is reached, the interface defect density will be defined by:

$$N_{it} \approx N_0. \tag{4.37}$$

The first models assumed that the hydrogen-related reactions were of the form: Si-H $\rightarrow$ Si $\cdot$ + $\cdot$H, where only one-dimensional diffusion of atomic hydrogen was assumed. Later models were expanded by incorporating molecular hydrogen (H_2), three-dimensional diffusion in the gate oxide and defect assisted dimerization of hydrogen via:

$$Si - H + \cdot H \rightarrow Si \cdot + H_2. \tag{4.38}$$

This suggests that atomic hydrogen near the interface may introduce new defects. Substituting the diffusion of D_H by D_{H_2}, a $t_s^{1/6}$ time-dependent behavior can be found [145]. Using the defect assisted dimerization of molecular hydrogen, the recovery (passivation) process is described by the reverse reaction:

$$Si \cdot + H_2 \rightarrow Si - H + \cdot H; \tag{4.39}$$

$$Si \cdot + \cdot H \rightarrow Si - H. \tag{4.40}$$

Before Equation 4.40 can take place, the H atom needs to diffuse to another available Si atom with a dangling bond. During diffusion, a competing reaction with Equation 4.38 may take place, so that effectively no recovery takes place. The chance of reacting according to Equation 4.38 instead of Equation 4.40 becomes higher if the ratio $\frac{N_{it}}{N_0}$ becomes lower, indicating that the recovery mechanism eventually ends up in a steady-state.

The first R&D model describes the BTI-induced shift in electrical parameters by the (de-)passivation of Si-H bonds and the role of hydrogen. However, the contribution due to hole (de-)trapping and oxide defects are not taken into account [133, 136]. Later contributions to the model assumed that the shift in parameter due to N_{it} is unrelated to contributions by N_{ot}, splitting the shift in threshold voltage in several components:

$$\Delta V_t = \Delta V_{t,it} + \Delta V_{t,ot}. \tag{4.41}$$

Even though the model describes the influence of hydrogen on the degradation and recovery rate, there is some mismatch with the literature on the role and model parameters of hydrogen [133]. *I.e.*, the R&D model assumes that

the process of hydrogen (de-)passivation of dangling bonds at the interface is a fast reaction, although the Si-H bond is reported to be stable. Furthermore, the R&D model assumes that the forward and reverse reaction rate of Equation 4.42 have approximately equal reaction rates and the same activation energy: $E_{a,R\&D} \approx 0.2$ eV, to ensure fast (de-)passivation:

$$\mathrm{Si-H} \rightleftharpoons \mathrm{Si}\cdot + \mathrm{H}\cdot . \tag{4.42}$$

However, this value for the activation energy does not match with literature (Chapter 3) and experimentally found values for the activation energy (Chapter 5). Recovery rates by molecular hydrogen are reported to follow the passivation step during fabrication with an activation energy of $E_a \approx 1.5$ eV [58, 133]. Furthermore, if the recovery process of BTI was only dependent on the back diffusion of hydrogen, the recovery rate should depend on the stress time. The longer the stress time, the longer there is time for the hydrogen to diffuse away from the Si/SiO_2 interface [146].

4.3.2 Defect Centric model (DC Model)

The defect-centric (DC) model assumes that charge (de-)trapping is mainly responsible for the degradation/relaxation behavior, although hydrogen can play a (minor) role [147]. The model uses a four-state model (expanded from the earlier two-state model), multi-state/nonradiative multiphonon (NMP) models to describe BTI. It was first assumed that existing SiO defects in the gate oxide (**E** in Figure 3.1) can be described by 4 states [148, 149]. Figure 4.5 shows a schematic visualization of the process and the four states (neutral stable (1), neutral meta-stable (1'), charged meta-stable (2') and charge stable (2). When a bias is applied and hole capture takes place, the oxide-defect from the neutral stable state to the charge stable state via the metastable (2') state ($1 \rightarrow 2' \rightarrow 2$). The relaxation phase is described by hole emission that happens from the charge stable state to the neutral stable state via a fixed trap when a higher bias is applied ($2 \rightarrow 2' \rightarrow 1$) or via a switching oxide trap when a lower bias is applied ($2 \rightarrow 1' \rightarrow 1$) [150, 151].

Here depend the capture/emission time constants of each defect on the temperature and the emission/capture activation energy, which is visible on capture-emission time maps [152, 153]. Using the capture-emission time maps, two distributions corresponding to a permanent, P, and reversible, R, component were found to be uncorrelated. The permanent part is assumed to be partly made up of interface states [136, 154, 155], but oxide traps contribute more significantly to the permanent part [148].

The relaxation phase of both components can be modeled by the empirically found, universal relaxation equation [147, 156]:

$$\Delta V_t(t_{rec}) = P + R = P + \frac{R_0}{1 + B\xi(t_{rec})^{\beta}}, \tag{4.43}$$

where R_0 is the recoverable component at $t_{rec} = 0$, B and β are fitting parameters and $\xi(t_{rec}) = \frac{t_{rec}}{t_s}$. The permanent component is here modeled as

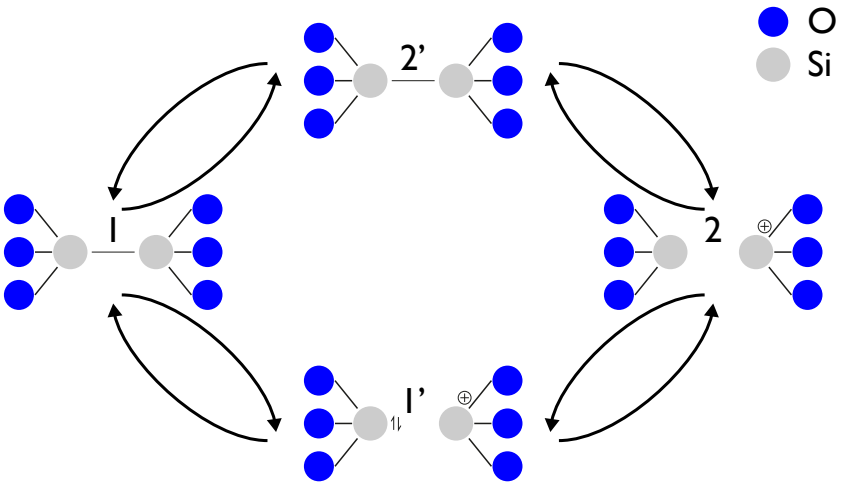

Figure 4.5: Four states of the defect, modeled around the oxide defect in the gate oxide. Image after [148].

being not recoverable, however, it is to be observed to be 'semi permanent' and recovery does occur at specific bias/temperature conditions [157].

The role of atomic hydrogen is incorporated into the model to account for the introduction of the more permanent interface states when a device is stressed for long stress times at a high-stress temperature. The gate-side hydrogen release model [158] assumes that hydrogen can dissociate from the oxide-gate interface and diffuse rapidly into the gate oxide [159], where it can get trapped and change the hydrogen distribution, resulting in a quasi permanent (P) defect, making this model a reaction-limited process.

The DC model describes the degradation and relaxation behavior by charge (de-)trapping, where hydrogen only plays a minor role in the process. Current models are expanded by including the role of hydrogen released from the oxide-gate interface, however, it still plays a minor role. It is argued that hole de-trapping happens in a fast process, so that at longer periods the data seems to be less consistent with the DC model [160]. Furthermore, it was argued that the model does not always seem to be consistent across various material types and degradation/recovery conditions (bias, temperature, ac vs dc conditions) [133, 160] and that physics-based models are needed for DC and AC stress for quantitative predictions [133].

4.4 TDDB and SILC

Although the main point of interest of this thesis is hydrogen-related defects, HCI and BTI may also introduce oxide defects and to be taken into account, as discussed in the previous section. Some oxide defects will be present right after fabrication (see Chapter 3), which may act as a tunneling/hopping center and assist a charge carrier to go through the insulator (Frenkel-Poole emission). When a gate-source voltage is applied to a device, new oxide defects may be created over time [161] in addition to the already existing oxide defects [162--164]. When a lower gate-source bias is applied over a long time, Stress-Induced Leakage Current (SILC) will take place. The creation of new oxide defects will result in more trap-assisted tunneling of charge carriers through the insulator, which gives rise to an increase in the gate current over time [165]. When a high bias is applied over a long time, Time-Dependent Dielectric Breakdown (TDDB) may take place, where sufficient oxide traps are created in the gate oxide to form a conducting path through the insulator, *i.e.* dielectric breakdown takes place [166--168].

4.5 Thermal Degradation and Heating Effects

Temperature affects the degradation rate during electrical stress, *i.e.* the degradation rate will increase for BTI and decrease for HCI at a higher stress temperature. Besides affecting the degradation rate during electrical stress, a high temperature may also induce thermal degradation, with or without any bias. Figure 4.6 shows V_t as a function of the anneal temperature, measured at $T_m = 25$ °C, where the devices were exposed to increasingly higher anneal temperatures in air (**Method A** of Section 2.3) when no bias was applied. During each step, the device was kept at the anneal temperature for $t_a = 2$ hours. Up to an anneal temperature of $T_a \approx 400$ °C no significant ΔV_t is observed. Higher temperatures show an increase, indicating that thermal degradation of this device takes place when it is annealed in air and when $T_a > 400$ °C.

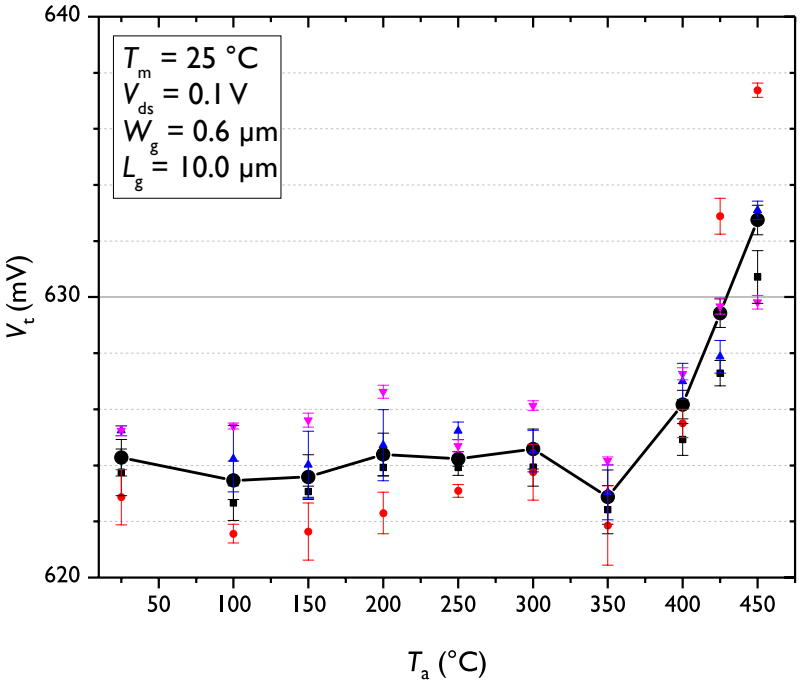

Figure 4.6: Threshold voltage of four devices as a function of the anneal temperature. The devices are measured at $T_m = 25$ °C.

Thermal degradation may be explained by thermal dissociation of Si-H bonds at the interface, which is in line with earlier reports that temperature range [87, 88]. Furthermore, when annealing is done in air at $T_a > 450$ °C, the color of the chip starts to change (left of Figure 4.7) and small bubbles begin to form on the bond pads, indicating that recovery by annealing cannot be achieved of this devices at such high temperatures.

Besides thermal degradation, an elevated temperature may have a healing influence on certain device parameters. This would be make it necessary to balance positive and negative effects of an elevated temperature. Devices

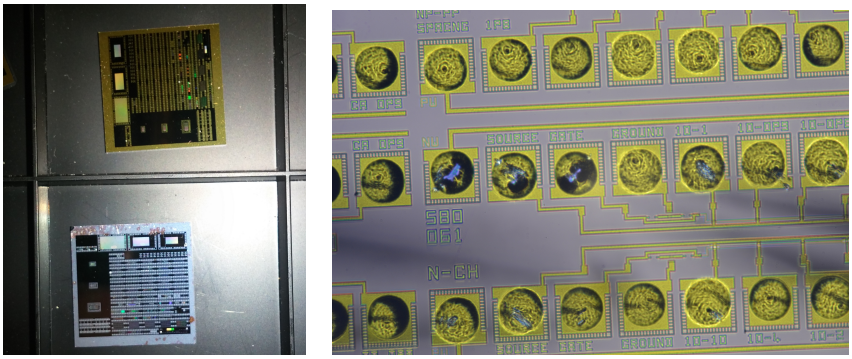

Figure 4.7: Left: A chip before anneal (top) and after the anneal (bottom), where a color change can be observed due to the anneal. Right: Bond pads begin to shows bubbles after a high temperature anneal, making accurate measurement more difficult.

fabricated with a self-curable gate have been created [169, 170], where electrical annealing using Joule heat through a built-in heater in a gate is used to repair the defects. A local temperature at the gate of $T_a > 800$ °C is reached for a short moment of time $t_a < 1$ ms, suggesting that a longer anneal time at a higher temperature is necessary to heat up the whole device and induce thermal degradation. This method is however energy inefficient, making it an inconvenient method to induce recovery on chip level, repairing all transistors on a chip.

Newer generations of transistors, *i.e.* FinFETs and UTB SOI transistors, may have a reduced thermal conductivity with the substrate [171]. This will make it harder for the hot-carriers to lose heat, increasing the device temperature. This self-heating effect will increase the degradation rate for BTI and HCI in smaller devices [172, 173], however, a higher temperature may also favor a higher recovery rate (see Section 5). The effect on the number of fins in a FinFET on the HCD is studied in [174, 175], where is reported that an increase in the number of fins makes it harder to lose the generated heat, *i.e.* the fewer fins present, the lower the effect of self-heating on the degradation [176]. This change in dimensions and the self-heating effect may result in a shift in degradation/recovery equilibrium for devices on chip level.

4.6 Plasma Induced Damage (PID)

Plasma processing is widely used during the fabrication process of devices, *e.g.* for etching. When a MOSFET is exposed to plasma, plasma-induced damage (PID) may take place, which is based on charging damage, physical damage or radiation damage [177--179]. During plasma processing the gate dielectric experiences electrical stress by the conduction current or the potential difference between the gate electrode and the Si substrate [180]. This electrical stress may generate defects in the gate oxide or at the Si/SiO_2 interface [181], increasing the gate current [182].

Depending on the RF power to create the plasma, P_{rf}, and the plasma species, energetic ions accelerated by the electric field may damage the device. Furthermore, degradation due to radiation can take place, explained by charging of the device and photoconduction currents in the gate dielectric due to photon irradiation (UV) and the introduction of new defects, created by the generation of new electron-hole pairs [183].

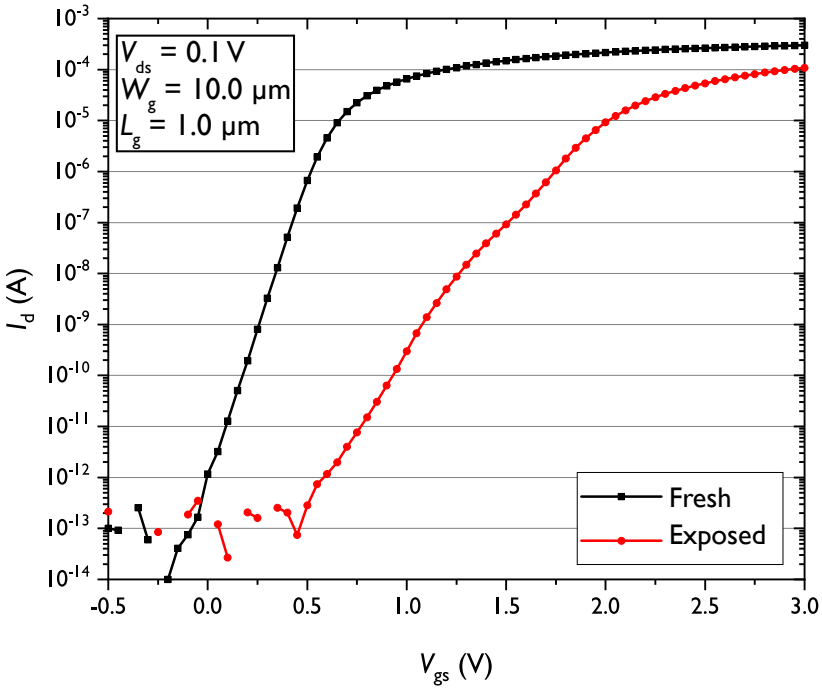

Figure 4.8: IV-curve of a fresh device before and after exposure to hydrogen plasma (P_{rf} = 2 kW.)

The effect of PID on a device is shown in Figure 4.8, where a fresh, undegraded device was heated up (T_a = 200 °C) and exposed to a plasma made of hydrogen and nitrogen. An increase in V_t, SS and N_{cp} is measured, indicating that the device suffers from plasma-induced damage. In addition, the appearance of a subthreshold hump [184] can be observed, indicating a build-up of fixed charge and the introduction of new defects. Figure 4.9 shows the CP

current before (black) and after (red) exposure to the plasma of the same device. Besides an increase in I_{CP} due to the introduction of new interface defects, the fixed charge caused a shift to the right with respect to the black curve, visualized with the gray curve (black curve multiplied by 25). When high frequency ($f_{cp} = 3$ MHz) CP measurements are compared to lower frequency CP-measurements, only a minor increase in the number of oxide traps could be measured.

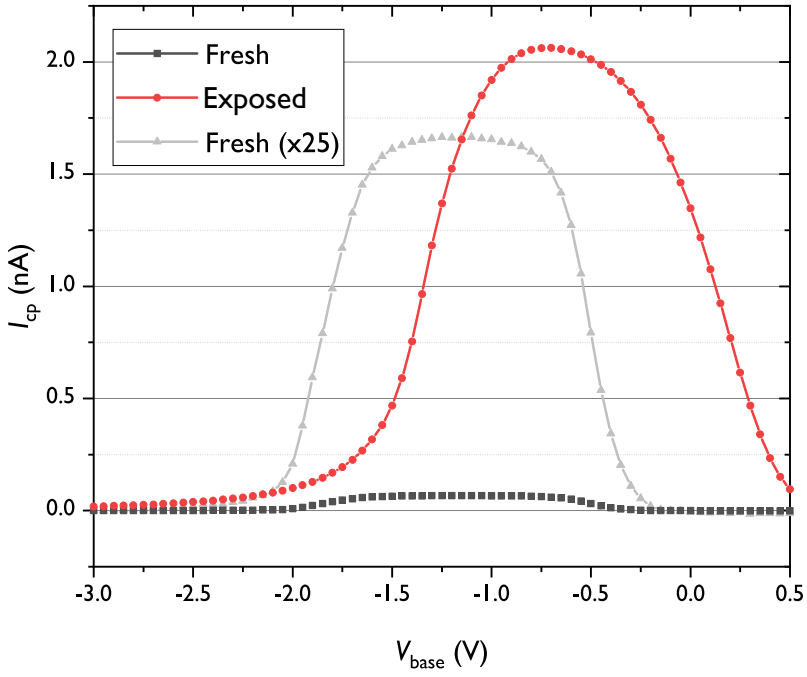

Figure 4.9: Charge pumping current before (black) and after (red) hydrogen plasma exposure. The curve before plasma is increased with a factor 25 (gray) to visualize the build-up of fixed charge (shift to the right).

4.7 Summary and Conclusion

During the operation of a device, various degradation mechanisms take place. Although various material/operation-specific improvements have been made to minimize the degradation, it is not possible to completely remove them, which will eventually lead to device breakdown and its end-of-life. The main conclusions of this chapter are:

- The various degradation mechanisms may introduce material changes in the device during its lifetime.
- Although various methods have been used to minimize degradation, it is not possible to completely prevent all degradation.
- New defects that were first passivated with hydrogen have a big influence on the reliability of a device.

To minimize the effect of defects and extend the lifetime, the next chapter will discuss various methods to increase the recovery and recovery rate after degradation.

CHAPTER 5

Enhancing Recovery

5.1 Introduction

Silicon-based devices like MOSFETs will degrade during their operating lifetime, resulting in a shift in various parameters that electrically define the device (Chapter 4). When the parameter shift exceeds a preset value, the device cannot be used anymore. It is possible to (partly) repair the introduced damage using various methods. For instance, processes used during the fabrication of the device have proven to have a positive influence on electrically degraded devices too. The recovery processes to enhance the recovery rate include annealing [185--188], the introduction of passivating material (*e.g.* hydrogen), light-soaking [189] and applying an appropriate bias [190] to the device or the combination of above. Degradation mechanisms will introduce charge trapping, defect formation in the gate oxide and at the interface, and although there is still some discussion to what degree (Chapter 4), there is however consensus that for both degradation and recovery, hydrogen plays a pivotal role [91].

In this thesis, the focus is on hydrogen-related recovery where the goal of the recovery step is visualized in Figure 5.1. First, hydrogen will depassivate from the interface due to degradation, introducing P_b-centers. Next, hydrogen may repassivate the created interface defects during a recovery step and the device can revert back to the initial situation after fabrication. The hydrogen density at the interface is related to the concentration and diffusion of hydrogen species (H, H^+, H_2) in the device. The diffusion rate in Si and SiO_2 is known to be different [159], suggesting that the materials in the immediate vicinity of the defective interface matter for recovery. Electrical stress will break Si-H bonds at the Si/SiO_2-interface of passivated devices, but a decrease in the number of interface states is even reported if no passivation step during fabrication was done [57]. This indicates that there is a steady-state passivation level, depending on various factors, *e.g.* temperature.

Parts of this chapter have appeared in [MJdeJ:206, 214]

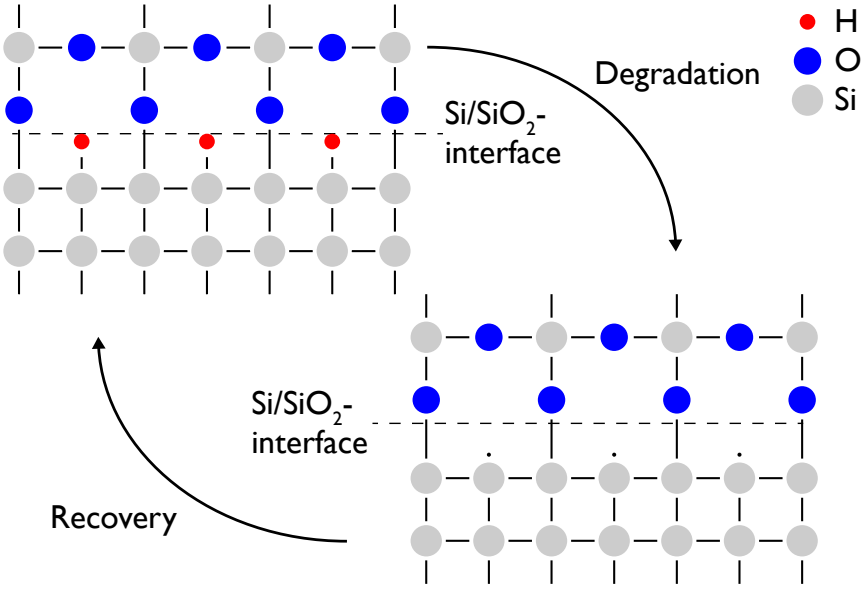

Figure 5.1: Device with a passivated (top left) and a depassivated interface (bottom right).

This chapter will discuss various methods to induce and enhance recovery in an electrically degraded device (nMOS). Recovery will reduce the stress-induced shift in parameters [191, 192] back to or approach the initial value of a fresh device. Some recovery methods affect the recovery rate not significantly and will be discussed briefly: the influence of light (Section 5.2) and the influence of a bias applied to the gate (Section 5.3).

The recovery rate can be more affected using the anneal temperature and the ambient the device is annealed at. This will be discussed in more detail in Section 5.4 and Section 5.5.

5.2 Light-soaking

During the life of solar cells, light-induced damage (LID) may take place. New boron-oxygen related defects are introduced in the solar cell when it is exposed to light, which will result in a lower efficiency. Exposure to light during annealing (recovery step) was found to have also a positive effect on the reliability and efficiency of p-type Czochralski Silicon solar cells [189, 193, 194]. During light-soaking annealing ($\approx$ 10 *suns*), high-intensity illumination can be used to accelerate defect formation and the charge state control of hydrogen and B-O defects is used to induce long-lasting passivation of B-O defects [195]. This prevents the creation of B-O defects due to light-induced damage of the Staebler-Wronski effect [196].

Light-soaking during annealing of HCD devices does not enhance the recovery to overcome the Staebler-Wronski effect (since no B-O defects are created

during HCl), but it raised the question of whether light-soaking could tune the charge state of H-atoms and influence the recovery rate for the experiments discussed in this thesis. A few experiments have been done to investigate the influence of light on the recovery rate of HCl degraded devices. When the device parameters are monitored during the anneal step, the recovery rate is visible in the slope from the stressed parameter value back to the post-anneal value as a function of anneal time. A change in the recovery slope should be observed if light (light intensity: > 5.6 Mlux, Color Temperature $T \approx 6500$ K, Volpi IntraLED 2020) affects the recovery rate and is turned on halfway through the recovery step. However, no change in recovery rate was observed when V_t, N_{it} were measured as a function of time, suggesting that the recovery rate cannot be improved by the use of light-soaking under the experimental conditions in this thesis.

5.3 Bias

Bias-dependent recovery is reported [197], where a bias may have a positive influence on the recovery rate. When a bias is applied to a device during measurement, in some cases the amount of degradation and recovery depends on the number of measurements done [198]. This is also visible when IV-measurements are done before and after a CP-measurement, where a small difference in V_t (recovery) can be measured ($\Delta V_t \approx 3$ mV).

The repassivation of interface defects depend on the supply (and thus concentration) of hydrogen at the interface. It was observed that hydrogen ions could be moved in the gate oxide by applying a bias due to proton drift [73]. Due to a positive bias, protons will move from the top of the gate oxide towards the Si/SiO_2-interface and would provide a higher concentration of passivation species under the right conditions [199]. When hydrogen is moved towards the Si/SiO_2-interface by applying a bias to the gate, this would lead (locally) to a higher concentration of hydrogen. Depending on the equilibrium between protons, molecular hydrogen and Si-H bonds, it raised the question of whether it may potentially enhance the recovery rate under the experimental conditions discussed in this thesis. The experiments mentioned above used a gate oxide where the oxide thickness had a sufficient thickness ($t_{ox} > 40$ nm), to ensure that hydrogen can move to and from the P_b centers within the gate oxide. The charged hydrogen ions will affect V_t when it is near the interface to create a proton-based non-volatile memory [73, 199].

To investigate if a gate bias can be used to enhance the recovery rate under the experimental anneal conditions, *e.g.* by moving hydrogen inside a thinner gate oxide, a device ($t_{ox} = 7$ nm) was degraded by HCl and recovery was done at an elevated temperature. The device was degraded at room temperature ($t_s = 3 \cdot 10^3$ s, $V_{gs} = 2.1$ V, $V_{ds} = 4.5$ V, $\Delta V_t \approx 320$ mV), after which the device is annealed at $T_a = 150$ °C. Initially, only recovery as a function of anneal time due to the temperature step is observed (without applying any bias to the gate). After $t_a \approx 2 \cdot 10^3$ s, a bias is applied to the gate, and a change in recovery rate

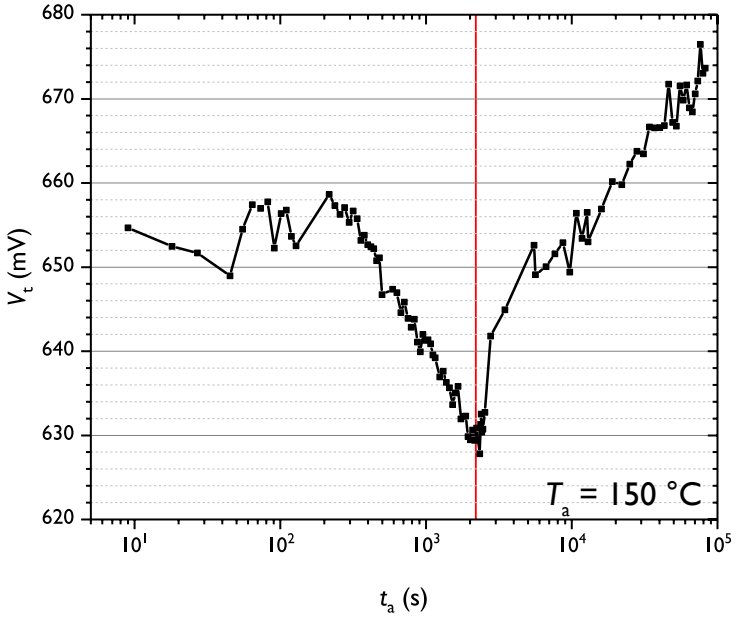

Figure 5.2: Recovery of V_t of a nMOS as a function of the anneal time at $T_a = T_m = 150$ °C (W/L = 10.0 µm/0.8 µm). Left of the red line: no bias is applied to the device. Right of the red line: a gate bias of $V_{gs} = -4.5$ V is applied to the device.

should be visible if the bias has a positive/negative influence by a change in the recovery slope.

First, no change in the recovery rate of the threshold voltage is observed when a bias is applied, however, when a larger bias is used (on a different device), ΔV_t starts to increase, indicating that degradation takes place ($V_{ds} = 0$ V, $V_{gs} = -4.5$ V). Figure 5.2 shows that V_t becomes larger after $t_a \approx 2 \cdot 10^3$ s, when the bias is applied to the gate of the device.

Some recovery takes place due to annealing the device, however, no significant improvement in recovery rate by applying a gate bias was observed under the experimental conditions. A possible explanation could be that an electric field has no significant influence on the local hydrogen concentration, since the gate oxide is thin enough to have an uniform concentration of proton or that the proton concentration in the gate oxide is too low. To minimize the number of mechanisms that can affect the recovery rate and since bias did not have a significant, positive influence on the recovery rate, the remainder of the thesis has a focus on material-specific solutions with a stronger influence on the recovery of electrically degraded devices (temperature, ambient).

5.4 Recovery Experiments in a Nitrogen Ambient

Total recovery of a hot-carrier degraded device takes place after annealing at $T_a \approx 400$ °C [200] within a reasonable anneal time ($t_a < 2$ hours). At lower temperatures, only partial recovery takes place, but at a higher recovery rate than at room temperature. Various anneal methods include: using a thermochuck, joule heating of the gate [201, 202], using a microheater [187, 203, 204], or using joule heating with a gate all around device [205].

This section will provide the analysis of the experimental data investigating the spontaneous recovery of hot-carrier degraded devices in a nitrogen ambient as a function of the anneal temperature, the gate length and cooling rate. The experimental results formed the basis for Reference [206]. Since no hydrogen was supplied from the outside via an ambient, it was assumed that hydrogen in the gate stack itself provide all passivation material, see Chapter 3.

5.4.1 Experimental

Hot-carrier stress was applied for a cumulative stress time of $t_s = 3$ ks ($T_s = 25$ °C) if not otherwise specified. The drain-source bias was kept at $V_{ds} = 4.5$ V (except for the longest channel device, $L = 10$ μm) and the gate-source bias was kept so that $|I_b|$ was maximum, according to Table 5.1. There was a delay of 1 s between the stress and measurement phase, to minimize short time-scale recovery components and only take potential long-term effects into account. The electric parameters were determined by the average of 15 IV-curves.

Table 5.1: HCI stress conditions for nMOSFETs of various gate lengths ($W = 10.0$ μm) for $t_s = 3$ ks.

L (μm)	V_{gs} (V)	V_{ds} (V)
0.6	1.7	4.5
0.7	1.7	4.5
0.8	2.1	4.5
0.9	2.1	4.5
1.0	2.1	4.5
10.0	1.7	6.5

Positive bias temperature instability (PBTI) was measured on a separate device under identical gate-source bias conditions as for HCI with the source and drain terminal kept connected to the ground [207]. The BTI stress caused no measurable ΔV_t (< 1 mV), indicating that BTI degradation can be neglected in this experimental investigation.

After the stress phase, the devices were annealed die for die in a nitrogen ambient (temperature ramp rate: $\sim 8\ ^{°C}/_{min}$) according to Figure 2.13a for 60 minutes. No bias was applied to the device terminals during the anneal step. After characterization at room temperature, the devices were annealed again in a nitrogen ambient at increasing higher temperatures (from $T_a = 100$ °C up to $T_a = 540$ °C). After the anneal at $T_a = 500$ °C, an anneal at $T_a = 400$ °C and

an anneal at $T_a = 350$ °C were done again, each followed by characterization at room temperature.

5.4.2 Anneal temperature dependence

The influence of the anneal temperature on the HCI-induced ΔV_t is shown in Figure 5.3. Characterization was always done at $T_m = 25$ °C, where the temperature indicates an anneal for $t_a = 7200$ s at T_a. The similar V_{ds} over all gate lengths resulted in different HCD induced ΔV_t. The recovery behavior depends on the anneal temperature, where more recovery is induced after an anneal at a higher temperature. After an anneal at $T_a = 350$ °C to $T_a = 400$ °C, $\Delta V_t \approx 0$, suggesting complete recovery has taken place. This temperature coincides with the before mentioned temperature during the PMA step and corresponds with the earlier reported temperature where total recovery takes place [188, 200, 208]. The devices with more degradation show a higher absolute recovery rate, although normalized to the maximum ΔV_t of each gate length, all devices show similar recovery.

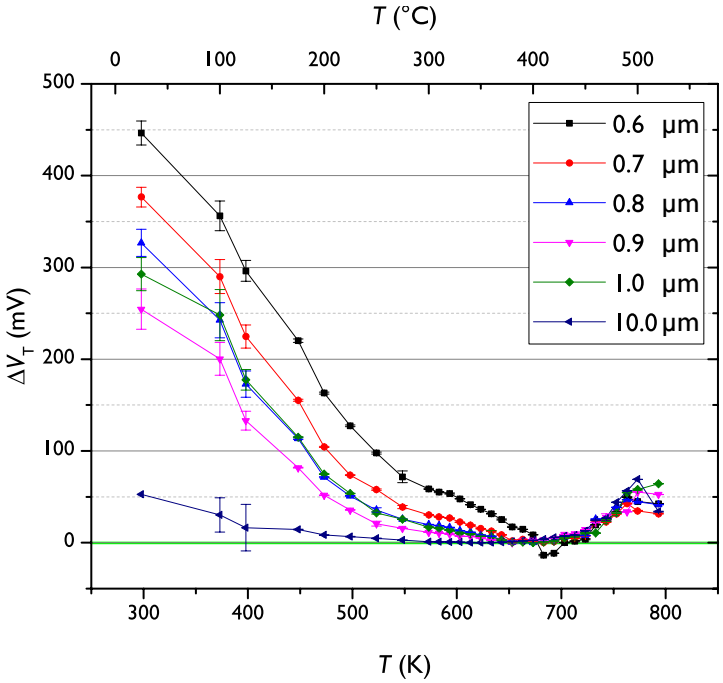

Figure 5.3: The shift in the threshold voltage as a function of anneal temperature. The devices have a gate width of $W = 10$ µm, a gate oxide thickness of $t_{ox} = 4.5$ nm and the legend indicates L in µm. Characterization was done at $T_m = 25$ °C.

A temperature of $T_a \approx 400$ °C corresponds to a thermal energy higher than the bonding energy of Si-H bonds. Exposure to higher temperatures, $T_a > 450$ °C, results in an increase of V_t. This temperature coincides with earlier

reported temperature where thermal degradation starts to take place [87, 209], suggesting that more P_b-centers at the Si/SiO_2-interface are introduced by the anneal due to the dissociation of the Si-H bond. The shift in V_t is similar for all devices, suggesting that defects are introduced at the same rate/concentration, regardless of the gate length.

Since total recovery can be achieved in devices with hot-carrier induced degradation, an additional anneal was performed after the last data point of Figure 5.3 where thermal degradation had taken place. The anneal was done at $T_a = 400$ °C and $T_a = 350$ °C, the temperature where total recovery was observed in Figure 5.3, to verify if thermal degraded devices show similar recovery. However, no significant recovery was observed after the additional anneal step, indicating a different kind of damage is caused by thermal degradation. A possible explanation is that hydrogen may diffuse out of the device, similar to the out-diffusion of hydrogen into vacuum [87]. This may lead to a lower hydrogen concentration for the recovery step, however, this is not in line with recovery observed at even higher temperatures [203, 204].

Stesmans' model of Equation 3.13 may be used to model the time-dependent recovery. Using Equation 2.14 and Equation 2.15 and the assumption that $\Delta V_t \propto \Delta N_{it}$ and $\Delta N_{it} \gg N_{unstressed} \rightarrow N_0 \approx \Delta N_{it}$, Stesmans' model can be used in combination with $DeltaV_t$ to model the recovery of Figure 5.3 up to a temperature of $T_a \approx 400$ °C and describe the ratio between the unpassivated interface defects ($[P_b]$) and the maximum number of interface defects (N_0).

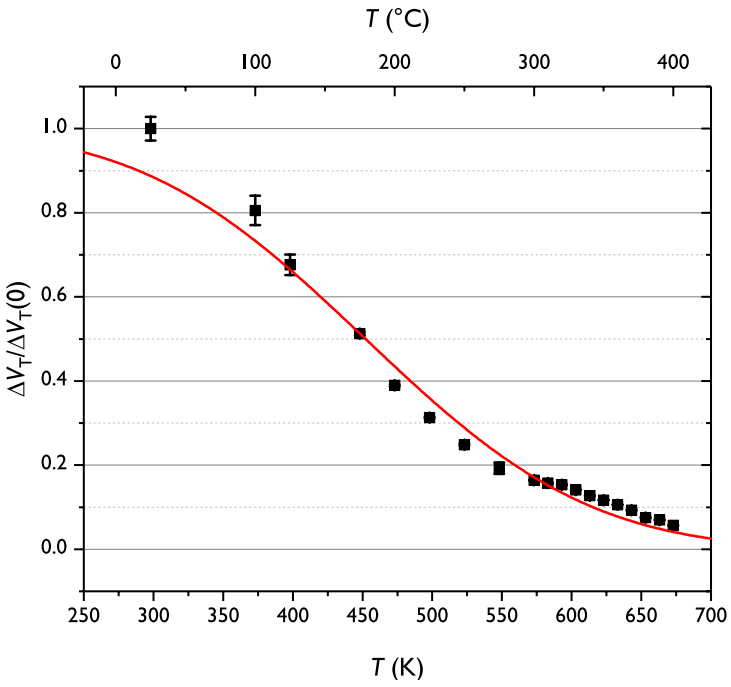

Figure 5.4: The data of the device with $L = 0.6$ µm in Figure 5.3 fitted by the passivation model of Stesmans [65].

The volume concentration of molecular hydrogen in SiO_2, $[H_2]$, is assumed to be $\approx 10^{18}$ cm^{-3} [210] and we assume that no significant change in hydrogen concentration takes place when $T_a < 400$ °C. Solving Equation 3.13 under the previously mentioned assumptions using the least-squares method, the forward reaction rate parameters of $E_f = 1.39$ eV, $\sigma_{E_f} = 0.369$ eV and $k_{f,0} = 2 \cdot 10^{-7}$ cm^3/s are found, resulting in the fit of Figure 5.4.

Note that besides the assumption that the hydrogen concentration does not change, annealing was done on one device at increasing higher temperatures, giving a cumulative effect at the higher temperatures. Since recovery shows a linear dependence on log scale, the extra recovery at a higher temperature is mainly attributed to a higher anneal temperature over the longer cumulative recovery time. Although the values are somewhat different than previously reported values [65, 188], the model of Stesmans' is consistent with the data of the relative ΔV_t-recovery.

5.4.3 Gate length dependence

The previous section showed that the recovery of hot-carrier degraded devices by annealing is in line with Stesmans' passivation model. The model assumes that the passivation rate depends on the concentration of hydrogen at the Si/SiO_2-interface, where a higher concentration will lead to a higher passivation rate and more recovery. Since the various materials that make up a MOSFET (Figure 2.1) will contain different concentrations of hydrogen due to differences in solubility (Chapter 3), devices of different technologies and dimensions may have different recovery rates. Defects created in a device of a smaller gate length will be located closer to the source, drain and spacers of a MOSFET, where a different hydrogen concentration may influence the passivation rate.

To investigate if the recovery by annealing of degraded devices is affected by gate length, devices of various gate lengths are stressed by hot-carrier injection. Although the defect creation will be primarily located (relatively) close to the drain, regardless of gate length, it is assumed that sufficient defects will be created at a different absolute distance from the drain. A roughly similar ΔV_t was induced in the devices, after which the devices were annealed at increasing higher temperatures, where characterization was done at $T_m = 25$ °C. The absolute shift in g_m due to recovery of the devices as a function of anneal temperature of ΔV_t is shown in Figure 5.5. This experiment is similar to Figure 5.3, but where the difference in absolute ΔV_t after stress will be smaller for all gate lengths. The relative recovery of Δg_m is shown in Figure 5.6, where a typical value before (after) stress is $g_m = 663$ (318) μA/V ($W = 0.6$ μm.)

Both figures show recovery as a function of anneal temperature, however, no strong relation between gate length and anneal temperature up to $T_a = 350$ °C can be observed, suggesting that the concentration of hydrogen for passivation is not strongly affected by the gate length of the devices within this gate length range.

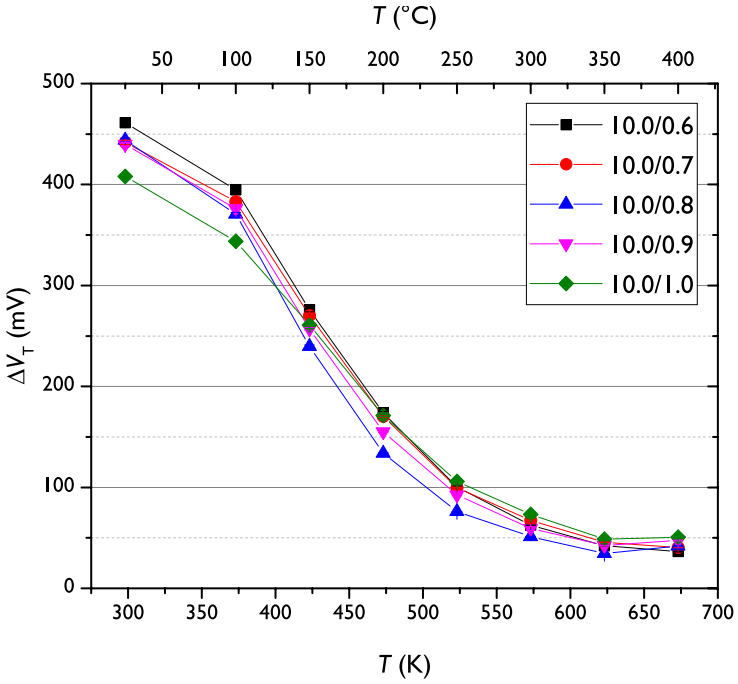

Figure 5.5: Recovery of ΔV_t as a function of the applied thermal treatment. Characterization was done at $T_m = 25$ °C. The legend indicates W/L in µm/µm and the gate oxide thickness was $t_{ox} = 4.5$ nm.

5.4.4 Cooling rate dependence

It is reported that during the hydrogenation process of polycrystalline silicon thin-film transistors in forming gas, the concentration of hydrogen gettered at the grain boundaries in the poly-Si films can be influenced by the cooling rate [209]. It was proposed that most hydrogenation does not take place at the temperature of maximum passivation ($T_a = 400$ °C), but during cooling down from this temperature. It was noted that at $T_a = 400$ °C a significant portion of hydrogen is re-emitted due a thermal energy higher than the binding energy.

The authors of Reference [209] proposed that the total amount of hydrogen gettered at the grain boundary was determined during the cooling process, where the cooling rate determines the diffusion distance/area from where hydrogen can getter at the grain boundary. This raises the question of whether the cooling rate can be used to increase the hydrogen concentration at the Si/SiO_2-interface and subsequently enhance the passivation rate.

The three cooling rate processes investigated are: quench cooling, where the device is rapidly cooled, slow cooling, where the device is cooling in a linear manner to room temperature (RT) and stepped cooling, where the anneal temperature lowers in step wise manner to RT. Figure 5.7 shows the schematic representation of the influence of the cooling rate on the area from where hydrogen (red circles) may diffuse towards the Si/SiO_2-interface and contribute

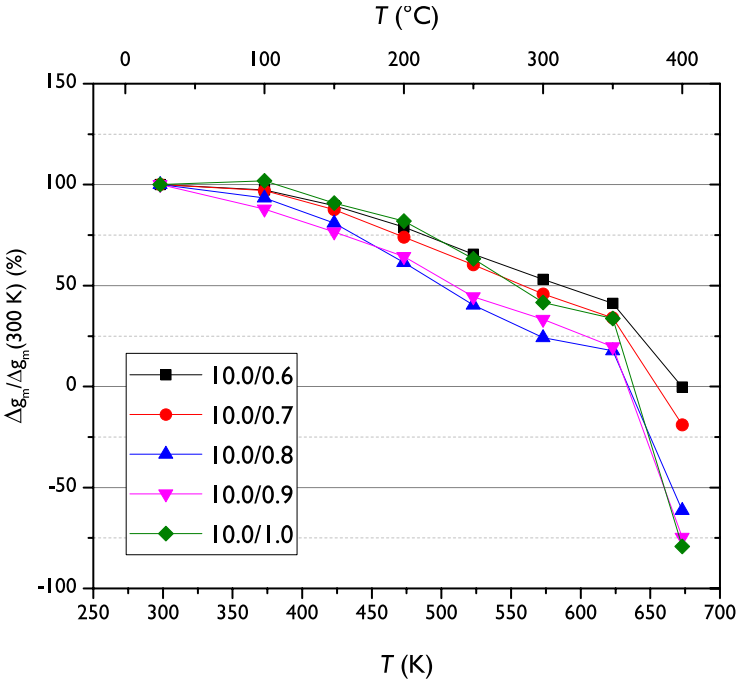

Figure 5.6: Relative recovery of Δg_m. The percentage indicates how much of the HCD induced Δg_m is still present. Characterization was done at $T_m = 25\ ^\circ C$. The legend indicates W/L in µm/µm and the gate oxide thickness was $t_{ox} = 4.5$ nm.

to the passivation process.

Degradation was done according to Table 5.1. The quench cooling (the blue curve in Figure 5.8) was done by removing the device from the furnace. The slow cooling (the black curve) had a cooling rate of $6\ ^{\circ C}/_{min}$. The stepped cooling (the red curve) was done with steps of $\Delta T = 18\ ^\circ C$, after which the temperature was kept constant for 10 minutes. This was done step by step to a temperature of $T_a \approx 110\ ^\circ C$, below which any extra recovery should be negligible [188].

Figure 5.9 shows the recovery of SS (top) and the recovery of $I_{d,lin}$ (bottom) as a function of the annealing temperature. Similar recovery behavior of SS and $I_{d,lin}$ are seen for all cooling rates, suggesting that the cooling rate has no strong influence on the hydrogen concentration at the Si/SiO_2-interface and the recovery rate. No significant difference in recovery was observed between the devices of different gate lengths.

In summary, the devices show no significant difference in recovery as a function of the cooling rate, suggesting that hydrogen does not getter at the interface in a similar manner as reported by Shika *et al.* [209]. The difference may be attributed to a different physical situation, in particular, the annealing ambient and the difference between poly-silicon grain boundaries and the Si/SiO_2-interface. Since no clear cooling rate dependency on the recovery rate

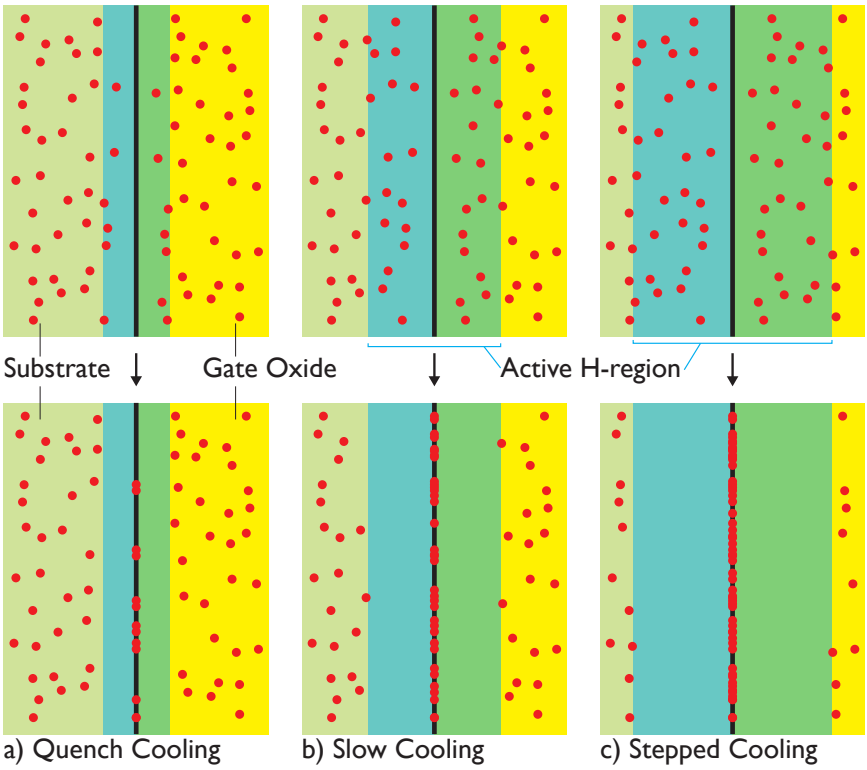

Figure 5.7: Schematic visualization of the gettering process under various cooling rates. The top row visualizes the situation at the anneal temperature, whereas the lower row visualizes the situation after cooling down. The blue area indicates which part of the device can contribute hydrogen (red circles) to the passivation process.

was found for the devices under study, it is assumed that the cooling does not enhance the local concentration of hydrogen.

5.4.5 Difference in Recovery Rates of Device Parameters

The parameters SS and V_t are affected by the number of interface defects, N_{it}, oxide defects and fixed charge in the oxide (Equation 2.3 and Equation 2.15). Figure 5.10 shows SS as a function of V_t [211], where the slope can be used to indicate if the proportion of the degradation and recovery contributed to interface defects [212] will change. The green line is a guide to the eye, indicating a constant proportion of the degradation contributed to ΔN_{it}. During stress, the degradation of V_t and SS do not change perfectly proportional at the same rate for different stress times, in contrast to an earlier report [212]. This may be explained by fixed charge, that gets introduced when the device is stressed for a longer time, changing the measured SS (Equation 2.4). The recovery phase does follow the proportionality line until almost complete recovery is achieved for increasing higher temperatures.

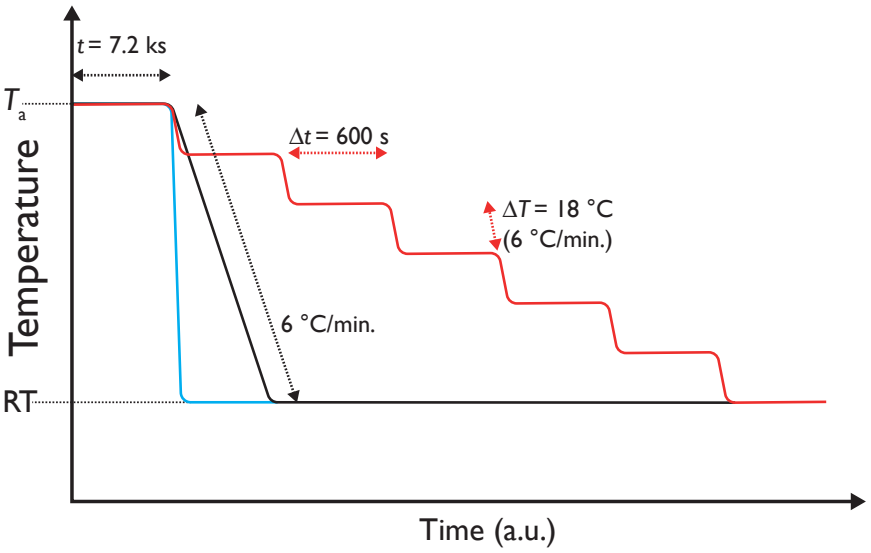

Figure 5.8: Different types of cooling process, quench cooling (blue), slow cooling (black) and stepped cooling (red) from the annealing temperature (T_a) to room temperature (RT).

Similar to Figure 5.10, when $\Delta g_{m,max}$ is plotted as a function of $\Delta I_{d,lin}$, (close) to linear behavior is observed. This suggests that a similar type of defect affects both $g_{m,max}$ (Equation 2.8) and $I_{d,lin}$ (Equation 2.12), possibly degradation of the mobility μ. Note: this thesis does not investigate how the mobility is affected by HCl, so effects like the gate depletion effect of the n^+-polysilicon gate change the effective gate oxide capacitance C_{ox} and have an influence on the mobility [2].

It would be expected that after annealing, all the damage in the device, *i.e.* shifts in parameters, show comparable recovery. However, when the correlation between $g_{m,max}$ and ΔV_t is given in Figure 5.11, the data suggests that this is not the case. It seems that V_t recovers with a higher rate than g_m at the lower anneal temperatures, suggesting that interface/oxide defects and trapped charge recover at different rates. Furthermore, in contrast to Figure 5.10, an S-curve is observed instead of linear behavior. Similar behavior is observed for $I_{d,lin}$ too and for all cooling rates, where a more profound S-curve was observed at a smaller gate length.

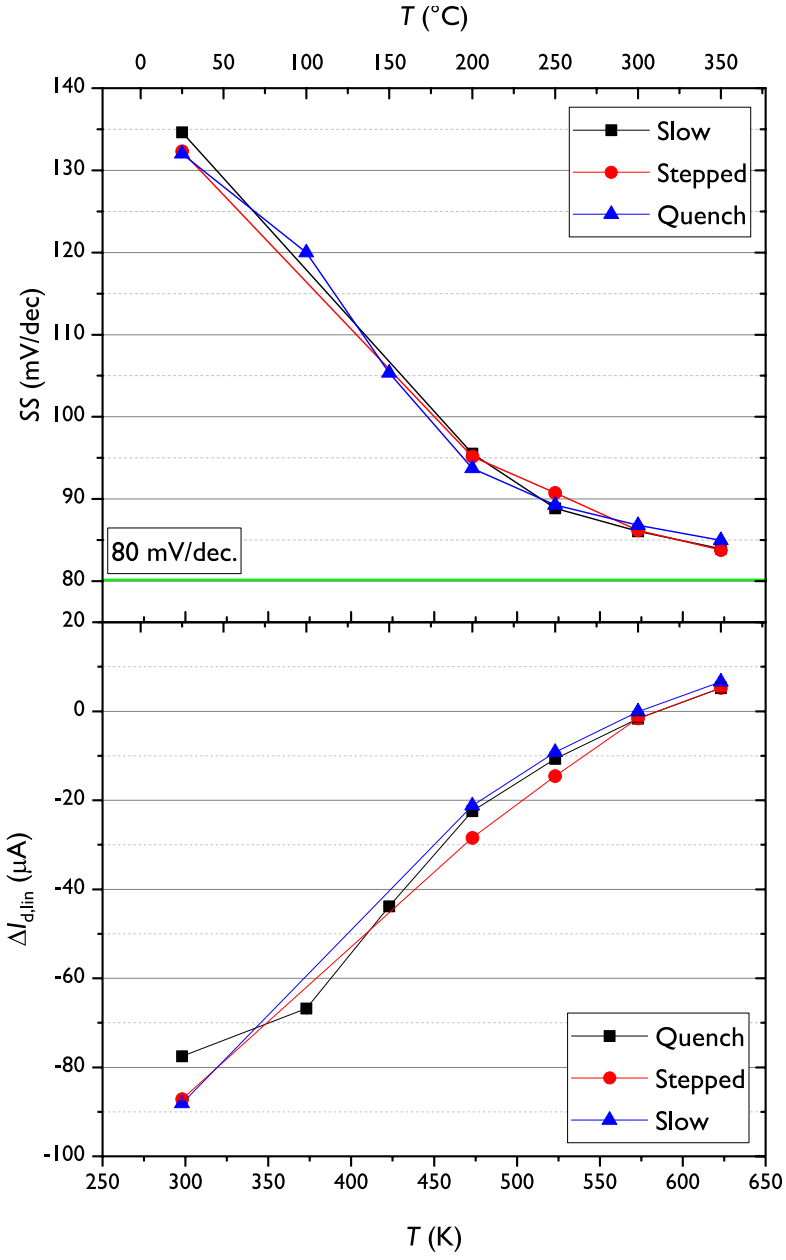

Figure 5.9: Recovery of SS (top) and $\Delta I_{d,lin}$ (bottom) of the devices with W/L = 10.0/0.6 in μm as a function of T_a (t_{ox} = 4.5 nm). The legend indicates the cooling method. Characterization was done at T_m = 25 °C, where SS was determined between V_{gs} = 0.05 V and V_{gs} = 0.45 V and the green line indicates the value of the fresh device ($\sim$ 80 $^{mV}/_{dec}$). $I_{d,lin}$ was determined at V_{gs} = 2 V .

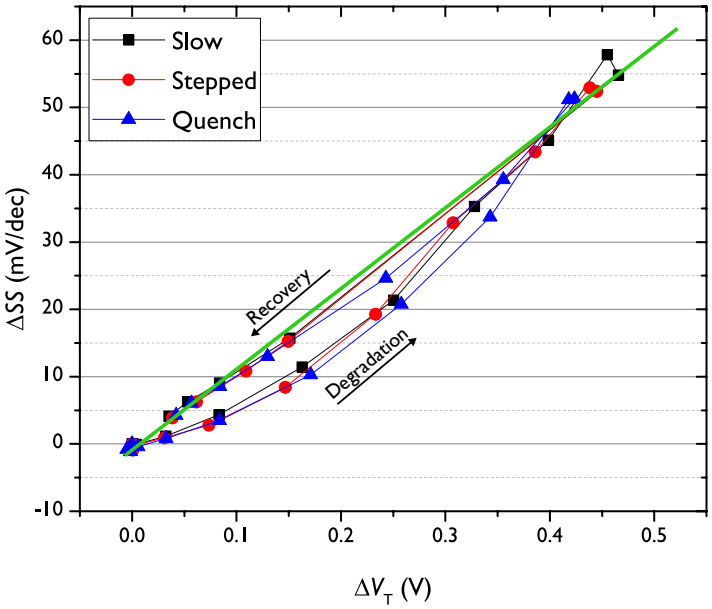

Figure 5.10: Correlation between ΔSS and ΔV_t of the devices with W/L = 10.0/0.6 in µm. The legend indicates the cooling rate. The subthreshold swing was measured between V_{gs} = 0.05 V and V_{gs} = 0.4 V at T_m = 25 °C. The green line is a guide to the eye to indicate a proportional recovery rate for V_t and SS.

5.5 Recovery in various Ambients

In the experiments described above, it was found that the recovery after hot-carrier degradation is not affected by gate length or cooling rate, but that the passivation rate has an anneal time/temperature dependence in line with Stesmans' model (Equation 3.13). The model assumes that the passivation rate depends on the hydrogen concentration at the interface and the forward reaction rate. The forward reaction depends on the given technology and fabrication processes and is assumed to not change significantly during the degradation/recovery process. One might however be able to influence the recovery through the hydrogen concentration in the chip and at the Si/SiO_2-interface itself.

The dielectric always contains some amount of hydrogen due to the various fabrication process that involve hydrogen. Recovery in the section above was achieved without supplying hydrogen externally, presumably assisted by the available hydrogen in the chip itself. It is reported that the vertical diffusion in the dielectric is fast enough that the reaction is not diffusion limited, but reaction limited [43, 200], which suggests that either the maximum solubility is reached in those experiments, or that Equation 3.13 needs to be extended. The impact of hydrogen from an external source (ambient) on the recovery depends among others on the solubility of hydrogen in the gate oxide and the back-end

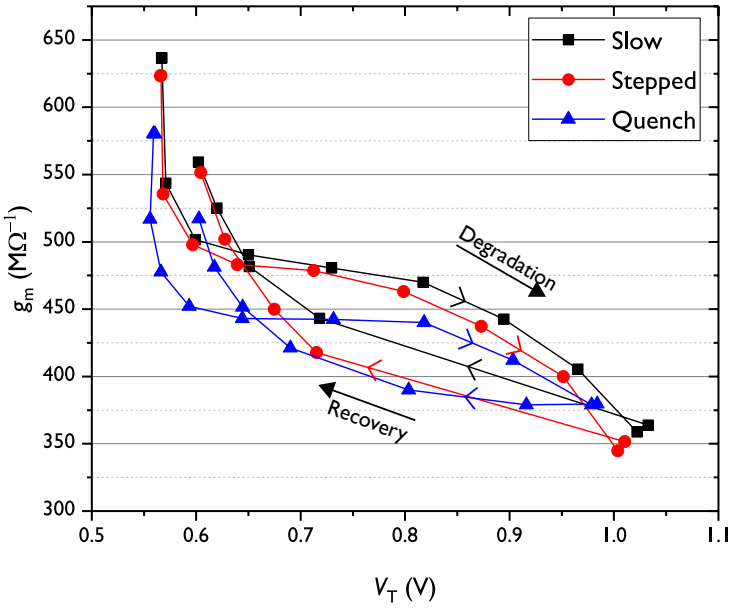

Figure 5.11: Correlation between $g_{m,max}$ and V_t of the devices with W/L = 10.0/0.6 in µm. The legend indicates the cooling rate. The measurement of g_m and V_t were performed at $T_m = 25$ °C.

dielectric, where an external source may ensure a sufficient supply of hydrogen. Stesmans' model raises the question of whether a supply of H_2 from the outside may increase the [H_2] [210] at the interface and accelerate the recovery rate.

Furthermore, Equation 3.13 assumes that only the concentration of *molecular* hydrogen influences the recovery rate. Molecular hydrogen is the most stable hydrogen species, however, radicals (H^0, H^+, H^-, etc.) are more reactive and are also used for passivation. In particular, a hydrogen plasma is often used in silicon solar cell fabrication [45]. The recovery rate can perhaps be improved by introducing more reactive hydrogen radicals in the device [213] (instead of only H_2) to improve the reaction rate with the dangling bonds.

Stesmans' model predicts that (almost) complete recovery is possible, but to achieve this within a short time frame ($t_a < 1$ hour) a temperature of at least $T_a = 400$ °C is needed. At lower temperatures, a longer time is needed to get almost complete recovery ($t_a >$ decades for typical microchip operating temperatures). This section presents the results of recovery experiments on HCI degraded nMOSFETs by annealing in various ambients at a lower temperature and discusses how the recovery time can be decreased [214].

5.5.1 Experimental

In this study, the general effects of hydrogen on the recovery of hot-carrier degraded nMOSFETs from the industry have been studied. All devices are Research&Development samples and are fabricated up to the first metal layer.

Table 5.2: Designed gate width (W), length (L) and oxide thickness (t_{ox}) of the studied nMOSFETs and characterization techniques.

	Technology		
W/L (μm/μm)	*A*	*B*	*C*
10.0/1.0	X	X	X
10.0/0.6		X	X
10.0/0.5	X	X	X
10.0/0.35	X		
10.0/0.25	X	X	
1.0/0.25	X	X	
t_{ox} (nm)	7.0	5.3	4.5
Measurement	IV, CP	IV	IV

Three different technologies (technology A, B and C) from consecutive generations have been investigated. All technologies are bulk-Si-based, have a poly-Si gate and a SiO_2 gate oxide.

Technology A has devices made in two variants: in one variant, hydrogen is used during the passivation step. The other variant uses deuterium in the passivation step [215] (see Chapter 7). Different from the other two, Technology B features a silicon nitride scratch protection layer and gate protection diodes. Technology C has the thinnest gate oxide; it was also used in earlier experiments investigating recovery by annealing in Section 5.4. Table 5.2 specifies the dimensions of the studied devices.

Characterization (CP- and IV-characterization) and degradation were done at $T_m = 25\,^{\circ}C$ in air. The electrical stress consisted of Drain Avalanche Hot-Carrier Injection (DAHC) for $t_s = 300$ s. The applied drain-source voltage depended on the used technology and gate length, L, varying between $V_{ds} = 4.2$ V and $V_{ds} = 4.8$ V. The gate voltage, V_{gs}, was set to maximum bulk current, $|I_{bulk}|$.

Figure 5.12 (top) shows ΔN_{cp} due to different degradation conditions of hydrogen or deuterium passivated devices. In line with the literature, a factor 2-3 difference in degradation can be observed due to the isotope effect [216]. The different ΔN_{cp} values as a function of gate length are not only due to L but also relate to the adapted bias conditions per device, as mentioned earlier.

However, when the *recovery* of a device parameter is plotted after annealing in relative terms, such as shown in the bottom of Figure 5.12, the differences between individual devices are no longer visible. In the experiments, the amount of recovery is always proportional to the amount of damage inflicted earlier; it only depends on the ambient and, in some cases, on the presence of a silicon nitride layer. This also holds for the other monitored transistor parameters. Therefore, the findings are presented in terms of relative recovery in the remainder of this section. This further allows combining data from different channel lengths into a single box plot to indicate the found experimental variations.

Experiments have been performed to investigate the recovery as a function

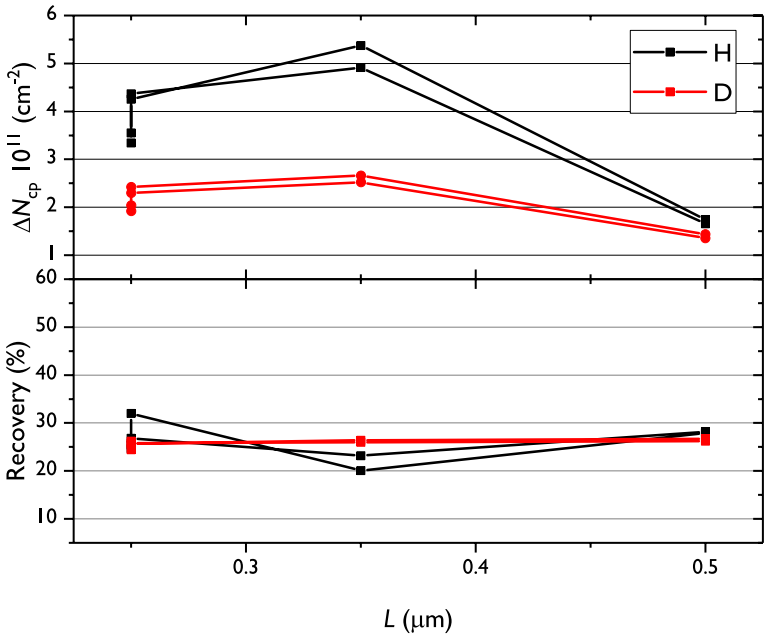

Figure 5.12: The gate length dependence of the degradation ΔN_{cp} of H/D passivated devices (technology A) in absolute values (top) and the recovery after the anneal in an H_2 ambient in relative terms (bottom).

of the gate length and the repassivation of hydrogen versus deuterium passivated devices. The results confirmed earlier results in Section 5.4.3 [206] that gate length has no strong influence on the recovery rate. Also, a similar recovery mechanism plays a role in the recovery of both hydrogen and deuterium passivated devices, which will be further discussed in Chapter 7 [217]. This is explained by the fact that even for deuterium passivated devices, hydrogen is present in the dielectric and may (mainly) contribute to the repassivation step. After many cycles of degradation and recovery, the deuterium passivated devices will become hydrogen passivated (Chapter 7).

5.5.2 Ambients

After the degradation step described in the section above, the device are annealed in various ambients to induce and enhance the recovery rate. Each set of devices was annealed in different ambients at $T_a = 200$ °C for 60 minutes. This anneal time and temperature will correspond to partial recovery, which means that a positive or a negative effect on the recovery rate can be observed from an increased or decreased overall recovery. The temperature ramp (at 10 mbar, $t = 30$ minutes) and cool down (at 1 bar) were done in argon gas, inert to the recovery process.

Some recovery can take place during the temperature ramp, however, it is assumed that most recovery takes place during the one-hour anneal time

at the highest temperature. It is assumed that the presence of Ar or N_2 has no significant influence on the recovery; argon anneals are therefore used as a reference to the other experiments.

The ambients were: Ar; a mixture of Ar and H_2 (partial H_2 pressure of 0.4 mbar); and the same Ar + H_2 mixture and pressure with a remote RF plasma. The minimum power to ignite the plasma was 200 W; the maximum was 2 kW. Furthermore, atomic hydrogen was created by hot-wire thermal cracking of undiluted molecular hydrogen at low-pressure (0.1 mbar) in a dedicated experimental setup [218]. Molecular hydrogen is led along a tungsten filament, which heats up and thermally cracks the hydrogen into atomic hydrogen before reaching the samples. The experimental process is summarized in Figure 5.13.

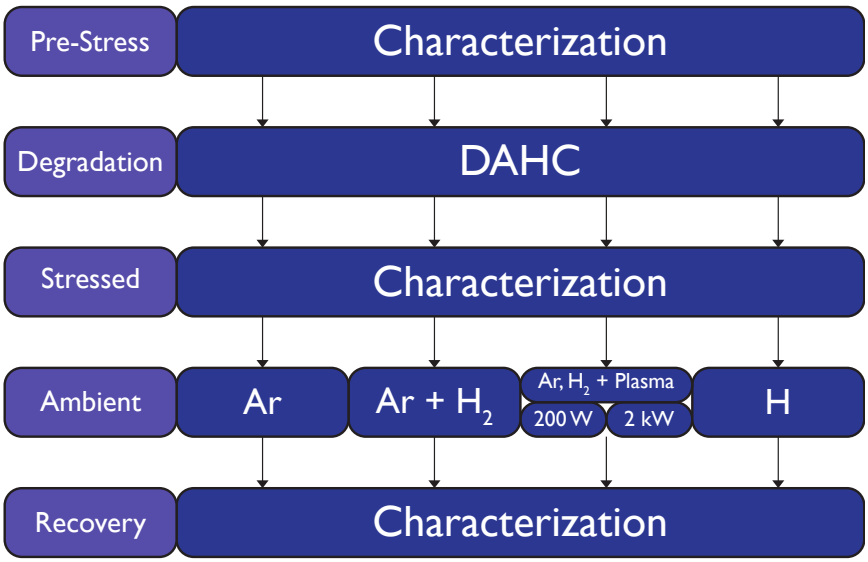

Figure 5.13: Schematic of the experimental process.

5.5.3 Argon (Low Pressure)

Figure 5.14 shows the effect of hot-carrier degradation and annealing in an Ar ambient on the drain current of an exemplary device. Table 5.3 shows the values of the parameters extracted from the IV- and CP-measurements. Degradation and recovery are visible by the significantly shifting curves and parameters (see Table 5.3). Averaged over all devices of different gate lengths and passivation species, a recovery of approximately 23.2% for ΔN_{cp} is achieved by annealing in argon. Furthermore, V_t and SS show similar recovery rates ($\approx$ 40%), as well as $g_{m,max}$ and $I_{d,lin}$ ($\approx$ 10%), which is line with Section 5.4.5. This further suggest that different defects in the device recover at different rates, *e.g.* mobility, interface states, trapped charge etc.

Figure 5.15 shows the I_{cp} of a fresh device, after stress and after the anneal (top figure). The graph shows that after degradation, the I_{cp} per pulse increases,

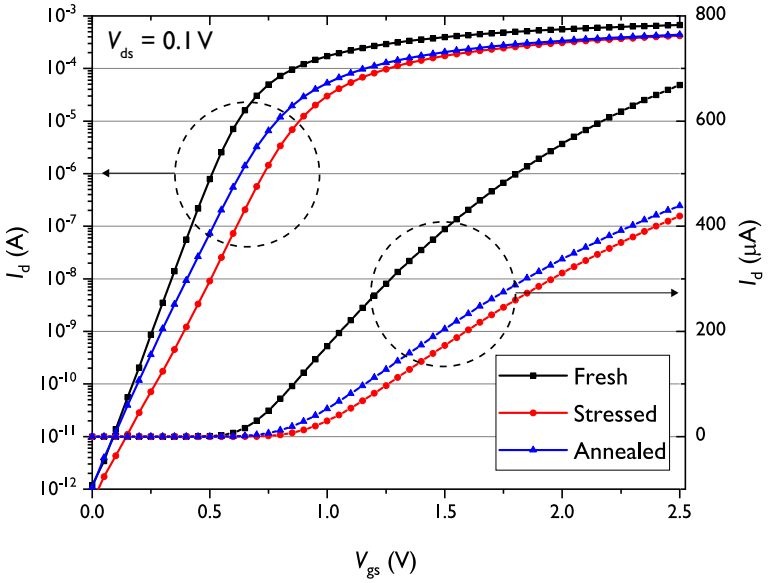

Figure 5.14: Effect of exposing a HCI degraded device to an argon ambient ($L = 0.35$ μm) of technology A ($t_s = 300$ s, $V_{ds} = 4.8$ V, $V_{gs} = 1.7$ V).

indicating that new recombination centers are created. These defects are recovered after the anneal, *i.e.* the I_{cp} per pulse decreases. The bottom figure shows the ΔI_{cp} between the CP-measurement after stress and after the anneal, *i.e.* the figure shows the defects that are recovered by the anneal treatment.

	Fresh	*Stressed*	*Annealed*	*Recovery*
V_t (mV)	669	954	843	38.9%
$g_{m,max}$ (μA/V)	508	336	346	5.8%
$I_{d,lin}$ (μA)	550	334	364	13.9%
SS (mV/dec)	84	116	103	40.6%
N_{cp} (10^{10} cm^{-2})	3.4	60.1	49.7	18.3%

Table 5.3: Parameter values belonging to the IV-curves of Figure 5.14. The CP-measurement has been performed using a frequency of $f_{cp} = 100$ kHz ($L = 0.35$ μm, technology A). The measurements were done at $T_m = 25$ °C.

Charge-pumping can be used to distinguish interface and border traps (Chapter 2. In these experiments no significant difference in I_{cp} is observed when the CP-data measured at a frequency of $f_{cp} = 100$ kHz and $f_{cp} = 3$ MHz are compared. This suggests that mainly interface states are created/repaired in the degradation/recovery step, visualized in Figure 5.16 (after Figure 5.15). The assumption is that the frequency dependence only emerges when more severe damage is inflicted to the device, in order to produce significant amounts of deep oxide traps [23] and that a comparison of relative recovery can be made at the various CP-frequencies, see Chapter 7.

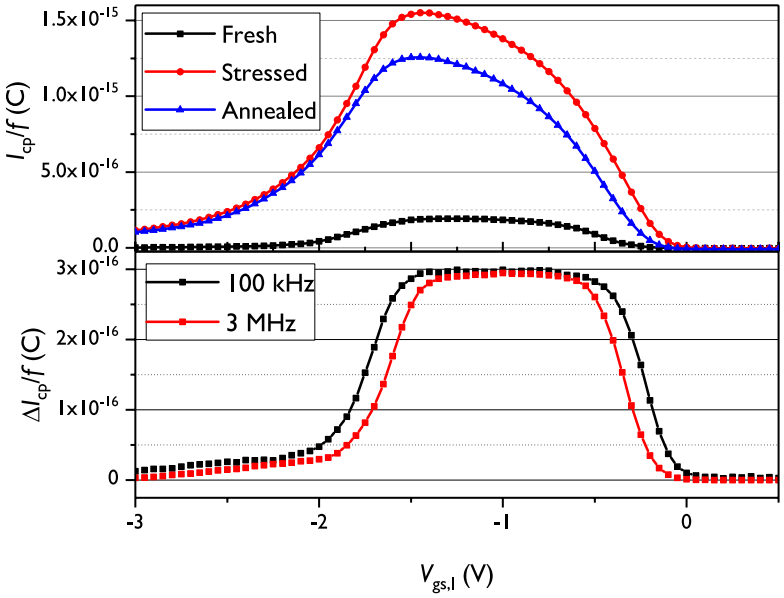

Figure 5.15: Top: The charge per pulse of I_{cp} (f_{cp} = 100 kHz) for a fresh, a stressed and an annealed (in argon) device. Bottom: The ΔI_{cp} per pulse recovered due to the anneal, measured at two frequencies.

5.5.4 Argon + Molecular Hydrogen (Low Pressure)

The effect of externally supplied H_2 on the recovery rate at low concentrations is investigated by comparing the recovery in Ar to recovery in an Ar-H_2 mixture. Figure 5.17 shows the percentage of N_{cp} present after exposure to various ambients. The recovery rates between an Ar and H_2-ambient are similar, but a small hydrogen pressure seems to be beneficial for the recovery rate, even at this low concentration. This finding is in line with Stesmans' model, where the effective hydrogen concentration at the Si/SiO_2-interface is important for the recovery rate and can be tweaked using an external hydrogen supply.

5.5.5 Hydrogen Plasma (Low Pressure)

Radicals are highly reactive, so the recovery of hot-carrier degraded devices using hydrogen radicals may be enhanced compared to recovery in a molecular hydrogen ambient. Hydrogen radicals can be produced in a hydrogen plasma, where the concentration of hydrogen radicals depends on the used RF power. The highest available RF power (2 kW) in the experimental setup should result in the highest concentration of hydrogen radials, however, it also results in plasma-induced degradation (Section 4.6, Figure 4.8).

A plasma power this high is therefore unsuitable to investigate possible beneficial effects of reactive hydrogen species. At the lowest possible RF power of 200 W, PID effects are much reduced and some recovery takes place, see

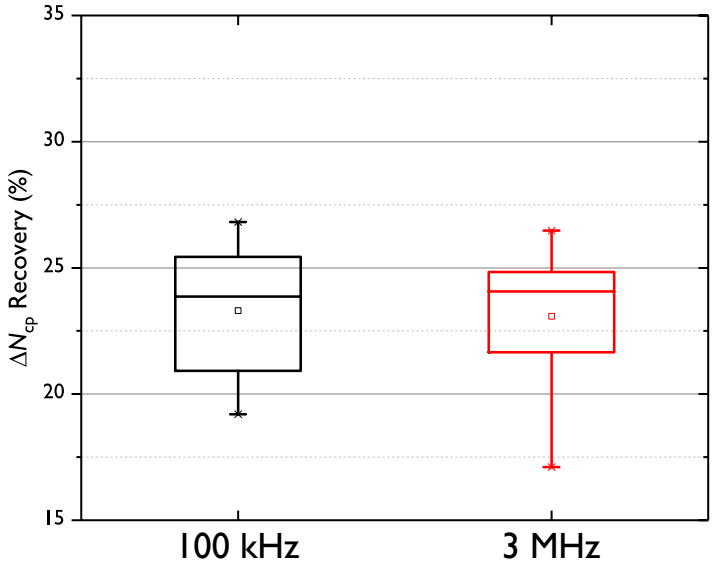

Figure 5.16: Recovery of ΔN_{cp} of devices (technology A) after an Ar-anneal. The CP-measurements are done using a frequency of $f_{cp} = 100$ kHz (black) and $f_{cp} = 3$ MHz at $T_m = 25$ °C. Each data box represents the recovery of all device dimensions (see Table 5.2).

Figure 5.17. However, this recovery is lower than with the HCl degraded devices exposed to the Ar or Ar + H_2 ambient, indicating that recovery and plasma damage occur at the same time. (In the figure, negative recovery indicates a further increase of ΔN_{cp} caused by the plasma treatment.)

The assumption that plasma damage plays a role in these experiments is supported by gate leakage measurements. Figure 5.18 shows the gate current as a function of the gate-source voltage after exposure to different ambients. The gate leakage remains very low on the devices exposed to an Ar or H_2 ambient, suggesting no change in the gate oxide. Exposure to the plasma resulted in an increase in gate current at higher gate bias, and more so when the plasma power is higher. In combination with Figure 5.17, this suggests that any possible positive effects of using radicals on the recovery rate do not outweigh the negative effects of exposure to hydrogen plasma in this experiment.

5.5.6 Atomic Hydrogen (Low Pressure)

To investigate the influence of radicals on the recovery rate and circumvent PID, atomic hydrogen radicals are produced in a different manner. Atomic hydrogen can be produced by thermal cracking instead of creating a plasma. A chip with hot-carrier degraded devices from technology C (Table 5.2) is annealed in an atomic hydrogen ambient and compared to samples annealed in a nitrogen ambient of Section 5.4, for the same temperature and time. A similar recovery

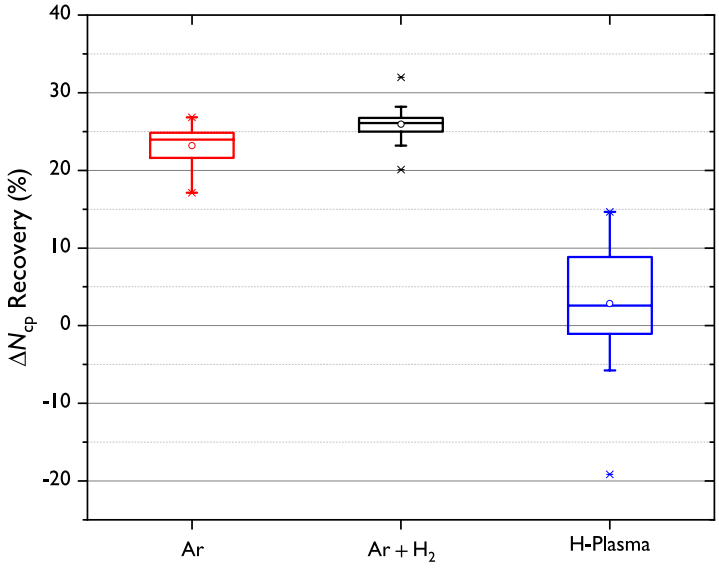

Figure 5.17: Recovery of ΔN_{cp} due to HCI degradation (in % of maximum ΔN_{cp}) after annealing in an argon, hydrogen plus argon or a hydrogen plasma (P_{rf} = 200 W) ambient on devices of technology A. The recovery over all device dimensions are taken into account (see Table 5.2)

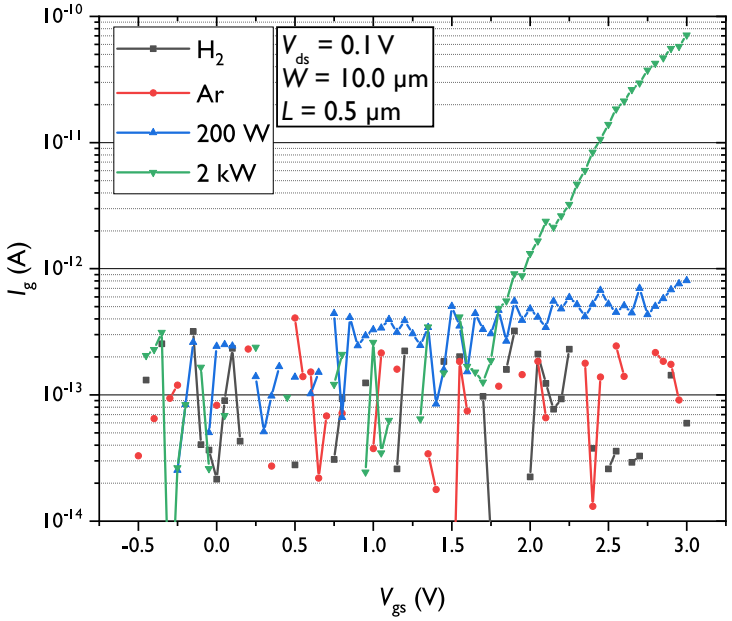

Figure 5.18: Gate current of hydrogen passivated hot-carrier degraded devices (technology A) after the anneal in various ambients.

rate is observed, indicating negligible effects of atomic hydrogen on the recovery process(es).

This suggests that either insufficient atomic hydrogen reaches the Si-SiO_2 interface, or that atomic hydrogen has no (net) passivating effect at this interface. Earlier experiments have shown that the atomic hydrogen in this setup can reach the chip surface [218]. However, atomic hydrogen is highly reactive and it may have reacted inside the back-end of the device, before reaching the Si-SiO_2-interface.

5.5.7 Role of Silicon Nitride Scratch Protection Layer

Recovery of HCD devices by exposure to a hydrogen ambient was further investigated using the devices of Technology A and B, where in line with expectation, PID was prevented by the protection diode. Figure 5.19 shows the recovery of ΔSS of devices with and without the silicon nitride layer in an H_2 ambient and in a low-power hydrogen RF plasma. The data show that the devices without the silicon nitride layer recover more in a hydrogen ambient compared to the devices with the layer. This can be explained by the silicon nitride acting as a diffusion barrier for hydrogen, preventing outside hydrogen to contribute to the recovery step.

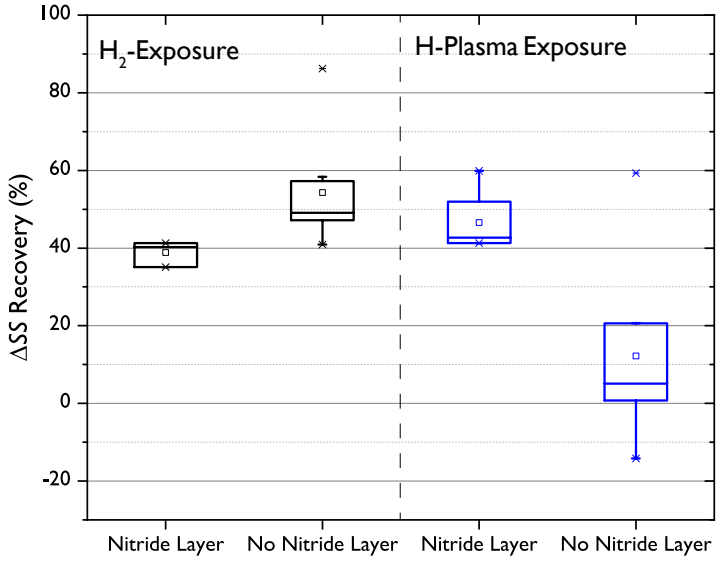

Figure 5.19: Recovery in the shift in SS due to HCD (in % of maximum ΔSS) after exposure to an H_2-ambient (Left) or exposure to a hydrogen plasma (P_{rf} = 200 W) (Right). The devices are from technology A and B.

A silicon nitride layer blocks any ambient hydrogen from entering the chip and similarly locks hydrogen inside the devices. The recovery in a nitride-capped chip can therefore be purely attributed to the hydrogen already present in

the gate stack. Such nitride protection layers are very common in integrated circuit manufacturing and as a consequence one has to rely on an internal hydrogen supply to enhance the recovery rate through an elevated hydrogen concentration [219].

5.5.8 Nitrogen + Molecular Hydrogen (High Pressure)

In the previous sections, the data suggested that externally supplied hydrogen ambient will result in enhanced recovery, even if the (partial) pressure of hydrogen is low. In line with Stesmans' model, it is expected that if more hydrogen can be supplied to the Si/SiO_2-interface even more recovery can be achieved. However, depending on the used technology and fabrication process, the improvement in hydrogen concentration could be constrained by the maximum solubility of hydrogen in the device at a specific temperature (Chapter 3). If more hydrogen can be dissolved in the device, a more pronounced difference in recovery rate due to hydrogen compared to the results of Section 5.5.4 can be observed.

To investigate an improvement in recovery, devices have been degraded by HCl according to Table 5.3 and subsequently annealed in a pure nitrogen ambient ($P_{N_2} = 5.1$ bar, inert to the recovery process) and a ($P_{H_2} = 0.6$ bar, $P_{N_2} = 4.5$ bar) for $t_a = 2$ weeks ($t_a > 10^6$ s), at an elevated temperature $T_a = 100$ °C.

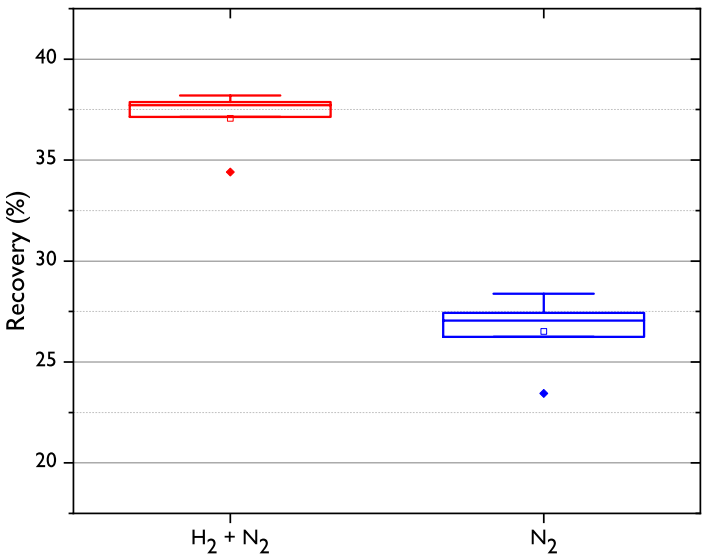

Figure 5.20: Relative recovery ΔN_{cp} of hot-carrier degraded devices after an anneal ($T_a = 100$ °C) at elevated pressures ($P_{total} = 5$ bar). Characterization was done at $T_m = 25$ °C.

Recovery due to the long time anneal is shown in Figure 5.20, where the

amount of recovery indicates how much of the increase in CP-current due to HCl is removed. CP measurements have been performed at $T_m = 25\ ^\circ C$, where 0% indicates that no recovery has taken place. A more pronounced improvement in recovery rate is visible when hydrogen is used compared to the devices exposed to a pure nitrogen ambient, compared to exposure to a low-pressure hydrogen ambient. The concentration of hydrogen in the ambient is much larger ($P_{H_2} = 0.6$ bar versus $P_{H_2} = 0.4$ mbar) and provides more hydrogen in addition of the hydrogen already present in the chip. It is indicative, that the recovery rate is indeed hydrogen concentration-dependent and as high as possible hydrogen concentration is necessary to improve the recovery rate.

5.6 Summary and Conclusion

Devices degraded by hot-carrier injection can recover under the right circumstances. The recovery of the devices seems to follow the passivation model proposed by Stesmans, where the recovery depends on various factors, *i.e.* anneal temperature, anneal time, technology and the availability of the passivation species, hydrogen, for the defects. Due to the various fabrications steps, hydrogen is always present in the gate and recovery can take place when a temperature treatment is applied, however, even at low concentration, externally supplied hydrogen will result in a higher recovery rate at operating temperature. A temperature treatment is shown to be the most effective method to repair device damage within a reasonable time frame, where an anneal temperature of $T_a = 350-400\ ^\circ\mathrm{C}$ is needed to induce total recovery of a hot-carrier degraded device. To reach this temperature periodically, the energy needed makes this temperature too high and energy inefficient to be practical for commercial applications. In addition, this temperature will negatively affect other areas of the chip (solder, packaging). Applying a temperature treatment at a lower temperature will only induce partial recovery of a hot-carrier degraded device, where the usual operating temperature in the order of $T \approx 150\ ^\circ\mathrm{C}$ corresponds to roughly 50 % recovery within a reasonable time frame. To investigate how various methods/material properties can influence the recovery rate in a positive or negative way, various experiments have been conducted. The main findings described in this chapter are:

- The recovery rate could not be enhanced under the experimental conditions in combination with light-soaking.
- The recovery rate could not be enhanced under the experimental conditions by applying a bias.
- Stesmans' model is experimentally tested and seems to model the recovery to a high degree.
- The cooling rate from anneal temperature to measurement temperature does not seem to play a significant role in the recovery rate.
- In line with earlier reports, more recovery takes place at higher temperatures and complete recovery within a reasonable time frame can be used if a temperature of at least $T_a = 400\ ^\circ\mathrm{C}$ is used. Exposure to temperatures in excess of $T_a > 500\ ^\circ\mathrm{C}$ induces permanent, unrecoverable thermal degradation. In addition, out-diffusion of hydrogen may start to take place.
- The geometric dimensions of a device do not seem to have a significant influence on the recovery rate. The distribution of hydrogen in the device was assumed to be uniform under the experimental conditions, regardless of the material/gate dimensions.
- Device parameters recover at different recovery rates, suggesting that more than one type of defect recovers.
- Externally supplied hydrogen seems to enhance the recovery rate, even at low concentrations. More recovery under the same experimental conditions is achieved if hydrogen is supplied from a higher pressure ambient.

• Using hydrogen radicals does not seem to improve the recovery rate. Exposing hot-carrier degraded devices to a hydrogen radical ambient lead to a negligible difference in recovery (atomic hydrogen exposure) or even less recovery, accompanied by new PID damage (hydrogen plasma exposure).
• A silicon nitride scratch protection layer acts as a diffusion barrier preventing hydrogen to enter the device from the outside. Similarly, hydrogen is assumed to be unable to leave the chip if such a diffusion barrier is used.

Combining these findings, the recovery rate of hydrogen-related defects can be improved by increasing the supply of the passivation species. Especially if hydrogen under high pressure is locked inside the device using a diffusion barrier, preventing out-diffusion of hydrogen. These considerations may have a positive influence on the recovery rate of hydrogen-related defects. However, usually other defects than only interface defects are created during the degradation step, *e.g.* charging, oxide traps. In the next chapter, the difference in the recovery rate of different defects is investigated.

CHAPTER 6

Recovery: Fast versus Slow Traps

6.1 Introduction

When an HCI-degraded device was annealed, it resulted in (partial) recovery (Chapter 5), depending on the anneal temperature and the concentration of hydrogen at the Si/SiO_2-interface. This recovery process could be described in terms of the passivation of dangling bonds by hydrogen, where the interface defects were created during the hot-carrier stress phase. This recovery process is commonly described by the passivation model (Equation 3.13) proposed by Stesmans [65], which describes the hot-carrier induced shift in device parameters, *e.g.* V_t, back to its original, pre-stress value, see Chapter 5. However, the hot-carrier induced parameter shift cannot be attributed to only the (de-)passivation of interface defects; the structural change in the gate dielectric and charge (de-)trapping of oxide- or interface-defects also play a role [212, 221], as described in Chapter 3. This makes the proportionality relation between V_t and N_{it} of Equation 2.17 invalid:

$$\Delta N_{it} \not\propto \Delta V_t. \tag{6.1}$$

If Stesmans' model describes the recovery of interface states and thus the recovery of device parameters in terms purely based on hydrogen passivation, the predicted recovery rate will deviate if a significant number of non-hydrogen-related defects are present. The difference in predicted recovery and experimental results will be exacerbated even more if there is a stark difference in recovery mechanism and recovery rate between different types of defects. This chapter will discuss various experiments performed to investigate if the presence of non-hydrogen-related defects at the Si/SiO_2-interface or in the gate oxide may lead to a different recovery rate and to what degree Stesmans' model predictions can deviate from experiments.

Parts of this chapter have appeared in [220]

6.2 Experimental

The devices under study in this chapter are long-channel nMOS devices with a gate width of $W = 10.0$ μm, a gate length of $L = 0.5$ μm and a gate oxide thickness of $t_{ox} = 7.0$ nm of SiO_2. Method **B** of Figure 2.13 was used to distinguish how the type of defect affects the recovery rate of the devices. Hot-carrier injection was used to induce degradation, where the drain-source voltage was kept at $V_{ds} = 4.5$ V and the gate-source voltage at $V_{gs} = 1.9$ V for $t_s = 10$ ks, the condition where $|I_b|$ is maximum for DAHC. BTI was measured on separate devices under similar gate-source bias conditions as for HCI, (drain kept at a floating bias) and a delay of 1 s was used to measure V_t. No long-term BTI contribution to ΔV_t was observed.

6.3 Charge Detrapping

When the recovery of hot-carrier degraded devices is described using Stesmans' hydrogen passivation model, the recovery rate depends strongly on the anneal temperature (T_a), where a higher anneal temperature will result in a higher recovery rate. The stress temperature (T_s) should not affect the recovery rate according to Stesmans' model, only the concentration of interface states, regardless of how they were introduced. When a device is annealed, a temperature step may take place before the recovery starts, *i.e.* the annealing temperature is higher than the stress temperature. Assumed is that negligible recovery takes place at lower temperatures compared to the actual anneal temperature (this of course is only the case when $T_m < T_a$).

To investigate if the recovery rate is affected by a temperature step and not only the anneal temperature, three sets of devices were stressed and recovered at two temperatures. One temperature was at room temperature as a reference and the other at a temperature that the thermochuck could reach within a reasonable time, see Section 2.4. Two sets had an identical temperature during stress and recovery: $T_s = T_a = 25$ °C and $T_s = T_a = 85$ °C. One set had a temperature step, $T_s = 25$ °C and $T_a = 85$ °C. It was assumed that a negative temperature step ($T_s > T_a$) would not result in relevant data, since most recovery would take place shortly after a stress phase ends.

Figure 6.1 shows the recovery of the hot-carrier induced shift in threshold voltage (ΔV_t) as a function of anneal time (t_a), corrected for the healing delay effect of Figure 2.15 (Section 2.4.2) by subtracting the delay in threshold voltage shift. The shift in V_t is calculated with respect to the first measurement after stress when the anneal/recovery temperature is reached. The devices that were stressed and annealed/recovered at the same temperature (denoted with squares and circles) show a small recovery as a function of recovery time, however, increasing the temperature after stress (temperature step) will increase the recovery rate of V_t, even after a correction due to a difference in HCI induced degradation (due to temperature dependence of HCD), suggesting that a higher recovery rate is present.

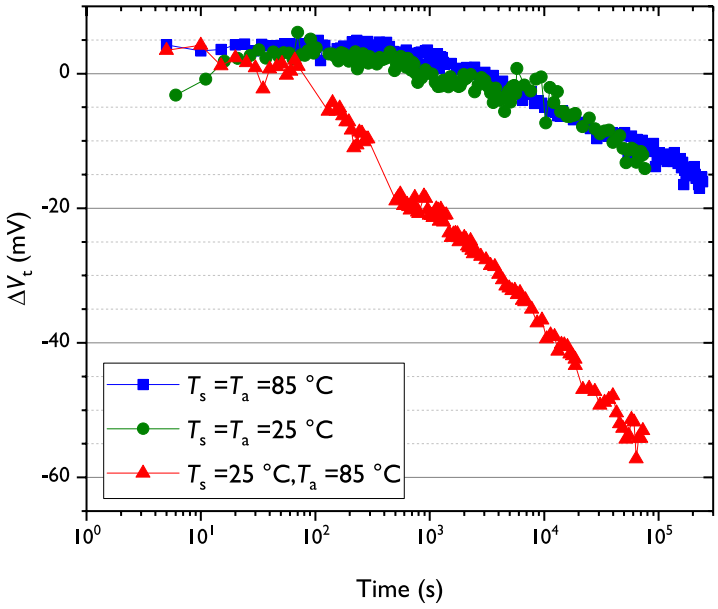

Figure 6.1: The shift in V_t as a function of anneal/recovery time with respect to the first measured V_t after stress at T_a. The red triangles denote a temperature step between the stress and recovery phase, the green circles and the blue squares denote devices where the stress and recovery temperature was the same.

Similar behavior may be observed in BTI degraded devices. It is reported that devices degraded due to BTI can significantly recover at lower temperatures compared to devices degraded by hot-carrier injection [136, 222]. This recovery at a lower temperature can be attributed to recovery mechanisms like discharging of oxide traps ($E_a \approx 0.2$ eV) [136, 223] and to a lesser degree to the repassivation of interface traps. This recovery behavior is described by a permanent (P) and a recoverable part (R), where it is assumed that the discharging of oxide defects plays a major role for the time-dependent recoverable part [133, 224]. Similar to the passivation mechanism described by Stesmans, the time constants for detrapping from the defects are temperature-dependent via an Arrhenius dependency [156, 224]:

$$\tau(\Delta E_B, T) = \tau_0 \exp\left(\frac{\Delta E_b}{k_b T}\right), \tag{6.2}$$

where k_b is the Boltzmann constant and ΔE_b is the tunneling barrier. This results in a recovery behavior that seems to be linear on $\log(t)$-scale of interest and can be described by an empirically found, universal relaxation equation (Equation 6.3) [136, 147, 156, 225]:

$$\Delta V_t(t) = P + \frac{R_0}{(1 + B\xi(t)^\beta)}, \tag{6.3}$$

where the parameters B and β are fitting parameters and ξ is the ratio between stress and recovery time: $\xi = \frac{t_a}{t_s}$. The recoverable component depends on the total amount of introduced defects (R_0) that can recover as a function of recovery time and temperature. The permanent component P does not significantly change during the recovery time (within the experimental time window), however, it is reported that complete recovery of BTI degraded devices can take place after an anneal of sufficient temperature. It will recover, but with a much smaller recovery rate than the recoverable component or that a higher anneal temperature is necessary to induce recovery of this component [154, 226, 227].

It was observed that when a temperature increase takes place during the recovery step, the recovery rate first accelerates until a new $\log(t_a)$-dependent recovery rate is reached [222, 224]. Temperature-dependent discharging of oxide defects (Equation 6.2) [224, 228--230] could play a role in the recovery of hot-carrier degraded devices as well [231].

Figure 6.2 shows the shift in the interface defect density (ΔN_{it}) measured with the CP-measurements (Section 2.2) as a function of the shift in the threshold voltage after degradation (squares) and after the subsequent anneal (triangles) at two different temperatures. The black diagonal lines denote proportionality between V_t and N_{it}. When there is a significant amount of trapped charge and oxide traps present and ΔV_t is not proportional to ΔN_{it} at both temperatures, Equation 6.1 becomes more clear.

The fact that ΔV_t is not proportional to ΔSS, is in line with the V_t measurements when they are done before and after the CP-measurement: a small, but reproducible decrease is observed ($\Delta V_t = 3$ mV). The difference may be explained by charge detrapping by the applied voltage pulse on the gate during the CP-measurement.

Recovery of ΔV_t after HCD was observed at lower temperatures before, however, besides interface trap recovery, detrapping may have been involved here as well [232--235].

To differentiate between recovery due to discharging and repassivation of interface defects, charge-pumping characterization has been done, see Chapter 2.2. The recovery of the charge per cycle (I_{cp}/f_{cp}) as a function of anneal/recovery time, measured under similar conditions as the data for Figure 6.1, is shown in Figure 6.3 ($T_a = 85$ °C, $f_{cp} = 100$ kHz). Here the value 0 at $t_a \approx 100$ s indicates that no recovery has yet taken place.

The red curve is from a device degraded at $T_s = 25$ °C, after which a temperature step took place to the anneal temperature and the blue curve is of a device degraded at $T_s = 85$ °C. In contrast to Figure 6.1, the recovery rate did not show an enhancement in recovery rate after the temperature step, indicating that a temperature step does not affect the recovery rate of interface states. This means that the interface state recovery rate is only affected by the anneal temperature and not by the HCI stress temperature, again in line with Stesmans' passivation model.

Applying a temperature treatment to HCD devices will not only recover P_b-

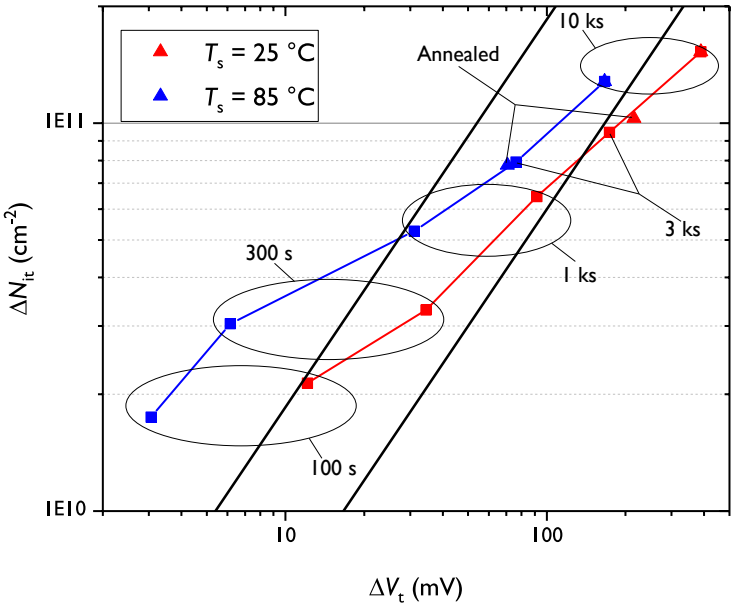

Figure 6.2: The shift in N_{it} and V_t at various cumulative degradation times and after annealing. The blue curve indicates a sample where $T_s = T_a = 85$ °C. All measurements for the red curve were done at $T_m = 85$ °C. The red curve indicates a sample where $T_s = 25$ °C and $T_a = 85$ °C. All measurements for the blue curve have been done at $T_m = 25$ °C.

centers, but detrapping and recovery of border/oxide traps may also take place. This leads to threshold voltage recovery being affected by charge detrapping (Figure 6.1). Recovery of the CP-current results in a recovery rate more in line with Stesmans' model (Figure 6.3). However, when the CP-current is used to determine the density of traps, it will make use of all defects that can act as a recombination center, not only the hydrogen-related interface states. Furthermore, after stress and during annealing oxide defects can be transformed into interface defects [236], clouding the exact recovery mechanism that takes place. In the next section, the experiments to distinguish the recovery of non-hydrogen-related oxide traps and the hydrogen-related interface states will be discussed, and how both may affect the total recovery rate.

6.4 Differentiating between Interface and Oxide Trap Recovery

In order to quantify the recovery rate of the (fast) hydrogen-related interface defects and the (slow) oxygen-related border defects, it is necessary to distinguish both types of traps during characterization. The charge-pumping method takes the deeper and slower traps into account at lower CP-frequencies due to the longer time constant for emission of deeper traps [198], whereas only the

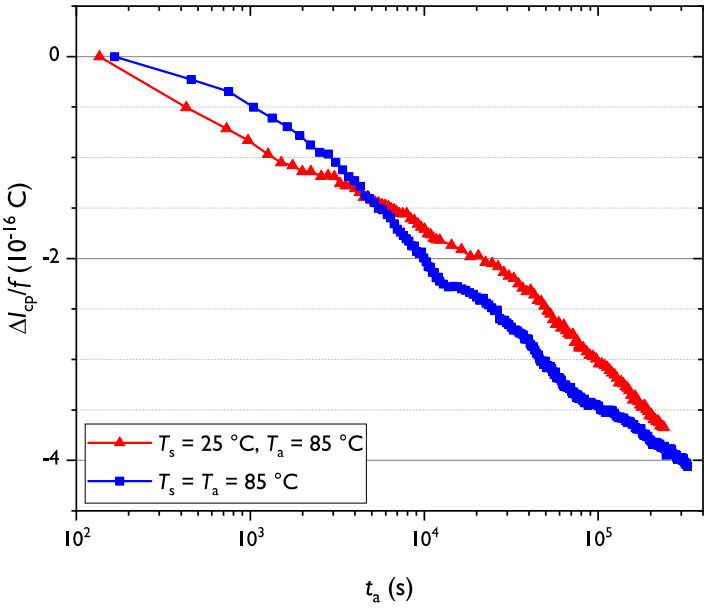

Figure 6.3: Recovery of the charge per cycle at $f_{cp} = 100$ kHz as a function of anneal time. Red: recovery of a device, where $T_s = 25$ °C, $T_a = 85$ °C. Blue: recovery of a device, where $T_s = T_a = 85$ °C.

fast (interface) traps are taken into account at the higher CP-frequencies. The difference in CP-current at a low or high CP-frequency (f_{cp}) is used to get a better understanding of the recovery behavior of both types of defects (Section 2.2.3) and how they work in parallel.

Figure 6.4 compares the CP-current per cycle correlated to the ΔV_t due to degradation for all CP-frequencies. If only the introduction of new interface traps contributes to the shift in threshold voltage, the proportionality ratio $\Delta V_t \propto \Delta N_{it}$ should be observed for all frequencies. The data shows that ΔV_t is correlated with the charge per cycle, $\frac{\Delta I_{cp}}{f_{cp}}$, but that there is a frequency dependency. Overall, the relative increase is bigger in ΔV_t than for ΔN_{it}, or: it does not affect ΔN_{it} in the same way as it affects ΔV_t, possibly fixed charge or oxide traps. The slope is $3.8 \cdot 10^{11}$ cm^{-2}/V for $f_{cp} = 10$ kHz and $2.8 \cdot 10^{11}$ cm^{-2}/V for f_{cp} =1 MHz at $T_m = 25$ °C, suggesting that at lower frequencies a combination of traps (ΔN_{it} and ΔN_{ot}) is measured, again in line with Equation 2.26 and Equation 6.1. Note that discharging may also play a role, see the previous section.

The shift in charge per cycle with respect to a fresh, undegraded device for all frequencies after stress ($t_s = 1$ ks, $t_s = 10$ ks, $T_s = 25$ °C) and after anneal ($T_a = 85$ °C) is shown in Figure 6.5, where all CP-measurements were done at $T_m = 25$ °C. After $t_s = 1$ ks of hot-carrier induced stress, a similar increase in $\Delta I_{cp}/f_{cp}$ can be observed for all frequencies (the 1 ks stress line is horizontal). This indicates that in this time frame mainly new fast traps are

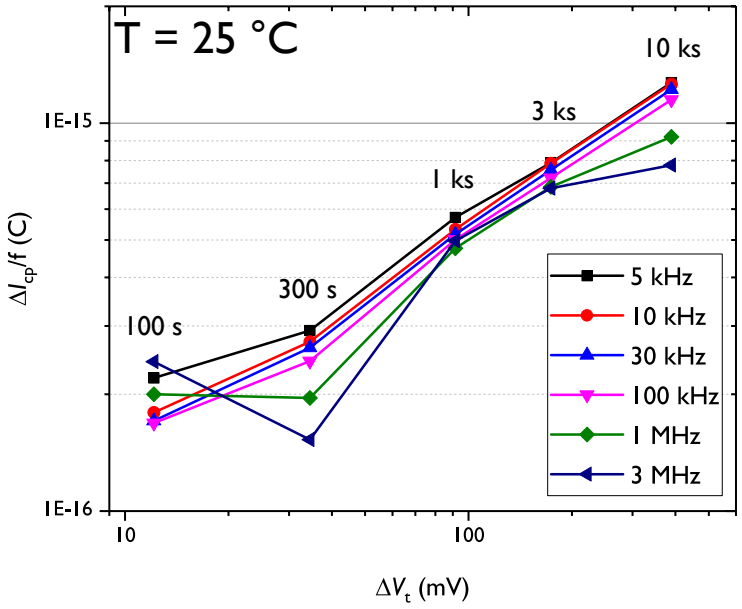

Figure 6.4: Progress of ΔI_{cp} per cycle as a function of ΔV_t during degradation. The time near the data points indicate the cumulative stress time.

introduced presumably interface traps.

When the same device is stressed for 9 ks more, t_s =10 ks of cumulative hot-carrier stress, the CP-current per cycle increases over all frequencies. The increase is more significant at the lower CP-frequencies, *e.g.* f_{cp} = 10 kHz, compared to the higher CP-frequencies, *e.g.* f_{cp} = 3 MHz (the 10 ks stress line is curved). This suggests that a combination of both fast, interface traps and slower, oxide are present, after the 10 ks of stress. Initially mainly interface traps are introduced after a hot-carrier induced stress phase and after the concentration of available Si-H bonds to break drops also deeper (oxide) traps are created.

The charge per cycle measured after the anneal step (after cooling down to the measurement temperature) shows a decrease, indicating that recovery of traps introduced during the stress phase has taken place. The recovery step resulted in a roughly equal decrease of $\Delta I_{cp}/f_{cp}$ for all frequencies (the line keeps a similar 'curve'), suggesting that mainly traps that can be measured at all frequencies, *i.e.* N_{it}, are removed. The passivation of these interface traps can be described by Stesmans' passivation model (Chapter 5). However, this device has a combination of interface and oxide traps, making the percentage of recovery of the number of recombination centers N_{rc} frequency depended: at f_{cp} = 10 kHz roughly 33% of the created ΔI_{cp} is removed due to the anneal step and roughly 50% of the created recombination centers when ΔI_{cp} is measured at f_{cp} = 3 MHz.

The difference in absolute recovery is also visible in Figure 6.6, where the

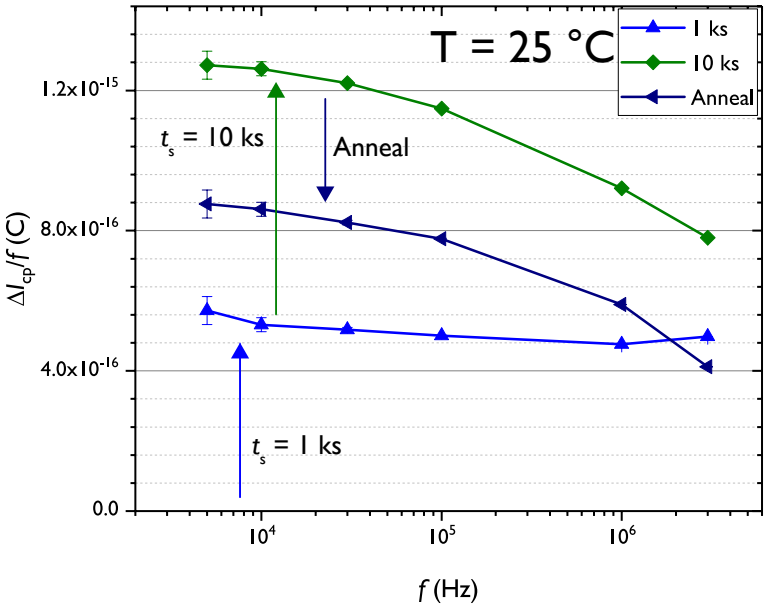

Figure 6.5: The change in CP-current per pulse as a function of the CP-frequency after electrical stress and after annealing in air ($T_a = 85$ °C). The measurement was always performed at $T_m = 25$ °C. The arrows indicate how the CP-current per cycle progresses after stress and after annealing.

recovery of the shift in charge per pulse is set as a function of anneal time ($T_a = 85$ °C) for all frequencies. The recovery shows a log-like recovery behavior for all frequencies and the recovery rate seems to follow the same absolute recovery rate, regardless of the used CP-frequency and hence the measured concentration of recombination centers. Since the absolute recovery rate seems to be similar for all frequencies, regardless of the used CP-frequency, Figure 6.6 suggests that mainly one recovery mechanism dominates the recovery process at this anneal temperature, presumably the passivation of the fast interface states.

Since Stesmans' model only assumes the recovery of interface states due to hydrogen passivation and describes the ratio between unpassivated and passivated defects (Equation 3.13), an underestimation of the recovery rate is made if the deeper defects aren't taken into account (the 30% versus 50% recovery of Figure 6.5).

The data of Figure 6.6 suggests that the recovery of I_{cp} has a recoverable and a permanent component, similar to the universal relaxation equation. Although Equation 6.3 is generally used to describe recovery after BTI, it can also be used as a fitting function to distinguish a permanent and recoverable component of recovery after HCD. Applying the universal relaxation rate to the data of the CP-measurements, it results in the fitted lines of Figure 6.6. Note that although the universal relaxation curve does not give any information

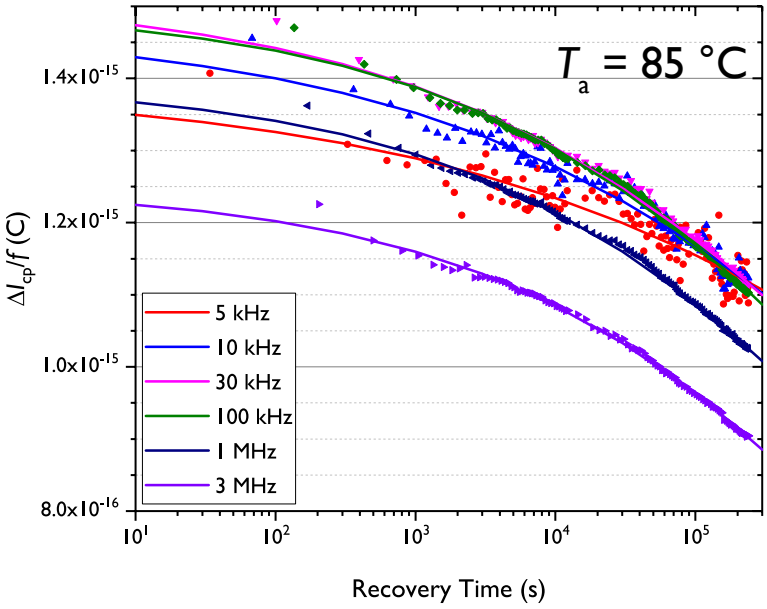

Figure 6.6: Recovery of I_{cp} per cycle as a function of the anneal/recovery time at different frequencies. The lines indicate the fit of the data according to Equation 6.3.

on the physical recovery mechanism, it can be used to fit and compare the recovery data at different frequencies.

The fitting parameter β of Equation 6.3 used for the fit of Figure 6.6 shows a small increase for higher frequencies when fitted with the least-squares method, which is shown in Figure 6.7. This may be explained by a small recovery rate for oxide traps [237].

As mentioned in Section 2.2, the CP-current can be used to calculate the density of recombination centers, where they depend on low CP-frequency (LF) and high CP-frequency (HF) by:

$$\begin{aligned} \text{LF} : N_{\text{cp,LF}}(t_a) &= N_{\text{it}}(t_a) + N_{\text{ot}}(t_a); \\ &= N_{\text{it},0} + \Delta N_{\text{it}}(t_a) + N_{\text{ot},0} + \Delta N_{\text{ot}}(t_a); \end{aligned} \tag{6.4}$$

$$\begin{aligned} \text{HF} : N_{\text{cp,HF}}(t_a) &= N_{\text{it}}(t_a); \\ &= N_{\text{it},0} + \Delta N_{\text{it}}(t_a). \end{aligned} \tag{6.5}$$

Using Equation 6.4, Equation 6.5, the data in Figure 6.6 and the data fit, acquired using the universal relaxation curve, the recovery of N_{it} and N_{ot} as a function of anneal time is plotted in Figure 6.8. Here is assumed that at the highest frequency ($f_{\text{cp}} = 3$ MHz), mainly N_{it} contributes to the CP-current and contributions due to N_{ot} can be neglected.

Figure 6.8 suggests that the oxide traps (blue line) have a slow recovery rate, which is in line with Figure 6.7. The difference in recovery rate with respect to the maximum I_{cp} between N_{it} and N_{ot} is shown in Figure 6.9, where no

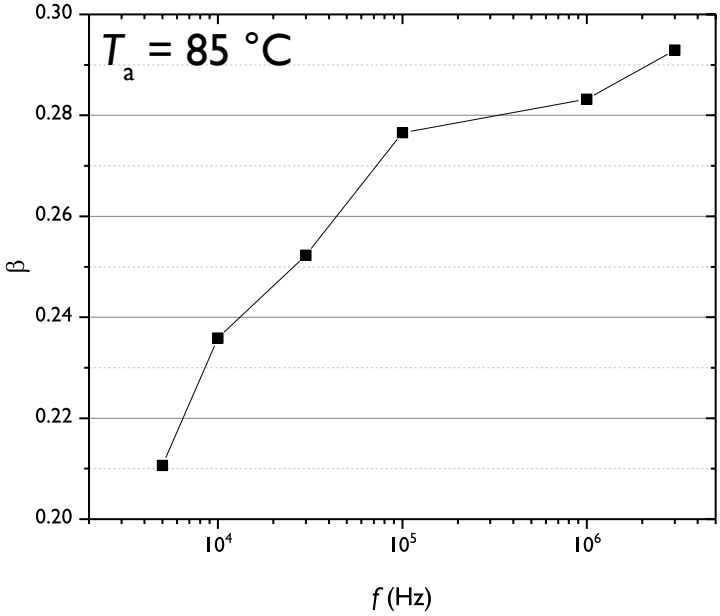

Figure 6.7: Fitting parameter β of Equation 6.3 as a function of the CP-frequency.

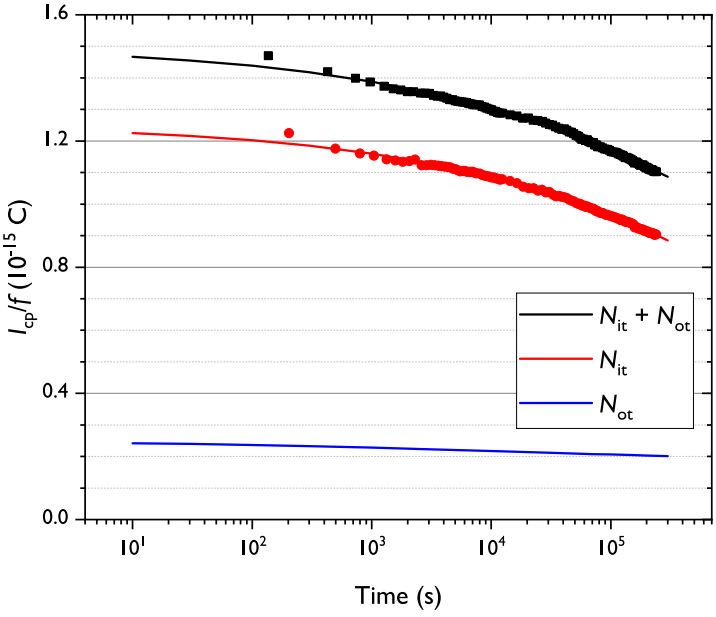

Figure 6.8: Total I_{cp} per cycle attributed to N_{it} ($f_{cp} = 3$ MHz) and the combination of N_{it} and N_{ot} ($f_{cp} = 100$ kHz). The difference between the two fitted lines (fitted using Equation 6.3) is used to calculate N_{ot} recovery.

recovery is denoted by 0. The defects attributed to N_{ot} do recover, albeit slower than the defects attributed to N_{it} (≈ 7 times slower after $3 \cdot 10^5$ seconds

of annealing according to Figure 6.9).

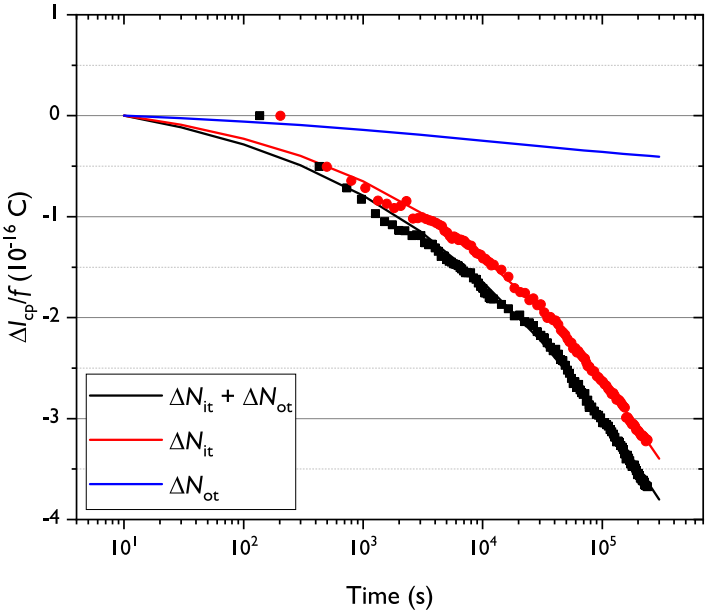

Figure 6.9: Recovery of I_{cp} per cycle at $T_a = 85$ °C attributed to the recovery of ΔN_{it} ($f_{cp} = 3$ MHz) and the combination of ΔN_{it} and ΔN_{ot} ($f_{cp} = 100$ kHz).

The data fit of Figure 6.7 is used to make an interpolation of the data points at different frequencies to create Figure 6.9. However, some considerations to be taken into account are that the data of Figure 6.9 is acquired with the assumption that at $f_{cp} = 3$ MHz, oxide traps do not contribute significantly to the charge pumping current. Furthermore, the universal relaxation curve results in a relatively good fit of the data, but the equation assumes the presence of a permanent and recoverable part and is originally not intended to model interface and oxide trap recovery. Furthermore, the permanent part is only semi-permanent, *i.e.* oxide trap recovery does take place but significantly less than interface trap recovery, which may affect the fit of the reversible part in Equation 6.3.

The experiments discussed in this section suggest that the methods to affect the recovery rate (Chapter 5), affect the recovery mechanism that has the highest recovery rate (and thus has the biggest influence on the healing of the device) at operating temperatures of commercially available chips. As a side note: oxide trap recovery may be affected when other treatments are used, *e.g.* an anneal in an oxygen ambient.

6.5 Summary and Conclusion

In this chapter, the recovery of hot-carrier degraded nMOS by annealing and the role of different types of defects play have been investigated. Hot-carrier injection will lead to the introduction of hydrogen-related interface states, resulting in a shift in electrical parameters. The previous chapter showed that the recovery of hydrogen-related defects can be described by the passivation model of Stesmans. In addition to hydrogen-related defects, charge (de-)trapping and the introduction/recovery of oxide traps play a role in the lifetime of devices and the stress induced parameter shift. This may lead to different recovery rates for, among others, ΔV_t, where also factors such as the stress temperature need to be taken into account. If the amount of non-hydrogen-related defects in the device is significant enough, the model that describes the recovery in terms of hydrogen passivation will deviate more and more from experimental results. In summary, the effect of different recovery rates of different defects on the parameter shift recovery is investigated. The main findings described in this chapter are:

- Hot-carrier degradation leads to various types of defects, *i.e.* trapped charge, oxide-related border traps and hydrogen-related interface traps, depending on the stress conditions.
- Hydrogen-related interface defects are introduced early in the stress phase, oxygen-related border traps will be introduced later in the stress phase.
- A temperature step between degradation and recovery results in more (relative) recovery of the threshold voltage, compared to degradation and recovery at the same temperature. Presumably, a temperature step enhances charge detrapping. This increase in recovery was not observed when the interface defect density was measured.
- Charge-pumping measurements suggest that both interface and border traps recover at a temperature where partial recovery takes place.
- The recovery data indicates that interface states recover faster than border traps at $T_a = 85$ °C, suggesting that hydrogen has a more significant influence on the recovery rate.

Combining these findings, the conclusion can be made that due to the various recovery mechanisms with different recovery rates, Stesmans' model needs to be extended to describe the recovery of parameter shifts after hot-carrier injection accurately if a significant amount of non-hydrogenated defects are present. Interface defects seem to recover faster than oxide-related defects and interface defects are also the first to be introduced in a device after hot-carrier stressing. This suggests that to make a device that has significant recovery under normal operating conditions, it is important to minimize the formation (and impact) of the oxide defects, as they may recover slower. In the next chapter, various ways to minimize defect creation in the degradation step and how it may benefit the total lifetime of a device will be discussed.

CHAPTER 7

Influence of the Stress Phase on the Stress/Recovery Cycles

7.1 Introduction

In the previous chapters, the recovery of hot-carrier degraded devices has been discussed, where various treatments during the recovery step may enhance the recovery rate, *e.g.* introducing a passivation material externally. However, under normal operation conditions, for instance, a chip in a laptop, it is not possible to supply (re-)passivation material from the outside (using an ambient). Then the amount of recovery that takes place purely depends on the materials already present in the device. When out-diffusion of the passivation material takes place (and hence lowers the concentration of the passivation material) or when only partial recovery can be induced, the device does not return to its prestress characteristics. Although significant recovery may be induced and a significant extension of the lifetime may be achieved, the stress and fabrication process still have a deciding influence on the total lifetime, albeit in combination with the recovery process.

To extend the lifetime of a device as much as possible, various methods have been proposed in the past to enhance the resistance to degradation. This leads to an increase in the time needed until a first recovery step needs to be performed. For instance, instead of using hydrogen as a passivation species, halogens can be used during the fabrication process to passivate the dangling bonds at the Si/SiO_2-interface, *e.g.* fluorine [238]. These types of devices are shown to have a higher resistance to HCI-induced degradation, however, it is reported that it will result in a higher susceptibility to other degradation mechanisms, *e.g.* TDDB [239]. Although not part of the research in this thesis, enhancing the lifetime of devices using halogens as a passivation material may result in interesting trade-offs of various degradation mechanisms in the future,

Parts of this chapter have appeared in [MJdeJ:217]

possibly in combination with the recovery mechanisms of different types of defects.

Another way of enhancing the lifetime of silicon-based devices, is passivating the dangling bonds at the Si/SiO_2-interface using the heavier isotope of hydrogen: deuterium. Research done by Hess and Lyding showed that D-passivated devices show a higher resistance to electrical degradation compared to H-passivated devices, known as the (Giant) Isotope effect [216]. Although earlier research had a focus on the influence of deuterium passivation on degradation by hot-carriers, it is unclear how D-passivated devices are affected by a recovery (*e.g.* anneal) step and how deuterium affects the cumulative lifetime of a device if multiple cycles of degradation and recovery are taken into account.

The frequency of degradation/recovery cycles and stress time per cycle itself may influence the total cumulative lifetime of a device. During degradation different types of defects are created at different moments of the degradation phase. Experiments from Chapter 6 suggest that initially mainly interface states are introduced during the HCI stress phase. At longer stress times, the newly introduced defects will be a combination of oxide and interface defects. The different types of defect may recover at a different recovery rate, *e.g.* the recovery rate of interface defects was found to be higher than the recovery rate of oxide defects. When these two characteristics are combined, the stress phase may be reduced to make sure the recovery step is initiated before the permanent, difficult to recover defects are introduced. During the next stress phase, the recovered defects may break again and recover during the recovery step. Over multiple cycles of degradation/recovery mainly one type of defect is created and recovered. Although the number of recovery steps would increase, adjusting the stress time may lead to a beneficial effect on the cumulative total lifetime of a device.

In this chapter, experiments investigating if the fabrication process (isotope effect) or multicyclic degradation/recovery behavior on the lifetime of MOSFET devices will be discussed and how it may affect the total, cumulative lifetime of a device.

7.2 Isotope Effect - Degradation

Deuterium passivation is done during the fabrication process, where it is necessary that the deuterium is incorporated at the end of the various fabrication processes [110, 216, 240]. If it is incorporated at an earlier stage, it may desorb from the interface due to a high temperature anneal and be replaced by the last supplied passivation species, *i.e.* hydrogen, in the last anneal step, the PMA step [241--244]. This is usually done in a high pressure forming gas anneal, where a combination of D_2 and N_2 is used to introduce the deuterium atoms to passivate the dangling bonds.

The isotope effect was initially explained in terms of the weight difference between hydrogen and deuterium (almost twice the mass), which may affect various mass-dependent factors [245], *e.g.* diffusion rate [246] or the acceleration

to an anti-bonding state [247]. Since for both hydrogenated and deuterated devices hot-carrier degradation takes place via a multi vibrational excitation model, modeled after a truncated harmonic oscillator (Figure 4.4, Section 4.2.2), it was proposed that the difference in degradation could be explained by phonon coupling between the passivated bonds and the silicon bulk. It was pointed out by Van de Walle and Jackson [248] that the vibrational frequency of the bending mode for hydrogen passivated P_b-centers is around 650 cm^{-1}, whereas the vibrational frequency of deuterium passivated P_b-centers is around 460 cm^{-1}, close to the frequency of the bulk transverse optical (TO) phonon states ($\sim$ 463 cm^{-1}). Since the frequencies are close to each other, coupling of the bending mode of the deuterium passivated bonds may take place to the phonons in the Si bulk [249], which may lead to de-excitation/pathway for dissociation of charge carriers in the truncated harmonic oscillator model, whereas silicon-hydrogen bonds are less likely to lose energy in this manner. Since the bond rarely breaks after one collision and needs multiple charge carriers to break in combination with Si-D bonds to be more likely to relax and lose energy, deuterium passivated devices are more resistant to electrical degradation than hydrogen passivated devices.

Figure 7.1 shows the effect of deuterium passivation (red) compared to a device with hydrogen passivation (blue). The threshold voltage is plotted as a function of the cumulative stress time at $T_m = T_s = 25$ °C for both devices, where a total stress time of $t_s = 10^4$ s at a drain-source voltage of $V_{ds} = 4.5$ V and a gate-source voltage at $V_{gs} = 2.1$ V is used, the bias conditions where maximum degradation due to DAHC takes place ($|I_{b,max}|$).

The devices (long channel nMOS) under study in this section had a gate width of $W_g = 10.0$ µm, a gate length of $L_g = 0.35$ µm and a gate oxide thickness of $t_{ox} = 7$ nm. A mixture of O_2 and D_2 was used during the oxidation step and a mixture of H_2 or D_2 with N_2 was respectively used during the PMA step, to passivate the dangling bonds at the Si/SiO_2-interface. Further documentation of the devices can be found in [240]. The slow, long-term degradation and recovery of HCD were investigated using Method **C** of Figure 2.13. A delay of 1 s between the stress phase and characterization was used to minimize any short-term recovery effects.

The deuterium passivated devices were fabricated more than 15 years ago and even after not being used and kept in storage (in air at room temperature) for 15+ years, the beneficial effects of the isotope effect on the lifetime and the level of degradation are still visible in Figure 7.1. The threshold voltage shifts roughly a factor ≈ 4 faster for D-passivated devices compared to H-passivated devices. In combination with earlier findings of stability of the Si-D bond at elevated temperatures [240, 242], this indicates that Si-D bonds are stable enough to prevent dissociation when no external stress (*e.g.* electrical, temperatures > $T > 520$ °C) is applied.

The shift in V_t ($\Delta V_{t,s}$) due to the creation of interface defects depends on the applied bias/electric field, stress temperature (T_s) and stress time (t_s), see Chapter 4. This shift depends on the temperature via an Arrhenius depen-

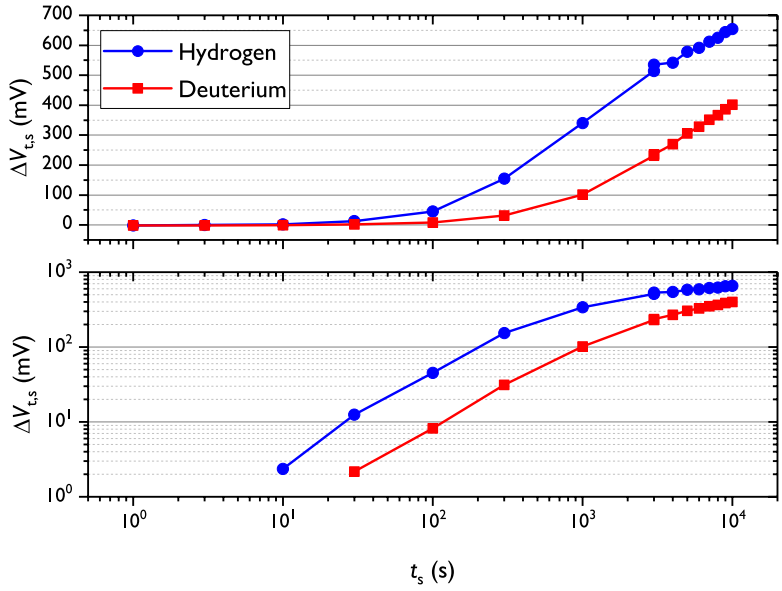

Figure 7.1: Shift in V_t due to HCD of H- and D-passivated devices, where identical stress conditions are applied. The top and bottom graphs show the same data, in lin-log and log-log scale.

dence [250]:

$$\Delta V_{t,s} \propto e^{\frac{E_a}{k_b T_a}}. \tag{7.1}$$

The recovery process may not follow the same principles as the degradation process, however, it is assumed that Arrhenius behavior is still expected when diffusion and reaction mechanisms determine the recovery [251].

Chapter 6 showed that, depending on stress conditions, the shift in threshold voltage could be explained by the introduction of a combination of interface and oxide defects and trapped charge in the gate oxide. Since the gate current did not change significantly after degradation, $I_g \approx$15 nA before and after $t_s = 10^4$ s, the assumption was made that oxide traps do not play a significant role under these experimental conditions. In this section, it is assumed that ΔV_t gives a reasonably good indication for the total amount of hot-carrier induced degradation of interface states and can be used to investigate the role of hydrogen/deuterium on the recovery of interface states. Note that charge-pumping experiments could exclude any charge (de-)trapping/oxide trap contribution and give the possibility to quantify the change in N_{it}.

7.3 Isotope Effect - Recovery

Devices passivated with hydrogen show recovery as a function of anneal temperature, anneal time and concentration of passivation species at the Si/SiO_2-interface (Chapter 5). In this section, it is assumed that the recovery of D-passivated devices will depend on the same parameters as for H-passivated devices.

The recovery of interface defects introduced by hot-carrier injection was done by annealing in air, using an M300 thermochuck from Att Systems (temperature ramp rate: $\Delta T_a = 0.1\ ^\circ C/s$) to $T_a = 200\ ^\circ C$ and annealed for $t_a = 1500$ s. It was assumed that the passivation species present inside the gate would be sufficient for significant recovery, see Chapter 3. Subsequently, the device is cooled down to room temperature, characterized and stressed again under the same stress conditions, as shown in Method **C** of Figure 2.13.

The threshold voltage as a function of the cumulative time (stress and recovery time) is shown in Figure 7.2 for four stress/anneal cycles. During the stress phase, the deuterium passivated devices show a bigger absolute ΔV_t than the hydrogen-passivated devices under identical stress conditions. During the recovery step, done under identical anneal conditions, both the hydrogen and deuterium passivated devices show similar levels of recovery, but relatively more for the D-passivated device (since there was less degradation). The difference in stress and recovery induced ΔV_t seems to diminish over subsequent cycles, where it is not visible anymore during the last cycle. Over time, the devices seem to behave more and more alike, stress and recovery-wise show a similar ΔV_t.

Next, the recovery of the hydrogen and deuterium passivated devices as a function of the anneal time in the first recovery phase is compared, as shown in Method **B** of Figure 2.13. Fresh devices are stressed by HCI at $T_a = 25\ ^\circ C$, after which the wafer was brought to an elevated temperature (T_a) for recovery. Upon reaching T_a; V_t, $g_{m,max}$ and $I_{d,lin}$ are periodically measured as a function of anneal time in air at five different temperatures ($T_a = 50, 85, 120, 150$ and $175\ ^\circ C$ - one device per anneal temperature). The linear drain current, $I_{d,lin}$, is measured at $V_{ds} = 0.1$ V and $V_{gs} = 2.0$ V. The threshold voltage shift during recovery is defined as:

$$\Delta V_{t,r}(t_a) = V_{t,r}(t_a) - V_{t,r}(0). \tag{7.2}$$

When $t_a = 0$ s, the thermochuck reaches the anneal temperature and the degradation is at its maximum at that specific anneal temperature. In a similar fashion, the anneal time-dependent recovery of Δg_m and $\Delta I_{d,lin}$ is calculated. Using Equation 7.2, the shift in the threshold voltage due to recovery will be negative.

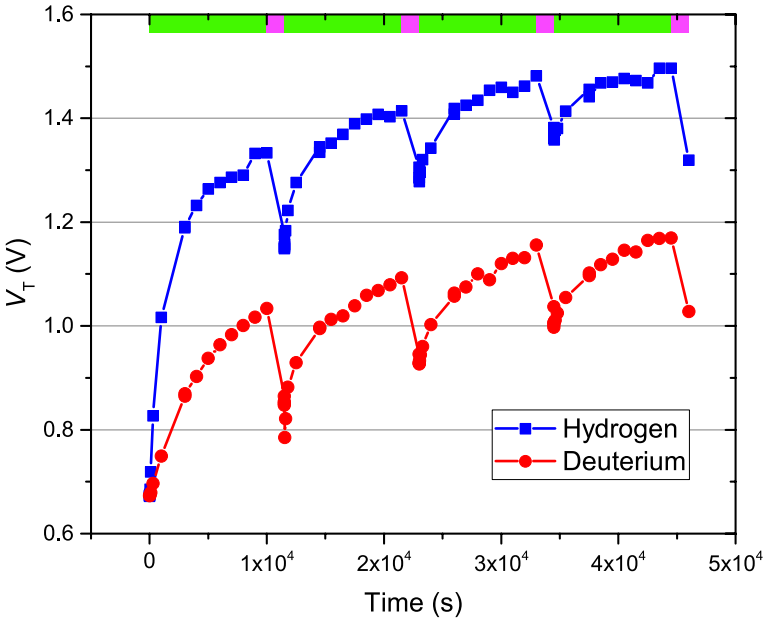

Figure 7.2: The threshold voltage as a function of the cumulative time. After each cycle of $t_a = 10^4$ s of HCl stress (green), the device is annealed at $T_a = 200$ °C for 1500 s (magenta). Characterization and stress were done at $T_m = T_s = 25$ °C.

7.3.1 Threshold Voltage Recovery

The recovery of the threshold voltage of hot-carrier degraded H/D- passivated devices is shown in Figure 7.3, where the data is acquired using the measurement process of Method **B** of Figure 2.13. At $t_a = 0$ s, the device reached the anneal temperature after the temperature step and the maximum ΔV_t is measured. At this time no shift in V_t due to recovery has taken place, *i.e.* $\Delta V_{t,r} = 0$ V. The recovery for both types of devices appears to follow a similar $\log(t_a)$ dependency [252].

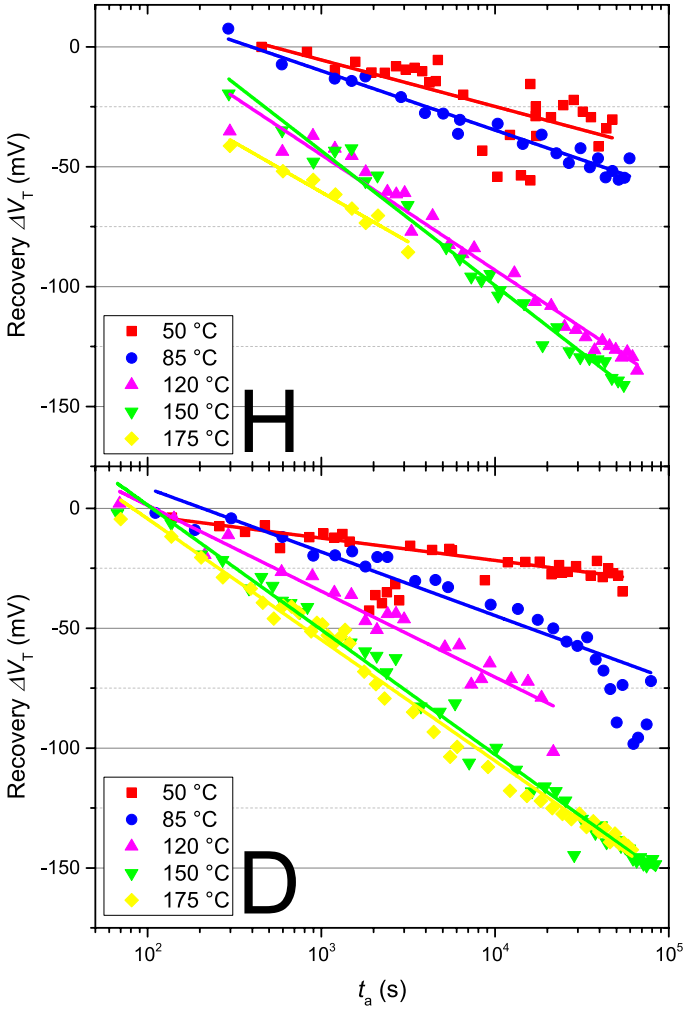

Figure 7.3: Recovery of V_t of the H-/D-passivated devices after $t_s = 10^4$ s of stress at $T_s = 25$ °C at different T_a. The lines are a guide for the eye.

7.3.2 Recovery of $I_{d,lin}$

The recovery of hot-carrier induced $\Delta I_{d,lin}$ in H/D- passivated devices is shown in Figure 7.4. At $t_a = 0$ s, the device reached the anneal temperature after the temperature step and has maximum degradation. As with the recovery of ΔV_t, the recovery behavior of $\Delta I_{d,lin}$ indicate a $\log(t_a)$ dependence. A higher elevated temperature will lead to a higher recovery rate and the data suggests further that the absolute amount of recovery is almost the same for both devices. The H-passivated devices endured more degradation, so the relative recovery is smaller than for the D-passivated devices.

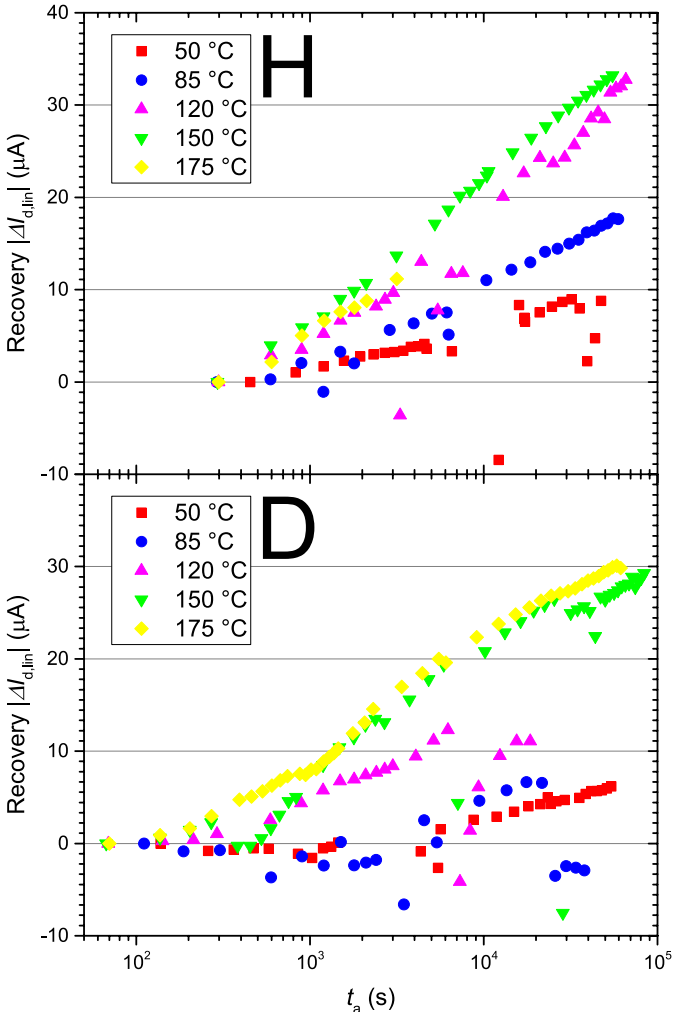

Figure 7.4: Recovery of $I_{d,lin}$ at $V_{gs} = 2$ V of the H-/D-passivated devices after $t_s = 10^4$ s of stress at $T_s = 25$ °C at different T_a.

7.3.3 Recovery ΔV_t vs $\Delta g_{m,max}$

If recovery of interface states/decharging takes place proportional to each other for each degradation/recovery cycle, the recovery of g_m should be proportional to the recovery of V_t. The transconductance is plotted as a function of the threshold voltage for the different cycles in Figure 7.5 for the H- and D-passivated devices.

After a new cycle is started, V_t should decrease and g_m should increase again, which is visible in both figures. Each new cycle seems to follow and continue on the previous cycle, suggesting that under the experimental conditions the interface states recover proportional to the recovery of trapped charge and that ΔV_t is indeed a reasonably good method to compare the recovery of hydrogen and deuterium passivated devices.

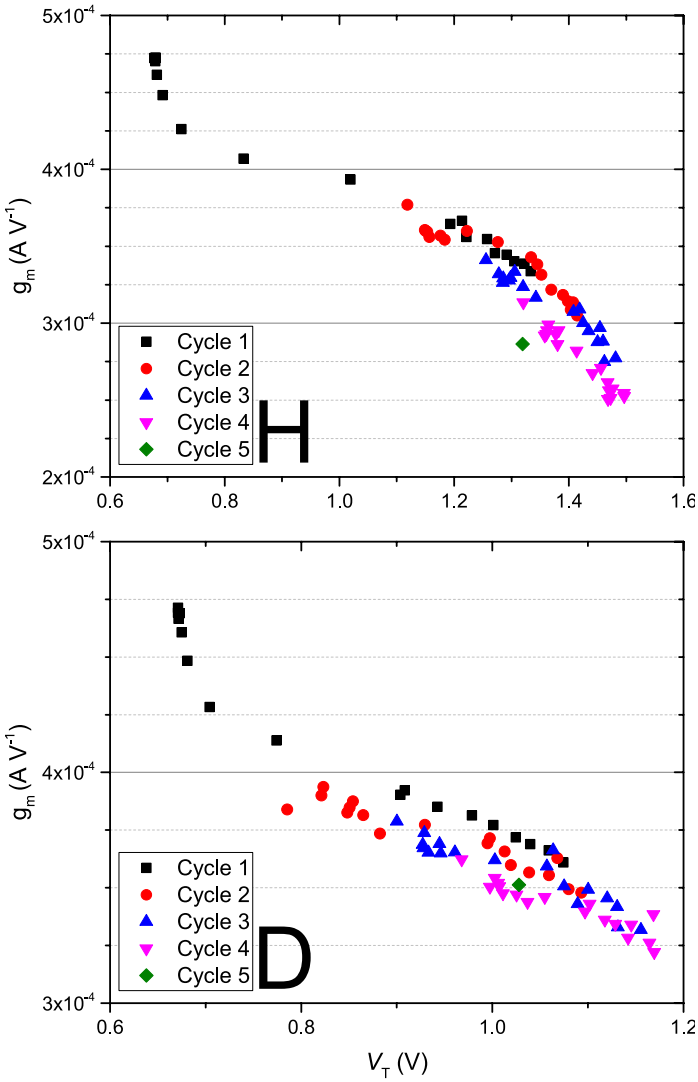

Figure 7.5: Transconductance as a function of the threshold voltage for the H- (top) and D-passivated (bottom) device for different degradation/anneal cycles, both are measured at $T_m = 25\,^{\circ}C$.

7.3.4 Arrhenius Dependency

The Arrhenius temperature dependence of the recovery of ΔV_t according to Equation 7.1 is shown in Figure 7.6. For this figure $|\Delta V_t|$ is determined at $t_a = 3$ ks from a fit (guide for the eye) of Figure 7.3. Using Equation 7.1 and Figure 7.6, the activation energy can be determined as $E_{a,H_2} = 0.176$ eV and $E_{a,D_2} = 0.181$ eV for H- and D-passivated devices respectively, indicating the same activation energy.

The similar E_a for both devices suggests that a similar recovery process takes place, regardless of the isotope used during the passivation step. Since hydrogen

is always present in the devices due to the various fabrication steps that involve hydrogen [83], the recovery may be explained by hydrogen passivation. Deuterium has a lower diffusion coefficient [253, 254], making it easier for hydrogen atoms to reach and to repassivate dangling bonds at the Si/SiO_2 interface.

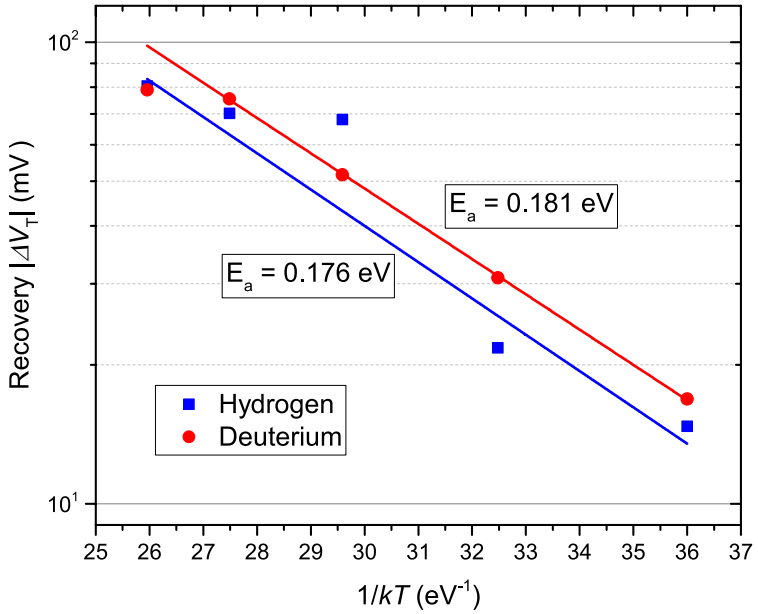

Figure 7.6: Arrhenius relationship between $|\Delta V_{t,r}|$ at $t_a = 3 \cdot 10^3$ s and the recovery temperature.

Note that the activation energy for recovery is calculated using Equation 7.1 and not Equation 3.13. The value for the activation energy is reported before and in line with earlier reported values for hot-carrier degradation (albeit negative, since passivation instead of depassivation takes place), however, this is not in line with the value for the activation energy used to describe passivation according to Stesmans' model [65, 188, 255]. Later experiments (Chapter 5 and Chapter 6) suggested that the bond energy of silicon-hydrogen bonds is in the order of $E_a \approx 1.5$ eV and that charging can play a role in the recovery of V_t, suggesting the need of more experimental data using other methods, *e.g.* charge-pumping method, to exclude other degradation and recovery mechanisms (Si-O bond breaking, slow/fast-traps, charge (de-)trapping), which will result in more clarity on the repassivation of Si-D bonds after degradation and confirm the hypothesis.

7.3.5 Isotope Effect after Multiple Degradation/Recovery Cycles

The hypothesis to explain the degradation/recovery cycle of a deuterium passivated device is visualized in Figure 7.7. Initially, a device passivated during the last fabrication step with deuterium (PMA step), has almost completely deuterium passivation at the Si/SiO_2-interface. The device is more resilient

to HCl-induced depassivation due to the isotope effect, enhancing the time until the maximum allowed parameter shift is reached. When the degraded device is annealed and recovery takes place, deuterium and hydrogen present in the gate stack will repassivate the dangling bonds introduced during the degradation step. Here hydrogen is introduced in the device during the various steps of the fabrication process where hydrogen is involved. Since repassivation is done of a combination of hydrogen and deuterium, the reliability of the once deuterated device will become more and more similar to a normal hydrogenated device. The degradation behavior will start to behave more in line with devices completely passivated with hydrogen.

After multiple degradation/recovery cycles, the dangling bonds at the Si/SiO_2-interface will be passivated by both hydrogen and deuterium. The ratio between hydrogen/deuterium passivation will go to the ratio of both isotopes in the gate stack/back end of the device.

Note: the assumption in this experiment has been made that the unstressed device has mainly deuterium passivation at the Si/SiO_2-interface, but has a combination of both isotopes in the rest of the device. To verify if this assumption is fair to be made, the same experiment could be done where every step in the fabrication process is done using deuterium instead of hydrogen.

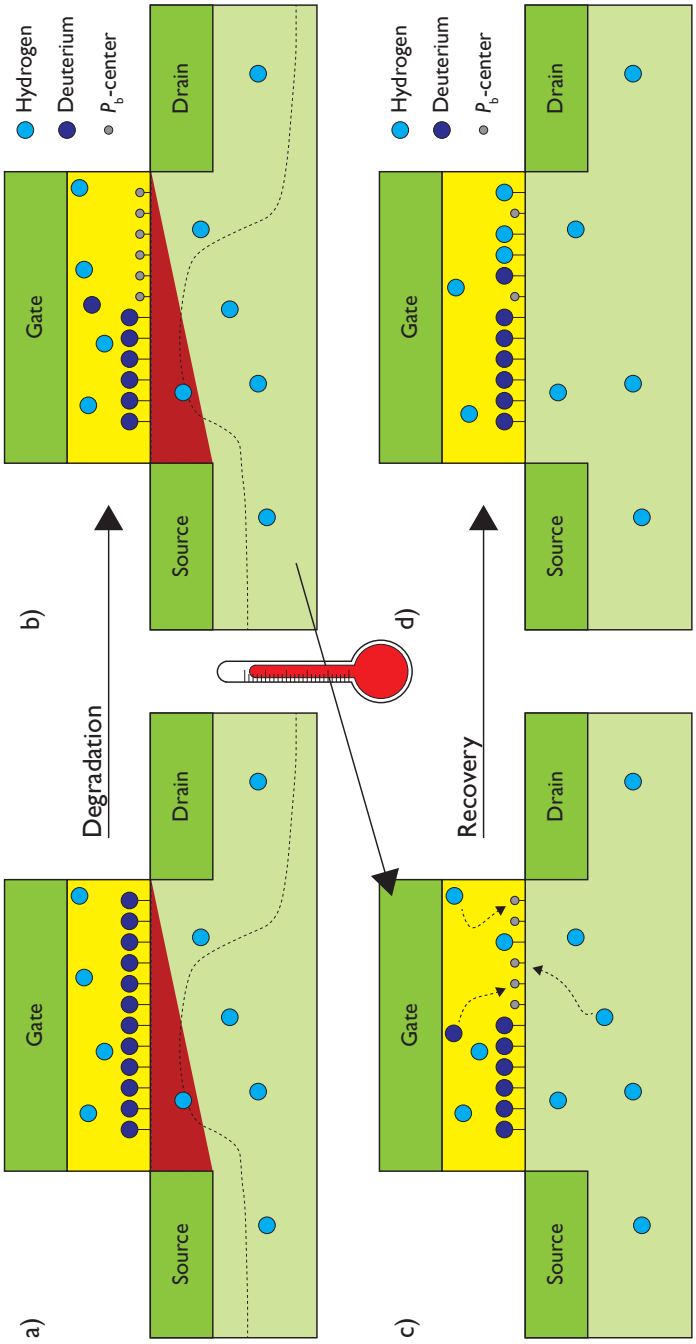

Figure 7.7: Effect of degradation/recovery on D-passivated samples: a) Prestress: Device has D-passivation. b) Degradation: Depassivation of deuterium. c) Recovery: H- and D-repassivation. d) Post recovery: Device is partial H- and D-passivated.

7.4 Multi Cyclic Degradation and Recovery

Besides using a different material as passivation material during the fabrication of the device (Section 7.3), the reliability of devices may be affected by changing the procedure of how electrical stress is applied. BTI stress tests are generally performed under DC stress conditions, where the device degrades continuously until breakdown or end-of-life takes place. When devices are not stressed continuously under DC conditions, but under AC/pulsed DC conditions (more in line with operating conditions), it was observed that less degradation took place, even when corrected for the cumulative stress times (50% stress time under 50% duty cycle) [160, 256--258]. When a BTI stress phase stops, relaxation of trapped charge in the gate oxide due will start to take place, which may be enhanced if the reverse bias is applied to the gate (AC versus pulsed DC), resulting in (partial) recovery and less overall degradation. When an uninterrupted BTI stress is applied, the devices will not benefit from relaxation, resulting in a higher stress level after the stress phase is finished.

Note that the argument can be made that DC BTI is factually only the first part of an AC BTI period. It would be fairer to compare devices with identical cumulative stress and recovery times. However, when a device under DC stress reaches its end-of-life during this first part of the period, the recovery phase is irrelevant/cannot have a positive effect on the total degradation level. Furthermore, the duty cycle of the AC stress is of importance for the lifetime prediction: the ratio of stress/recovery time indicates how much time a device has to recover the induced damage [152]. Although a duty cycle with a low stress/recovery time ratio will result in less cumulative degradation, it is realistic to expect that there will be a minimum value for the ratio to ensure the percentage of time the device is used (*i.e.* operates) will be non-negligible. *E.g.*, an recovery/stress time ratio of 10^6:1 will remove most of the degradation due to the long recovery time, but a recovery time of more than eleven days after one second of use is not realistic under normal operating conditions.

Furthermore, the capture and emission of charge carriers strongly depend on the capture/emission time constants (τ_c/τ_e) [152, 259]. Here a smaller emission time constant will result in more recovery, where the traps with the smaller τ_e are more likely to detrap. It is proposed that the combination of partial recovery due to AC BTI in combination with a small τ_e will result in a change of the distribution of trap levels. *I.e.* during the recovery phase, the traps with the lowest emission time constant will detrap first, increasing the average trap level of the remaining traps. Similarly, the next stress phase will first introduce the trap levels with the lowest capture time constant, lowering the mean trap level. If only partial recovery had taken place and the second stress phase started with already present traps, the average trap level will increase with each cycle.

Degradation by AC hot-carrier injection is reported to be frequency independent [260], however, it raises the question of whether the same assumption can be made for HCI degradation in combination with a recovery (anneal) step. *I.e.* if partial recovery of hot-carrier induced interface defects (Chapter 5, Figure 7.2)

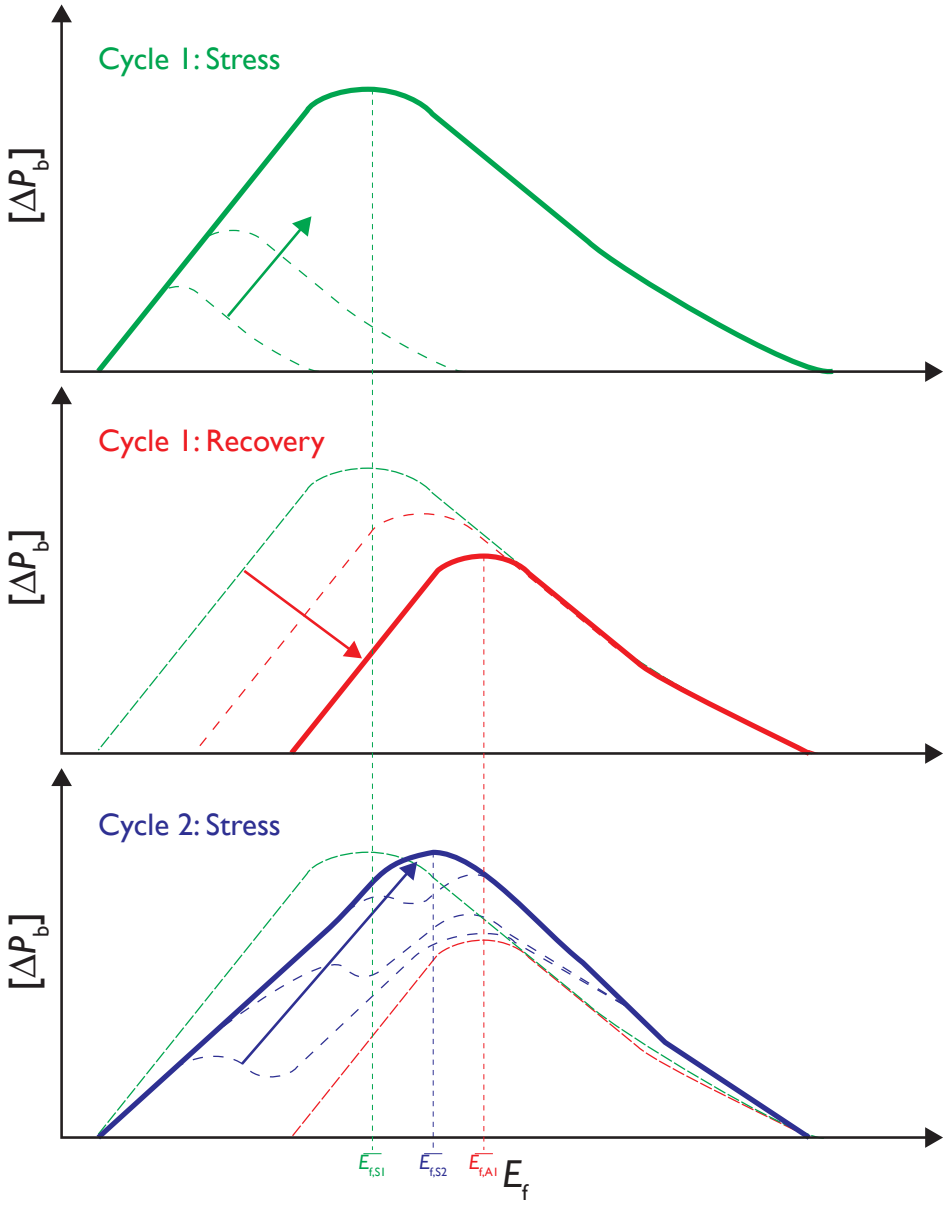

Figure 7.8: Hypothetical energy distribution of the broken Si-H bonds. Top: the first stress phase introduces new defects. Middle: the recovery phase removes some of the introduced defects. Bottom: second stress phase introduces new defects. Based on [237]

affects the Si-H bond energy distribution. Figure 7.8 shows the hypothetical evolution of the mean Si-H bond energy. Here it is assumed that during the first degradation step the defects introduced due to HCI can be described to be normally distributed (Top). The mean bond energy after the first stress

phase can be described by $\overline{E_{a,s1}}$. The temperature-dependent passivation of interface defects can initially be described in terms of a normalized distribution of the bond energy energies, where the defects with the lower Si-H bond energy tend to repassivate slightly easier compared to higher energy Si-H bonds (Middle) [65, 188, 255]. This would result in a decrease in the number of interface states, but an increase in the mean Si-H bond energy after the first recovery phase: $\overline{E_{a,r1}}$. Next, the stress phase of the second degradation/recovery cycle starts (Bottom). Since only partial recovery had taken place in the previous cycle, some broken higher energy Si-H bonds are present. Although mainly lower energy bonds will be broken, also some new higher energy Si-H bonds will be broken, increasing the mean bond energy of P_b centers after the second degradation step: $\overline{E_{a,s2}}$ [255]. Figure 7.8 suggests that the mean bond energy of degradation and recovery will be:

$$\overline{E_{a,s1}} < \overline{E_{a,s2}} \ll \overline{E_{a,r1}}. \tag{7.3}$$

Using this hypothesis, it may be possible to change the lifetime of devices if a higher frequency for degradation/anneal cycles (*i.e.* shorter cycle time) is used. If interface defects with the lowest bond energy tend to be (de-)passivated first during the various degradation/recovery cycles, the same defects created/repaired often compared to a device that has only one degradation/recovery cycle. This suggests that if two identical devices endure the same cumulative stress/recovery times, they may end with a different level of degradation remaining. The device that had only one recovery step, the recovery could be described as the recovery of bond-energy a normal distribution according to Stesmans' model, whereas the device with had n degradation/recovery cycles could only describe the first cycle according to Stesmans' model, whereas the remaining $n-1$ cycles could not [255].

To investigate the effect of degradation/cycle frequency on the total cumulative degradation, two chips with cumulative identical stress/anneal times are tested (Table 7.1). There was a factor 3 difference between the stress/recovery times and thus also the frequency of degradation/recovery cycles, $f_{ChipII} = \frac{f_{ChipI}}{3}$. During the stress phase, a drain-source bias of $V_{ds} = 4.8$ V and a gate-source bias of $V_{gs} = 2.2$ V was applied, whereas no bias was applied during the recovery/anneal step ($T_a = 200$ °C). The anneal step was done in air using a thermochuck.

Table 7.1: Cycle

	t_s (s)	t_a (min)
Chip I	1000	30
Chip II	3000	90

In a similar way, the frequency of degradation/recovery cycles may affect the defect distribution between oxide and interface traps. Chapter 6 suggested that hot-carrier degraded devices will initially be affected by the introduction of new interface defects, whereas oxide defects will be introduced at a later

stage. During the recovery step, interface traps will have a faster recovery rate (Chapter 6). As a consequence, when the stress time is sufficiently long to introduce more and more oxide traps, less recovery will take place in the anneal step. If degradation/recovery cycles with a higher frequency are used, fewer oxide traps will be introduced, and less total unrecoverable damage is present after the stress phase.

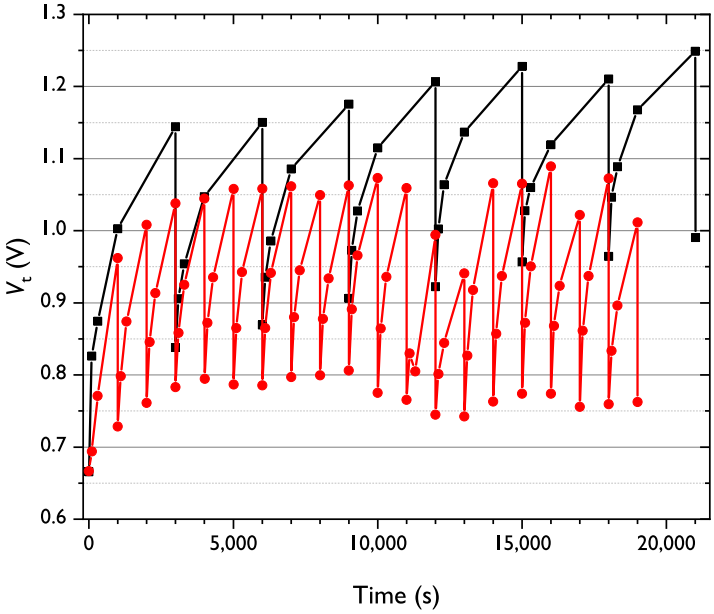

Figure 7.9: Threshold voltage as a function of time after various degradation and recovery cycles. The stress phase was $t_s = 1$ ks (red) or $t_s = 3$ ks (black). Recovery was always done by annealing at $T_a = 200$ °C.

Figure 7.9 and Figure 7.10 show the cyclic behavior of V_t and ΔN_{rc} as a function of time. The threshold voltage is extracted according the ELR method of Section 2.1.1 and ΔN_{rc} is extracted using the CP-method of Section 2.2. The data is not conclusive and cannot be used to make an accurate assumption, however, the data suggests that the effective degradation/stress frequency has some influence on the type of defect that is created and the cumulative amount of degradation that is induced in the device (different parameter shift after the recovery step). Future experimental research may be done to investigate this in more detail, for instance by looking into the ratio of N_{it}/N_{ot} as a function of different cycle times.

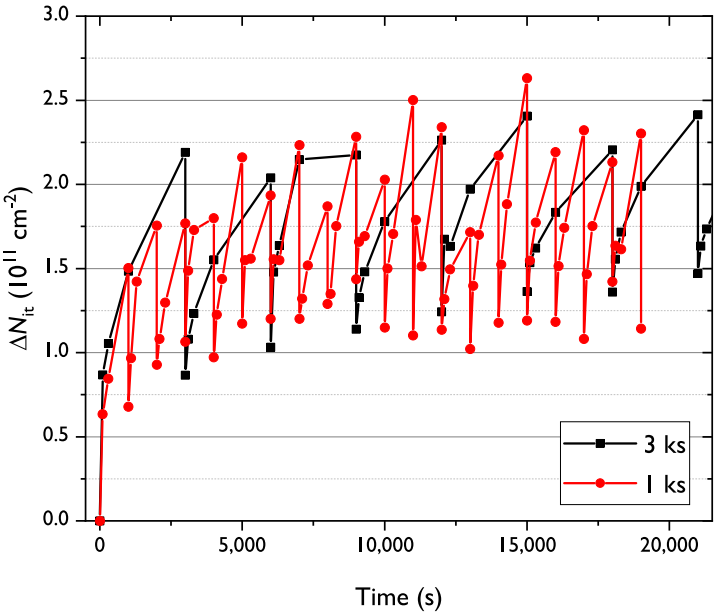

Figure 7.10: Shift in the interface defect density as a function of time after various degradation and recovery cycles. The stress phase was $t_s = 1$ ks (red) or $t_s = 3$ ks (black). Recovery was always done by annealing at $T_a = 200$ °C.

7.5 Summary and Conclusion

In this chapter, the influence of the stress phase on multiple degradation/recovery cycles and the cumulative lifetime of a device is investigated. Due to the isotope effect, *i.e.* the use of deuterium instead of hydrogen as a passivation species for dangling bonds at the Si/SiO_2-interface, less degradation may be observed when exposed to HCl. This will extend the time needed for the first recovery cycle, extending the total cumulative lifetime.

When a temperature treatment is applied to the devices after HCl degradation and recovery takes place, the devices seem to have similar recovery rates and behavior, regardless of passivation species. Furthermore, when (partially) recovered devices are electrically stressed again (same stress as during the first stress cycle), the beneficial effects of the isotope effect seem to diminish. After several degradation/recovery cycles, the deuterium and hydrogen passivated devices start to act more alike, suggesting that the differences between the types of (initial) passivation start to diminish.

Since hydrogen is always present in the gate stack due to the various fabrication steps that involve hydrogen, it is always involved in the passivation of dangling bonds during the recovery step, regardless of the passivation species of a fresh device, and effectively replace Si-D bonds for Si-D bonds. Although deuterium may also be involved during the recovery step, multiple degrada-

tion/recovery cycles will lead to a higher contribution of Si-H bonds and the ratio between hydrogen and deuterium used as a passivation species will be in line with the hydrogen/deuterium ratio in the whole device. As a consequence, multiple degradation/recovery cycles will make the hydrogen and deuterium passivated devices look more alike and the beneficial isotope effect will diminish. An (expensive) solution to prevent repassivation by hydrogen, would be to prevent hydrogen to interact with the device at all, *i.e.* if all steps during the fabrication processes that involve hydrogen will be done with deuterium, possibly in combination with a diffusion barrier that prevents hydrogen from reaching the interface from out of the device.

Besides affecting the type of passivation at the Si/SiO_2-interface, the degradation/recovery cycle may affect the type of introduced defects itself. When bonds of lower energy are broken and repaired first during the degradation and recovery phase respectively, they may be introduced/repaired frequently with subsequent degradation/recovery cycles. Some higher energy bond defects are created after prolonged stress time (not only Si-H bonds, but also oxide traps as described in the previous chapter), which may be prevented if the recovery step is performed within a (relatively) short stress time. *I.e.* the frequency of degradation/recovery cycles may affect the total cumulative degradation due to the introduction/removal of the same defect often, even if a cumulative identical stress and recovery condition is used. The main findings described in this chapter are:

- Deuterium passivated devices maintain their enhanced reliability due to the isotope effect after very long shelf times, *i.e.* no significant depassivation at room temperature if no electrical stress is applied.
- Less HCl-induced degradation due to the isotope effect diminishes after several degradation/recovery cycles.
- Repassivation of interface states by hydrogen could explain that initially, deuterium passivated devices start to behave like hydrogen passivated devices.
- The types of defects introduced by electrical degradation may be affected by the stress/recovery time ratio and frequency.

In conclusion, when a device undergoes multiple degradation/recovery cycles, various considerations may affect the total lifetime. For instance, the time per stress cycle up to the recovery step, how often recovery takes place and the fabrication material of the device itself.

CHAPTER 8

Conclusions & Recommendations

In this chapter, the most important conclusions presented in this thesis are summarized, followed by a presentation of the original contributions. Finally, some research questions for future work are proposed, that can help with the next steps towards a self-healing device.

8.1 Summary & Conclusions

In **Chapter 2**, *Device Characteristics and Characterization*, the theoretical background of a MOSFET and the charge-pumping measurement technique was discussed and how the extracted parameters are used to describe the degradation of devices. The characterization techniques used for the experiments in this thesis are discussed, as well as some experimental considerations that had to be taken into account, *e.g.* the influence of temperature on measurements.

In **Chapter 3**, *The Role of Hydrogen*, the role of hydrogen in the device and at the Si/SiO_2 interface was discussed. Special attention was paid to Stesmans' General Simple Thermal model that explains the passivation of dangling bonds in terms of a normal distribution of the bond energy and what can influence the concentration of hydrogen in a device.

In **Chapter 4**, *Degradation*, a short overview of various degradation mechanisms is given. Although degradation mechanisms may introduce various types of defects, the main focus was on hydrogen-related defects introduced by hot-carrier injection and how those defects may affect the reliability of a device.

In **Chapter 5**, *Enhancing Recovery*, various methods to enhance recovery are discussed. Even at low room temperature, some recovery takes place, even though the recovery rate is very slow and not practical under normal operating conditions. Some methods did not enhance the recovery rate (atomic hydrogen

ambient, using light), however, an enhanced recovery rate is observed when more hydrogen is introduced during the recovery step.

In **Chapter 6**, *Recovery: Fast versus Slow Traps*, non hydrogen-related defects, *i.e.* oxide traps, and their recovery are discussed. Charge-pumping characterization gives a more direct indication of the recovery rate compared to IV-measurements and is used to differentiate between both types of defects. Furthermore, longer degradation times may introduce oxide defects, which are more difficult to recover than hydrogen-related defects.

In **Chapter 7**, *Influence of the Stress Phase on the Stress/Recovery Cycles*, the influence of the stress condition on the degradation/recovery cycle is investigated. In addition, replacing hydrogen with deuterium as the passivation species during the device fabrication step makes the device less susceptible to degradation, *i.e.* the Isotope Effect. However, subsequent recovery steps will use a combination of hydrogen and deuterium to repassivate interface defects, diminishing the beneficial effect of the Isotope effect. Furthermore, the hypothesis is raised that during the stress phase, different degradation conditions/times may introduce different types of defects that can have a lower or higher recovery rate. This can be used to tweak the degradation conditions and raises the question of whether recovery can be induced under more operation favorable conditions.

8.2 Original contributions

The work presented in this thesis that resulted in several papers is discussed in **Chapter 5**, **Chapter 6** and **Chapter 7**. The original contributions of these papers can be summarized as:

- Temperature-induced recovery of hot-carrier degraded device seems to follow Stesmans' Generalized Passivation Model, there are however indications that it needs to be expanded to model the recovery accurately.
- Hydrogen in the gate stack may provide sufficient passivation material to repair all defects, however, the recovery rate can be enhanced significantly when H_2 is added externally by means of a high-pressure ambient of molecular hydrogen. Other hydrogen species seem to be less beneficial to the recovery process.
- Different types of defect may affect device parameters in a different way and do not recover at the same recovery rate.
- A diffusion barrier such as the commonly used Si_3N_4 scratch protection layer may prevent externally offered hydrogen from contributing to the recovery process or help contain the hydrogen in the gate stack.
- Oxide defects are created after longer hot-carrier stress times and recover slower compared to interface defects at an anneal temperature of $T_a = 85\ ^\circ C$.

- The Isotope Effect retards the degradation process, however, the recovery process also reintroduces hydrogen to the Si/SiO_2-interface.

- Varying the time to the next recovery step may be used to degrade/recover certain types of defects and extend the cumulative lifetime of a device.

8.3 Recommendations

The main goal of the "Self-Healing in Transistors"-project was to set the first steps on the road to a self-healing MOSFET device. During the lifetime of a device, defects will be introduced in the device, which will lead to a shift in various operating parameters. When the number of defects in the device and the shift in parameters is too big, the circuit fails and the end-of-life is reached. A Self-Healing device would be able to repair defects in the device without help from outside the device. Depending on the number of times recovery can take place, the lifetime could be extended significantly, possibly in combination with improved performance.

In this research, a better understanding of various degradation/recovery steps and conditions were acquired. To build further on the findings of this thesis, some recommendations and suggestions for future research are:

- Investigation of degradation/recovery cycles of devices where during fabrication all steps that involve hydrogen are replaced by deuterium:
  → ***Will the beneficial effects of the Isotope Effect stay present after multiple degradation/recovery cycles?***

- Investigation of multicyclic degradation/recovery steps in combination with partial/total recovery of parameters:
  → ***How many repair cycles can be induced and are repaired devices indistinguishable from fresh devices?***

- Investigation of multicyclic degradation/recovery steps/times on the total cumulative lifetime of a device:
  → ***Are different types of defects created/repaired at different stress times and can that be used to extend the lifetime of a device?***

- Investigation of trade-offs between various degradation mechanisms in combination with recovery mechanisms:
  → ***If one parameter (e.g. material) has a beneficial effect on a certain degradation (recovery) mechanism, how does it affect other degradation (recovery) mechanisms?***

- Investigation of a local source for hydrogen inside the gate stack:
  → ***Can a local hydrogen source provide a stable, constant supply of hydrogen and enhance the recovery rate?***

8.4 Considerations and Predictions for the Future

The end goal of the research discussed is to produce a self-healing device that can repair itself completely, as if it was a fresh, new device. Current research has a focus on minimizing degradation mechanisms, specifically hot-carrier degradation, one of the main bottlenecks for high-performance semiconductor logic. In this thesis various methods to investigate and enhance the recovery of hot-carrier degraded devices have been discussed, as well as some recommendations for future experimental research. However, this research had a primary focus on the recovery of hydrogen-related defects.

A completely self-healing device should be able to heal every type of defect, regardless of the degradation mechanism or defect. Furthermore, future research should investigate if the healing of other types of defects is in competition with the healing of hydrogen-related defects and a balance may have to be found, which may limit complete self-healing of the whole device as well as limitations on how often self-healing can take place. For instance, an increase in hydrogen concentration may enhance the recovery rate of interface states, but may also increase depassivation of certain hydrogen-related bonds or passivate dangling bonds of oxide-related defects in the gate oxide, preventing their recovery. In other words, research has to be done under which circumstances the cure may be worse than the disease. Similarly, if complete self-healing of a device is achieved, this may be in competition with the self-healing of the whole chip (*e.g.* interconnects, packaging).

Contemporary research has a focus on prevention of degradation and it tends to be easier to optimize existing reliability than to implement a whole new (recovery) mechanism. In combination with the need of balancing all the healing mechanisms and reliability issues, it is likely that in the near future (< 10 years) it is more cost-effective that the main focus will stay on degradation prevention. This will lead to incremental improvements of reliability, however, the focus may shift towards recovery over degradation prevention when more is known on how to balance these recovery mechanisms and how to implement them cost-effectively. The research of this thesis has proven that significant recovery can be achieved and future research will build on the findings and research on the recovery of hydrogen-related defects. This would may make it possible to reduce their impact on the total lifetime to such a level that other, better manageable reliability issues take over.

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Bibliography

[1] S. Engineering. (2021). [Online]. Available: https://semiengineering.com/confluence-of-automotive-trends-impacting-semi-design/

[2] S. Sze and M.-K. Lee, *Semiconductor devices: physics and technology; 3rd ed.* Hoboken, NJ: Wiley, 2012. [Online]. Available: https://cds.cern.ch/record/1632394

[3] D. J. Smith, "Chapter 2 - understanding terms and jargon," in *Reliability, Maintainability and Risk (Ninth Edition)*, ninth edition ed., D. J. Smith, Ed. Butterworth-Heinemann, 2017, pp. 15 -- 30. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780081020104000029

[4] K. Okada, "Fundamental feol reliability: Defect generation in gate dielectrics to induce dielectric breakdown and device degradation (tutorial)," 04 2017.

[5] K. Rupp. karlrupp/microprocessor-trend-data. [Online]. Available: https://github.com/karlrupp/microprocessor-trend-data

[6] M. D. Hager, P. Greil, C. Leyens, S. van der Zwaag, and U. S. Schubert, "Self-healing materials," *Advanced Materials*, vol. 22, no. 47, pp. 5424--5430, 2010. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201003036

[7] S. R. White, J. S. Moore, N. R. Sottos, B. P. Krull, W. A. S. Cruz, and R. C. R. Gergely, "Restoration of large damage volumes in polymers," *Science*, vol. 344, no. 6184, pp. 620--623, 2014. [Online]. Available: https://www.science.org/doi/abs/10.1126/science.1251135

[8] J. Schmitz, "Self-healing in semiconductors," in *Future Trends in Microelectronics, Mallorca, Spain*, 2015.

[9] D. Kahng, *Silicon-Silicon Dioxide Surface Device*, 1960, pp. 583--596. [Online]. Available: https://www.worldscientific.com/doi/abs/10.1142/9789814503464_0076

[10] G. W. Neudeck and R. F. Pierret, "Field effect devices," in *Ser. Modular Series on Solid State Devices*. Addison-Wesley, 1990, vol. 4.

[11] R. J. Van Overstraeten, G. J. Declerck, and P. A. Muls, "Theory of the MOS transistor in weak inversion-new method to determine the number of surface states," *IEEE Transactions on Electron Devices*, vol. 22, no. 5, pp. 282--288, 1975.

[12] B. K. Boksteen, J. Schmitz, and R. J. E. Hueting, "Interface trap density estimation in finfets using the g_m/i_d method in the subthreshold regime," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1814--1820, 2016.

[13] J. R. Brews, "Subthreshold behavior of uniformly and nonuniformly doped long-channel MOSFET," *IEEE Transactions on Electron Devices*, vol. 26, no. 9, pp. 1282--1291, 1979.

[14] T. Grotjohn and B. Hoefflinger, "A parametric short-channel MOS transistor model for subthreshold and strong inversion current," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 1, pp. 100--112, 1984.

[15] R. van Langevelde and F. M. Klaassen, "Effect of gate-field dependent mobility degradation on distortion analysis in MOSFETs," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 2044--2052, 1997.

[16] X. Zhao, J. Xu, L. Liu, P. Lai, and W. Tang, "Repair of oxygen vacancies and improvement of HfO_2/MoS_2 interface by NH_3-plasma treatment," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4337--4342, Oct 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8811757

[17] R. Woltjer, G. M. Paulzen, H. G. Pomp, H. Lifka, and P. H. Woerlee, "Three hot-carrier degradation mechanisms in deep-submicron PMOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 1, pp. 109--115, 1995.

[18] A. Ortiz-Conde, F. G. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, no. 4, pp. 583 -- 596, 2002. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271402000276

[19] R. Wang, J. Dunkley, T. A. DeMassa, and L. F. Jelsma, "Threshold voltage variations with temperature in MOS transistors," *IEEE Transactions on Electron Devices*, vol. 18, no. 6, pp. 386--388, June 1971.

[20] T. Ishihara, Y. Nakasaki, D. Matsushita, K. Tatsumura, and K. Kato, "Interface defect engineering for high-performance mosfets with novel carrier mobility model: Theory and experimental verification," *AIP Advances*, vol. 10, no. 5, p. 055020, 2020. [Online]. Available: https://doi.org/10.1063/5.0005813

[21] C. Schlünder, J. Berthold, F. Proebster, A. Martin, W. Gustin, and H. Reisinger, "On the influence of BTI and

HCI on parameter variability," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, April 2017, pp. 2E--4.1--2E--4.8.

[22] J. S. Brugler and P. G. A. Jespers, "Charge pumping in MOS devices," *IEEE Transactions on Electron Devices*, vol. 16, no. 3, pp. 297--302, March 1969.

[23] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Transactions on Electron Devices*, vol. 31, no. 1, pp. 42--53, Jan 1984.

[24] T. Aichinger and M. Nelhiebel, "Charge pumping revisited - the benefits of an optimized constant base level charge pumping technique for MOS-FET analysis," in *2007 IEEE International Integrated Reliability Workshop Final Report*, Oct 2007, pp. 63--69.

[25] S. Sahhaf, R. Degraeve, M. Cho, K. D. Brabanter, P. Roussel, M. Zahid, and G. Groeseneken, "Detailed analysis of charge pumping and ldVg hysteresis for profiling traps in SiO_2/HfSiO(N)," *Microelectronic Engineering*, vol. 87, no. 12, pp. 2614 -- 2619, 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931710002716

[26] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-k dielectrics reliability issues," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 1, pp. 5--19, March 2005. [Online]. Available: https://ieeexplore.ieee.org/document/1435384

[27] R. N. Hall, "Electron-hole recombination in germanium," *Phys. Rev.*, vol. 87, pp. 387--387, Jul 1952. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.87.387

[28] W. Shockley and W. T. Read, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835--842, Sep 1952. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.87.835

[29] D. Buchanan and D. Felnhofer, *On the Characterization of Electronivally Active Defects in High-K Dielectrics*, 02 2006, pp. 41--59.

[30] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Transactions on Electron Devices*, vol. 36, no. 7, pp. 1318--1335, July 1989.

[31] C. Viswanathan and V. Ramgopal Rao, "Application of charge pumping technique for sub-micron MOSFET characterization," *Microelectronic Engineering*, vol. 40, no. 3, pp. 131 -- 146, 1998, electrical and Physical Characterization. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931798002664

[32] G. Van den Bosch, G. Groeseneken, and H. E. Maes, "On the geometric component of charge-pumping current in MOSFETs," *IEEE Electron Device Letters*, vol. 14, no. 3, pp. 107--109, March 1993.

[33] Aichinger, Thomas and Nelhiebel, Michael, *Characterization of MOSFET Interface States Using the Charge Pumping Technique*. Cham: Springer International Publishing, 2015, pp. 231--255. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_8

[34] B. Ruch, G. Pobegen, and T. Grasser, "Investigation of the temperature dependence of hot-carrier degradation in Si MOSFETs using spectroscopic charge pumping," *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4092--4098, 2020.

[35] B. Ruch, G. Pobegen, C. Schleich, and T. Grasser, "Generation of hot-carrier induced border and interface traps, investigated by spectroscopic charge pumping," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, pp. 1--6.

[36] T. Aichinger, M. Nelhiebel, and T. Grasser, "On the temperature dependence of NBTI recovery," *Microelectronics Reliability*, vol. 48, no. 8, pp. 1178 -- 1184, 2008, 19th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008). [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271408002333

[37] M. W. Feil, K. Puschkarsky, W. Gustin, H. Reisinger, and T. Grasser, "On the physical meaning of single-value activation energies for BTI in Si and SiC MOSFET devices," *IEEE Transactions on Electron Devices*, pp. 1--8, 2020.

[38] H. Haddara, "Drain current charge pumping: a new technique for interface trap characterization in VLSI MOS transistors," in *Proceedings of the Sixteenth National Radio Science Conference. NRSC'99 (IEEE Cat. No.99EX249)*, Feb 1999, pp. D5/1--D5/7.

[39] K. Kato, D. Matsushita, K. Muraoka, and Y. Nakasaki, "Agglomeration and uniform growth of Si_3N_4 on Si(100): Experiments and first-principles calculations," *Phys. Rev. B*, vol. 78, p. 085321, Aug 2008. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.78.085321

[40] J. Robertson, "High dielectric constant oxides," *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265--291, 2004. [Online]. Available: https://doi.org/10.1051/epjap:2004206

[41] Y. Nishi, "Study of silicon-silicon dioxide structure by electron spin resonance i," *Japanese Journal of Applied Physics*, vol. 10, no. 1, pp. 52--62, jan 1971. [Online]. Available: https://doi.org/10.1143/jjap.10.52

[42] S. Franssila, *Thermal Oxidation*. John Wiley & Sons, Ltd, 2010, ch. 13, pp. 153--163. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119990413.ch13

[43] M. L. Reed, "Models of Si-SiO_2 interface reactions," *Semiconductor Science and Technology*, vol. 4, no. 12, p. 980, 1989. [Online]. Available: http://stacks.iop.org/0268-1242/4/i=12/a=003

[44] D. Varghese, G. Gupta, L. M. Lakkimsetti, D. Saha, K. Ahmed, F. Nouri, and S. Mahapatra, "Physical mechanism and gate insulator material dependence of generation and recovery of negative-bias temperature instability in p-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 7, pp. 1672--1680, July 2007.

[45] S. Jik Lee, S. Hwan Kim, D. Won Kim, K. Hyung Kim, B. Kyu Kim, and J. Jang, "Effect of hydrogen plasma passivation on performance of hit solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 1, pp. 81 -- 83, 2011, 19th International Photovoltaic Science and Engineering Conference and Exhibition (PVSEC-19) Jeju, Korea, 9-13 November 2009. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0927024810002977

[46] A. Soman, U. Nsofor, L. Zhang, U. Das, T. Gu, and S. Hegedus, "Hydrogen plasma post-deposition treatment for passivation of a-si/c-si interface for heterojunction solar cell by correlating optical emission spectroscopy and minority carrier lifetime," in *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*, 2017, pp. 1828--1831.

[47] A. Kamgar, D. P. Monroe, and W. M. Mansfield, "Passivation of interface-states in large-area Si devices using hydrogen implantation," *IEEE Electron Device Letters*, vol. 24, no. 7, pp. 448--450, July 2003. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/1217293

[48] I. A. Shkrob, B. M. Tadjikov, S. D. Chemerisov, and A. D. Trifunac, "Electron trapping and hydrogen atoms in oxide glasses," *The Journal of Chemical Physics*, vol. 111, no. 11, pp. 5124--5140, 1999. [Online]. Available: https://doi.org/10.1063/1.479740

[49] A. Yokozawa and Y. Miyamoto, "First-principles exploration of possible trap terminators in SiO_2," *Applied Physics Letters*, vol. 73, no. 8, pp. 1122--1124, 1998. [Online]. Available: https://doi.org/10.1063/1.122103

[50] A.-M. El-Sayed, M. B. Watkins, T. Grasser, V. V. Afanas'ev, and A. L. Shluger, "Hydrogen-induced rupture of strained Si-O bonds in amorphous silicon dioxide," *Phys. Rev. Lett.*, vol. 114, p. 115503, Mar 2015. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.114.115503

[51] L. R. C. Fonseca, A. L. Xavier, M. Ribeiro, C. Driemeier, and I. J. R. Baumvol, "Hydrogen trapping in oxygen-deficient hafnium silicates," *Journal of Applied Physics*, vol. 102, no. 4, p. 044108, 2007. [Online]. Available: https://doi.org/10.1063/1.2769790

[52] Y. Higashi, R. Takaishi, K. Kato, M. Suzuki, Y. Nakasaki, M. Tomita, Y. Mitani, M. Matsumoto, S. Ogura, K. Fukutani, and K. Yamabe, "Mechanism of gate dielectric degradation by hydrogen migration from the cathode interface," *Microelectronics Reliability*, vol. 70, pp. 12 -- 21, 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271417300173

[53] P. Hamer, B. Hallam, R. S. Bonilla, P. P. Altermatt, P. Wilshaw, and S. Wenham, "Modelling of hydrogen transport in silicon solar cell structures under equilibrium conditions," *Journal of Applied Physics*, vol. 123, no. 4, p. 043108, 2018. [Online]. Available: https://doi.org/10.1063/1.5016854

[54] G. Pobegen, M. Nelhiebel, and T. Grasser, "Detrimental impact of hydrogen passivation on NBTI and hc degradation," in *2013 IEEE International Reliability Physics Symposium (IRPS)*, April 2013, pp. XT.10.1--XT.10.6.

[55] R. A. Kohler, R. A. Kushner, and K. H. Lee, "Total dose radiation hardness of MOS devices in hermetic ceramic packages," *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1492--1496, Dec 1988.

[56] M. Houssa, S. D. Gendt, J. L. Autran, G. Groeseneken, and M. M. Heyns, "Role of hydrogen on negative bias temperature instability in HfO_2-based hole channel field-effect transistors," *Applied Physics Letters*, vol. 85, no. 11, pp. 2101--2103, 2004. [Online]. Available: https://doi.org/10.1063/1.1784549

[57] M. Houssa, V. V. Afanas'ev, A. Stesmans, M. Aoulaiche, G. Groeseneken, and M. M. Heyns, "Insights on the physical mechanism behind negative bias temperature instabilities," *Applied Physics Letters*, vol. 90, no. 4, p. 043505, 2007. [Online]. Available: https://doi.org/10.1063/1.2434176

[58] K. L. Brower, "Kinetics of H_2 passivation of P_b centers at the (111) Si-SiO_2 interface," *Phys. Rev. B*, vol. 38, pp. 9657--9666, Nov 1988. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.38.9657

[59] ------, "Dissociation kinetics of hydrogen-passivated (111) Si-sio$_2$ interface defects," *Phys. Rev. B*, vol. 42, pp. 3444--3453, Aug 1990. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.42.3444

[60] I. Hirano, K. Kato, Y. Nakasaki, S. Fukatsu, Y. Mitani, M. Goto, S. Inumiya, K. Sekine, and M. Sato, "Novel TDDB mechanism for p-FET accelerated by hydrogen from HfSiON film," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 424--429.

[61] L. Tsetseris, D. Fleetwood, R. Schrimpf, X. Zhou, I. Batyrev, and S. Pantelides, "Hydrogen effects in MOS devices," *Microelectronic Engineering*, vol. 84, no. 9, pp. 2344 -- 2349, 2007, iNFOS 2007. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931707004273

[62] E. Cartier, J. H. Stathis, and D. A. Buchanan, "Passivation and depassivation of silicon dangling bonds at the Si/SiO2 interface by atomic hydrogen," *Applied Physics Letters*, vol. 63, no. 11, pp. 1510--1512, 1993. [Online]. Available: https://doi.org/10.1063/1.110758

[63] C. G. Van de Walle, Y. Bar-Yam, and S. T. Pantelides, "Theory of hydrogen diffusion and reactions in crystalline silicon," *Phys. Rev. Lett.*, vol. 60, pp. 2761--2764, Jun 1988. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.60.2761

[64] A. Stesmans, "Structural relaxation of p_b defects at the (111)si/sio$_2$ interface as a function of oxidation temperature: The p_b-generation--stress relationship," *Phys. Rev. B*, vol. 48, pp. 2418--2435, Jul 1993. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.48.2418

[65] ------, "Passivation of P_{b0} and P_{b1} interface defects in thermal (100) Si/SiO_2 with molecular hydrogen," *Applied Physics Letters*, vol. 68, no. 15, pp. 2076--2078, 1996. [Online]. Available: https://doi.org/10.1063/1.116308

[66] ------, "Revision of H_2 passivation of $p_b$interface defects in standard (111)Si/SiO_2," *Applied Physics Letters*, vol. 68, no. 19, pp. 2723--2725, 1996. [Online]. Available: https://doi.org/10.1063/1.115577

[67] A. R. Wilkinson and R. G. Elliman, "Kinetics of h_2 passivation of Si nanocrystals in sio_2," *Phys. Rev. B*, vol. 68, p. 155302, Oct 2003. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.68.155302

[68] Y. . Lee, R. Nachman, K. Seshan, D. . Kau, and N. Mielke, "Role of hydrogen anneal in thin gate oxide for multi-metal-layer CMOS process," in *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059)*, April 2000, pp. 186--190.

[69] D. B. Strukov and R. S. Williams, "Exponential ionic drift: fast switching and low volatility of thin-film memristors," *Applied Physics A*, vol. 94, no. 3, pp. 515--519, 2009.

[70] D. Shaw, *Diffusion in Semiconductors*. Cham: Springer International Publishing, 2017, pp. 1--1. [Online]. Available: https://doi.org/10.1007/978-3-319-48933-9_6

[71] N. Nickel, "Hydrogen transport in doped and undoped polycrystalline silicon," *Microelectronics Reliability*, vol. 47, no. 6, pp. 899 -- 902, 2007, modelling the Negative Bias Temperature Instability. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271406003805

[72] O. Musseau, S. Krawiec, P. Paillet, A. Courtot-Descharles, and O. Gruber, "Generation and confinement of mobile charges in buried oxide of SOI substrates," in *1999 Fifth European Conference on Radiation and Its Effects on Components and Systems. RADECS 99 (Cat. No.99TH8471)*, Sep. 1999, pp. 251--255. [Online]. Available: https://ieeexplore.ieee.org/document/858590

[73] K. Vanheusden and R. A. B. Devine, "The role of interface states in hydrogen-annealing-induced mobile proton generation at the $Si-SiO_2$ interface," *Applied Physics Letters*, vol. 76, no. 21, pp. 3109--3111, 2000. [Online]. Available: https://doi.org/10.1063/1.126539

[74] A. Courtot-Descharles, P. Paillet, J. Leray, and O. Musseau, "First principles calculations of hydrogen annealed amorphous SiO_2 structures and Si/SiO_2 interface for non volatile memories," *Materials Science in Semiconductor Processing*, vol. 3, no. 1, pp. 143 -- 148, 2000. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369800100000160

[75] T. Yamaguchi, M. Sawada, K. Asai, K. Kobayashi, and M. Yoneda, "Hydrogen ion drift into underlying oxides by RF bias during high-density plasma chemical vapor deposition," *Japanese Journal of Applied Physics*, vol. 44, no. 11, pp. 7863--7868, nov 2005. [Online]. Available: https://doi.org/10.1143%2Fjjap.44.7863

[76] G. T. Yu and S. Yen, "Hydrogen ion diffusion coefficient of silicon nitride thin films," *Applied Surface Science*, vol. 202, no. 1, pp. 68 -- 72, 2002. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0169433202008863

[77] E. Cartier, D. A. Buchanan, and G. J. Dunn, "Atomic hydrogen-induced interface degradation of reoxidized-nitrided silicon dioxide on silicon," *Applied Physics Letters*, vol. 64, no. 7, pp. 901--903, 1994. [Online]. Available: https://doi.org/10.1063/1.110990

[78] Z. Liu, M. Wilde, T. Takeshita, S. Fujieda, and K. Fukutani, "A novel strategy for ideal MOS stack of high dielectric reliability," in *2013 IEEE International Integrated Reliability Workshop Final Report*, Oct 2013, pp. 62--68.

[79] A. D. Marwick, J. C. Liu, and K. P. Rodbell, "Hydrogen redistribution and gettering in alcu/ti thin films," *Journal of Applied Physics*, vol. 69, no. 11, pp. 7921--7923, 1991. [Online]. Available: https://doi.org/10.1063/1.347483

[80] T. Pompl, K. . Allers, R. Schwab, K. Hofmann, and M. Roehner, "Change of acceleration behavior of time-dependent dielectric breakdown by the beol process: indications for hydrogen induced transition in dominant degradation mechanism," in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.*, April 2005, pp. 388--397.

[81] S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Dual behavior of H^+ at $Si-SiO_2$ interfaces: Mobility versus trapping," *Applied Physics Letters*, vol. 81, no. 10, pp. 1839--1841, 2002. [Online]. Available: https://doi.org/10.1063/1.1504879

[82] Z. Liu, S. Ito, S. Hiroshima, S. Koyama, M. Makabe, M. Wilde, and K. Fukutani, "Mobile and stable hydrogen species in the interface layer between poly silicon and gate oxynitride," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 417--423.

[83] G. I. Isai, "ECR plasma deposited SiO_2 and Si_3N_4 layers: a room temperature technology," Ph.D. dissertation, Enschede, June 2003. [Online]. Available: http://doc.utwente.nl/41455/

[84] S. A. Steward, "Review of hydrogen isotope permeability through materials," 8 1983. [Online]. Available: https://www.osti.gov/biblio/5277693

[85] H. Yukawa, T. Nambu, and Y. Matsumoto, "13 - design of group 5 metal-based alloy membranes with high hydrogen permeability and strong resistance to hydrogen embrittlement," in *Advances in Hydrogen Production, Storage and Distribution*, A. Basile and A. Iulianelli, Eds. Woodhead Publishing, 2014, pp. 341--367. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780857097682500134

[86] B. Sopori, Y. Zhang, and N. M. Ravindra, "Silicon device processing in H-ambients: H-diffusion mechanisms

and influence on electronic properties," *Journal of Electronic Materials*, vol. 30, no. 12, pp. 1616--1627, Dec 2001. [Online]. Available: https://doi.org/10.1007/s11664-001-0181-1

[87] J. H. Stathis, "Dissociation kinetics of hydrogen-passivated (100) Si/SiO_2 interface defects," *Journal of Applied Physics*, vol. 77, no. 12, pp. 6205--6207, 1995. [Online]. Available: https://doi.org/10.1063/1.359148

[88] M. W., "Hydrogen-modification of electronic surface, bulk, and interface properties of Si," *physica status solidi (a)*, vol. 159, no. 1, pp. 25--37, 1997. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/1521-396X%28199701%29159%3A1%3C25%3A%3AAID-PSSA25%3E3.0.CO%3B2-C

[89] P. S. Winokur, H. E. Boesch, J. M. McGarrity, and F. B. McLean, "Field- and time-dependent radiation effects at the SiO_2/Si interface of hardened MOS capacitors," *IEEE Transactions on Nuclear Science*, vol. 24, no. 6, pp. 2113--2118, Dec 1977.

[90] C. Guerin, V. Huard, and A. Bravaix, "General framework about defect creation at the $Si\text{-}SiO_2$ interface," *Journal of Applied Physics*, vol. 105, no. 11, p. 114513, 2009. [Online]. Available: https://doi.org/10.1063/1.3133096

[91] S. Mahapatra, D. Saha, D. Varghese, and P. B. Kumar, "On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1583--1592, July 2006.

[92] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact modeling and simulation of circuit reliability for 65-nm CMOS technology," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 509--517, Dec 2007.

[93] M. Brox and W. Weber, "Dynamic degradation in MOSFET's. i. the physical effects," *IEEE Transactions on Electron Devices*, vol. 38, no. 8, pp. 1852--1858, 1991.

[94] Y. Liu, X. Jiang, L. Wang, Y. En, and R. Wang, "Distinguishing interfacial hole traps in (110), (100) high-k gate stack," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, March 2019, pp. 1--4.

[95] S. Tyaginov and T. Grasser, "Modeling of hot-carrier degradation: Physics and controversial issues," in *2012 IEEE International Integrated Reliability Workshop Final Report*, Oct 2012, pp. 206--215.

[96] S. Shin, M. A. Wahab, M. Masuduzzaman, M. Si, J. Gu, P. D. Ye, and M. A. Alam, "Origin and implications of hot carrier degradation of gate-all-around nanowire III-V MOSFETs," in *2014 IEEE International Reliability Physics Symposium*, June 2014, pp. 4A.3.1--4A.3.6.

[97] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *Journal of Applied Physics*, vol. 65, no. 6, pp. 2342--2356, 1989. [Online]. Available: https://doi.org/10.1063/1.342824

[98] P. Heremans, G. Van den Bosch, R. Bellens, G. Groeseneken, and H. E. Maes, "Temperature dependence of the channel hot-carrier degradation of n-channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 37, no. 4, pp. 980--993, 1990.

[99] C. R. Crowell and S. M. Sze, "Temperature dependence of avalanche multiplication in semiconductors," *Applied Physics Letters*, vol. 9, no. 6, pp. 242--244, 1966. [Online]. Available: https://doi.org/10.1063/1.1754731

[100] E. Takeda, Y. Nakagome, H. Kume, and S. Asai, "New hot-carrier injection and device degradation in submicron MOSFETs," *IEE Proceedings I - Solid-State and Electron Devices*, vol. 130, no. 3, pp. 144--150, June 1983.

[101] E. Takeda, N. Suzuki, and T. Hagiwara, "Device performance degradation to hot-carrier injection at energies below the $Si\text{-}SiO_2$energy barrier," in *1983 International Electron Devices Meeting*, Dec 1983, pp. 396--399.

[102] E. Maricau and G. Gielen, *CMOS Reliability Overview*. New York, NY: Springer New York, 2013, pp. 15--35. [Online]. Available: https://doi.org/10.1007/978-1-4614-6163-0_2

[103] C. Hu, "Lucky-electron model of channel hot electron emission," in *1979 International Electron Devices Meeting*, Dec 1979, pp. 22--25.

[104] Chenming Hu, Simon C. Tam, Fu-Chieh Hsu, Ping-Keung Ko, Tung-Yi Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement," *IEEE Transactions on Electron Devices*, vol. 32, no. 2, pp. 375--385, Feb 1985.

[105] Simon Tam, Ping-Keung Ko, and Chenming Hu, "Lucky-electron model of channel hot-electron injection in MOSFET'S," *IEEE Transactions on Electron Devices*, vol. 31, no. 9, pp. 1116--1125, Sep. 1984.

[106] T. Brozek, D. Hahn, and C. R. Viswanathan, "Anomalous degradation of MOS structures in substrate hot electron injection experiments," *Microelectronic Engineering*, vol. 28, no. 1, pp. 337 -- 340, 1995, insulating Films on Semiconductors. [Online]. Available: http://www.sciencedirect.com/science/article/pii/016793179500071F

[107] E. Takeda, *IEE Proceedings I (Solid-State and Electron Devices)*, vol. 131, pp. 153--162(9), October 1984. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/ip-i-1.1984.0041

[108] S. Tyaginov, *Physics-Based Modeling of Hot-Carrier Degradation*. Cham: Springer International Publishing, 2015, pp. 105--150. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_4

[109] S. E. Rauch and F. Guarin, *The Energy Driven Hot Carrier Model*. Cham: Springer International Publishing, 2015, pp. 29--56. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_2

[110] K. Hess, L. Register, W. McMahon, B. Tuttle, O. Aktas, U. Ravaioli, J. Lyding, and I. Kizilyalli, "Theory of channel hot-carrier degradation in MOSFETs," *Physica B: Condensed Matter*, vol. 272, no. 1, pp. 527 -- 531, 1999. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0921452699003634

[111] K. Hess, A. Haggag, W. McMahon, K. Cheng, J. Lee, and J. Lyding, "The physics of determining chip reliability," *IEEE Circuits and Devices Magazine*, vol. 17, no. 3, pp. 33--38, 2001.

[112] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. Lyding, "The effects of a multiple carrier model of interface trap generation on lifetime extraction for MOSFETs," 2002, pp. 576--579. [Online]. Available: https://briefs.techconnect.org/papers/the-effect-of-a-multiple-carrier-model-of-interface-trap-generation-on-lifetime-extraction-for-mosfets/

[113] W. McMahon, A. Haggag, and K. Hess, "Reliability scaling issues for nanoscale devices," *IEEE Transactions on Nanotechnology*, vol. 2, no. 1, pp. 33--38, 2003.

[114] H. Kamrani, D. Jabs, V. d'Alessandro, N. Rinaldi, T. Jacquet, C. Maneux, T. Zimmer, K. Aufinger, and C. Jungemann, "Microscopic hot-carrier degradation modeling of SiGe HBTs under stress conditions close to the SOA limit," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 923--929, 2017.

[115] O. Penzin, A. Haggag, W. McMahon, E. Lyumkis, and K. Hess, "Mosfet degradation kinetics and its simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 6, pp. 1445--1450, 2003.

[116] S. E. Rauch, F. J. Guarin, and G. LaRosa, "Impact of e-e scattering to the hot carrier degradation of deep submicron NMOSFETs," *IEEE Electron Device Letters*, vol. 19, no. 12, pp. 463--465, Dec 1998.

[117] S. E. Rauch, G. La Rosa, and F. J. Guarin, "Role of e-e scattering in the enhancement of channel hot carrier degradation of deep-submicron NMOSFETs at high v/sub gs/ conditions," *IEEE Transactions on Device and Materials Reliability*, vol. 1, no. 2, pp. 113--119, June 2001.

[118] S. E. Rauch and G. La Rosa, "The energy driven paradigm of NMOSFET hot carrier effects," in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.*, April 2005, pp. 708--709.

[119] T.-C. Shen, C. Wang, G. Abeln, J. Tucker, J. Lyding, P. Avouris, and R. Walkup, "Atomic-scale desorption through electronic and vibrational excitation mechanisms," *Science*, vol. 268, no. 5217, pp. 1590--1592, 1995.

[120] A. Bravaix, V. Huard, F. Cacho, X. Federspiel, and D. Roy, *Hot-Carrier Degradation in Decananometer CMOS Nodes: From an Energy-Driven to a Unified Current Degradation Modeling by a Multiple-Carrier Degradation Process*. Cham: Springer International Publishing, 2015, pp. 57--103. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_3

[121] Y. M. Randriamihaja, V. Huard, X. Federspiel, A. Zaka, P. Palestri, D. Rideau, D. Roy, and A. Bravaix, "Microscopic scale characterization and modeling of transistor degradation under hc stress," *Microelectronics Reliability*, vol. 52, no. 11, pp. 2513 -- 2520, 2012. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271412001229

[122] C. Guerin, V. Huard, and A. Bravaix, "The energy-driven hot-carrier degradation modes of nMOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 2, pp. 225--235, June 2007.

[123] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. M. Roux, and E. Vincent, "Hot-carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 531--548.

[124] S. Tyaginov, I. Starkov, C. Jungemann, H. Enichlmair, J. Park, and T. Grasser, "Impact of the carrier distribution function on hot-carrier degradation modeling," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, Sep. 2011, pp. 151--154.

[125] M. Jech, S. Tyaginov, B. Kaczer, J. Franco, D. Jabs, C. Jungemann, M. Waltl, and T. Grasser, "First-principles parameter-free modeling of n- and p-fet hot-carrier degradation," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec 2019, pp. 24.1.1--24.1.4.

[126] M. Jech, B. Ullmann, G. Rzepa, S. Tyaginov, A. Grill, M. Waltl, D. Jabs, C. Jungemann, and T. Grasser, "Impact of mixed negative bias temperature instability and hot carrier stress on MOSFET characteristics-part ii: Theory," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 241--248, Jan 2019.

[127] M. Jech, A.-M. El-Sayed, S. Tyaginov, A. L. Shluger, and T. Grasser, "*ab initio* treatment of silicon-hydrogen bond rupture at si/sio_2 interfaces," *Phys. Rev. B*, vol. 100, p. 195302, Nov 2019. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.100.195302

[128] M. Jech, G. Rott, H. Reisinger, S. Tyaginov, G. Rzepa, A. Grill, D. Jabs, C. Jungemann, M. Waltl, and T. Grasser, "Mixed hot-carrier/bias temperature instability degradation regimes in full <italic>V</italic>_G, <italic>V</italic>_D bias space: Implications and peculiarities," *IEEE Transactions on Electron Devices*, vol. 67, no. 8, pp. 3315--3322, 2020.

[129] S. Tyaginov, A. Grill, M. Vandemaele, T. Grasser, G. Hellings, A. Makarov, M. Jech, D. Linten, and B. Kaczer, "A compact physics analytical model for hot-carrier degradation," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, pp. 1--7.

[130] G. G. Harman, R. L. Raybold, and O. L. Meyer, "Direct observation of charge storage in the surface states of silicon," *Journal of Applied Physics*, vol. 34, no. 2, pp. 380--383, 1963. [Online]. Available: https://doi.org/10.1063/1.1702616

[131] D. R. Kerr, J. S. Logan, P. J. Burkhardt, and W. A. Pliskin, "Stabilization of SiO2 passivation layers with P2O5," *IBM Journal of Research and Development*, vol. 8, no. 4, pp. 376--384, 1964.

[132] H. Kükner, S. Khan, P. Weckx, P. Raghavan, S. Hamdioui, B. Kaczer, F. Catthoor, L. Van der Perre, R. Lauw-

ereins, and G. Groeseneken, "Comparison of reaction-diffusion and atomistic trap-based BTI models for logic gates," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 182--193, 2014.

[133] J. H. Stathis, S. Mahapatra, and T. Grasser, "Controversial issues in negative bias temperature instability," *Microelectronics Reliability*, vol. 81, pp. 244 -- 251, 2018. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271417305991

[134] N. Khoshavi, R. A. Ashraf, R. F. DeMara, S. Kiamehr, F. Oboril, and M. B. Tahoori, "Contemporary CMOS aging mitigation techniques: Survey, taxonomy, and methods," *Integration, the VLSI Journal*, vol. 59, pp. 10 -- 22, 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167926017301876

[135] T. Yamamoto, K. Uwasawa, and T. Mogami, "Bias temperature instability in scaled p+ polysilicon gate p-MOSFET's," *IEEE Transactions on Electron Devices*, vol. 46, no. 5, pp. 921--926, May 1999.

[136] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modelling," *Microelectronics Reliability*, vol. 46, no. 1, pp. 1 -- 23, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271405000351

[137] M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, "Dynamic recovery of negative bias temperature instability in p-type metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 83, no. 8, pp. 1647--1649, 2003. [Online]. Available: https://doi.org/10.1063/1.1604480

[138] M. Denais, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, A. Bravaix, V. Huard, and F. Perrier, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, 2004, pp. 109--112.

[139] H. Reisinger, U. Brunner, W. Heinrigs, W. Gustin, and C. Schlunder, "A comparison of fast methods for measuring nbti degradation," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 531--539, 2007.

[140] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004--2014, 1977.

[141] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for pmosfets," in *IEEE International Electron Devices Meeting 2003*, Dec 2003, pp. 14.4.1--14.4.4.

[142] M. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Reliability*, vol. 45, no. 1, pp. 71 -- 81, 2005. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271404001751

[143] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam, "Recent issues in negative-bias temperature instability: Initial degradation, field dependence of interface trap generation, hole trapping effects, and relaxation," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2143--2154, Sept 2007.

[144] S. Kumar, R. Anandkrishnan, N. Parihar, and S. Mahapatra, "A stochastic framework for the time kinetics of interface and bulk oxide traps for BTI, SILC, and TDDB in MOSFETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4741--4748, 2020.

[145] A. T. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, and S. Krishnan, "Negative bias temperature instability mechanism: The role of molecular hydrogen," *Applied Physics Letters*, vol. 88, no. 15, p. 153518, 2006. [Online]. Available: https://doi.org/10.1063/1.2191828

[146] T. Grasser, K. Rott, H. Reisinger, M. Waltl, P. Wagner, F. Schanovsky, W. Goes, G. Pobegen, and B. Kaczer, "Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI," in *2013 IEEE International Electron Devices Meeting*, 2013, pp. 15.5.1--15.5.4.

[147] T. Grasser, W. Gos, V. Sverdlov, and B. Kaczer, "The universality of NBTI relaxation and its implications for modeling and characterization," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, April 2007, pp. 268--280.

[148] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. Wagner, F. Schanovsky, J. Franco, M. T. Toledano Luque, and M. Nelhiebel, "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3652--3666, 2011.

[149] W. Goes, Y. Wimmer, A.-M. El-Sayed, G. Rzepa, M. Jech, A. Shluger, and T. Grasser, "Identification of oxide defects in semiconductor devices: A systematic approach linking dft to rate equations and experimental evidence," *Microelectronics Reliability*, vol. 87, pp. 286--320, 2018. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271417305796

[150] Y. Kim, S. Han, H. Kang, and B. Kang, "Recovery of negative bias temperature instability induced degradation of p-MOSFETs with SiON gate dielectric," *Microelectronic Engineering*, vol. 85, no. 9, pp. 1932 -- 1936, 2008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931708003201

[151] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability [pmosfets]," in *IEEE International Electron Devices Meeting 2003*, Dec 2003, pp. 14.3.1--14.3.4.

[152] H. Reisinger, T. Grasser, K. Ermisch, H. Nielen, W. Gustin, and C. Schlünder, "Understanding and modeling AC BTI," in *2011 International Reliability Physics Symposium*, April 2011, pp. 6A.1.1--6A.1.8.

[153] K. Joshi, S. Mukhopadhyay, N. Goel, and S. Mahapatra, "A consistent physical framework for n and p BTI in HKMG MOSFETs," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, April 2012, pp. 5A.3.1--5A.3.10.

[154] V. Huard, "Two independent components modeling for negative bias temperature instability," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 33--42.

[155] B. Djezzar, A. Benabdelmoumene, B. Zatout, D. Messaoud, A. Chenouf, H. Tahi, M. Boubaaya, and H. Timlelt, "Recovery investigation of NBTI-induced traps in n-MOSFET devices," *Microelectronics Reliability*, vol. 110, p. 113703, 2020. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271420300482

[156] Y. Yonamoto, "Recovery behavior in negative bias temperature instability," *Microelectronics Reliability*, vol. 54, no. 3, pp. 520 -- 528, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271413004733

[157] T. Grasser, T. Aichinger, G. Pobegen, H. Reisinger, P.-J. Wagner, J. Franco, M. Nelhiebel, and B. Kaczer, "The 'permanent' component of nbti: Composition and annealing," in *2011 International Reliability Physics Symposium*, 2011, pp. 6A.2.1--6A.2.9.

[158] T. Grasser, M. Waltl, Y. Wimmer, W. Goes, R. Kosik, G. Rzepa, H. Reisinger, G. Pobegen, A. El-Sayed, A. Shluger, and B. Kaczer, "Gate-sided hydrogen release as the origin of "permanent" NBTI degradation: From single defects to lifetimes," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 20.1.1--20.1.4.

[159] D. L. Griscom, "Diffusion of radiolytic molecular hydrogen as a mechanism for the post-irradiation buildup of interface states in SiO_2-on-Si structures," *Journal of Applied Physics*, vol. 58, no. 7, pp. 2524--2533, 1985. [Online]. Available: https://doi.org/10.1063/1.335931

[160] N. Parihar, U. Sharma, S. Mukhopadhyay, N. Goel, A. Chaudhary, R. Rao, and S. Mahapatra, "Resolution of disputes concerning the physical mechanism and DC/AC stress/recovery modeling of negative bias temperature instability (NBTI) in p-MOSFETs," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. XT--1.1--XT--1.11.

[161] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, vol. 98, no. 12, p. 121301, 2005. [Online]. Available: https://doi.org/10.1063/1.2147714

[162] J. W. McPherson and H. C. Mogul, "Underlying physics of the thermochemical e model in describing low-field time-dependent dielectric breakdown in SiO2 thin films," *Journal of Applied Physics*, vol. 84, no. 3, pp. 1513--1523, 1998. [Online]. Available: https://doi.org/10.1063/1.368217

[163] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes, "New insights in the relation between electron trap generation and the statistical properties of oxide breakdown," *IEEE Transactions on Electron Devices*, vol. 45, no. 4, pp. 904--911, 1998.

[164] J. H. Stathis, "Percolation models for gate oxide breakdown," *Journal of Applied Physics*, vol. 86, no. 10, pp. 5757--5766, 1999. [Online]. Available: https://doi.org/10.1063/1.371590

[165] G. S. Ristic, "Influence of ionizing radiation and hot carrier injection on metal-oxide-semiconductor transistors," *Journal of Physics D: Applied Physics*, vol. 41, no. 2, p. 023001, 2008. [Online]. Available: http://stacks.iop.org/0022-3727/41/i=2/a=023001

[166] Moazzami and Chenming Hu, "Stress-induced current in thin silicon dioxide films," in *1992 International Technical Digest on Electron Devices Meeting*, Dec 1992, pp. 139--142. [Online]. Available: https://ieeexplore.ieee.org/document/307327

[167] J. De Blauwe, R. Degraeve, R. Bellens, J. Van Houdt, P. Roussel, G. Groeseneken, and H. E. Maes, "Study of DC stress induced leakage current (SILC) and its dependence on oxide nitridation," in *ESSDERC '96: Proceedings of the 26th European Solid State Device Research Conference*, Sep. 1996, pp. 361--364. [Online]. Available: https://ieeexplore.ieee.org/document/5437074

[168] G. Lee, C. Kim, M. Yoo, J. Hur, and Y. Choi, "Effect of off-state stress on gate-induced drain leakage by interface traps in buried-gate fets," *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5126--5132, Dec 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8891777?source=tocalert&dld=dXR3ZW50Z55ubA%3D%3D

[169] J. Park, D. Moon, M. Seol, C. Kim, C. Jeon, H. Bae, T. Bang, and Y. Choi, "Self-curable gate-all-around MOSFETs using electrical annealing to repair degradation induced from hot-carrier injection," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 910--915, March 2016.

[170] C. Jeon, C. Kim, J. Park, U. Jeong, B. Lee, K. R. Kim, and Y. Choi, "Lf noise analysis for trap recovery in gate oxides using built-in joule heater," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5081--5086, Dec 2017.

[171] E. Pop, R. Dutton, and K. Goodson, "Thermal analysis of ultra-thin body device scaling [soi and finfet devices]," in *IEEE International Electron Devices Meeting 2003*, 2003, pp. 36.6.1--36.6.4.

[172] D. S. Lee, D. Varghese, A. Sonnet, J. Joh, A. Venugopal, and S. Krishnan, "Impact of self-heating effect in hot carrier injection modeling," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 315--318. [Online]. Available: https://ieeexplore.ieee.org/document/8393666

[173] C. Prasad, "A review of self-heating effects in advanced CMOS technologies," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4546--4555, Nov 2019.

[174] H. Jiang, S. Shin, X. Liu, X. Zhang, and M. A. Alam, "Characterization of self-heating leads to universal scaling of HCI degradation of multi-fin SOI finfets," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, April 2016, pp. 2A--3--1--2A--3--7. [Online]. Available: https://ieeexplore.ieee.org/document/7574506

[175] S. H. Shin, S. . Kim, S. Kim, H. Wu, P. D. Ye, and M. A. Alam, "Substrate and layout engineering to suppress self-heating in floating body transistors," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 15.7.1--15.7.4.

[176] W. Zhang, T.-L. Wang, Y.-H. Huang, T.-T. Cheng, S.-Y. Chen, Y.-Y. Li, C.-H. Hsu, C.-J. Lai, W.-K. Yeh, and Y.-L. Yang, "Influence of fin number on hot-carrier injection stress induced degradation in bulk finfets," *Microelectronics Reliability*, vol. 67, pp. 89 -- 93, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271416304012

[177] K. Eriguchi and K. Ono, "Quantitative and comparative characterizations of plasma process-induced damage in advanced metal-oxide-semiconductor devices," *Journal of Physics D: Applied Physics*, vol. 41, no. 2, p. 024002, jan 2008. [Online]. Available: https://doi.org/10.1088/0022-3727/41/2/024002

[178] K. Eriguchi, M. Kamei, Y. Takao, and K. Ono, "High-k MOSFET performance degradation by plasma process-induced charging damage - impacts on device parameter variation," in *2012 IEEE International Integrated Reliability Workshop Final Report*, 2012, pp. 80--84.

[179] K. Eriguchi and K. Ono, "Impacts of plasma process-induced damage on MOSFET parameter variability and reliability," *Microelectronics Reliability*, vol. 55, no. 9, pp. 1464 -- 1470, 2015, proceedings of the 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271415300913

[180] W. M. Greene, J. B. Kruger, and G. Kooi, "Magnetron etching of polysilicon: Electrical damage," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 9, no. 2, pp. 366--369, 1991. [Online]. Available: https://avs.scitation.org/doi/abs/10.1116/1.585577

[181] D. J. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," *Journal of Applied Physics*, vol. 78, no. 6, pp. 3883--3894, 1995. [Online]. Available: https://doi.org/10.1063/1.359905

[182] A. T. Krishnan, V. Reddy, and S. Krishnan, "Impact of charging damage on negative bias temperature instability," in *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, 2001, pp. 39.3.1--39.3.4.

[183] T. Yunogami, T. Mizutani, K. Suzuki, and S. Nishimatsu, "Radiation damage in SiO2/si induced by VUV photons," *Japanese Journal of Applied Physics*, vol. 28, no. Part 1, No. 10, pp. 2172--2176, oct 1989. [Online]. Available: https://doi.org/10.1143/jjap.28.2172

[184] H. Brut and R. M. D. A. Velghe, "Contribution to the characterization of the hump effect in MOSFET sub-micronic technologies," in *ICMTS 1999. Proceedings of 1999 International Conference on Microelectronic Test Structures (Cat. No.99CH36307)*, 1999, pp. 188--193.

[185] J. Rafí, E. Simoen, K. Hayama, A. Mercha, F. Campabadal, H. Ohyama, and C. Claeys, "Hot-carrier-induced degradation of drain current hysteresis and transients in thin gate oxide floating body partially depleted SOI NMOSFETs," *Microelectronics Reliability*, vol. 46, no. 9, pp. 1657 -- 1663, 2006, proceedings of the 17th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. Wuppertal, Germany 3rd-6th October 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271406002356

[186] J. Franco, B. Kaczer, G. Eneman, P. J. Roussel, M. Cho, J. Mitard, L. Witters, T. Y. Hoffmann, G. Groeseneken, F. Crupi, and T. Grasser, "On the recoverable and permanent components of hot carrier and NBTI in Si pmosfets and their implications in $Si_{0.45}Ge_{0.55}$ pmosfets," in *2011 International Reliability Physics Symposium*, April 2011, pp. 6A.4.1--6A.4.6.

[187] J. Han, M. Kebaili, and M. Meyyappan, "System on microheater for on-chip annealing of defects generated by hot-carrier injection, bias temperature instability, and ionizing radiation," *IEEE Electron Device Letters*, vol. 37, no. 12, pp. 1543--1546, Dec 2016.

[188] G. Pobegen, *Recovery from Hot Carrier Induced Degradation Through Temperature Treatment*. Cham: Springer International Publishing, 2015, pp. 221--230. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_7

[189] B. Hallam, A. Herguth, P. Hamer, N. Nampalli, S. Wilking, M. Abbott, S. Wenham, and G. Hahn, "Eliminating light-induced degradation in commercial p-type czochralski silicon solar cells," *Applied Sciences*, vol. 8, no. 1, 2018. [Online]. Available: http://www.mdpi.com/2076-3417/8/1/10

[190] L. Åke Ragnarsson and P. Lundgren, "Electrical characterization of $P_b$centers in (100)Si-SiO_2 structures: The influence of surface potential on passivation during post metallization anneal," *Journal of Applied Physics*, vol. 88, no. 2, pp. 938--942, 2000. [Online]. Available: https://doi.org/10.1063/1.373759

[191] H. T. Lue, P. Y. Du, C. P. Chen, W. C. Chen, C. C. Hsieh, Y. H. Hsiao, Y. H. Shih, and C. Y. Lu, "Radically extending the cycling endurance of flash memory (to 100m cycles) by using built-in thermal annealing to self-heal the stress-induced damage," pp. 9.1.1--9.1.4, Dec 2012.

[192] D. I. Moon, J. Y. Park, J. W. Han, G. J. Jeon, J. Y. Kim, J. Moon, M. L. Seol, C. K. Kim, H. C. Lee, M. Meyyappan, and Y. K. Choi, "Sustainable electronics for nano-spacecraft in deep space missions," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 31.8.1--31.8.4.

[193] B. J. Hallam, P. G. Hamer, S. Wang, L. Song, N. Nampalli, M. D. Abbott, C. E. Chan, D. Lu, A. M. Wenham, L. Mai, N. Borojevic, A. Li, D. Chen, M. Y. Kim, A. Azmi, and S. Wenham, "Advanced hydrogenation of dislocation clusters and boron-oxygen defects in silicon solar cells," *Energy Procedia*, vol. 77, pp. 799 -- 809, 2015, 5th International Conference on Silicon Photovoltaics, SiliconPV 2015. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1876610215008814

[194] B. Hallam, D. Chen, M. Kim, B. Stefani, B. Hoex, M. Abbott, and S. Wenham, "The role of hydrogenation and gettering in enhancing the efficiency of next-generation Si solar cells: An industrial perspective," *physica status solidi (a)*, vol. 214, no. 7, 7 2017. [Online]. Available: https://doi.org/10.1002/pssa.201700305

[195] K. Sakurai, H. Tomita, S. Tokuda, D. Schmitz, K. Ogawa, H. Shibata, and A. Masuda, "Rapid recovery of cigs solar cells from pid stress with light soaking," in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 2000--2002.

[196] D. L. Staebler and C. R. Wronski, "Reversible conductivity changes in discharge-produced amorphous Si," *Applied Physics Letters*, vol. 31, no. 4, pp. 292--294, 1977. [Online]. Available: https://doi.org/10.1063/1.89674

[197] F. E. Pagaduan, A. Hamada, C. Y. Yang, and E. Takeda, "Hot-carrier detrapping mechanisms in MOS devices," *Japanese Journal of Applied Physics*, vol. 28, no. 11A, p. L2047, 1989. [Online]. Available: http://stacks.iop.org/1347-4065/28/i=11A/a=2047

[198] P. Hehenberger, T. Aichinger, T. Grasser, W. Gos, O. Triebl, B. Kaczer, and M. Nelhiebel, "Do NBTI-induced interface states show fast recovery? A study using a corrected on-the-fly charge-pumping measurement technique," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 1033--1038.

[199] A. Sharma, S. G. J. Mathijssen, E. C. P. Smits, M. Kemerink, D. M. de Leeuw, and P. A. Bobbert, "Proton migration mechanism for operational instabilities in organic field-effect transistors," *Phys. Rev. B*, vol. 82, p. 075322, Aug 2010. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.82.075322

[200] G. Pobegen, S. Tyaginov, M. Nelhiebel, and T. Grasser, "Observation of normally distributed energies for interface trap recovery after hot-carrier degradation," *IEEE Electron Device Letters*, vol. 34, no. 8, pp. 939--941, Aug 2013. [Online]. Available: https://ieeexplore.ieee.org/document/6553102

[201] G. Lee, C. Kim, J. Park, T. Bang, H. Bae, S. Kim, S. Ryu, and Y. Choi, "A novel technique for curing hot-carrier-induced damage by utilizing the forward current of the pn-junction in a MOSFET," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1012--1014, Aug 2017.

[202] G.-B. Lee, C.-K. Kim, T. Bang, M.-S. Yoo, J.-Y. Park, and Y.-K. Choi, "Analysis of damage curing in a MOSFET with joule heat generated by forward junction current at the source and drain," *Microelectronics Reliability*, vol. 104, p. 113548, 2020. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271419302148

[203] J. Park, J. Hur, and Y. Choi, "Demonstration of a curable nanowire finfet using punchthrough current to repair hot-carrier damage," *IEEE Electron Device Letters*, vol. 39, no. 2, pp. 180--183, Feb 2018.

[204] J. Park, D. Moon, G. Lee, and Y. Choi, "Curing of aged gate dielectric by the self-heating effect in MOSFETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 777--788, 2020.

[205] C. Gupta, A. Gupta, S. Tuli, E. Bury, B. Parvais, and A. Dixit, "Characterization and modeling of hot carrier degradation in n-channel gate-all-around nanowire FETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 1, pp. 4--10, Jan 2020.

[206] M. J. de Jong, C. Salm, and J. Schmitz, "Towards understanding recovery of hot-carrier induced degradation," *Microelectronics Reliability*, vol. 88-90, pp. 147 -- 151, 2018, 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2018). [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271418306073

[207] B. Ullmann, M. Jech, K. Puschkarsky, G. A. Rott, M. Waltl, Y. Illarionov, H. Reisinger, and T. Grasser, "Impact of mixed negative bias temperature instability and hot carrier stress on MOSFET characteristics—part i: Experimental," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 232--240, 2019.

[208] A. A. Katsetos, "Negative bias temperature instability (nbti) recovery with bake," *Microelectronics Reliability*, vol. 48, no. 10, pp. 1655 -- 1659, 2008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S002627140800098X

[209] Y. Shika, T. Bessho, Y. Okabe, H. Ogata, S. Kamo, K. Kitahara, and A. Hara, "Impact of the hydrogenation process on the performance of self-aligned metal double-gate low-temperature polycrystalline-silicon thin-film transistors," *Japanese Journal of Applied Physics*, vol. 52, no. 3S, p. 03BB01, 2013. [Online]. Available: http://stacks.iop.org/1347-4065/52/i=3S/a=03BB01

[210] J. E. Shelby, "Molecular diffusion and solubility of hydrogen isotopes in vitreous silica," *Journal of Applied Physics*, vol. 48, no. 8, pp. 3387--3394, 1977. [Online]. Available: https://doi.org/10.1063/1.324180

[211] P. Hashemi and T. Ando, "Chapter 6 - sige devices," in *High Mobility Materials for CMOS Applications*, ser. Woodhead Publishing Series in Electronic and Optical Materials, N. Collaert, Ed. Woodhead Publishing, 2018, pp. 205--229. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780081020616000069

[212] Z. Yu, J. Zhang, R. Wang, S. Guo, C. Liu, and R. Huang, "New insights into the hot carrier degradation (HCD) in FinFET: New observations, unified compact model, and impacts on circuit reliability," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 7.2.1--7.2.4. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/8268344

[213] J. F. Zhang, C. Z. Zhao, G. Groeseneken, R. Degraeve, J. N. Ellis, and C. D. Beech, "Hydrogen induced positive charge generation in gate oxides," *Journal of Applied Physics*, vol. 90, no. 4, pp. 1911--1919, 2001. [Online]. Available: https://doi.org/10.1063/1.1384860

[214] M. J. de Jong, C. Salm, and J. Schmitz, "Effect of Ambient on the Recovery of Hot-Carrier Degraded Devices," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, pp. 1--6.

[215] A. J. Hof, A. Kovalgin, R. van Schaijk, W. M. Baks, and J. Schmitz, "Gate oxide reliability and deuterated CMOS processing," in *IEEE International Integrated Reliability Workshop Final Report, 2004.*, Oct 2004, pp. 7--10.

[216] J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing," *Applied Physics Letters*, vol. 68, no. 18, pp. 2526--2528, 1996. [Online]. Available: https://doi.org/10.1063/1.116172

[217] M. J. de Jong, C. Salm, and J. Schmitz, "Observations on the recovery of hot carrier degradation of hydrogen/deuterium passivated NMOSFETs," *Microelectronics Reliability*, vol. 76-77, pp. 136 -- 140, 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271417303220

[218] A. Y. Kovalgin, M. Yang, S. Banerjee, R. O. Apaydin, A. A. I. Aarnink, S. Kinge, and R. A. M. Wolters, "Hot-wire assisted ALD: A study powered by in situ spectroscopic ellipsometry," *Advanced Materials Interfaces*, vol. 4, no. 18, p. 1700058, 2017. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/admi.201700058

[219] H. Y. Wong, S. Motzny, V. Moroz, S. Mishra, and S. Mahapatra, "Finfet NBTI degradation reduction and recovery enhancement through hydrogen incorporation and self-heating," in *2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2017, pp. 101--104.

[220] M. J. de Jong, C. Salm, and J. Schmitz, "Recovery after hot-carrier injection: Slow versus fast traps," *Microelectronics Reliability*, vol. 100-101, p. 113318, 2019, 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2019). [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271419304615

[221] Z. Yu, Z. Sun, R. Wang, J. Zhang, and R. Huang, "Hot carrier degradation-induced dynamic variability in finfets: Experiments and modeling," *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1517--1522, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9025752

[222] B. Kaczer, T. Grasser, J. Roussel, J. Martin-Martinez, R. O'Connor, B. J. O'Sullivan, and G. Groeseneken, "Ubiquitous relaxation in BTI stressing - new evaluation and insights," in *2008 IEEE International Reliability Physics Symposium*, April 2008, pp. 20--27.

[223] G. X. Duan, J. Hatchtel, X. Shen, E. X. Zhang, C. X. Zhang, B. R. Tuttle, D. M. Fleetwood, R. D. Schrimpf, R. A. Reed, J. Franco, D. Linten, J. Mitard, L. Witters, N. Collaert, M. F. Chisholm, and S. T. Pantelides, "Activation energies for oxide- and interface-trap charge generation due to negative-bias temperature stress of Si-capped SiGe-pmosfets," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 3, pp. 352--358, Sep. 2015.

[224] T. Aichinger, M. Nelhiebel, and T. Grasser, "Unambiguous identification of the NBTI recovery mechanism using ultra-fast temperature changes," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 2--7.

[225] B. Kaczer, T. Grasser, R. Fernandez, and G. Groeseneken, "Toward understanding the wide distribution of time scales in negative bias temperature instability," *ECS Transactions*, vol. 6, no. 3, pp. 265--281, 2007. [Online]. Available: http://ecst.ecsdl.org/content/6/3/265.abstract

[226] T. Grasser, T. Aichinger, H. Reisinger, J. Franco, P.-J. Wagner, M. Nelhiebel, C. Ortolland, and B. Kaczer, "On the 'permanent' component of NBTI," in *2010 IEEE International Integrated Reliability Workshop Final Report*, 2010, pp. 2--7.

[227] C. Bénard, G. Math, P. Fornara, J.-L. Ogier, and D. Goguenheim, "Influence of various process steps on the reliability of PMOSFETs submitted to negative bias temperature instabilities," *Microelectronics Reliability*, vol. 49, no. 9, pp. 1008--1012, 2009, 20th European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271409002261

[228] A. J. Lelis, T. R. Oldham, H. E. Boesch, and F. B. McLean, "The nature of the trapped hole annealing process," *IEEE Transactions on Nuclear Science*, vol. 36, no. 6, pp. 1808--1815, Dec 1989.

[229] D. Ang, C. Ling, and Y. Yeow, "Study of hot-carrier degradation in submicrometer ldd NMOSFET's from 1f noise and charge pumping current measurements at different temperature anneals," *Microelectronic Engineering*, vol. 28, no. 1, pp. 257 -- 260, 1995, insulating Films on Semiconductors. [Online]. Available: http://www.sciencedirect.com/science/article/pii/016793179500054C

[230] B. S. Doyle and G. J. Dunn, "Recovery of hot-carrier damage in reoxidized nitrided oxide MOSFET's," *IEEE Electron Device Letters*, vol. 13, no. 1, pp. 38--40, Jan 1992.

[231] P. Cuevas, "A simple explanation for the apparent relaxation effect associated with hot-carrier phenomenon in MOSFETs," *IEEE Electron Device Letters*, vol. 9, no. 12, pp. 627--629, Dec 1988.

[232] S.-T. Chang, N. M. Johnson, and S. A. Lyon, "Capture and tunnel emission of electrons by deep levels in ultrathin nitrided oxides on silicon," *Applied Physics Letters*, vol. 44, no. 3, pp. 316--318, 1984. [Online]. Available: https://doi.org/10.1063/1.94737

[233] T. Ong, M. Levi, P. Ko, and C. Hu, "Recovery of threshold voltage after hot-carrier stressing," *IEEE Transactions*

on Electron Devices, vol. 35, no. 7, pp. 978--984, July 1988.

[234] D. Vuillaume and A. Bravaix, "Charging and discharging properties of electron traps created by hot-carrier injections in gate oxide of n-channel metal oxide semiconductor field effect transistor," *Journal of Applied Physics*, vol. 73, no. 5, pp. 2559--2563, 1993. [Online]. Available: https://doi.org/10.1063/1.353065

[235] M. Garci, J. Kammerer, and L. Hebrard, "Compact modeling and electro-thermal simulation of hot carriers effect in analog circuits," in *2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)*, June 2014, pp. 125--128.

[236] D. Danković, I. M. V. Davidović, S. Djorić-Veljković, S. Golubović, and N. Stojadinović, "Negative bias temperature instability in n-channel power VDMOSFETs," *Microelectronics Reliability*, vol. 48, no. 8, pp. 1313--1317, 2008, 19th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008). [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271408002023

[237] K. Zhao, J. H. Stathis, A. Kerber, and E. Cartier, "PBTI relaxation dynamics after AC vs. DC stress in high-k/metal gate stacks," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 50--54.

[238] Y. L. Li, K. S. Chang-Liao, C. C. Li, C. H. Huang, S. F. Tsai, C. Y. Li, Z. Q. Hong, and H. K. Fang, "Electrical and reliability characteristics of finfets with high-k gate stack and plasma treatments," *IEEE Transactions on Electron Devices*, vol. 68, no. 1, pp. 4--9, 2021.

[239] K. P. MacWilliams, L. F. Halle, and T. C. Zietlow, "Improved hot-carrier resistance with fluorinated gate oxides," *IEEE Electron Device Letters*, vol. 11, no. 1, pp. 3--5, Jan 1990.

[240] C. Salm, A. Hof, F. Kuper, and J. Schmitz, "Reduced temperature dependence of hot carrier degradation in deuterated NMOSFETs," *Microelectronics Reliability*, vol. 46, no. 9, pp. 1617 -- 1622, 2006, proceedings of the 17th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. Wuppertal, Germany 3 - 6 October 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271406002629

[241] I. C. Kizilyalli, J. W. Lyding, and K. Hess, "Deuterium post-metal annealing of MOSFET's for improved hot carrier reliability," *IEEE Electron Device Letters*, vol. 18, no. 3, pp. 81--83, March 1997.

[242] A. J. Hof, "Deuterium in the gate dielectric of CMOS devices," Ph.D. dissertation, Univ. of Twente, Enschede, October 2004. [Online]. Available: http://doc.utwente.nl/67533/

[243] A. J. Hof, E. Hoekstra, A. Y. Kovalgin, R. van Schaijk, W. M. Baks, and J. Schmitz, "The impact of deuterated CMOS processing on gate oxide reliability," *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 2111--2115, Sept 2005. [Online]. Available: https://ieeexplore.ieee.org/document/1499103

[244] J. C. King and C. Hu, "Effect of low and high temperature anneal on process-induced damage of gate oxide," *IEEE Electron Device Letters*, vol. 15, no. 11, pp. 475--476, Nov 1994.

[245] W. McMahon, Y. Mamy-Randriamihaja, B. Vaidyanathan, T. Nigam, and N. Pimparkar, *From Atoms to Circuits: Theoretical and Empirical Modeling of Hot Carrier Degradation*. Cham: Springer International Publishing, 2015, pp. 3--27. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_1

[246] J. Lee, K. Cheng, Z. Chen, K. Hess, J. Lyding, Y.-K. Kim, H.-S. Lee, Y.-W. Kim, and K.-P. Suh, "Application of high pressure deuterium annealing for improving the hot carrier reliability of CMOS transistors," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 221--223, 2000.

[247] P. Avouris, R. Walkup, A. Rossi, T.-C. Shen, G. Abeln, J. Tucker, and J. Lyding, "STM-induced H atom desorption from Si(100): isotope effects and site selectivity," *Chemical Physics Letters*, vol. 257, no. 1, pp. 148--154, 1996. [Online]. Available: https://www.sciencedirect.com/science/article/pii/0009261496005180

[248] C. G. Van de Walle and W. B. Jackson, "Comment on "reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing" [appl. phys. lett. 68, 2526 (1996)]," *Applied Physics Letters*, vol. 69, no. 16, pp. 2441--2441, 1996. [Online]. Available: https://doi.org/10.1063/1.117664

[249] K. Hess, I. C. Kizilyalli, and J. W. Lyding, "Giant isotope effect in hot electron degradation of metal oxide silicon devices," *IEEE Transactions on Electron Devices*, vol. 45, no. 2, pp. 406--416, Feb 1998.

[250] M. Rafik, X. Garros, G. Ribes, G. Ghibaudo, C. Hobbs, A. Zauner, M. Muller, V. Huard, and C. Ouvrard, "Impact of TiN metal gate on NBTI assessed by interface states and fast transient effect characterization," in *2007 IEEE International Electron Devices Meeting*, Dec 2007, pp. 825--828. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/4419075

[251] S. E. Tyaginov, I. Starkov, H. Enichlmair, J. M. Park, C. Jungemann, and T. Grasser, "Physics-based hot-carrier degradation modeling," *The Electrochemical Society Transactions*, vol. 35, no. 4, pp. 321--352, 2011. [Online]. Available: http://ecst.ecsdl.org/content/35/4/321.abstract

[252] R. Shangqing, YangHong, T. Bo, X. Hao, L. Weichun, T. Zhaoyun, X. Yefeng, X. Jing, W. Dahai, L. Junfeng, Y. Jiang, Z. Chao, C. Dapeng, Y. Tianchun, and W. Wenwu, "Characterization of positive bias temperature instability of NMOSFET with high- k /metal gate last process," *Journal of Semiconductors*, vol. 36, no. 1, p. 014007, 2015. [Online]. Available: https://iopscience.iop.org/article/10.1088/1674-4926/36/1/014007

[253] H. Park and C. R. Helms, "The effect of annealing treatment on the distribution of deuterium in silicon and in silicon oxide systems," *J. Electrochem. Soc.*, vol. 139, no. 7, pp. 2042--2046, 1992.

[254] L. Nuccio, "Diffusion of small molecules in amorphous SiO_2: effects on the properties of the material and on its point defects," Ph.D. dissertation, Palermo, February 2009. [Online]. Available:

http://www1.unipa.it/lamp/NuccioPhDThesis.pdf

[255] M. Vandemaele, J. Franco, S. Tyaginov, G. Groeseneken, and B. Kaczer, "Modeling of repeated FET hot-carrier stress and anneal cycles using Si-H bond dissociation/passivation energy distributions," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 1454--1460, 2021.

[256] A. Chenouf, B. Djezzar, A. Benadelmoumene, H. Tahi, and M. Goudjil, "Reliability analysis of CMOS inverter subjected to AC amp; DC NBTI stresses," in *2014 9th International Design and Test Symposium (IDT)*, Dec 2014, pp. 142--146.

[257] N. Parihar, N. Goel, A. Chaudhary, and S. Mahapatra, "A modeling framework for NBTI degradation under dynamic voltage and frequency scaling," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 946--953, 2016.

[258] N. Parihar, N. Goel, S. Mukhopadhyay, and S. Mahapatra, "BTI analysis tool - modeling of NBTI DC, AC stress and recovery time kinetics, nitrogen impact, and EOL estimation," *IEEE Transactions on Electron Devices*, vol. 65, no. 2, pp. 392--403, 2018.

[259] S. Mukhopadhyay and S. Mahapatra, "An experimental perspective of trap generation under BTI stress," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2092--2097, 2015.

[260] G. Sasse, "Reliability engineering in rf cmos," Ph.D. dissertation, University of Twente, Netherlands, Jul. 2008, http://doc.utwente.nl/59032/.

Appendix: Symbols and Abbreviations

List of Symbols and Constants

A_g	Gate Area	μm^2
C_{dep}	Depletion Capacitance	F
C_{it}	Interface Defect Capacitance	F
C_{ox}	Oxide Capacitance	F
D_0	Diffusion Constant	$cm^2\ s^{-1}$
$E_{a,f/r}$	Forward/Reverse Activation Energy	eV
E_a	Activation Energy	eV
$E_{c/v}$	Conduction/Valence Band Level	eV
E_f	Fermi Level	eV
ϕ_b	Bulk Potential	eV
ϕ_s	Surface Potential	eV
f_{cp}	Charge-Pumping Frequency	Hz
g_m	Transconductance	$A\ V^{-1}$
I_b	Bulk Current	A
I_g	Gate Current	A
I_{cp}	Charge Pumping Current	A
$I_{cp,it/ot/rc}$	Charge Pumping Current due to $N_{it}/N_{ot}/N_{rc}$	A
$I_{d,lin}$	Linear Drain Current	A
$I_{d,sat}$	Saturation Drain Current	A
κ_{Si}	Dielectric Constant Silicon	11.7
κ_{SiO_2}	Dielectric Constant Silicon Dioxide	3.9
κ_{HfO_2}	Dielectric Constant Hafnium Dioxide	25
k_b	Boltzmann constant	$8.617 \cdot 10^{-5}$ eV K^{-1}
$k_{f,0}$	Forward Reaction Rate Constant	cm^{-3}
$k_{r,0}$	Reverse Reaction Rate Constant	cm^{-3}
λ	Mean Free Path	μm
L_g	Gate Length	μm
μ	Charge Carrier Mobility	$cm^2\ V^{-1}\ s^{-1}$
$N_{it/ot}$	Interface/Oxide Defect Density	$cm^2\ s^{-1}$
N_{rc}	Recombination Center Density	$cm^2\ s^{-1}$
P_b	Interface defect	cm^{-2}
P_{H_2}	H_2 ambient pressure	bar
P_{N_2}	N_2 ambient pressure	bar
P_{rf}	RF power	W
q	Elementary Charge	$1.602 \cdot 10^{-19}$ C
SS	Subthreshold Swing	mV/dec
t_{ox}	Gate Oxide Thickness	nm
$t_{c/e}$	Capture/Emission Time	s
t_a	Anneal Time	s
t_s	Stress Time	s
$t_{r/f}$	Rise/Fall Time of a Voltage Pulse	s
T_a	Anneal Temperature	K (°C)

T_{chuck}	Chuck Temperature	K (°C)
T_m	Measurement Temperature	K (°C)
T_s	Stress Temperature	K (°C)
V_a	Voltage Pulse Amplitude	V
V_{fb}	Flat Band Voltage	V
V_t	Threshold Voltage	V
V_{bs}	Bulk-Source Bias	V
V_{ds}	Drain-Source Bias	V
V_{gs}	Gate-Source Bias	V
$V_{gs,l}$	Top Gate-Source Bias of a Pulse	V
$V_{gs,h}$	Bottom Gate-Source Bias of a Pulse	V
W_g	Gate Width	μm

List of Acronyms

CHC	Channel Hot Carrier
CP	Charge Pumping
CV	Capacitance-Voltage (Measurement)
CVS	Constant Voltage Stress
DAHC	Drain Avalanche Hot-Carriers
DB	Dangling Bond
DC	Defect Centered Model
EEDF	Electron Energy Distribution Function
EES	Electron Electron Scattering
ELR	Extraction from the Linear Regime
EOT	Equivalent Oxide Thickness
GST Model	General Simple Thermal Model
HCD	Hot-Carrier Degradation
HCI	Hot-Carrier Injection
EES	Electron-Electron Scattering
II	Impact Ionization
IV	Current-Voltage (Measurement)
MVE	Multi-Vibrational Excitation
LEM	Lucky Electron Model
MSM(AM)	Measurement-Stress-Measurement(-Anneal-Measurement)
NBTI	Negative Bias Temperature Instability
nMOSFET	n-channel Metal-Oxide-Semiconductor Field Effect Transistor
pMOSFET	p-channel Metal-Oxide-Semiconductor Field Effect Transistor
PBTI	Positive Bias Temperature Instability
PID	Plasma Induced Damage
PMA/POA	Post Metal/Oxide Anneal
RD	Radiation Damage
R&D	Reaction-Diffusion Model
RT	Room Temperature ($T \approx 22 - 25$ °C)
SILC	Stress Induced Leakage Current
TDDB	Time Dependent Dielectric Breakdown

List of publications

Journal Papers and Proceedings

1. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, "Observations on the Recovery of Hot-Carrier Degradation of Hydrogen/Deuterium Passivated nMOSFETs," *Microelectronics Reliability*, vol. 76-77, pp 135-140, 2017

2. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, "Towards understanding the Recovery of Hot-Carrier induced Degradation," *Microelectronics Reliability*, vol. 88-90, pp 147-151, 2018

3. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, "Recovery after Hot-Carrier Injection: Slow versus Fast Traps," *Microelectronics Reliability*, 113318, 2019

4. Alexander E.M. Smink, **Maurits J. de Jong**, Hans Hilgenkamp, Wilfred G. van der Wiel, Jurriaan Schmitz, "Anomalous Scaling of Parasitic Capacitance in FETs with a High-K Channel Material," *ICMTS Conference Proceedings*, 2020

5. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, "Effect of Ambient on the Recovery of Hot-Carrier Degraded Devices," *IRPS Conference Proceedings*, 2020

Conference Contributions

1. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Observations on the Recovery of Hot-Carrier Degradation of Hydrogen/Deuterium Passivated nMOSFETs* ESREF 2017, Oral Presentation, Bordeaux, France

2. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Self-Healing in Electronic Devices (SHIELD)* SAFE 2018, Poster Presentation, Enschede, the Netherlands

3. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Towards understanding the Recovery of Hot-Carrier induced Degradation* MESA$^+$ day, Poster Presentation, Enschede, the Netherlands

4. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Towards understanding the Recovery of Hot-Carrier induced Degradation* ESREF 2018, Oral Presentation, Aalborg, Denmark

5. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Recovery after Hot-Carrier Injection: Slow versus Fast Traps* SAFE 2019, Poster Presentation, Delft, the Netherlands

6. **Maurits J. de Jong**, Cora Salm and Jurriaan Schmitz, *Recovery after Hot-Carrier Injection: Slow versus Fast Traps* ESREF 2019, Oral Presentation, Toulouse, France

7. **Maurits J. de Jong**, C. Salm, J. Schmitz, "Effect of Ambient on the Recovery of Hot-Carrier Degraded Devices", IRPS 2020, Poster Presentation, Delft, the Netherlands

8. **Alexander E.M. Smink**, Maurits J. de Jong, Hans Hilgenkamp, Wilfred G. van der Wiel, Jurriaan Schmitz, "Anomalous scaling of parasitic capacitance in FETs with a high-K channel material", ICMTS 2020, Oral Presentation, Edinburgh, United Kingdom