Turn-off overvoltage characterization and mitigation in wide bandgap power transistors

Junyun Deng[1,2], Elmar Peters[3], Wenbo Wang[2], Prasanth Venugopal[1]
, Jelena Popovic[1], Braham Ferreira[1]
[1]University of Twente, Enschede, the Netherlands
[2]Shenzhen Institute of Wide-Bandgap Semicondutors, Shenzhen, China
[3]Elmar Solar, www.elmar.solar, the Netherlands
Email: j.deng@utwente.nl

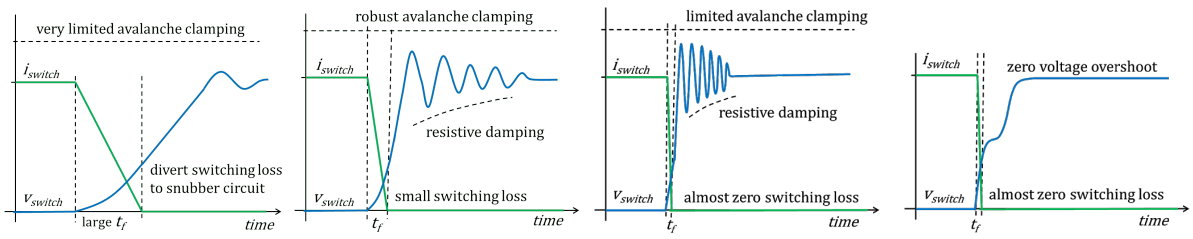
Keywords

≪Wide bandgap power transistors≫, ≪turn-off ringing characterization≫, ≪turn-off voltage overshoot mitigation≫, ≪high frequency switching≫.

Abstract

Turn-off ringing is a challenge caused by parasitic elements in power loop, resulting in switching losses, voltage breakdown and EMI issues. A worse case occurs while employing wide bandgap power transistors due to their fast turn-off. The conventional way to mitigate turn-off ringing is to reduce the commutation loop inductance or slow down transistors' switching speed. However, slow turn-off speed is undesirable due to low switching loss. In this work, it is demonstrated that fast turn-off of wide bandgap(WBG) transistors can facilitate minimizing voltage overshoot with well-tuned parasitic loop inductance. Based on the characterization of the turn-off transition, an analytical model is derived that shows voltage overshoot can be reduced without sacrificing low turn-off loss and simple PCB layout while allowing high loop inductances. The proposed technology can fully exploit the potential of wide bandgap transistors in extremely fast switching conditions.

Introduction



(a) First generation Si transistors (b) Current generation Si transistors (c) Conventional WBG transistors (d) WBG transistors with zero voltage overshoot

Fig. 1: Turn-off transients evolution of transistors

With the evolvement of power transistors, voltage overshoot mitigation techniques are continually developed. Fig. 1 depicts turn-off ringing variations with the evolution of power transistors. Due to the limited avalanching ability of the first generation Si transistors, snubbers are required to absorb excess damping energy [1]. For current generation switches, an increase of the switching speed of MOSFETs and IGBTs is actively pursued. To mitigate voltage overshoot damage,

avalanching ability is enhanced accordingly. WBG transistors feature an super fast transition speed. Consequently, parasitic ringing is more severe, associated with limited avalanching robustness of WBG transistors [2].This impairs the competence of WBG transistors.
To reduce voltage overshoot without sacrificing switching speed, reducing the parasitic inductance of the loop is necesssary, and minimizing the loop area is an effective method to achieve that [3],[4]. However, several trade-offs have to be made, which eventually limit the usage of semiconductor packages with large sizes that allows for bettering cooling and simple PCB layout with low costs. A promising approach to fully eliminate zero-voltage overshoot is introduced in [5], where impedance matching principle is applied by using parasitic inductance and parasitic capacitance. The effectiveness of this method is shown in Fig. 1d. However, it only gives one single optimum operating point, which largely restricts the scope of applications.
This paper offers fundamental insights into the turn-off transition of WBG transistors by employing the simpfiled switching model. A mathematical model is built, which characterizes connections between the turn-off voltage overshoot and the loop inductance and switching speed. It is exhibited that, in a phase leg configuration, WBG transistors can achieve zero voltage overshoot theoretically under several quantum working conditions. The simulation and experimental prototype are also established to prove and demonstrate the proposed theory.

Turn-off transition process analysis

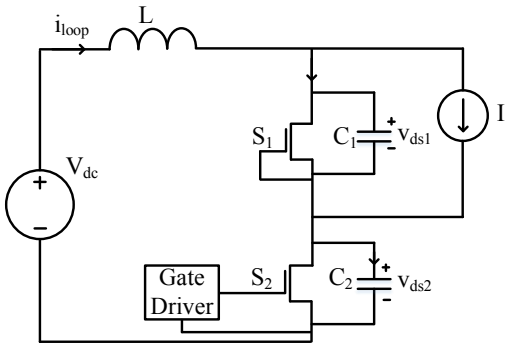


Fig. 2: A single-pulse setup based on a half leg GaN based configuration for turn-off transition

A typical circuit to model the turn-off transition in a phase leg configuration is shown in Fig. 2, where C_1 and C_2 are the transistors parasitic capacitance. Since its source pin is connected to the gate pin, the upper transistor S_1 acts like a synchronous rectifier. The lower side transistor S_2 is an active switch controlled by the gate driver.

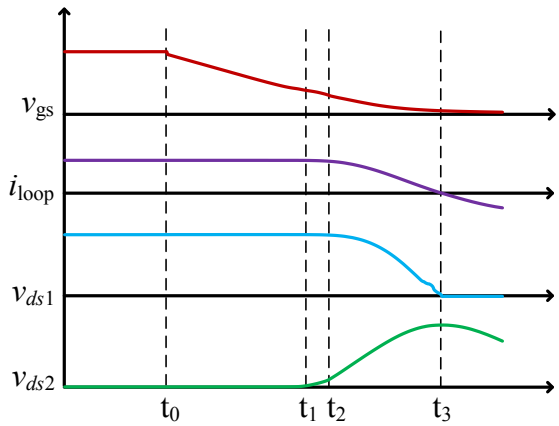


Fig. 3: Simulation voltage and current waveforms during turn-off transition

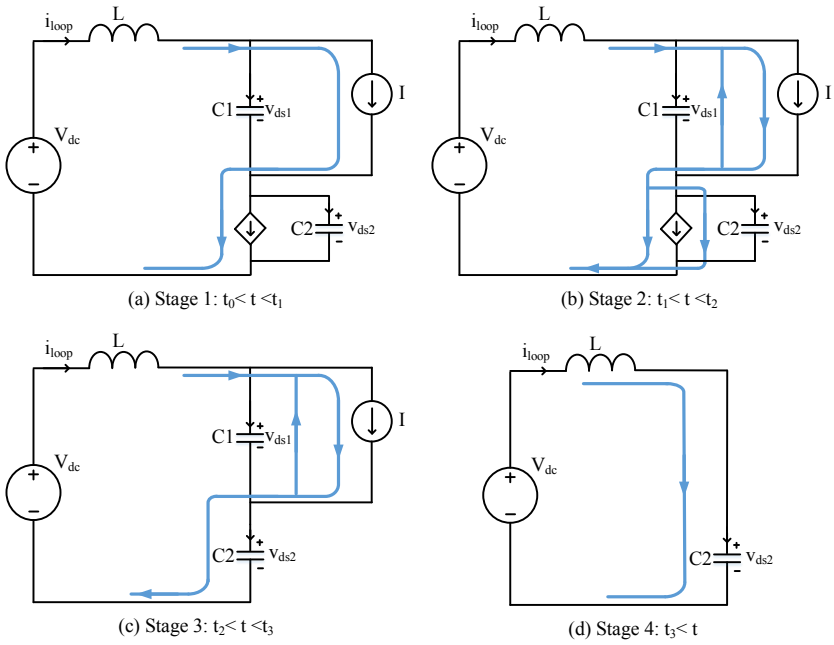


Fig. 4: switching subintervals during turn-off transition

A simulation for a GaN phase leg is carried out and results are plotted in Fig. 3. According to simulation waveforms, the turn-off transtion of GaN is divided into four subintervals. It should be noted that due to small Miller and gate to source capacitances (C_{gd} and C_{gs}) of GaN, the Miller plateau does not exisit in the turn-off transition of GaN. Instead, the gate to source voltage v_{gs} continually decreases with different falling rates. This phenomenon is also reported in [6]. Circuit states of four subintervals are plotted in Fig. 4.

Stage 1 ($t_0<t<t_1$): The first stage begins when the driving signal of S_2 drops. S_2 works in the linear region where channel current can be calculated by v_{gs}. Load current I flows through its channel. This stage ends when v_{gs} reaches the Miller voltage, which is determined by (1):

$$V_{Miller} = \frac{I}{g_{fs}} + V_{th} \tag{1}$$

The final condition of the circuit in the first stage is expressed as (2):

$$i_{loop}(t=t_1) = I \quad v_{ds1}(t=t_1) = V_{dc} \quad v_{ds2}(t=t_1) = 0 \tag{2}$$

Stage 2 ($t_1<t<t_2$): The channel current decreases from load current to zero and load current commutates to the upper and lower side intrisic capacitances C_1 and C_2. The channel turn-off time depends on the gate driver ability. The falling speed of channel current is assumed to be constant, which is expressed as (3):

$$I_{chan} = \begin{cases} I\frac{t_2-t}{t_2-t_1}, t_1 < t < t_2 \\ 0, t > t_2 \end{cases} \tag{3}$$

Therefore, during this oscillation process, i_{loop},v_{ds1} and v_{ds2} can be caculated as:

$$i_{loop}(t) = C_e \frac{I\sqrt{LC_e}}{(t_2-t_1)C_2} \sin\omega_e(t-t_1) - \frac{C_1}{C_1+C_2}\frac{I(t-t_1)}{(t_2-t_1)} + I \tag{4}$$

$$v_{ds1}(t)=\frac{1}{C_1}\left(-\frac{C_1}{C_1+C_2}\frac{ILC_e}{t_2-t_1}\cos\omega_e(t-t_1)-\frac{C_1}{C_1+C_2}\frac{I(t-t_1)^2}{2(t_2-t_1)}\right)+V_{dc}+\frac{C_1C_2}{(C_1+C_2)^2}\frac{IL}{t_2-t_1} \tag{5}$$

$$v_{ds2}(t)=\frac{1}{C_2}\left(-\frac{C_1}{C_1+C_2}\frac{ILC_e}{t_2-t_1}\cos\omega_e(t-t_1)+\frac{C_2}{C_1+C_2}\frac{I(t-t_1)^2}{2(t_2-t_1)}\right)+\left(\frac{C_1}{C_1+C_2}\right)^2\frac{IL}{t_2-t_1} \tag{6}$$

where

$$C_e=\frac{C_1C_2}{C_1+C_2}\quad \omega_e=\sqrt{\frac{1}{LC_e}} \tag{7}$$

Stage 3 ($t_2<t<t_3$): For the channel current of S_2 decreases to zero at the beginning of this stage, this is a resonant interval between loop inductance L and transistor capacitances C_1 and C_2, where C_1 is dicharged and C_2 is charged. Hence circuit parameters can be calculated as,

$$i_{loop}(t)=\frac{C_2}{C_1+C_2}I+\left(i_{loop}(t_2)-\frac{C_2}{C_1+C_2}I\right)\cos\omega_e(t-t_2)-\omega_eC_e\left(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc}\right)\sin\omega_e(t-t_2) \tag{8}$$

$$v_{ds1}(t)=-\frac{1}{C_1+C_2}I(t-t_2)+\frac{1}{C_1\omega_e}\left(i_{loop}(t_2)-\frac{C_2}{C_1+C_2}I\right)\sin\omega_e(t-t_2)+\frac{C_2}{C_1+C_2}\left(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc}\right)\cos\omega_e(t-t_2)+v_{ds1}(t_2)-\frac{C_2}{C_1+C_2}\left(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc}\right) \tag{9}$$

$$v_{ds2}(t)=\frac{1}{C_1+C_2}I(t-t_2)+\frac{1}{C_2\omega_e}\left(i_{loop}(t_2)-\frac{C_2}{C_1+C_2}I\right)\sin\omega_e(t_2-t_1)+\frac{C_1}{C_1+C_2}\left(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc}\right)\cos\omega_e(t-t_2)+v_{ds2}(t_2)-\frac{C_1}{C_1+C_2}\left(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc}\right) \tag{10}$$

Stage 4 ($t_3<t$): When the third stage ends, v_{ds1} equals to zero and the drain and source terminal of upper transistor is shorted. Therefore, in this stage, the oscillation continues between C_2 and L and voltage overshoot on S_2 occurs. i_{1oop}, v_{ds1} and v_{ds2} can be expressed as:

$$i_{loop}(t)=\omega_2C_2\sqrt{\frac{L}{C_2}}i_{loop}(t_2)\cos\omega_2(t-t_3)-\omega_2\left(v_{ds2}(t_3)-V_{dc}\right)\sin\omega_2(t-t_3) \tag{11}$$

$$v_{ds1}(t)=0 \tag{12}$$

$$v_{ds2}(t)=V_{dc}+\sqrt{\frac{L}{C_2}}i_{loop}(t_3)\sin\omega_2(t-t_3)+\left(v_{ds2}(t_3)-V_{dc}\right)\cos\omega_2(t-t_3) \tag{13}$$

where

$$\omega_2 = \frac{1}{\sqrt{LC_2}} \tag{14}$$

Turn-off overshoot can be expressed from (13):

$$v_{ov}=\sqrt{(v_{ds2}(t_3)-V_{dc})^2+\left(\sqrt{\frac{L}{C_2}}i_{loop}(t_3)\right)^2} \tag{15}$$

For simplicity, an assumption is made as:

$$C_1 = C_2 = C \quad \Delta t = t_3 - t_2 \tag{16}$$

Each item in (15) can be found:

$$v_{ds2}(t_3)-V_{dc} = \sqrt{\frac{2L}{C}}\left(i_{loop}(t_2)-\frac{I}{2}\right)\sin\omega_e\Delta t + (v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc})\cos\omega_e\Delta t$$

$$i_{loop}(t_3)\sqrt{\frac{L}{C_2}}=\frac{1}{2}\sqrt{\frac{L}{C}}I+\sqrt{\frac{L}{C}}\left(i_{loop}(t_2)-\frac{I}{2}\right)\cos\omega_e\Delta t-\sqrt{\frac{1}{2}}(v_{ds1}(t_2)+v_{ds2}(t_2)-V_{dc})\sin\omega_e\Delta t \tag{17}$$

The object is to find minimal values of (15) and there are two different scenarios.The first case is employing an ideal driver, which can turn off the channel instantly. The second stage of turn-off transition is neglected. So the initial condition of the third stage is:

$$i_{loop}(t_2) = I \quad v_{ds1}(t_2) = V_{dc} \quad v_{ds2}(t_2) = 0 \tag{18}$$

So (15) and (17) can be simplified as:

$$v_{ov}=\sqrt{\left(\frac{I}{2}\sqrt{\frac{2L}{C}}\sin\omega_e\Delta t\right)^2+\left(\frac{1}{2}I\sqrt{\frac{L}{C}}+\frac{1}{2}I\sqrt{\frac{L}{C}}\cos\omega_e\Delta t\right)^2} \tag{19}$$

It is found ZOS can be achieved in conditions that:

$$\Delta t = n\pi\sqrt{LC_e} \quad I = \frac{V_{dc}}{n\pi}\sqrt{\frac{8C}{L}}\,(n=1,3,5,..) \tag{20}$$

If the transistor current rating is selceted to be the maximum ZOS turn-off current, the required loop parasitic inductance should be fixed at:

$$L = 8C\left(\frac{V_{dc}}{\pi I_{rate}}\right)^2 \tag{21}$$

An assumption is made that the capacitance per amp is a constant, which is the case in practice for the same chip process technology. Therefore, the transistor capacitance C is in linear proportion to the current rating and (20) can be simplified as,

$$\Delta t = \left(\frac{2C_{unit}V_{dc}}{\pi}\right)^2 \tag{22}$$

where C_{unit} is the transistor capacitance per amp. Consequently, ZOS realization is only determined by the bus voltage, which is independent on the power level.
Theoretically, in this case, there are multiple quantum states to achieve ZOS when the ratio of transistor capacitance and loop inductance satisfies a mathmatical expression related to the bus voltage and turn-off current.

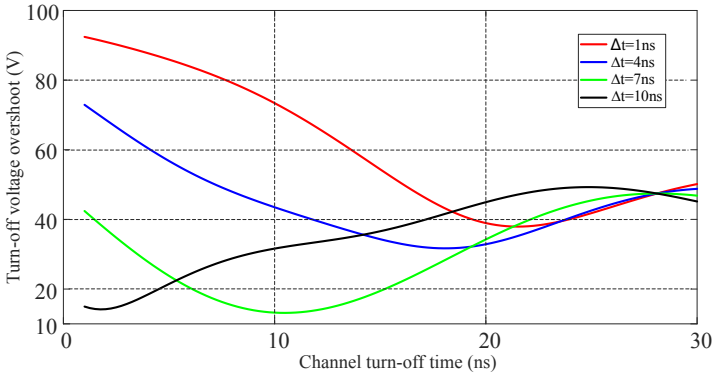


Fig. 5: Voltage overshoot under different channel turn-off time and Δt when L=50μH C=800pF I=12A

The second case is employing a practical driver. In reality, even for GaN, it still requires a short time for transistor channel to turn off. Moreover, the driving speed is limited by the driving loop oscillation. Therefore, the channel turn-off time also has an impact on the turn-off overshoot, which is determined by the driving capability. However, analytic solutions for minimal overshoot points in this case cannot be obtained in a closed loop form.

To give an intuitive understanding, the relationship between channel turn-off time and turn-off overshoot is plotted in Fig. 5 under several certain operating conditions. It can be found that a fast channel turn-off speed doesn't necessarily lead to a large overshoot. It depends on specific working conditions.

Simulation validation

In the above analysis, the upper and lower transistor capacitances are considered to be constant and equal. Actually, WBG transistor capacitances vary with their bias voltage. In this part, an simulation with the transistor SPICE model of EPC2034C(Enhancement GaN,200V/48A) is performed to investigate the impact of nonlinear behaviors. Loop parasitic inductance is set to be 80nH and the bus voltage is 100V in the simulation. Therefore, the calculated value of maximum turn-off current for ideal drivers to achieve ZOS is 10A.

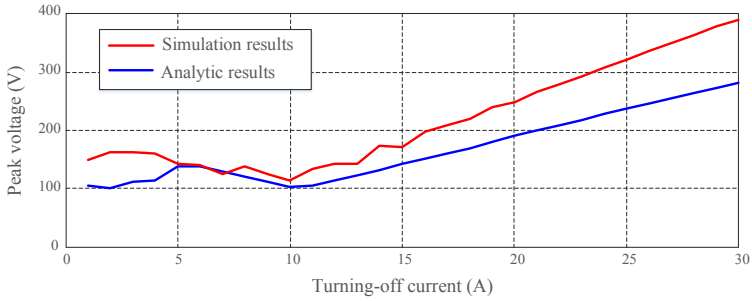


Fig. 6: The relationship comparsion of peak voltage and turn-off current under a strong driver in the anlysis and simulation

As shown in Fig. 6, although there is a discrepancy between theoretical results and simulation results due to nonlinear transistor capacitances, the simulation confirms the prensence of several

minimal overshoot points. It also breaks down a common misconception that fast switching or high turn-off current definitely result in a large voltage overshoot.

Experiment validation

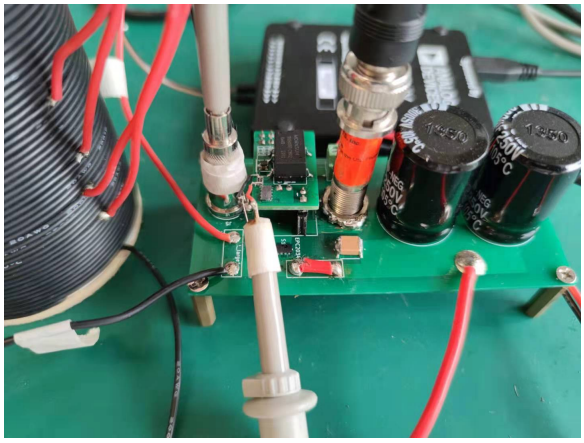


Fig. 7: Picture of experimental prototype

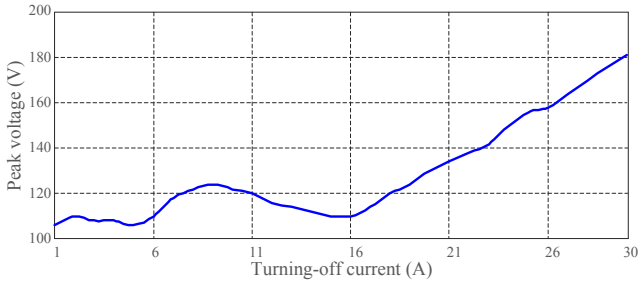


Fig. 8: The relationship of peak voltage and turn-off current in the experiment

In this part, an experimental prototype is build to validate the proposed theory and the topology is shown in Fig. 2. The ideal current source is realized by a 100μH inductor with a air core. To reduce parasitic capacitances of this large inductor, single layer winding structure is adopted. Loop parasitic inductance is mainly determined by an external wire, whose measured value is about 80nH. To guarantee a fast turn-off speed, the turn-off resistor is assigned to be zero. All experimental parameters are in accordance with the simulation. The turn-off current is regulated by controlling the turn-on time of the lower transistor. The prototype is prensented in Fig. 7 and the experimental results are measured in Fig. 8, which validate the existences of multiple minimal overshoot points.

Conclusion

This paper provides the methodology of turn-off voltage overshoot mitigation for WBG transistors. A turn-off transition model is proposed in this paper. The impacts of turn-off current and speed on turn-off overshoot are analyzed, which are validated by simulation and experiment results. The model proves if inductance and capacitance in the commutation loop are well tuned, there are multiple quantum states to realize ZOS at turn-off in theory. Additionally, it is shown that the nonlinear capacitance doesn't affect the presence of quantum states, only their values. Furthermore, the transition time is only a function of drain-source capacitance per ampere of the transistors, which means its application is independent of the power level. Therefore, the proposed theory can effectively push the boundary of switching frquency of WBG transistors.

References

[1] McMurray W.; Optimum snubbers for power semiconductors[J]. IEEE Transactions on Industry Applications, 1972 (5): 593-600.
[2] Kachi T, Kikuta D, Uesugi T. GaN power device and reliability for automotive applications[C]//2012 IEEE International Reliability Physics Symposium (IRPS). IEEE, 2012: 3D. 1.1-3D. 1.4.
[3] Reusch D, Strydom J.; Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter[J] ; IEEE Transactions on Power Electronics, 2013, 29(4): 2008-2015.
[4] Robutel R, Martin C, Buttay C, et al. Design and implementation of integrated common mode capacitors for SiC-JFET inverters[J]. IEEE transactions on power electronics, 2013, 29(7): 3625-3636.
[5] Matlok S.; Zero overvoltage switching - breaking the rules of parasitic inductance; Fraunhofer IISB Whitepaper; iisb.fraunhofer.de.
[6] Lidow A, De Rooij M, Strydom J, et al. GaN transistors for efficient power conversion[M]. John Wiley Sons, 2019.