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Harnessing charge injection in Kelvin probe force microscopy for the evaluation of oxides

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ARTICLE INFO

Handling editor: Marco Lanuzza

Keywords: KPFM C-AFM Dielectrics characterization Characterization techniques for dielectrics and interfaces Charge injection

1. Introduction

Advanced gate structures are nowadays ubiquitous in ultra-scaled transistor architectures [1]. Similarly, for memory devices, complex high-k materials are used for to engineer the density of deep traps used for storage media in high density devices such NAND [2-4]. Therefore, it is of great technological interest to develop sensing methodologies to study the behavior of charge injection in oxide materials and offer fast screening techniques to judge the impact of process conditions on dielectrics properties, such as trapped charges distribution, charge retention and trapping site density, among others. Previous works have shown how scanning probe microscopes can be successfully applied to study charge distribution and trapped charge in nitrides and oxides [4–7]. However, a quantitative analysis of the output from these electric atomic force microscopy (AFM) methods, remains complex (i.e., extracting concentration and/or polarity of the trapped charge), and often these methods are uncorrelated from standard characterization methods offering averaged electrical results. Here, we systematically use the probe of AFM for both charging and imaging thin oxide layers by a combination of conductive atomic force microscopy (C-AFM) and KPFM (Fig. 1a,b). Although not new, this report describes the use of this methodology to investigate the properties of different oxide deposition

ABSTRACT

We report on a quantitative use of Kelvin probe force microscopy (KPFM) for the analysis of charge injection in thin oxides. Here, thin dielectrics are investigated through an atomic force microscopy tip that is used as a movable (virtual) top-electrode. The charge is injected and read-out respectively by alternating the direct contact of the probe with the oxide, and with non-contact surface potential imaging. The contact potential difference (CPD) between the atomic force microscope tip and the oxide surface is used to measure the charge distribution under multiple electrical stress conditions, thus correlating locally trapped charge with dielectric properties.

> methods, showing detection sensitivity between dry and wet oxide growth techniques, and more in general for process qualification. In addition, we show a pathway for obtaining the characterization of gate stack structures under various electric field stress conditions. This is obtained by modifying the writing and read-out patterns on the oxide surface, thus providing a framework of interpretation for the direct probing of trapped charge in thin oxide using electrical AFM techniques. The objective beyond the quantitative extraction of trapped charge, is the comparative analysis of different post-deposition treatments of deposited films with potential applicability also at wafer level.

2. Experimental

The measurements are performed on reference Si/SiO₂ samples with thickness of 20 nm and different growth methods (i.e., wet vs. dry). Si ptype (N_A \sim 2E16/cm $^{-3})$ is used as substrate. In the second part of this work, we focus on HfO2-based gate stacks. The surface morphology and electrical properties of the sample are measured with a Bruker Icon AFM system equipped with conductive coated platinum tips (PPP-NCST-Pt, NanoAndMore, spring constant 7.4 N/m). Since charge injection is very sensitive to the oxide surface condition, all measurements are performed inside a glovebox with an inert nitrogen ambient to minimize

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https://doi.org/10.1016/j.sse.2021.108136

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Fig. 1. (a) Schematic of the two AFM techniques involved, namely C-AFM and KPFM. The two methods, i.e., contact, and non-contact are combined as shown in (b), to obtain the surface potential image and spectrum in response to an arbitrary dc stress on the thin oxide surface.



atmospheric contamination of the surface. In all measurements, the probe is grounded, and the voltage is applied to the sample's substrate.

3. Results

The process of charge injection is schematically reported in Fig. 1b. The charge is injected by applying a dc voltage to the probe scanning in contact with the oxide surface. Different values of the dc bias allow us to explore the response at different injection energies. The charge distribution is imaged in non-contact with KPFM, here an ac voltage is applied to the probe at a frequency of 2 kHz, to induce an alternating electrostatic interaction between the lifted probe and the surface. The distance between the probe and the surface is kept at 10 nm. The contact potential difference is measured with nanometer resolution by nullifying the electrostatic force at 2 kHz in every pixel by using a lock-in amplifier. The contact potential difference (CPD) can be plotted as a map providing a 2D image of the surface potential, or as the distribution of CPD values to make it simpler to compare results across different samples (Fig. 1b). The high degree of control over bias application during the C-AFM scan, allows to observe the evolution of charge injection as a function of the tip-sample voltage. As example, Fig. 2a shows the twodimensional CPD map in the area $5 \times 5 \,\mu\text{m}^2$ previously stressed. Individual steps for each stress condition can be seen in the KPFM profile (Fig. 2b): the decrease (increase) of CPD following positive (negative) charge injection, is the result of holes (electrons) trapped in the oxide layer that modify the work function of the oxide surface. Here, the gradual dependance of the CPD with the dc stress is used to extract the bias required for the compensation of the remnant charge in the pristine layer i.e., the surrounding pristine area. A similar concept is used in Fig. 2c where we show the dependance of the measured CPD with stress polarity. The application of positive/negative bias on the tip allows the injection of electrons/hole from the p-type Si into the oxide. This process, schematically shown in the inset of Fig. 2c, will be assisted by

Fig. 2. (a) KPFM map and (b) profile of incremental dc programming (200 mV increment) on the surface of SiO₂. Here, the dc stress in contact mode is increased with small steps to find the condition for reversal in the response, i.e., mimicking the search for V_{FB} conditions of the tip-sample system. (c) Schematic of the charge injection configuration as a function of the tip bias and comparison of CPD obtained at different stress conditions. (d) Profiles collected for dry and wet oxides are compared using KPFM maps in a spectroscopic mode.



Fig. 3. (a) Multi-bias dc stress charge injection scheme used for HfO₂-based gate stack. (b) Leakage current studied using C-AFM in the range of interest. (c) Schematic band diagram of the tip-sample system. (d) CPD profile and (e) associated field-dependent charge injection plot. Note that the gate stack was not exposed to any high temperature anneal (>800 °C), customarily used in commercial logic technologies to reduce dielectric defect density.

different injection mechanisms, depending on the film thickness and quality [4,6,8]. One of the consequences is that we can use this approach to discriminate between small electrostatic differences in oxides grown with different processes, i.e., by comparing the distribution of CPD for injected charge (as in Fig. 2d for wet vs. dry SiO₂). The latter is repeated on various oxide thicknesses in the range 5–20 nm, to rule out thicknessinduced effects. We consistently obtain the same directional shift in all the spectra, thus indicating a material dependent role of trapping site density for the different growth methods.

In the next section we use the same approach for the analysis of HfO₂based gate stack. HfO₂ (~1.8 nm thick) is deposited on a thermal SiO₂ interfacial layer (~1.2 nm) grown by in-Situ Steam Generation at 600 °C on a 300 mm wafer. A final anneal (400 °C-20' in molecular H₂) was performed to passivate the Si/SiO₂ interface. Here, we use the dc writing scheme shown in Fig. 3a to explore multiple electric field stress conditions. This allows to study charge injection at different energies while maintaining the same measurement time of a single contact scan. Fig. 3b shows the dependence of the experimental CPD on the amplitude of the pulse used for charge injection with the schematic of the tip-sample system (Fig. 3c). First, we extract the difference between the CPD in the pristine area and the value obtained at 0 V dc stress, to be used a flatband equivalent of the tip-sample system. This value is used to calculate the overdrive voltages (V_{ov}) applied during the injection experiments, and therefore to estimate the corresponding electric fields in the SiO₂ interfacial layer as $E_{ox} \sim V_{ov}$ /CET (where CET stands for the Capacitance Equivalent Thickness of the SiO₂/HfO₂ stacks, i.e., ε/C_{ox}). Thus, a fielddependent charge injection plot as shown in Fig. 3e can be made. To benchmark gate stacks with different oxide thicknesses, the measured CPD shifts could be then used to estimate the trapped oxide charge density as $\Delta N_{eff} = \Delta V * C_{ox}/q$ [/cm²], i.e., by considering for simplicity the trapped charge profile as confined in a single charge sheet located at the Si/SiO₂ interface. Note, alternative more complex approaches have been presented in literature for a quantitative estimation of the trapped charge density using numerical solutions of Poisson's equation [5,9].

While this approach appears promising to correlate the KPFM characterization with standard reliability characterization of a fully fabricated device, it is important to monitor two additional elements, namely (1), the leakage current associated with the selected range of bias stress, and (2), the formation of surface modifications such as tip-induced melting or oxidation, resulting from the voltage application. The latter is clearly a signature of undesired tip-sample interactions beyond charge injection, that can alter the final read-out. Therefore, after selecting the range of voltage stress, it is important to check the quality of the surface to make sure the morphology is not affected. Similarly, it is important to quantify leakage during the dc stress phase, as this can have a major impact on the number of charges that are exchanged in the tip-sample system and thus on the actual read-out. In Fig. 3b we show the I-V characteristic obtained with the AFM probe for the HfO₂ sample. The thin oxide has substantial electronic leakage (in range pA - nA) when stressed over ± 3 V. This sets the limit for the electric field stress conditions that are accessible to our method, as the CPD obtained beyond these values results from the convolution of both the impact of leakage and charge injection. This effect is visible in the CPD profile (Fig. 3d), when comparing the absence of CPD shift for stress conditions 2 V and 5 V. Finally, it worth noting that triboelectric effects (not discussed here) can have an important role on the final measured contrast [10,11]. Therefore, we consider key to calibrate the impact of CPD shift induced by the rubbing of the contact phase, before any quantitative analysis using this approach. In summary, adding on previous works on KPFM for the analysis of charge trapping in various materials [7,8], we report on the combined use of KPFM and C-AFM for the rapid qualification of process development (here addressing thin oxide films). Through the use of optimized contact scans with a biased probe, creating concentric boxes or staircase structures, we demonstrate (1) the sensitivity of the methodology for the qualification of different type of oxides, and (2) the possibility to explore field-dependent charge injection plot for a quantitative comparison between deposition techniques of thin dielectrics. Beyond the use on blanket oxide films, this concept could be generalized also to be applied at the early stage of device integration flow, thus reducing the time for analysis, the number of wafers required and fabrication costs.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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