Superconducting Circuits without Inductors Based on Bistable Josephson Junctions

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Magnetic flux quantization in superconductors allows the implementation of fast and energy-efficient digital superconducting circuits. However, information representation in magnetic flux severely limits the functional density and is a long-standing problem. Here, we introduce the concept of superconducting digital circuits that do not utilize magnetic flux and have no inductors. We argue that neither the use of geometric nor kinetic inductance is promising for the scaling down of superconducting circuits. The key idea of our approach is the utilization of bistable Josephson junctions, allowing the representation of information through the Josephson energy. Since the proposed circuits are composed only of Josephson junctions, they can be called all-Josephson junction (all-JJ) circuits. We present a methodology for the design of circuits consisting of conventional and bistable junctions. We analyze the principles of the circuit's functioning, ranging from simple logic cells to an 8-bit parallel adder. The utilization of bistable junctions in the all-JJ circuits is promising for the simplification of schematics and a decrease of the JJ count, leading to space efficiency.

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I. INTRODUCTION

The promised end to Moore's law [1] nowadays gives rise to "beyond Moore's" technologies. An appropriate alternative to complementary metal oxide semiconductor (CMOS) technology should be fast and scalable, while providing the highest energy efficiency. Superconducting electronics is attractive in this context.

Superconductor technology is known for high clock frequencies, $f_c \sim 2 - 50$ GHz [2], and low energy dissipation per logic operation, down to several zJ [3]. The advantage over CMOSs in energy efficiency reaches 2 to 6 orders of magnitude, depending on the logic and algorithm utilized [2,4–7]. This is especially valuable for operation at low temperatures. At standard $T = 4.2$ K, the cost of refrigeration is 1000 times the dissipated energy [4,8]. These unique features make superconducting circuits the most promising candidates for developing scalable computing systems that operate across the gradient between room temperature and the temperature of a cryogenic payload. They are suitable for frontier technologies, such as quantum computers, cognitive radio, scalable sensors, and the quantum internet [9].

At the same time, the integration density of superconducting circuits is far lower than that of current CMOSs. Recently demonstrated benchmark circuits for the latest 250- and 150-nm MIT Lincoln Laboratory (LL) processes were shift registers with 7.4×10^6 and 1.3×10^7 Josephson junctions (JJs)/cm^2 circuit density, respectively [10]. With the 4 JJ/bit cell, the functional density is less than 10 Mbit/cm^2, showing the need for improvement. Since there is no direct analog of a CMOS transistor in the superconducting element base [5], scaling to higher density requires the development of special approaches.

The function of superconducting logic circuits is based on the effect of magnetic flux quantization, instead of the modulation of conductance [6,7]. This allows a discrete representation of information in the form of a single-flux quantum (SFQ), $\Phi_0 = h/2e$ (where h is Planck's constant, e is the electron charge). The basic element of broadly used rapid SFQ (RSFQ) [11] logic is a superconducting loop interrupted by Josephson junctions, see Fig. 1(a). If the loop inductance, L, is high enough that $I_c L \approx \Phi_0$ (where I_c is the JJ critical current), then a SFQ can be held in the

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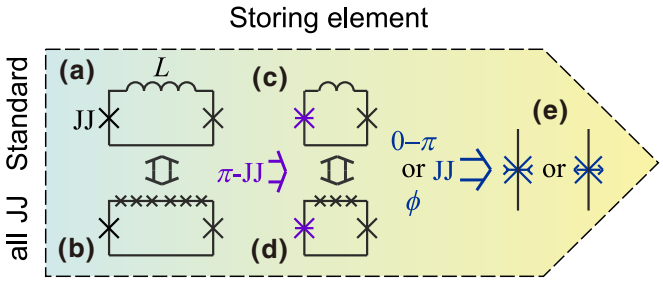

FIG. 1. Storage element based on conventional 0-JJ with (a) and without (b) inductor, 0-JJ and π-JJ with (c) and without (d) inductor, and bistable $0-\pi$ JJ and ϕ-JJ (e). See Fig. 2 for descriptions of JJ symbols.

loop, representing logic "1," while the absence of a SFQ means logic "0."

Here, we consider different approaches for the miniaturization of the RSFQ basic cell. This includes analysis of the scalability of the inductor, substitution of the inductor by Josephson junctions, and the utilization of magnetic JJs of various kinds. The last of these results in the possibility of replacing the basic cell with a single bistable Josephson junction (see Fig. 1). We complement this by proposing a design methodology for superconducting circuits without inductors based on bistable JJs. Our design is based on a basic block. Modification and complication of its schematic allow us to obtain various logic cells. We demonstrate the validity of the proposed methodology using the design of an 8-bit parallel adder as an example. We conclude the article with a brief discussion of the obtained results and outline further research directions.

II. MINIATURIZATION OF BASIC CELL

A. Scaling of inductor

Theoretical estimation [12] of the maximum density of SFQ-based circuits utilizing geometrical inductance of wires corresponds to already achieved $\sim 10^7$ JJ/cm^2. A further decrease of the line width and spacing is problematic because of nearly exponential growth in mutual inductance and cross talk between the inductors [13]. The main approach to shrink the inductor is related to the utilization of kinetic inductance. Here, energy stored in the inductor corresponds to the kinetic energy of the superconducting current, not to the magnetic field around a wire. The critical current of the inductor, I_{CK}, must be greater than that of a Josephson junction, which, in turn, should be much greater than the noise current, $I_{CK} > I_c \gg I_n = (2\pi/\Phi_0)k_BT$ (where k_B is the Boltzmann constant), to provide a low bit-error rate. The noise current at the operation temperature, $T = 4.2$ K, is $I_n \approx 0.18$ μA. A typical value of the Josephson junction's critical current is $I_c \sim 0.1$ mA, so that the inductance of a storage cell is $L_{cell} \approx \Phi_0/I_c \sim 20$ pH.

For a real type-II superconductor film with width w, which is much larger than the coherence length, $w \gg \xi$, the wire critical current, I_{CK}, is a fraction of the Ginzburg-Landau (GL) depairing critical current, $I_{CK} \approx \eta I_{GL} = wd\eta\Phi_0/(3\sqrt{3}\xi\mu_0\lambda^2)$ [14,15]. Here, d is the thickness of the wire, λ is the London magnetic penetration depth, and μ_0 is the vacuum permeability. The critical-current reduction [13], $\eta \sim 0.1$, is caused by the entry and motion of Abrikosov vortices from the film edges.

The kinetic inductance of a thin wire is $L_k = l\mu_0\lambda^2/(wd)$, where l is the wire length and $d \ll \lambda$. The required cell inductance is $L_{cell} = L_k \sim l/(wd)$. The critical current of the inductor must also be greater than the JJ, so $I_c < I_{CK} \sim wd$. Therefore, the minimum wire length and its cross-section area are determined by the chosen material and the quality of the wire edges. For a reasonable ratio, $I_{CK}/I_c \geq 4$, and some "dirty" superconductors, such as MoN_x, Nb-Ti-N, or NbN, with high kinetic inductance (where $\lambda \approx 500$ nm, $\xi \approx 10$ nm, $\xi/\eta = 44$ nm [13]), the wire's geometric parameters are $l = (I_{CK}/I_c)3\sqrt{3}\xi/\eta \geq 0.9$ μm and $wd = l\mu_0\lambda^2/L_{cell} \geq 14\,000$ nm^2.

If the wire's width is equal to the minimum feature size of standard SFQ5ee MIT LL process technology, $w = 350$ nm, the wire's thickness is $d \geq 40$ nm, so that the wire's cross-section aspect ratio is $w/d \leq 8.75$. The area of the kinetic inductor is $wl \geq 0.32$ μm^2, which is close to the typical area of a Josephson junction, $\pi w^2 \approx 0.4$ μm^2. Implementation of the inductor requires about 2.5 squares while the value of inductance per square is $L_{k\square} \leq 8$ pH. The obtained numbers show that the utilization of kinetic inductance is a good solution for current technological processes.

However, the convenience of using the kinetic inductance at smaller scales is questionable. For example, a reduction of the inductor width to $w = 90$ nm requires an increase in its thickness to $d \approx 160$ nm (if the length is $l = 0.9$ μm) to preserve its critical current. Here, the wire's cross-section aspect ratio is $w/d \approx 0.56$, which presents difficulties for fabrication. At the same time, the inductance per square becomes 4 times smaller, so that implementation of the inductor is much less effective at the new scale. A safe threshold for kinetic inductor scaling is about $w = (I_{CK}3\sqrt{3}\xi\mu_0\lambda^2/\eta\Phi_0)^{1/2} \approx 120$ nm, which provides a square cross section of the wire. Based on these estimations, we conclude that basic cell scaling requires further research into alternative methods.

B. Superconducting loop without inductor

If a SFQ is inside the standard cell shown in Fig. 1(a), the Josephson phase of one of the junctions is close to $2\pi n$ (where n is an integer), while the phase of another one is about $2\pi(n-1)$, so that the total phase increment in the circuit is 2π. These Josephson phase values correspond to minima of the

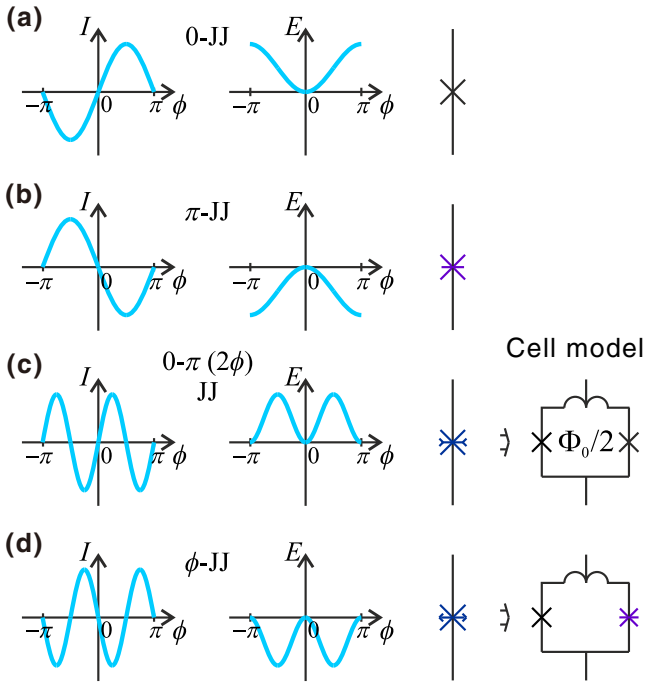

FIG. 2. Current-phase relation, $I(\phi)$; energy-phase relation, $E(\phi)$; and symbols of 0-JJ (a), π-JJ (b), $0-\pi$ JJ (c), and ϕ-JJ (d). CPR and EPR of $0-\pi$ and ϕ-JJ are presented for the case of the suppressed first harmonic of their CPRs. Cell models are presented for $0-\pi$ (2ϕ) and ϕ-JJ.

conventional superconductor-insulator-superconductor JJ (0-JJ hereafter) energy-phase relation (EPR), $E/E_{J0} = 1-\cos(\phi)$, where ϕ is the Josephson phase, and $E_{J0} = I_c\Phi_0/2\pi$ is the Josephson energy, see Fig. 2(a). This EPR corresponds to a sinusoidal current-phase relation (CPR), $I = I_c\sin(\phi)$, where I is the current flowing through the junction.

Josephson junctions in the storage cell can be connected by a stack of JJs instead of an inductor [16,17], see Fig. 1(b). Such a cell can be called an all-Josephson-junction (all-JJ) circuit. If the critical currents of the JJs in a stack are identical, the phase drop for each of them is $2\pi/N$, where N is the number of JJs in the stack. To prevent the JJs from switching, this phase drop should be less than $\pi/2$ (in accordance with the 0-JJ CPR). Reliable operation of circuits is supposed to be provided with a phase drop of about $\pi/3$ [16]. This gives six JJs in a stack that can be implemented, e.g., using two 3-JJ stacks [17].

C. π Josephson junction

The issue of a rather large number of JJs in a stack can be mitigated by the introduction of a JJ with a ferromagnetic interlayer in its weak-link region, providing the π-phase shift of its CPR, $I = I_c\sin(\phi+\pi)$ (π-JJ hereafter) [18,19]. The CPR and EPR of π-JJ are presented in Fig. 2(b). The π-JJ symbol is a cross with a dash in the middle. With a π-JJ in a loop, the phase increment corresponding to the magnetic half-flux quantum already exists in the cell. The cell inductance can be reduced correspondingly, and the number of JJs in the substituting stack can be decreased down to three, see Figs. 1(c) and 1(d) [20–28]. In the RSFQ toggle (T) flip-flop, it is possible even to completely substitute the inductor with a π-JJ [20–22]. Unfortunately, this cannot be a general solution for all circuits. The constraints of this method come from the persistent current arising due to the π-JJ's inherent phase shift. This current flows out into the neighboring cells and may alter their power supplies and disrupt their operation. The direction of this current is determined by the circuit state, and thus, cannot be compensated for by constant-bias-current adjustment.

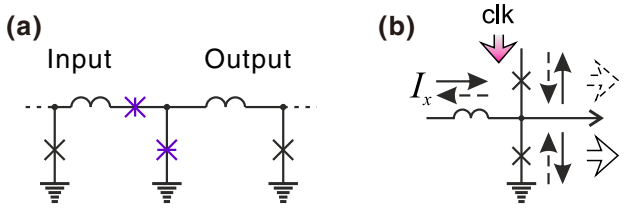

FIG. 3. (a) Two-loop circuit with π-JJs. (b) Balanced comparator [11].

A design methodology utilizing two π-JJs connected in series is proposed to circumvent this issue [24]. Figure 3(a) illustrates the idea. Here, the Josephson phase of each of the π-JJs is about $\pi+2\pi n$, while that of the 0-JJ in the input circuit is about $2\pi n$; combined, the phase shift is $2\pi n$, allowing a state with $n=0$, and thus, zero phase shift and zero current [see also Figs. 2(a) and 2(b)]. This allows the safe connection of the circuit input to conventional RSFQ cells. At the same time, the $\pi+2\pi n$ phase drop on the central π-JJ means that the 0-JJ of the output loop is outside the minimum potential energy. Minimization of the total energy of the π- and 0-JJs leads to states with a noticeable current in the output loop, which can have opposite directions. This provides the opportunity to read out the circuit state by using the conventional balanced comparator shown in Fig. 3(b) [11]. The latter is composed of two JJs connected in series, one of which is switched by the clock (clk) pulse, depending on the direction of the measured current, I_x. Many widely used cells, such as a delay (D) flip-flop and nondestructive read-out (NDRO) [24], or AND and OR logic cells [25], can be designed within the framework of this approach.

D. Bistable Josephson junctions

The main requirement for a storage cell is the existence of two stable states, with and without an SFQ inside. However, the desired bistability can even be obtained with a single bistable Josephson junction. In this case, the storage

element of the circuits reduces to this a single JJ, and its state does not relate to a SFQ.

The bistability corresponds to the existence of the second harmonic in the JJ's CPR, $I = A\sin(\phi) + B\sin(2\phi)$. If $|B| > A/2$, the EPR has a double-well shape [29]. In the case of the positive second-harmonic amplitude, $B > 0$, the JJ's energy minima are located at phase values of zero and π [29]. This junction is, therefore, called the $0-\pi$ JJ [30–32]. Notably, the disappearance of the first harmonic here leads to a doubling of the CPR. In this case, the JJ is called 2ϕ-JJ [33–37]. If the second-harmonic amplitude is negative, $B < 0$, the JJ's energy minima are symmetrically located around zero at $\pm\phi$ phases, where $|\phi| \leq \pi/2$ [29]. This JJ is called ϕ-JJ [32,38–42]. The CPR and EPR of $0-\pi$ and ϕ-JJs for the case of the suppressed first harmonic are presented in Figs. 2(c) and 2(d). The symbols of the JJs are similar to that of the π-JJ but with arrows added to the ends of the central dash, which are directed inside or outside for $0-\pi$ and ϕ-JJ, respectively.

The considered bistable junctions are relatively recently developed types of JJs. They have not yet been introduced into digital superconducting technology. While the optimal method for their fabrication is a technological challenge, they can already be modeled using cells composed of standard junctions [43]. The model of the 2ϕ-JJ is a superconducting loop with two 0-JJs and a half-flux quantum (HFQ) applied to the cell, see Fig. 2(c) [29]. The cell has a small but finite inductance. A smaller inductance results in a smaller cell critical current, and thus, the cell's CPR is closer to a double-sine function. Here, the decrease of the first-harmonic amplitude is caused by the circulating current induced by the HFQ, while the second-harmonic amplitude, and hence, the effective critical current of the junction, is determined by the inductance.

In a very similar way, a ϕ-JJ can be modeled by a cell with 0- and π-JJs, see Fig. 2(d) [29]. It is shown that a Josephson transmission line (JTL) composed of such cells (modeling ϕ-JJs) is capable of transmitting a HFQ [26–28]. The move toward manipulation with a HFQ instead of a SFQ makes the HFQ circuits more power efficient than any other superconducting logic circuits [28]. Notably, the small inductance in the cell model can be substituted by 0-JJs to obtain the all-JJ circuit [29].

The utilization of bistable JJs seems promising with respect to power and space efficiency. Below, we propose a design methodology for circuits without inductors based on bistable 2ϕ-JJs. The latter are chosen because their cell model contains only conventional 0-JJs, see Fig. 2(c). Since the proposed design requires only two types of JJs, conventional 0-JJs and bistable 2ϕ-JJs, this simplifies the experimental verification of prototype circuits. The information bit in the circuits is represented as the presence or absence of a 2π superconducting phase change. This phase change can be transferred along the circuit by the application of a bias current.

III. DESIGN METHODOLOGY

A. Basic block

The dynamics of the 2ϕ-JJ, as well as the 0-JJ, is described by the well-known resistively shunted junction model with capacitance (RSJC) [44] (see also the Supplemental Material [29] for details):

$$i = A\sin\phi + B\sin 2\phi + \alpha\dot{\phi} + \ddot{\phi}, \tag{1}$$

where current flowing through the junction, i, and the amplitudes of the CPR harmonics, A and B, are normalized to the critical current of a reference junction, I_c. Dots indicate derivatives with respect to time, t, normalized to the inverse plasma frequency, $\tau = t\omega_p$, which is determined by the constants of a certain fabrication process, $\omega_p = \sqrt{2\pi j_c/\Phi_0 c}$, where j_c is the critical current density of Josephson junctions and c is their specific capacitance. $\alpha = \omega_p/\omega_c$ is the Josephson junction's damping coefficient, and $\omega_c = 2\pi I_c R/\Phi_0$ is the junction's characteristic frequency; R is the junction's resistance in the normal state.

Each type of junction considered has only one harmonic dominating in the CPR. Therefore, the dominating harmonic determines the critical current of the junction. Since the circuits consist only of JJs and each JJ has only two parameters, the critical current and the damping coefficient [29], these parameters determine the circuit dynamics. The former reflects the strength of superconducting coupling, which determines the potential barrier for JJ switching, while the latter reflects the duration of switching.

The proposed circuits are based on the basic block designed in accordance with the methodology presented in Ref. [24]: the input loop is in a current-less state, while the different phases of the 2ϕ-JJ correspond to different currents circulating in the output loop.

The input loop is composed of one 0-JJ and two 2ϕ-JJs, see Fig. 4(a). The $2\pi n$ phase drop on the 0-JJ is distributed between the 2ϕ-JJs, meaning the phase drop is multiples of π on each of them. This corresponds to the current-less state of the loop due to the CPRs of the JJs used, see Fig. 2. Therefore, the loop can be connected to other circuits from the side of the 0-JJ.

A circulating current in the circuit with two 0-JJs and one 2ϕ-JJ, see Fig. 4(b), corresponds to a $\pi + 2\pi n$ phase drop on the latter. At the same time, the $2\pi n$ phase drop on the 2ϕ-JJ provides the current-less state. A combination of the two considered loops [Figs. 4(a) and 4(b)] forms our basic block, see Fig. 4(d).

In our simulations, we utilize all-Josephson junction (all-JJ) transmission lines (TLs) to apply and read out superconducting 2π phase changes to or from the circuits. These are the JTLs in which each inductor is substituted for a single Josephson junction, see the all-JJTL cell in Fig. 4(c). Parameters of the circuits, as well as a

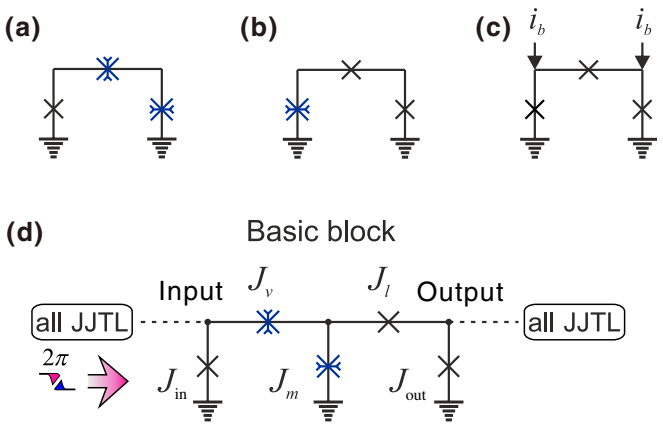

FIG. 4. Interface circuits to change (a) and read-out (b) 2ϕ-JJ state. (c) all-JJTL basic cell. (d) Schematic of basic block with interface all-JJTLs.

detailed description of their dynamics, are presented in the Supplemental Material [29].

The logic state of the basic block corresponds to the Josephson phase of the main 2ϕ-JJ, J_m, located in the center of the circuit [Fig. 4(d)]. J_m parameters are depicted on the (B,α) plane in Fig. 5(a) by a star as a reference point. The superconducting phase-change wave enters the basic block through junction $J_{\rm in}$ and can exit through junction $J_{\rm out}$. The interconnecting junctions, J_v and J_l, serve as the input and output valves in the wave-transfer process, respectively.

The block possesses four modes of operation, depending on the parameters of the input valve junction, J_v (B,α), as presented in Fig. 5(a). In a trivial case where junction J_v is sufficiently "weaker" and "faster" than the main junction, J_m, the input 2π phase-change wave switches $J_{\rm in}$ and exits through J_v (mode 1). In the opposite case, the input wave passes through J_m, switching it twice, and exits through $J_{\rm out}$ (mode 2).

More interesting modes of operation are obtained with a mixed ratio of parameters of the 2ϕ-JJs. If the input valve junction is weaker than the main junction, it starts to switch first, but if its switching takes a relatively long time, the main junction also has time to switch [see Fig. 5(b)]. In this way, the incoming 2π phase change is transformed into the π phase drops on the two 2ϕ-JJs. Since the output junction, $J_{\rm out}$, has a 2π periodic CPR, every second 2π phase-change wave passes through the basic block. Here, the block operates as a digital-frequency divider, like a T flip-flop (mode 3), see Figs. 5(b) and 5(c).

Simultaneous switching of the 2ϕ-JJs occurs over a relatively wide range of ratios of parameters (including the inverse ratio with the corresponding swap in the sequence of switching). Interestingly, an increase of the input valve junction's critical current results in another operation regime. Here, leakage of the interface all-JJTL's bias current into $J_{\rm out}$ provides its periodic switching, if

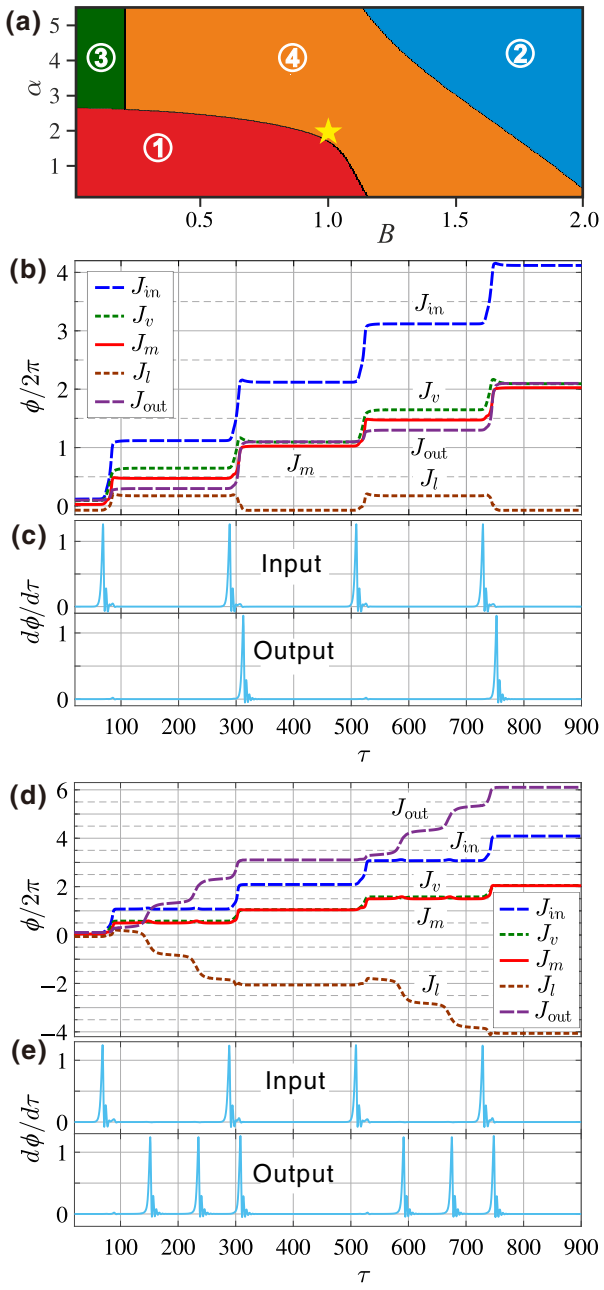

FIG. 5. (a) Input valve junction, J_v [shown in Fig. 4(d)], parameters (B,α) corresponding to different modes of basic block operation: 1, terminator; 2, transmission line; 3, digital frequency divider; 4, oscillator. Main junction, J_m, parameters are depicted by a star ($\star$). (b) Dynamics of phases of Josephson junctions and (c) voltage pulses $(d\phi/d\tau)$ corresponding to phase-change waves in the input and output all-JJTLs in mode 3 for $B_v = 0.1, \alpha_v = 5$. (d),(e) Same as before, corresponding to mode 4 ($B_v = 0.5$, $\alpha_v = 5$).

the J_m phase is about $\pi + 2\pi n$. This switching of $J_{\rm out}$ can be turned on and off by the switching of logic states of the basic block. In this mode 4, the block operates as a conventional SFQ-to-dc converter [11], see Figs. 5(d) and 5(e).

B. Controlled readout of 2ϕ-JJ states

Controlled readout of the circuit's logic state can be performed if the output of the basic block is designed as a balanced comparator [see Fig. 3(b) [11]]. In this case, another 0-JJ, J_r, is connected to the output loop, accordingly, see Fig. 6(a). A read 2π phase-change wave is applied to the pair of junctions J_r and J_{out}.

The NDRO is realized when the processes in the output loop do not significantly affect J_m. At the same time, the J_m phase is increased by about π with every 2π phase-change wave coming from the input loop. The circuit's operation is close to that of modes 3 and 4 considered above, but here the input wave never passes to the output. The direct passages of waves from the input to the output and back are blocked by making the output valve junction, J_l, "weak" and "fast" compared with the neighboring junctions, J_m and J_{out}. The dynamics of Josephson junctions and voltage pulses corresponding to the propagation of the phase-change waves in the input, read, and output all-JJTLs are presented in Figs. 6(b) and 6(c).

One can switch from NDRO operation to the destructive read-out (DRO) by changing the parameters of the output valve junction, J_l, namely, making it slower. The DRO is implemented when only the first input 2π phase-change wave increases the J_m phase by about π. Another π increase is only available with the read wave. Since J_m is connected to J_l, the slower phase increase at the point of their connection allows J_v to switch twice with every input 2π phase-change wave, if the J_m phase is about $\pi + 2\pi n$, see the Supplemental Material [29]. At the same time, with a slowdown of J_l, J_m has time to switch from the $\pi + 2\pi n$ state, while the J_{out} phase increases by 2π. The DRO cell operates as a D flip-flop, see Figs. 6(d) and 6(e).

Notably, read data can be easily inverted. This is achieved by a simple swap of the connection order of J_r and J_{out}, see Fig. 6(f). In this case, J_m and J_{out} are connected to the ground through J_r. Thus, the stationary distribution of the currents and dynamics of the junctions change, so that the circuit parameters require an additional adjustment, see the Supplemental Material [29]. Simulations of the dynamics of NDRO and DRO cells with output inversion are presented in Figs. 6(g) and 6(h) and Figs. 6(i) and 6(j), correspondingly. The DRO cell here performs synchronous data inversion, which is the NOT logic operation.

C. Example of a cell design

We present only a simple combination of input and output circuits to write and read the logic state encoded in a 2ϕ-JJ phase so far. The functionality of a cell can be increased by connecting additional branches. For example, the NDRO output joined with the DRO cell forms a NDRO cell with separate inputs to set or reset the latch, see Fig. 7(a). An additional output interface circuit providing the NDRO is circled by a dotted line. Josephson junctions of this circuit are marked by capital "R" in their subscripts. The designation of other Josephson junctions are the same as those given in Fig. 6(a). The 2π phase-change wave entering the cell through J_{in} switches the logic state by increasing the J_m phase by π, while that entering the cell through J_r resets the state. The critical current of the Josephson junction connecting the NDRO branch to the DRO cell is small to decouple these parts.

In the design of this cell, we divide all JJs into "fast" and "slow" ones, with a correspondingly small or large value of the damping coefficient, see Fig. 7(c). After an optimization procedure, we find that the working margins of the bias currents, as well as of the parameters of the Josephson junctions, are greater than $\pm 20\%$ during low-speed tests, see Figs. 7(b)–7(d). The margins are expected to shrink as the operation frequency increases.

We add a small parasitic inductance in series to every Josephson junction of the considered circuit to examine its effect. The normalized inductance value is $l = 2\pi I_c L/\Phi_0 = 0.5$ (1.65 pH for $I_c = 0.1$ mA). While the values of parameters become clearly shifted, after an additional optimization procedure, the working margins are restored to above $\pm 20\%$. This illustrates the importance of the careful extraction of parameters of the circuits from the layout as well as the overall robustness of the proposed design approach to the existence of parasitic inductors.

D. Benchmark logic circuit design

We verify the validity of the proposed design methodology through the design of an 8-bit parallel adder as an example. The basic element of this adder is a half adder (HA) presented in Fig. 8(a). Here, the phase of the main 2ϕ-JJ, J_m, is changed by every 2π phase-change wave coming from data lines a or b through $J_{v(a,b)}$ junctions. The interface circuit of the output sum (J_{ls}, J_{rs}, J_s) provides destructive readout of the J_m state. The interface circuit of the output carry $[J_{lc}, J_{c(a,b)}, J_c]$ provides a nondestructive readout of the J_m state before it is changed by the data phase-change waves. Therefore, the carry readout is asynchronous with respect to the clock. Notably, data can flow sequentially or simultaneously to the HA cell. In the last case, the output junction of the carry branch, J_c, is switched due to the total effect of the two 2π phase-change waves. This is similar to the operation of the RSFQ AND cell [11]. Parameters of the half-adder JJs are presented in Table II within the Supplemental Material [29].

Notably, just a single 2ϕ-JJ is sufficient here to provide data storage. This is in contrast to the RSFQ HA, where insensitivity to the data delay comes at the cost of doubling the SFQ storage circuit [45]. Thus, the number of JJs in the presented schematic is even smaller than that in the RSFQ counterpart, despite the substitution of inductors for JJs.

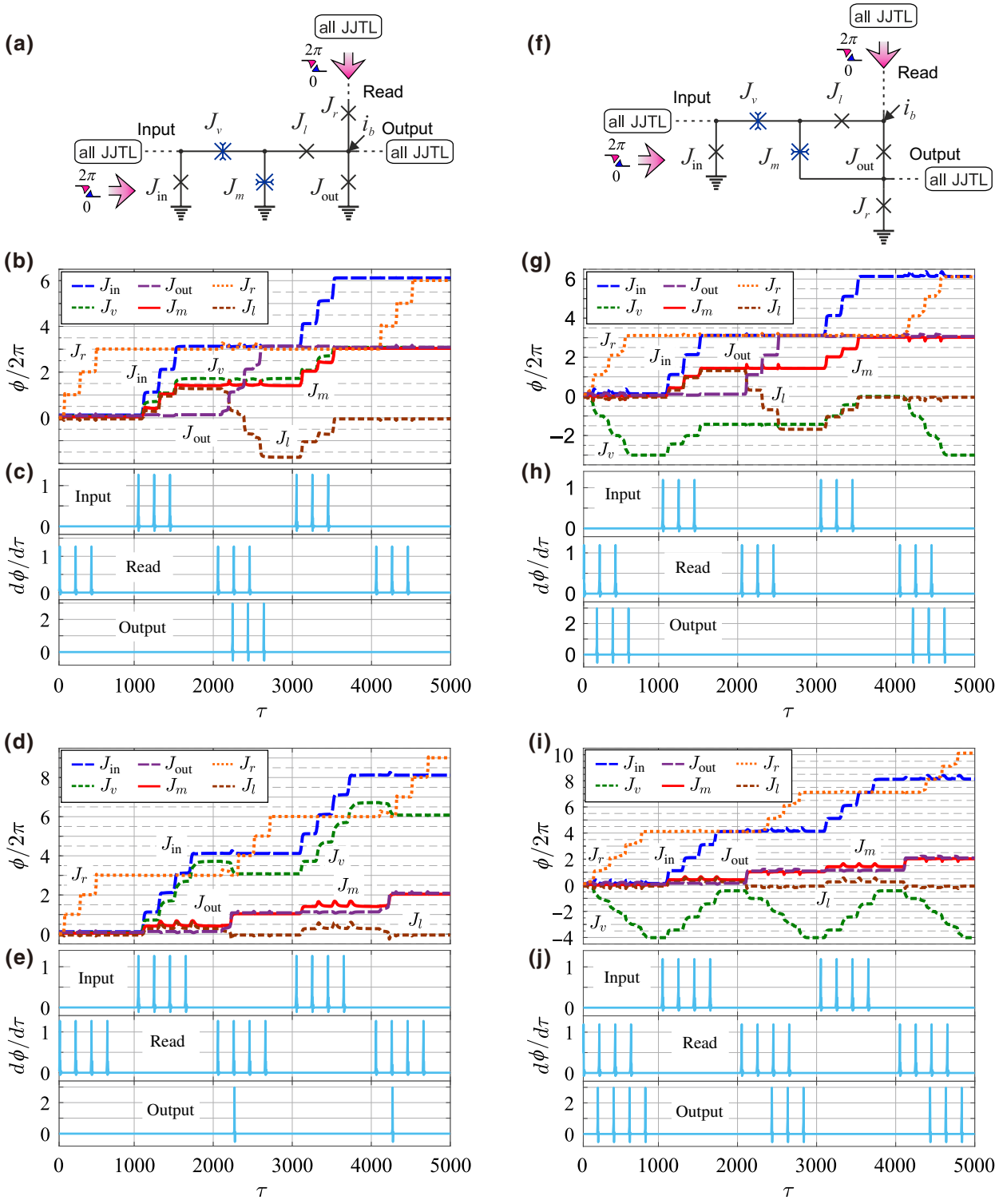

FIG. 6. (a) all-JJ cells based on basic block with controlled readout (NDRO and DRO) of main 2ϕ-JJ states without (a) and with (f) inversion of read data. Dynamics of phases of Josephson junctions and voltage pulses, corresponding to propagation of phase-change waves ($d\phi/d\tau$) in the input, read, and output all-JJTLs for NDRO (b),(c); DRO (d),(e); NDRO with output inversion (g),(h); and DRO with output inversion (i),(j) cells. Parameters of Josephson junctions are presented in Table I within the Supplemental Material [29].

An 8-bit ripple-carry-wave pipeline adder schematic is presented in Fig. 8(b). Its energy-efficient RSFQ (ERSFQ [46]) counterpart was proposed earlier as a process benchmark [47]. For an N-bit circuit, one needs $2N-1$ HA cells connected, in our case, by all-JJTLs and all-JJ confluence buffers (CBs). The total number of JJs in the

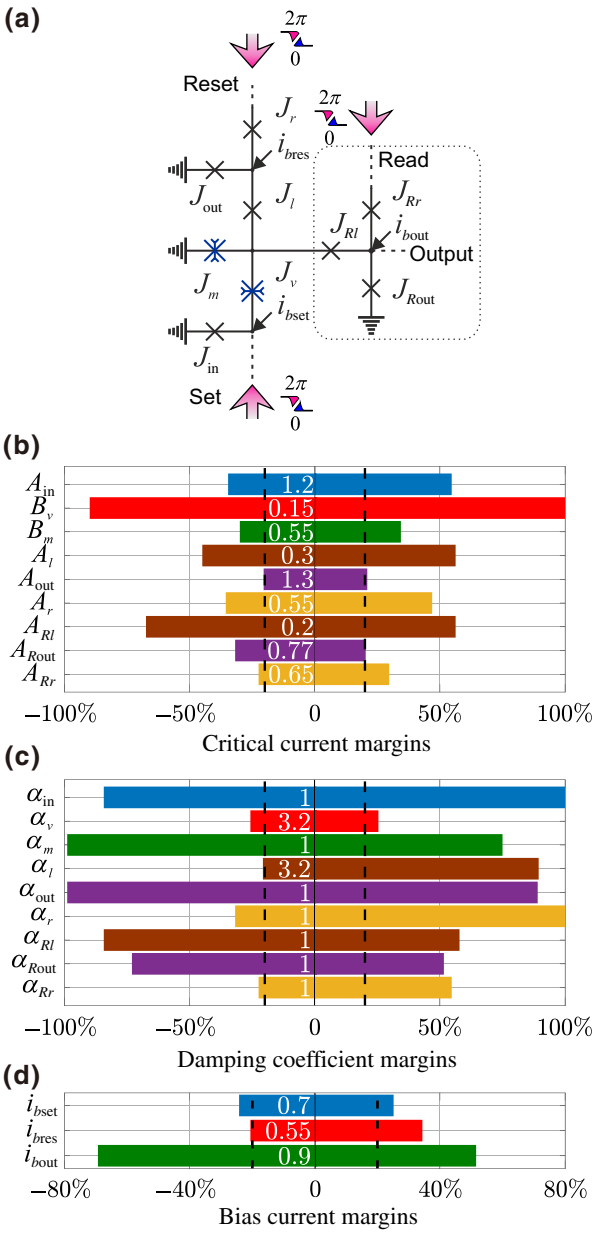

FIG. 7. (a) Schematic of NDRO cell with separate inputs to set or reset the latch formed from a combination of DRO cell with additional NDRO branch (latter is circled by a dotted line). Working margins of critical currents (b), damping coefficients (c), and bias currents (d). Optimal values of parameters are shown in corresponding panels. ±20% boundaries are shown by vertical dotted lines.

adder is 362 with 150 JJs in HAs (10 JJs per HA) and 212 JJs in all-JJTLs and CBs. An additional 150 JJs are in the clock distribution network. The summation operation is performed in a single clock cycle [47], with a total time delay (normalized to the inverse plasma frequency) of $\tau_\Sigma = 275$. The output data front is aligned, meaning that least significant and most significant bits are produced simultaneously.

The circuit's operation is simulated with various inputs. Voltage pulses corresponding to the phase-change waves in the a and b data branches, as well as in the sum branches, are shown in Figs. 8(c)–8(e), respectively. The last panel in Fig. 8(e) shows the output carry. The first example presents the summation of two randomly chosen numbers, $a = 0010\ 0111$ (39) and $b = 0101\ 0011$ (83), which results in the sum $= 0111\ 1010$ (122). The second example corresponds to the longest propagation of carry, $a = 0000\ 0001$ (1) and $b = 1111\ 1111$ (255), which results in the sum $= 0000\ 0000$ and generation of the output carry (256).

IV. DISCUSSION

With the presented utilization of 2ϕ-JJs, one can easily mimic the behavior of RSFQ circuits due to a certain 2ϕ-JJ CPR. However, other types of bistable junctions are also suitable. Using 0-π JJs instead of 2ϕ-JJs in the basic block would result in some shrinkage of the operation margins caused by a shallower depth of the potential well at $\phi = \pi$. Using ϕ-JJs with potential-energy minima at $|\phi| \leq \pi/2$ would additionally lead to some finite current in the output interface circuit in both states of the ϕ-JJ. Nevertheless, correct circuit operation is possible using these alternative implementations.

A nonzero first harmonic in the CPR provides two critical currents of the bistable JJ. This is due to different heights of potential barriers between the EPR minima. The difference in critical currents gives an opportunity to read out the state directly from the junction [41]. This could serve for further simplification of the schematics.

Logic states 0 and 1 correspond to zero and 2π phase changes in the presented circuits. At the same time, the operation of the cells is based on the transformation of the 2π phase change into π phase drops on the bistable JJs. One can consider an option for more complex information processing with the propagation of π phase-change waves. This includes the possibility of ternary logic-circuit design. Three options for the logical states can be associated with zero, π, and 2π phase changes. Manipulation with π phase-change waves instead of 2π ones can additionally increase the power efficiency [28].

The utilization of bistable JJs eliminates the need for SFQ storage, and hence, the necessity for technological implementation of the quantizing inductance. The inductor can be used as an interconnecting element or not used at all. The latter leads to the fact that the circuit's characteristics are determined only by the parameters of the Josephson junctions. Our results show that the all-JJ circuits can be designed using just a few values of JJ damping, which is promising for their implementation. While circuits without inductors can be implemented with more conventional 0- and π-JJs, the utilization of bistable Josephson junctions significantly decreases the total JJ count.

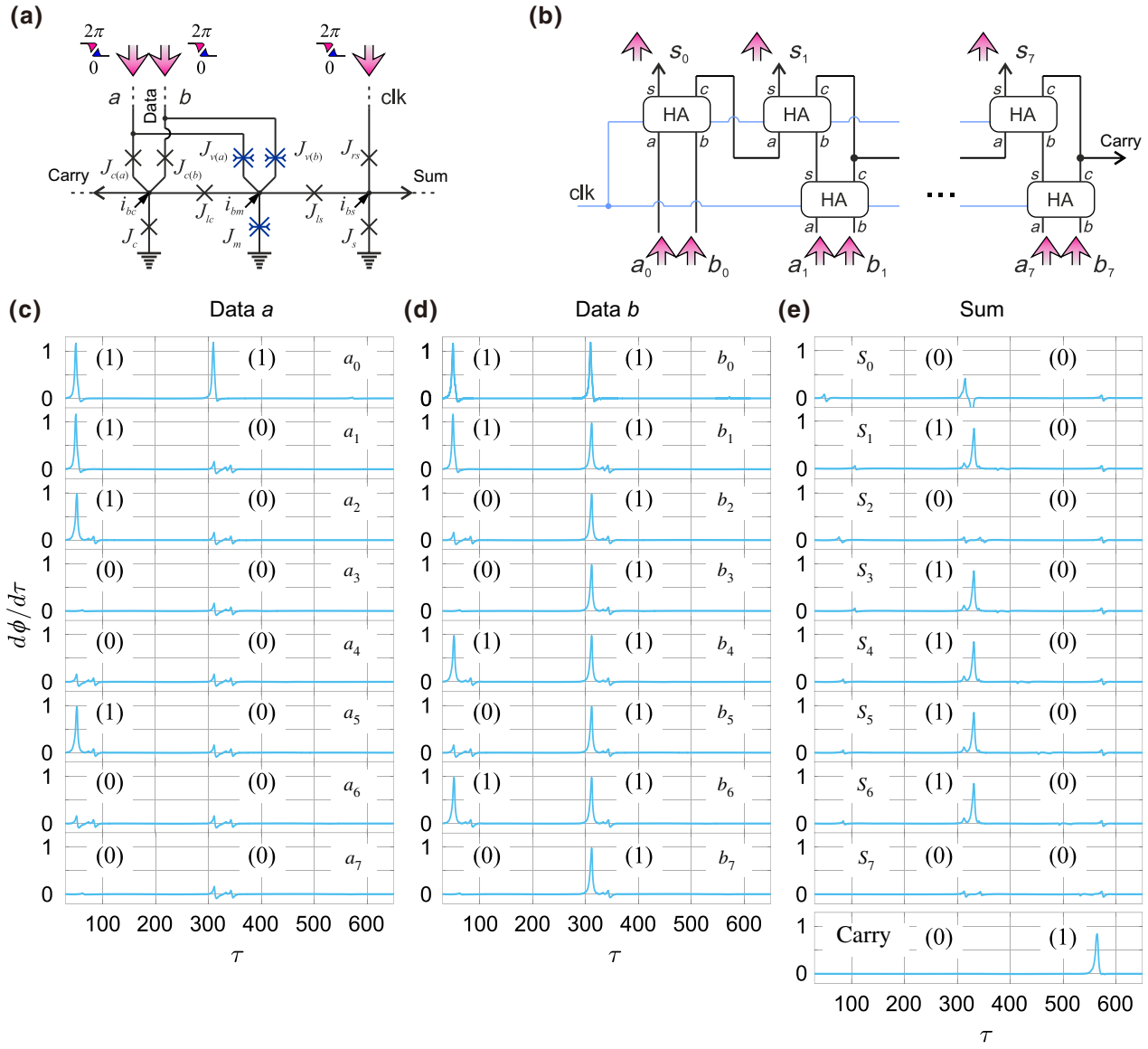

FIG. 8. (a) all-JJ half-adder schematic. (b) 8-bit ripple-carry adder schematic. Voltage pulses corresponding to phase-change waves in data branches *a* (c) and *b* (d), and sum branches (e); the bottom panel in the column presents the output carry.

We show that the all-JJ cells can be connected by all-JJTLs. However, the utilization of passive transmission lines (PTLs) looks more promising for long-range connections. It is shown that PTLs are suitable for high-density routing with low cross talk, allowing fast data transfer and precision-timing design of the circuits [48,49]. The cells can even be connected through PTLs only, although, with a relatively large width of PTLs, this option poses certain limitations on the integration density.

V. CONCLUSION

We consider different options for the implementation of the basic storage element of superconducting circuits. We argue that the use of inductors in conventional designs presents technological problems for scaling of the circuit. The utilization of a bistable Josephson junction as a storage element appears to be promising in this context. In this case, magnetic flux is not used as the physical representation of information. This eliminates the requirements imposed for inductors, including the possibility of completely removing them. We present a design methodology for the circuits without inductors based on bistable Josephson junctions. The methodology is used in the design of various basic cells, such as a controlled oscillator analogous to a conventional SFQ-to-dc converter, T flip-flop, D flip-flop, NDRO, NOT logic, and a half adder. A more complex benchmark logic circuit of an 8-bit parallel adder is designed as well. The working margins of the all-JJ NDRO cell with small parasitic inductances in

low-speed tests exceed ±20% in simulations. The cell is designed using only a couple of values of the JJ's damping coefficient, which is favorable for its implementation. The design of the half-adder cell shows that the total number of JJs in the all-JJ circuits can be less than that in the standard design. We conclude that the proposed utilization of bistable Josephson junctions is promising with respect to eliminating the need for quantizing inductance; possible simplification of the all-JJ circuit schematics; and a reduction of total JJ count, leading to space efficiency. The search for technological routes to bistable JJ fabrication and the development of information-processing methods using circuits based on such junctions are urgent tasks in this area of research.

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