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Novel Ultra-Low-Voltage Flip-Flops : Near-V_{th} Modeling and VLSI Integration

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***Abstract*—This paper presents two novel ultra-low-voltage (ULV) Single-Edge-Triggered flip-flops (SET-FF) based on the True-Single-Phase-Clocking (TSPC) scheme. By exploiting the TSPC principle, the overall energy efficiency has been improved compared to the traditional flip-flop designs while providing fully static, contention-free functionality to satisfy ULV operation. At 0.5V near-V_{th} level in 65nm bulk CMOS technology, the proposed SET-FFs demonstrate up to 11-45% and 7-20% of energy efficiency at 0% and 100% data activity rates compared to the best known SET-FFs. The proposed SET-FF can safely operate down to 0.24V of supply voltage without corrupting rail-to-rail voltage levels at its internal nodes. The integration of proposed SET-FFs in a 320-bit parallel shift register demonstrated up to 33% of clock network power, 17-39% of register power reductions compared to the state-of-the-art and commercial standard-cells at near-V_{th} level. In addition to these merits, with the aid of parasitic modeling, this paper re-evaluates the vital performance metrics of SET-FFs at near-V_{th} voltage domain, improving their characterization accuracy and enabling the VLSI integration for commercial end-use.**

Index Terms*—Single Edge Triggering, True Single Phase Clocking, Near/Sub-V_{th}, *Low Power Clock Network, Clock Slope Sensitivity, Ultra-Low-Voltage

I. INTRODUCTION

Flip-flops are essential sequential elements in synchronous designs, facilitating data storage and data synchronization in digital hardware [1]. Modern VLSI architectures typically require hundreds of thousands of flip-flops, given their complex pipeline structures [2]. Unlike the datapaths, the clock network's constraints are often stringent and its 100% activity rate leads to a significant portion of total power (∼40%) [3] to be consumed by the clock distribution. Hence a great emphasis was placed on improving flip-flops and thereby overall system-level energy efficiency in the past few years [4], [5].

The most well-established flip-flops are the single-edge-triggered flip-flops (SET-FF) due to their simple structure and compatibility with standard ASIC design flow. SET-FFs sample data at either the positive or negative edge of the clock signal. The conventional and the most common design of this kind is TGL24 [1] which can be found in commercial standard cell libraries. Due to the heavy clock loading of this design, transistor-level optimization of SET-FFs has been studied in recent research [4]–[6]. The recurring concept of true-single-phase-clocking (TSPC) has replaced the conventional dual-phase-clocking (DPC) scheme of the traditional designs. Unlike DPC, TSPC does not require complementary clock signals and does not need local clock buffers, leading to a two-fold reduction in clock load [5]. The total power dissipation of a flip-flop is given by:

$$P_{tot} = V_{DD}^2\{f_{clk}.(C_{clk} + C_{ff,clk}) + f_{dat}.C_{ff,dat}\} \quad (1)$$

where f_{clk}, f_{dat} represent the clock and the average data frequencies. C_{clk}, $C_{ff,clk}$ and $C_{ff,dat}$ are the capacitive loads seen at clock input, the internal clock paths and data paths respectively. In a nutshell, TSPC intends to minimize the previous two parameters.

In addition to the clock-load reduction, the fully static and contention-free operation is crucial for the ultra-low-voltage (ULV) operability. SET-FFs based on complementary master-slave latches have always been a good candidate for ULV operation [7] compared to some other alternatives such as pulse-triggered [8], [9] and C-element [10] based designs. A comprehensive analysis on their shortcomings against master-slave designs is given in [7], [11]. Despite these merits, certain prevalent master-slave SET-FFs such as XCFF [12], ACFF [13], TCFF [14] and 18T-FF [4] still suffer at ULV levels owing to the issues such as contention and lack of PVT resilience which have been already discussed in [5]. The TSPC24 [6] and TSPC18 [5] designs were found superior in terms of many aspects and hence will be used as the baselines in this paper.

Conventional CAD tools fall short when it comes to characterization and evaluation of non-conventional cell topologies. In evaluating certain parameters such as hold, recovery and removal times, the standard measurement scheme (i.e. 10% delay degradation point [15]) might fail to converge for certain designs and against certain operating conditions. Besides, the selection of a proper input stimuli for characterization plays a vital role at near-V_{th} levels. Therefore some alternative measurement schemes and the near-V_{th} parasitic modeling [16]–[18] will be studied in this paper.

To address all these concerns, we present more energy-efficient versions of TSPC SET-FFs, achieving the full-fledged functionality at ULV levels. The typical SET-FF operation and the issues of prevalent designs are detailed in Section II. Section III revisits the vital parameters of the flip-flops and the near-V_{th} modeling aiming at ULV operation. Section IV details the cell level merits of the SET-FFs based on Spice simulations. An accurate cell characterization strategy based on current composite source (CCS) modeling is presented

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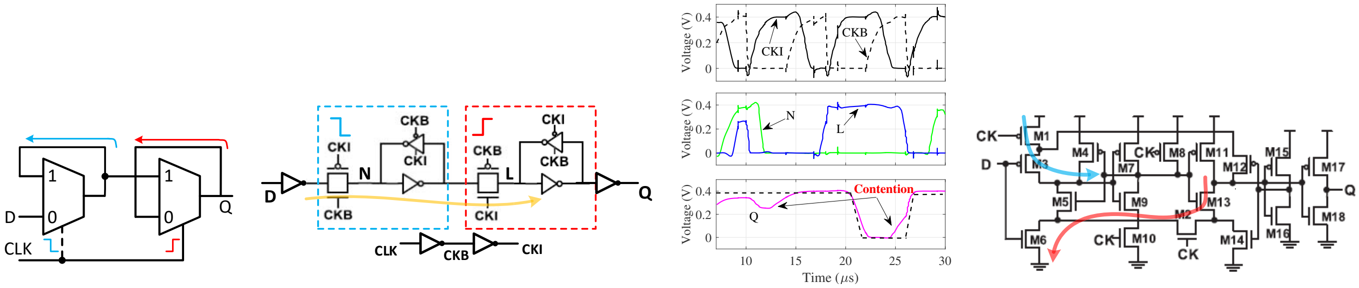


(a) (b) (c) (d)

Fig. 1: (a) SET-FF conceptual block diagram (b) TGL24 SET-FF (c) The clock overlap issue of TGL24 (SS, -40°C) at 0.4V (d) TSPC18 [5] worst-case setup(blue)/hold(red) paths

in Section IV. In Section V, the merits of the SET-FFs are evaluated in a higher-level integration (i.e. 320-bit Shift Register) through extensive post-layout simulations in 65nm bulk CMOS process technology. Finally, the conclusions are drawn in Section V.

II. MASTER-SLAVE LATCH SET-FFS

This section revisits the working principle and the critical features of the master-slave SET-FFs. Fig. 1(a) depicts a simplified block diagram of a SET design with multiplexer (MUX) based latches that operate in a complementary fashion. The data (D) captured at the negative clock phase (blue) will be immediately available at Q output by the next positive edge of the clock. Besides capturing, the input MUX should latch the captured data during the positive phase of the clock.

The conventional TGL24 [1] based on this master-slave arrangement is depicted in Fig. 1(b). This arrangement with input/output buffering is often found in commercial standard cell libraries. The clock overlap issue is a major concern in this design as depicted in Fig. 1(c). At ULV levels, a possible overlap between the negative (CKB) and the positive (CKI) phases of the clock can lead to data transparency (the orange arrow of Fig. 1(b)) between the capturing latch and the output MUX as well as between node *N* and *L*. Steeper clock transitions can alleviate this failure. However, this eventually increases the gate parasitics [16] of the local clock buffers and therefore the clock tree power.

With the aid of TSPC, this barrier can be overcome. Since TSPC does not require dual-phase clocking, it provides steeper clocked transitions ideal for ULV operation. Kim *et al.* [6] and Yunpeng *et al.* [5] proposed TSPC24 and TSPC18 designs based on this theory and their functionality has been proven to be superior at ULV levels. From TSPC**24** to TSPC**18**, the number of clocked transistors to the overall transistor count ratio has reduced from 5/**24** to 4/**18**. This is a significant improvement. The TSPC18 design with its worst-case setup(blue)/hold(red) paths is depicted in Fig. 1(d).

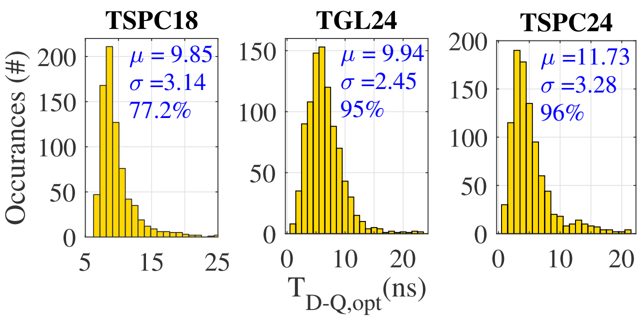


Fig. 2: PVT resilience and the 3σ yields (%) of 3 SET-FFs in terms of $T_{D\text{-}Q,opt}$ against 0.5V/TT/25°C and C_L=10fF conditions.

This design is superior in many aspects compared to other state-of-the-art designs. However, there is still room for improvement of two vital parameters: the hold time and the PVT resilience. Due to the long hold path as indicated in red color by M13→M2→M6 (obtained from simulations), the circuit performance under extreme ULV conditions becomes less favorable. This, on the other hand affects the optimal D-to-Q delay ($T_{D\text{-}Q,opt}$) and the clock-slope sensitivity (will be discussed later) [11] of the flip-flop. The PVT resilience of TGL24, TSPC24 and TSPC18 designs based on 1000 Monte Carlo iterations at typical near-V_{th} conditions is depicted in Fig. 2. As evident from the mean (μ) and the standard deviation (σ) values of $T_{D\text{-}Q,opt}$, the TSPC24 is the most PVT resilient design despite its very high clock load [5]. The latest TSPC18 design demonstrates the poorest 3σ yield despite its superiority. In a nutshell, this paper aims to overcome these drawbacks while providing a better energy profile than the latest TSPC18 design.

III. TSPC17 - PROPOSED FULLY-STATIC SET-FFS

The proposed SET-FFs based on complementary TSPC latches are depicted in Fig. 3(a)-(b). The left (M1-M10) and the right (M11-M17) portions of each circuit represent the negative (master) and the positive (slave) edge triggering latches of the SET-FF, respectively. The specific features of this design can be summarized as follows.

A. Fully Static Operation

Similar to TSPC18 [5], both TSPC17-V1/2 circuits have fully static storage elements in each latch. For instance, when D=0/CLK=0, the positive edge-triggered (left) latch captures $\overline{D}$ ('1') during the negative phase of the clock and stores it at node SP through M1 and M2. During this phase, node LKP is at logic '1' through M7, and therefore M4 is opened. As soon as the positive phase of the clock arrives (CLK=1), M7 closes and logic '1' at node SP opens M8 through M10, pulling node LKP at logic '0'. In this way, the original D ('0') is transferred

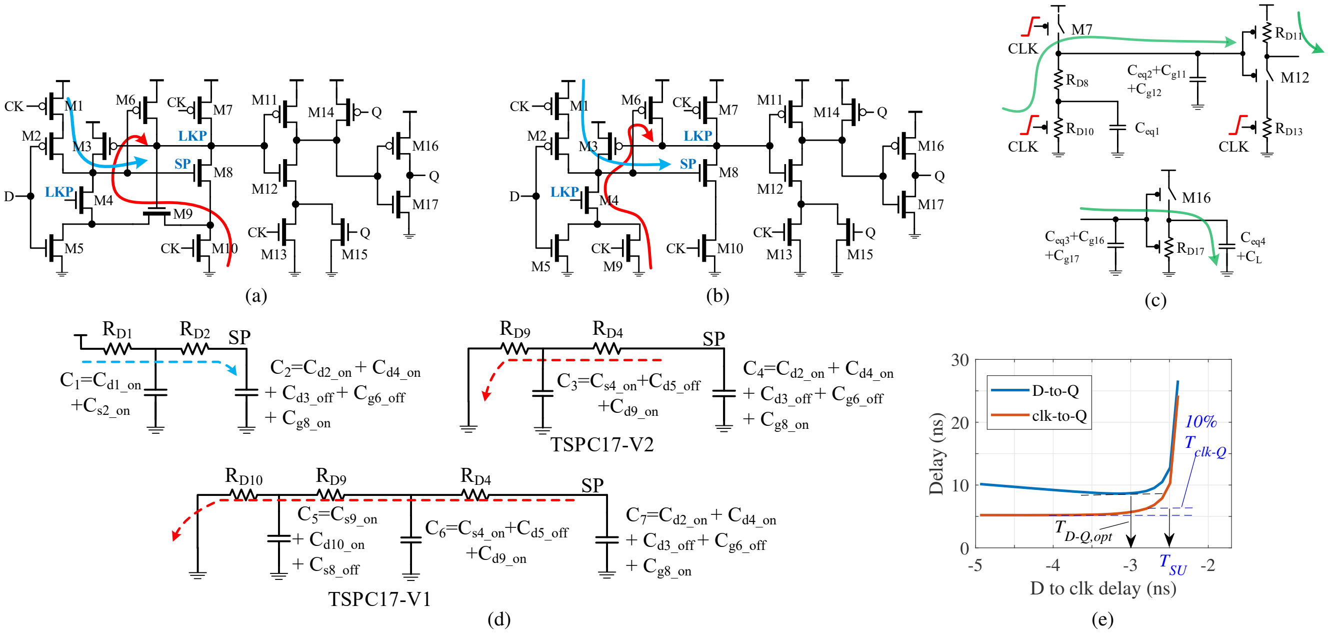

CK
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
D
Q
LKP
SP
(a)
(b)
CLK
R_{D8}
R_{D10}
R_{D11}
R_{D13}
R_{D17}
$C_{eq2}+C_{g11}+C_{g12}$
C_{eq1}
$C_{eq3}+C_{g16}+C_{g17}$
$C_{eq4}+C_L$
(c)
R_{D1}
R_{D2}
$C_1=C_{d1\_on}+C_{s2\_on}$
$C_2=C_{d2\_on}+C_{d4\_on}+C_{d3\_off}+C_{g6\_off}+C_{g8\_on}$
R_{D9}
R_{D4}
$C_3=C_{s4\_on}+C_{d5\_off}+C_{d9\_on}$
$C_4=C_{d2\_on}+C_{d4\_on}+C_{d3\_off}+C_{g6\_off}+C_{g8\_on}$
TSPC17-V2
R_{D10}
$C_5=C_{s9\_on}+C_{d10\_on}+C_{s8\_off}$
$C_6=C_{s4\_on}+C_{d5\_off}+C_{d9\_on}$
$C_7=C_{d2\_on}+C_{d4\_on}+C_{d3\_off}+C_{g6\_off}+C_{g8\_on}$
TSPC17-V1
(d)
Delay (ns)
30
20
10
0
-5
-4
-3
-2
D to clk delay (ns)
D-to-Q
clk-to-Q
10%
$T_{clk\text{-}Q}$
$T_{D\text{-}Q,opt}$
T_{SU}
(e)

Fig. 3: Proposed versions with worst-case setup(blue)/hold(red) paths indicated: (a) TSPC17-V1 (b) TSPC17-V2 (c) Clock slope sensitivity issue propagation in TSPC17-V2 (d) The worst-case setup/hold path parasitic decomposition of TSPC17-V1/V2 (e) $T_{D\text{-}Q}/T_{clk\text{-}Q}$ vs setup time (T_{SU}) of TSPC18 at 0.5VDD.

to node LKP. Furthermore, this new LKP value helps to sustain the original $\overline{D}$ ('1') value at node SP through M3 during the positive clock phase. This functionality is the same for both versions.

Similarly, when D=1/CLK=0, node SP reaches $\overline{D}$ ('0') through M4 and M5, so that M8 is closed. The original logic '1' stored at LKP (through M7) keeps conducting M4 through M9-M10 in version 1 and only through M9 in version 2 during the positive phase, preserving SP node at logic '0'. This eventually sustains logic '1' at LKP node through M6 during this period. To fully satisfy the static operation, M4 and M9 should be made smaller than M8 and M10 so that logic '1' at node SP when D=0/CLK=0, will not be reset during the next positive clock phase. This can be easily achieved by setting the W/L ratio of M4 to ∼2/3-1/2. The circuit is fully functional even for the standard minimum device sizing ($0.15\mu/0.06\mu$) in 65nm technology.

The slave latch (M11-M15) in both circuits is similar and transfers the stored value at node LKP to the output Q. The two circuits are only different by the arrangement of M9-M10. The clock load of the two versions is 4 and 5 gate inputs respectively. The slower hold path issue in TSPC18 is overcome in TSPC17-V1/2 designs by decoupling the D input transistors from the clocked transistors in the master latch, further improving the PVT immunity at ULV levels. This is indicated by the red arrows in Fig. 3(a)-(b).

B. Setup/Hold Time and $T_{D\text{-}Q}/T_{clk\text{-}Q}$ Delay Specifications

In the constraint measurements, always the worst-case specifications should be obtained from both '0/1' data inputs at the specific clock edge of the flip-flop. For instance, the parasitics along the M1-M2 path define the worst-case setup specification in both versions. Similarly, M10→M9→M4→M6 in TSPC17-V1 and M9→M4→M6 in TSPC17-V2 define the hold specifications. The improvement to these specifications is only restricted by the M4-M9 device sizing requirement stated in Section III-A. With the aid of parasitic modeling [16], the decomposed setup and hold paths of both circuits are depicted in Fig. 3(d).

Here, the charging and the discharging times of node SP through the given paths are considered as the minimum time delays for the D input to become stable and for M6 to properly latch the LKP value. R_D, $C_{d/s}$ represent the drain resistance and the parasitic capacitances (off/on state) of the MOSFETs respectively [16]. With the aid of the modeling scheme presented in [16], the minimum setup/hold requirements can be written as follows:

$$\begin{aligned} t_{setup} &= 0.69\ [R_{D1}C_1 + (R_{D1}+R_{D2})C_2] \\ t_{hold\_V1} &= 0.69\ [R_{D10}C_5 + (R_{D10}+R_{D9})C_6 + (R_{D10}+ \\ &\quad R_{D9}+R_{D4})C_7] \\ t_{hold\_V2} &= 0.69\ [R_{D9}C_3 + (R_{D9}+R_{D4})C_4] \end{aligned} \tag{2}$$

From [18], the expressions for the R_Ds at near-V_{th} levels can be reduced to:

$$R_{D\_P} \approx \frac{L}{(\lambda_{DS}+\lambda_{BS})WI_O} e^{\frac{-[(1+\lambda_{DS}+\lambda_{BS})V_{DD}-|V_{thp0}|]}{\eta v_T}} \tag{3}$$

$$R_{D\_N} \approx \frac{L}{(\lambda_{DS}+\lambda_{BS})WI_O} e^{\frac{-[(1+\lambda_{DS}+\lambda_{BS})V_{DD}-V_{thn0}]}{\eta v_T}} \tag{4}$$

where $\lambda_{BS/DS}$ represent the body and the DIBL effects of the MOSFETs. Other terms have their usual meanings [18]. Note that the term λ_{BS} will diminish in the transistors whose V_{BS}=0 (i.e. M1, M10). The hold value of TSPC17-V1 is slightly higher than the TSPC17-V2 version. Both have similar worst-case setup times. More importantly, we could consider the operation of the transistors to predict the nature of the hold constraints. For instance, when D=1/CLK=0 in TSPC17-V2, the corresponding value at node LKP is already latched through M5→M4→M6. As soon as CLK=1, the same condition is maintained through M9→M4→M6. The time difference between these two operations is too small, so that TSPC17-V2 should result in a negative or a quite small hold time. For TSPC17-V1, this should be larger than TSPC17-V2 or even slightly positive, due to the longer hold path M10→M9→M4→M6.

Another crucial parameter that is often overlooked in flip-flops is the data-to-Q delay ($T_{D\text{-}Q}$). Some authors only consider clk-to-Q ($T_{clk\text{-}Q}$) delay to evaluate circuit performance while it is not recommended as a rigorous metric for flip-flop performance [5], [11], [19]. On the other hand, ($T_{clk\text{-}Q}$) is an important parameter for CAD STA tools and therefore utilized in cell characterization rather than $T_{D\text{-}Q}$. In this work, we consider minimum $T_{D\text{-}Q}$ ($T_{D\text{-}Q,opt}$) as in [11] for the cell-level performance and energy measurements in Section IV. $T_{clk\text{-}Q}$ will be used along with the setup times in ASIC library generation. The relationship between these two parameters is highlighted in Fig. 3(e). As depicted, the $T_{D\text{-}Q}$ gradually converges to the minimum $T_{D\text{-}Q,opt}$ point and after that it exponentially increases. $T_{clk\text{-}Q}$ is almost a constant till its tripping point and it also exponentially converges to $T_{D\text{-}Q}$ due to the meta-stability of the flip-flop. Traditionally, the 10% delay degradation point (10% of constant $T_{clk\text{-}Q}$ as shown in Fig. 3(e)) [15] defines the setup time T_{SU} of the flip-flop.

C. Contention Free Operation

In the proposed TSPC17-V1/V2 versions, the excitation of the internal nodes (SP, LKP) occurs in different clock phases and it avoids contention in the master latch. For instance, M7 and M8-M10 or M1-M2 and M9-M10 paths never operate simultaneously. Similarly in the slave latch, the latching transistors M14 and M15 are blocked by M11 and M12 to avoid possible raise conditions at the output node. In this way, possible short circuit paths are avoided and the robustness of the circuits is improved at ULV levels.

D. Clock Load and Clock Slope Sensitivity

Both clock load and the clock slope sensitivity of flip-flops are vital parameters to the clock network design [11]. The TSPC relaxes the sizing of clocked transistors and in fact, minimizes the overall clock load. A higher clock slope sensitivity [19], on the other hand, requires larger clock buffers and this parameter was shown to be worst for the traditional TGL24 [19] design owing to the dual-phase clocking. However, this has not been evaluated for TSPC SET-FFs in previous literature. In a nutshell, the effective capacitive load seen at the clock input and the clock slope sensitivity determine the strength of the required clock buffers in the clock network design. In cell characterization, the sensitivity is usually quantified as the clk-to-Q rise/fall propagation delay against different clock slew rates and output loads.

Fig. 3(c) illustrates the clock slope sensitivity propagation of TSPC17-V2 from the master latch output to the entire slave latch. The opened switches denote off-state MOSFETs (i.e. M7) in the circuit. The inertial delay to a clocked transistor is defined as its gate input signal delay to activate the transistor. This entirely depends on the local parasitics [16] and the driving capability [19] of the clock drivers. The inertial delay is denoted by τ_{D} [16] and is evidently degraded by larger clock slopes. Considering the CLK=↑/D=0/Q→0 operation of Fig. 3(c), the $T_{clk\text{-}Q}$ delay through M10 in the slave circuit can be computed as [16]:

$$t_{clk-M10-Q} = \tau_{D10} + 0.69\,[R_{D10}C_{eq1} + (R_{D10}+R_{D8}) \\ (C_{eq2}+C_{g11}+C_{g12}) + R_{D11}(C_{eq3}+C_{g16}+C_{g17})) \\ + R_{D17}(C_{eq4}+C_L)] \tag{5}$$

where C_{eq}s represent equivalent drain/source parasitics and $t_{r/f}$ represents rise/fall times of the clock signal. Here it is assumed that the parasitic constant 0.69RCs to M11-M12 and M16-M17 gate terminals are larger than their τ_{D}s and hence their τ_{D}s are not added to the equation. Moreover from [16], the time variant nature of R_{D10} and C_{eq1} due to the degraded clock is given by:

$$C_{eq1} = \int_{t_1}^{t_2} C_k\,dt, \quad R_{D\_10} \ = \int_{t_1}^{t_2} R_k\,dt \quad ; \ t_{r/f} = t_1 - t_2 \tag{6}$$

It is evident from eq. (6) that the increased $t_{r/f}$ due to the clock slope degradation eventually increase τ_{D10}, R_{D10} and C_{eq1} parameters in eq. (5) and therefore a larger $T_{clk\text{-}Q}$.

IV. CELL-LEVEL PERFORMANCE EVALUATION

This section evaluates the cell-level figures of merits of the SET-FFs discussed in this paper. Prevalent designs such as TGL24 [1], TSPC24 [6] and TSPC18 [5] are compared to the designs proposed in this paper. All the designs were implemented in 65nm bulk CMOS technology with layout/parasitic extracted in the Cadence Virtuoso environment. The simulations were carried out in Cadence Spectre Spice environment. In all SET-FFs, PMOS/NMOS width ratio of internal devices was set to 0.28μ/0.2μ and the output driver (inverter) to 0.45μ/0.3μ, respectively. This specification is sufficient to withstand ULV operation and brings fairness to the evaluation. The worst-case input scenario for each metric of each SET-FF is considered. For instance, under typical conditions (TT, 25°C) at 100% data activity rate, TGL24 consumes its highest power when it samples logic '1'. Similarly, its worst-case $T_{D\text{-}Q,opt}$ is observed when CLK=↑/D=1.

A. Power, Delay and PDP of DET-FFs

Fig. 4(a)-(b) depict the true power consumption of SET-FFs against 100% and 0% data activity rates (α) at 100 MHz, under typical (TT/25°C) conditions. The measurement setup is depicted in Fig. 4(d). When α=100% (Fig. 4(a)), proposed versions (TSPC17-V1/2) consume the lowest power. They are followed by TSPC18, TSPC24 and TGL24, consuming 12-16%, 32-37% and 46-47% more power respectively at 1.2-0.5V levels. Interestingly, when α=0% (Fig. 4(b)), TSPC18 outperforms both proposed versions by ∼16-24% at 0.5-1.2V

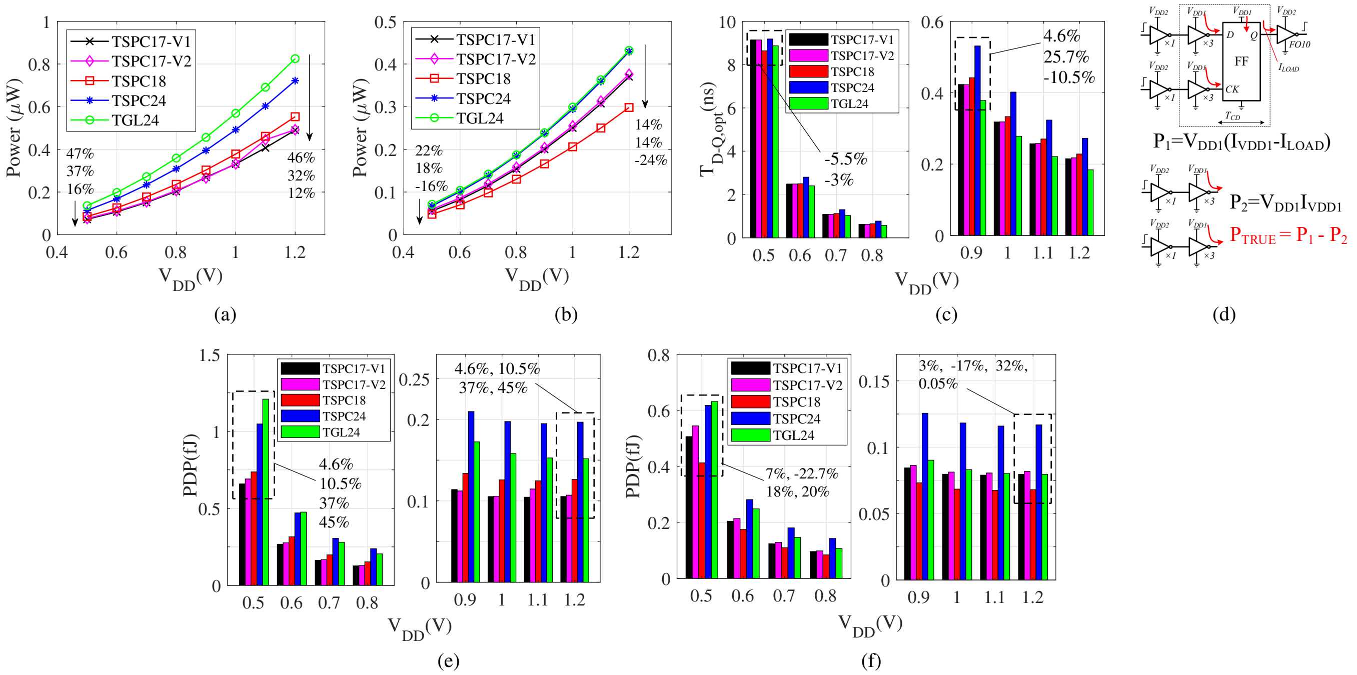


Fig. 4: (a)-(b) Power consumption at α=100-0% (c) Worst-case $T_{D\text{-}Q,opt}$ (d) True power measurement (excluding drivers and loads) (e)-(f) PDP (Power×$T_{D\text{-}Q,opt}$) at α=100-0%⟶All measurements under TT, 25°C conditions.

levels. Still the proposed versions are superior to TSPC24 and TGL24, consuming 14-18% and 14-22% less power at the same voltage levels. When the flip-flops are under a considerable switching activity rate, the proposed TSPC17-V1/2 designs are the best option for low power.

From Fig. 4(c), the TSPC24 is evidently the slowest design. The traditional TGL24 outperforms all other designs in most of the cases except at 0.5V. Proposed versions outperform TSPC18 and TSPC24 in all levels except at 0.5V. More specifically at 0.9V, TSPC17-V1/2 are 4.6%/25.7% faster than TSPC18/TSPC24 designs and 10.5% slower than TGL24. All in all, the proposed versions showcase balanced trade-offs between power-delay profiles.

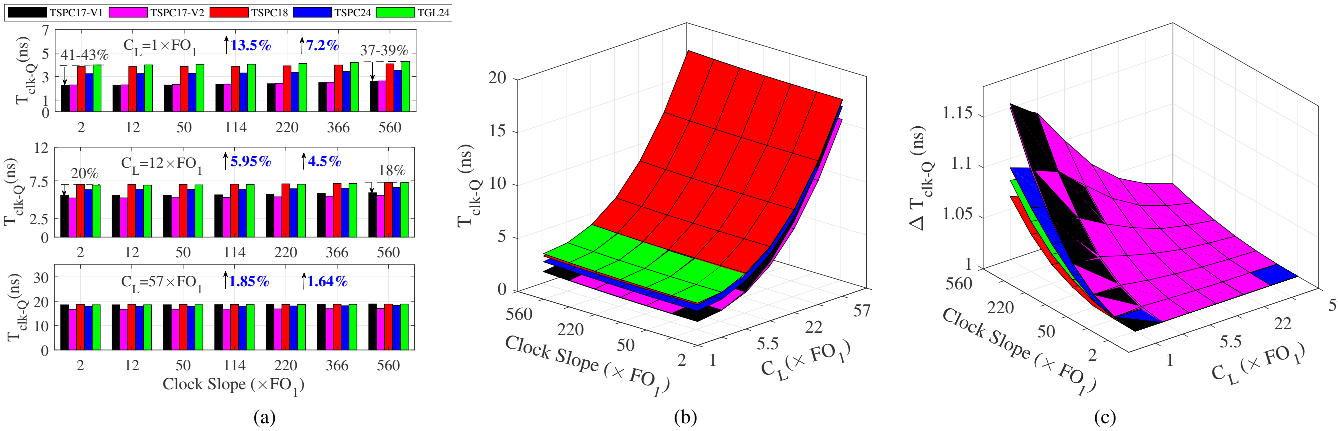
The overall energy efficiency of SET-FFs in terms of power-delay-product (PDP) is depicted in Fig. 4(e)-(f). This calculated by taking the product between power and $T_{D\text{-}Q,opt}$ [11]. When α=100%, similar to the power profile, proposed versions outperform all other designs. More specifically TSPC17-V1 is 4.6%, 10.5%, 37% and 45% better than TSPC17-V2, TSPC18, TSPC24 and TGL24 designs at 0.5V respectively. Similar savings can be observed at 1.2V as well. However when α=0%, TSPC18 becomes the most energy efficient design owing to its better delay and lower power at zero activity rates. Except this case, TSPC17-V1/2 versions demonstrate better or comparable energy efficiency to other designs at all voltage levels. Even though TSPC18 exhibits graceful numbers when α=0%, such scenarios rarely exist.

B. Clock Slope Sensitivity and $T_{clk\text{-}Q}$ Degradation

The impact of the clock slope sensitivity to the $T_{clk\text{-}Q}$ was briefed in Section III-D. Fig. 5 gives a deeper look into the impact of the clock slope and the output load to the propagation delays of flip-flops at 0.5V typical near-V_{th} level. This impact has been quantified by the increase of the $T_{clk\text{-}Q}$ propagation delays in Fig. 5 (a)-(b).

In [19], the clock slope sensitivity has only been evaluated as the factor of the increase of $T_{clk\text{-}Q}$ delay ($\Delta T_{clk\text{-}Q}$). However this does not accurately reflect the clock slope impact to the clock network design. In a realistic design environment, the absolute $T_{clk\text{-}Q}$ values are more meaningful to determine the required clock buffer strength than the $\Delta T_{clk\text{-}Q}$. Fig. 5(a) illustrates this behavior against different clock slopes and the output loads. Here FO1 load (C_L) represents the capacitive load of a ×1 inverter at Q output. Conversely, FO1 slope represents the clock slew when the ×1 clock driver drives ×1 inverter load. From Fig. 5(a), the lowest $T_{clk\text{-}Q}$ delay can be observed in proposed TSPC17-V2 version against all slope/loading conditions. This is followed by TSPC17-V1, TSPC24, TSPC18 and finally TGL24 respectively. More specifically when C_L=1×FO$_1$ and 12×FO$_1$, proposed versions are roughly 37-43% and 18-20% faster than the traditional TGL24 version. In the same figure, it can be observed that, when the clock slope increases from 2×FO$_1$ to 560×FO$_1$ at C_L=1×FO$_1$, the $\Delta T_{clk\text{-}Q}$ of TSPC17-V1 and TGL24 designs has increased by 0.35 ps from 2.25 ns (13.5%) and 0.31 ps from 3.9 ns (7.2%) respectively. For other loading conditions, this difference is smaller.

Fig. 5(b) represents the absolute values of $T_{clk\text{-}Q}$ for all slope/load conditions. As depicted, TSPC18 is the slowest design in most cases. The fastest design is TSPC17-V2 and it is followed by the rest similar to previous case. The normalized



(a) (b) (c)

Fig. 5: (a)-(b) Impact of the clock slope and the output load (C_L) of SET-FFs on T_{clk-Q} (c) ΔT_{clk-Q} against clock slope and C_L

T_{clk-Q} to the corresponding $T_{clk-Q,\ min}$ of each loading condition, or in other words ΔT_{clk-Q} is given in Fig. 5(c). Despite the faster T_{clk-Q} operation, the proposed designs now show a higher clock slope sensitivity (normalized to 1×FO$_1$ slope/load) compared to the other designs. However this should not be mistaken as an inferiority as the absolute values matter most in a realistic situation.

C. PVT Resilience of TSPC17-V1/2

Fig. 6 depicts the PVT variations of the proposed SET-FFs. Recall that the setup paths of the proposed designs are identical to the TSPC18 version. As anticipated in Section II, both TSPC17-V1/2 designs exhibit better μ, σ and yields compared to the latest TSPC18 design (see Fig. 2) thanks to their faster hold paths. However for the mentioned device aspect ratios (internal=0.28μ/0.2μ and output=0.45μ/0.3μ), still the TGL24 and TSPC24 designs demonstrate better resilience despite their circuit overhead. All in all, the proposed designs deliver balanced trade-offs between the PVT resilience and the power consumption.

V. NEAR-V_{th} CHARACTERIZATION STRATEGY

The accuracy at ULV levels is paramount for the characterization and VLSI integration of flip-flops. Even if the CCS scheme [20] is recommended for accurate timing, power or noise modeling, the automated characterization has posed a significant impediment to its adoption [21] and hence requires a pre-characterization flow. In particular, following measurement scenarios should be re-evaluated to improve the accuracy of ULV flip-flops.

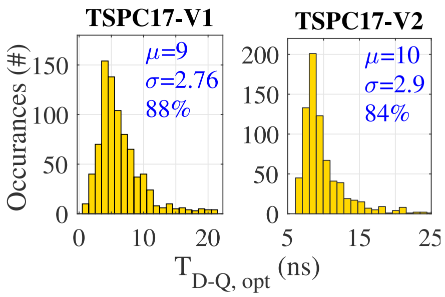


Fig. 6: PVT resilience and the 3σ yields (%) of TSPC17-V1/2 against 0.5V/TT/25°C and C$_L$=10fF conditions

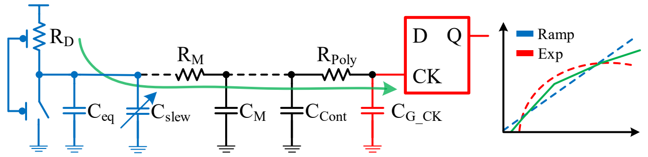


Fig. 7: CCS driver (blue) / receiver (red) model with RC networks

A. Stimuli generation in CCS driver model

Generally, a cell is characterized for different input slew and output load combinations similar to the case in Fig. 5(a)-(b). In reality, the input signal waveform to the cell may arrive from any driving cell. Hence the stimulus of a fast ramp function used in typical cell characterization may significantly differ from the actual pre-driver cell despite their same slew value. This is vital for flip-flops due to their impact on the design constraints. To minimize this error, it is recommended to use an averaged waveform signal [15] based on the empirical values of two extremes; a fast ramp function of no RC network and a slow/exponential function with a significant RC network. This situation is illustrated in Fig. 7. In this, the intrinsic parasitics to the CCS driver are denoted by R_D and C_{eq}. C_{slew} is a pure capacitive load and used to adjust the input slew value to the cell. R_{Poly}, C_{Cont} and C_{G_CK} represent the poly-silicon

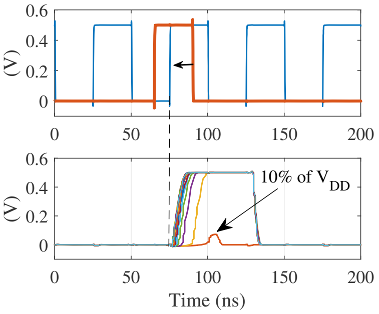


Fig. 8: Data (red) sweeping towards the clock signal (blue) and the glitch-peak criteria at 0.5V/TT/25°C.

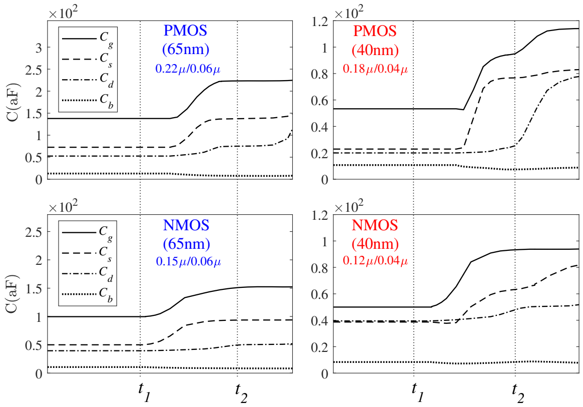


Fig. 9: The parasitic behavior of MOSFETs during the switching at near-V_{th} levels (off→on; rise/fall time = t_1-t_2) [16].

wire, the metal1-poly contact and intrinsic parasitics at the CCS receiver. The waveform *Ramp* and *Exp* represent the two extreme stimuli depending on the depth of R_M/C_M network and the drivers. The averaged piece-wise linear (PWL) waveform is represented in green. The commercial characterization tools (i.e. Cadence Liberate) can be instructed to pre-calculate the extremes and the average based on all possible driver/wire-load conditions. For instance, a given slew can be generated in *Ramp* and *Exp* fashions by using the strongest-driver/fastest RC wire-load and the weakest-driver/slowest RC wire-load combinations, respectively. The use of such an analytical waveform instead of an active driver avoids the impact of secondary effects such as Miller effect to the circuit.

B. Constraint Measurements

Typical flip-flop constraints include setup/hold, recovery/removal (asynchronous) and minimum pulse width measurements. Traditionally, these measurements were quantified by the 10% delay degradation method [15], [22], [23] similar to T_{SU} in Fig. 3(e). However in certain cases and for certain designs, the binary search algorithms [24] in the general setup cannot arrive to a solution. For instance, the hold time of TSPC17-V2 is quite small and therefore sweeping of D with respect to the CK (clock) results a diminutive resolution in clk-Q delays. In such a case, capturing the 10% output degradation point is difficult and the output glitch peak of the flip-flop which occurs before that can be considered as an alternative. Fig. 8 illustrates this behavior of the TSPC17-V2 design in which, the data pulse (red) is swept towards the rising edge of the clock (blue) signal. In this particular case, even if the 10% degradation is found by excessive number of bisection runs, the resulting hold time is too small and does not make much sense. Instead, the 10% V_{DD} crossing point of the output glitch peak is used. The removal constraint may utilize this method for the asynchronous (set/reset) inputs as well.

C. The Input Capacitance Measurements

In ASIC libraries, the capacitance measurements are stored as rise/fall dynamic capacitance under a specific input pin of a cell. The accuracy of these measurements is vital for flip-flops, i.e. direct impact on the clock network power. Typical cell characterization measures the instantaneous dynamic capacitance of an input during the switching time of the MOSFET [25]. This is fair for a timely invariant response (i.e. For C_{Cont} and C_M in Fig. 7) which is not the case for the intrinsic parasitics (C_{G_CK} in Fig. 7) owing to the weak channel formation and fringing effects [18] at near-V_{th} levels. The behavior of MOSFET's intrinsic parasitics in 65nm and 40nm nodes [16] is depicted in Fig. 9. Instead of the instantaneous capacitance, the effective average capacitance during t_1-t_2 period should be used in measurements. For C_{G_CK}, this can be calculated as:

$$C_{av} = \frac{1}{\frac{dV(t)}{dt}} \int_{t_1}^{t_2} i(t)\, dt \tag{7}$$

where *i(t)* and *dV(t)/dt* represent the CCS receiver injected current and the slew rate of the CCS driver waveform respectively. For better accuracy, the CCS capacitance measurement thresholds should be at 1% and 99% of the input V_{DD} level.

TABLE I: 320-bit Shift Register Gate-Level Power (μW) and Clk_{max} (ns)

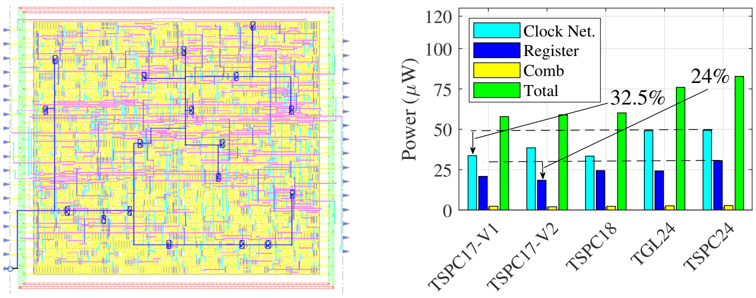
Design (μW/ns)	Power_SP	Power_GL	Clk_SP	Clk_GL
TSPC17-V1	41.40	41.60 (0.48%)	10.70	10.66 (0.37%)
TSPC17-V2	41.30	40.80 (1.21%)	11.10	11.00 (0.72%)
TSPC18	43.10	42.20 (2.09%)	11.00	11.10 (0.90%)
TSPC24	57.50	56.33 (2.03%)	12.50	12.50 (1.18%)
TGL24	67.76	67.97 (0.31%)	10.35	10.54 (1.80%)

TABLE II: 320-bit Shift Post-Layout Power (μW) and Clk_{max} (ns)

Design	Power(μW)	Clk_max	Clk_load(fF)	Area
	(α=100%→20%)	(ns)	(gate/wire)	(μm^2)
TSPC17-V1	57.86 (30%)→39.4 (30%)	14.8	683/177	3001
TSPC17-V2	58.90 (29%)→43.5 (22%)	14.5	793/186	2980
TSPC18	60.15 (27%)→38.7 (31%)	14.3	755/187	3101
TSPC24	82.74→56.0	15.0	1125/230	4338
TGL24	76.05 (8.1%)→54.6 (2.6%)	14.9	398/159	3304

VI. VLSI INTEGRATION OF ULV SET-FFS

This section summarizes the merits of the SET-FFs and the proposed characterization strategy in a large-scale integration. First, we present a lightweight experiment to evaluate the characterization accuracy of SET-FFs, only with gate-level parasitics. The 320-bit shift register (20 FFs in a chain×16 parallel chains) presented in [5] is utilized for this experiment. We use Cadence Liberate for cell characterization, including intra-cell parasitics, Synopsys Design Compiler for logic synthesis and Synopsys PrimeTime for the gate-level delay/power (Clk_{GL}/$Power\_{GL}$) measurements. The latter is compared to the Cadence Spectre Spice simulations (Clk_{SP}/$Power\_{SP}$) in Table I for different SET-FFs under 0.5V/TT/25°C conditions. Note that the 16 chains of 20 SET-FFs (in each chain) work concurrently at 100% data activity rate. The power consumption was measured at 71 MHz operation and the observations evidently reflect the cell-level merits of each SET-FF (Section IV-A) in the shift register integration. More importantly, the error between the gate-level digital simulations and the Spice-level analog simulations was maintained at $\leq$2% for all the designs thanks to the adopted characterization strategy.



(a)

(b)

Design / Cell Area	$V_{DD,min}$	Setup (ns)	Hold (ns)
	SS/-40°C	0.5V/TT/25°C	
TSPC17-V1 (6.2μm^2)	0.24V	3.0	0.14
TSPC17-V2 (6.2μm^2)	0.24V	2.5	0.02
TSPC18 (6.5μm^2)	0.28V	3.0	2.80
TSPC24 (7.8μm^2)	0.28V	4.2	0.25
TGL24 (6.9μm^2)	0.30V	1.8	0.83

(c)

Fig. 10: (a) Layout of the 320-bit shift register (clock tree highlighted) (b) Worst-case power break-down of the shift-register (0.5V/TT/25°C) (c) $V_{DD,min}$ and setup/hold specifications of the SET-FFs at worst and typical corners (setup/hold at C_L=FO4 and D/CLK slopes=1ns).

A. 320-bit Shift Register: SET-FFs in Isolation

A more comprehensive analysis based on the fully placed and routed designs in the Cadence Innovus environment is given in Table II. This accounts for both cell (*.lib)* / interconnect (*.spef*) level parasitics of the shift registers for which the numbers were obtained from less cumbersome digital simulations. In the physical design experiment, the maximum transition of the data paths (Tr_{max_d}), the clock network (Tr_{max_clk}) and the clock skew (t_{skew}) were set to 20%, 10% and 10% of the clock frequency (66.66 MHz) respectively under 0.5V/TT/25°C conditions. The hold buffers were not needed for this experiment. However, additional buffers have been used to fix the transition/capacitive violations in the data paths. For the clock-tree synthesis, only the balanced inverters (CKINVX) in the cell library were used.

The clock load ($\text{Clk}_{\text{\_load}}$) in Table II represents the summation of total gate inputs from the clock buffers, standard cells and the wire loads of the clock line. TSPC17-V1, TSPC17-V2, TSPC18, TSPC24 and TGL24 designs required 104, 117, 121, 180 and 70 clock-tree components respectively. Despite the local clock buffer usage in the TGL24 design (Fig. 1(b)), its clock input pin is just an inverter load. Therefore, the required number of clock network inverters/buffers during the clock-tree synthesis for TGL24 shift register is fairly lower than the other designs. Hence the lowest gate load of 398 fF in the clock line. Conversely, TSPC24 reported the highest number owing to its higher clock input load and higher $T_{clk\text{-}Q}$ sensitivity. These experimental results evidently justify that the absolute $T_{clk\text{-}Q}$ value has more impact to the clock network power than $\Delta T_{clk\text{-}Q}$ as mentioned in Section IV-B.

Moreover, the complexity of the TSPC24 cell slightly increases the routing congestion and therefore leads to a slightly higher wire load in the clock line. This is reflected in the area number as well. All designs have somewhat comparable critical path delays, while TSPC18 is the fastest design. This observation is aligned with $T_{D\text{-}Q}$ delays in Fig. 4(c). The proposed designs consume the lowest power in the shift register. TSPC17-V1, TSPC17-V2 and TSPC18 designs consume 30%, 29% and 27% less power than the most power-hungry design (TSPC24) at 100% data activity rate. Observations are similar for the 20% activity rate as well. As anticipated, these designs are even superior to the conventional TGL24 design in the commercial standard cell library. For the 320-bit shift register, a correlation between the gate-level and post-layout level power numbers can be clearly seen. The layout of the 320-bit shift register is illustrated in Fig. 10(a).

A detailed breakdown of the worst-case power (α=100%) for this experiment is given in Fig. 10(b). As depicted (the total power is already given in Table-II), the lowest clock network power is reported by TSPC17-V1 and TSPC18 designs and followed by TSPC17-V2. This is obvious since TSPC17-V2 requires 1 additional clocked transistor (see Fig. 3(a)-(b)). Consecutively, TGL24 and TSPC24 power numbers stand in this category. More specifically, TSPC17-V1's clock network power is 13.6%, 32.5% and 32.2% lower than TSPC17-V2, TSPC24 and TGL24 while being comparable to TSPC18. In the register power category, TSPC17-V2 saves roughly 11.4%, 24.6%, 39.8% and 24% of register power compared to TSPC17-V1, TSPC18, TSPC24, TGL24 designs respectively. All in all, TSPC17-V1/2 designs show their superiority in different categories.

Additional specifications related to the SET-FFs are summarized in Fig. 10(c). $V_{DD,min}$ represents the lowest voltage for which the circuit still functions correctly. The proposed versions can safely operate down to 0.24V at SS/-40°C process corner owing to the faster setup/hold paths of the circuits. This is also proven by the worst-case setup and hold values in the table. TSPC17-V1/2 report the smallest (positive) hold values and will, therefore relax the hold buffer requirement in complex digital designs.

CONCLUSION

This work presented novel ultra-low-voltage (ULV) SET-FFs based on the True-Single-Phase-Clocking scheme to improve the clock network and register power efficiency in digital subsystems. In addition to the power saving, proposed designs provide fully static, contention-free functionality to satisfy ULV operation. At 0.5V near-V_{th} level in 65nm bulk CMOS technology, the proposed SET-FFs demonstrate up to 11-45% and 7-20% of energy efficiency at 0% and 100% data activity rates compared to prevalent and commercial SET-FFs. In addition to these cell-level merits, this paper re-visits critical parameters of SET-FFs at near-V_{th} voltage domain and provided a strategy to improve their characterization accuracy within $\leq 2\%$ of Spice level simulations. This further enables the VLSI integration of these non-conventional cells for commercial end-use. The integration of proposed SET-FFs in a 320-bit parallel shift register demonstrated up to 33% of clock network power, 17-39% of register power reductions compared to the state-of-the-art and commercial standard-cells at typical near-V_{th} levels.

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