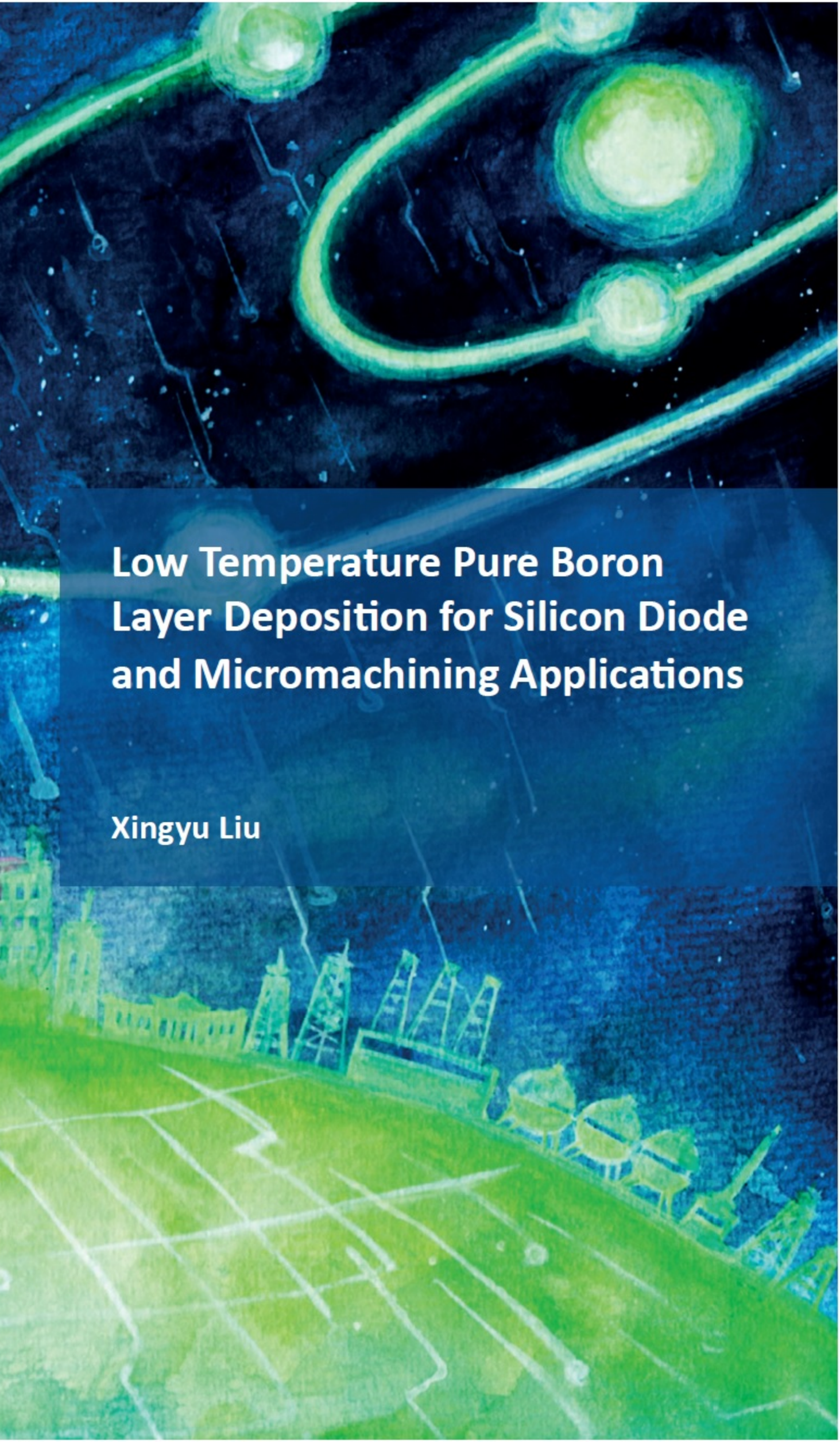

Low Temperature Pure Boron Layer Deposition for Silicon Diode and Micromachining Applications

Xingyu Liu

LOW TEMPERATURE PURE BORON LAYER DEPOSITION FOR SILICON DIODE AND MICROMACHINING APPLICATIONS

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To my family

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Chapter 1 Introduction

The evolution towards smaller devices for integrated circuits (ICs) has triggered the development of 2D materials, which in theory could lead to a new generation of high-performance devices of only a few nanometers in size. For example, graphene, a 2D sheet of well-organized honeycomb carbon atoms, has very promising properties such as high mobility and high material strength [1]. However, disappointments with respect to manufacturability and bandgap engineering have shifted much of the research efforts to a series of other, electronically promising, 2D materials, some of which have been successfully fabricated [2], such as silicene [3], germanene [4], monolayer molybdenum disulfide (MoS_2) [5], phosphorene [6], and borophene [7- 11]. Although the properties of these 2D materials are exciting, they all face major challenges as far as manufacturability is concerned [2]. Mechanical exfoliation as a fabrication method only renders poor efficiency and small sample sizes [12]. Liquid exfoliation suffers from a lack of control of the layer thickness, so the potential device material is mainly confined to layered structures with weak van der Waals forces between the layers [13]. Chemical vapor deposition (CVD) in theory can make the highest quality of 2D materials. However, it requires a catalytical substrate, usually metal, which brings with it another difficulty since damage free transfer is not trivial. Nevertheless, the desire to replace 3D doped regions by 2D layers with comparable electrical functionality is commanding. Therefore, attention is now also being directed towards the electrical properties of interfaces where 2D sheets of compounds are created with special bonding structures that do not occur in the bulk form [2]. For example, the newly discovered topological insulators, where the bulk behaves as an insulator but the surface has exotic metallic states [14], have aroused widespread research interest. The stable surface state and high light-absorption rate make them promising candidates for photodetection [15]. Bismuth selenide (Bi_2Se_3) is one of the most popular materials [16, 17] but, as for the other electrically promising 2D materials, topological insulators are facing many practical challenges mostly due to their fragility. Thus, also for these materials, there is a growing interest in looking at interface layers [2] where (1) the 2D electrical functions are formed by inherently more stable interface bonding, and (2) the "2D bulk" material works naturally as a protection layer, making the interface less susceptible to damage from varying environmental conditions.

This thesis puts focus on an example of a such an electrically interesting 2D interface layer, the boron-to-silicon interface, and presents a further investigation and development of what has been called PureB technology, including the "2D bulk" material itself. The term PureB was introduced almost a decade ago [18] to describe that pure boron (B) depositions on silicon created p^+-like regions without actually doping the bulk silicon. At the time, the B deposition was performed at 700°C by CVD in a commercially available ASM Epsilon Si or SiGe epitaxy system, using diborane (B_2H_6) as a precursor. When deposited on n-type Si, p^+n-like diodes were created with saturation currents as low as those obtained with conventional deep junction diodes. The light B doping of a few nm of the Si surface at 700°C was not enough to explain the diode characteristics and experiments with deposition temperatures down to 400°C showed that even at such low temperatures, where no bulk doping of the Si can be expected, there was an effective suppression of electron injection into the PureB regions. The junction depth at 700°C was already exceptionally low, only a few nm, but the low temperature p^+n-like diodes were realized with a metallurgical junction depth of zero nanometer. The exact origin of this special PureB diode behavior is still under investigation but overwhelming experimental evidence has suggested that the B-to-Si bonds created acceptor states where negative fixed charge was trapped, thus attracting holes to the interface [18- 20]. The resulting hole concentration was shown to be so high that a steep electrical field gradient up to the interface efficiently repelled the electrons, reducing recombination in the p-type region [21, 22].

In this thesis work, the investigation of PureB diodes, in particular those fabricated at temperatures below 500°C was continued. There were several indications in earlier work that the quality of the PureB diodes degraded as the deposition temperature decreased. This was seen as a decrease in the conduction through the hole layer along the B-to-Si interface [19, 23], and as an increase of the roughness of the B-layer itself, as the temperature decreased [24]. To gain more information on the properties of the PureB diodes as a function of deposition conditions, several new experimental methods were developed in this thesis work to enable an evaluation of the diode and associated B-layer quality directly after the deposition, i.e., without any metal contacts or isolation layers on the B. A dedicated electrical characterization method was developed to separate the hole and electron currents in the diodes so that the suppression of the electron injection could be monitored and minimized in a controlled manner. The electron current density, J_e, and the

sheet resistance, R_{sh}, of the interfacial hole layer, became the main "figures of merit" (FOM) used to develop the new B layers. At the start of this thesis work, ellipsometry, TEM and AFM imaging had clearly exposed the increasing roughness of the B-layers and connected it to a reduction in the completeness of the B coverage of the Si surface as the temperature decreased, implying a lower concentration of the desirable acceptor states at the surface and an increase of R_{sh}.

In this thesis work, effort was put into also developing wet etch methods to analyze the B-layers. They were resistant to etchants like hydrofluoric acid (HF), tetramethylammonium hydroxide (TMAH) and potassium hydroxide (KOH), but could be slowly removed in an aluminum (Al) metal etch. The latter property was used to estimate the compactness of the deposited layers, and the integrity of the B-layers was evaluated by immersion in TMAH, that would attack the underlying Si only through weak spots in the layers. These electrical and material analysis methods gave a fast-turnaround-time way of evaluating the as-deposited B-layers. The compactness of the B layer was used to make predictions of what the reliability of the PureB diodes would be in different device applications, and the B-coverage of the Si surface was linked to the ability to form the B-Si bonds responsible for the desired interfacial layer of holes.

One of the attractive features of 700°C PureB technology is that it is not only very manufacturable, but also fully front-end CMOS compatible [25]. With the reduction of the B deposition temperature to values below 500°C, it also becomes back-end compatible, which considerably increases the applicability [18]. Therefore, the main goal of this thesis work was to explore this deposition regime, and the search was on for finding deposition methods that would result in minimal values of J_e, and R_{sh} at as low as possible deposition temperatures. Experiments were performed on 5 different deposition systems. High-quality B-layers were regularly donated by the epitaxy company Lawrence Semiconductor Research Laboratory (LSRL) in Tempe, Arizona (US). LSRL provides a Si/SiGe epitaxy service to industry, using ASM Epsilon reactors, and have included PureB in their portfolio. Such epitaxy systems are not widely available in industry, and if they are available, the B-deposition is often deemed incompatible with the existing epitaxy processes being run on the systems. Therefore, it was also of interest to investigate the use of more commonly-used and less contamination-susceptible equipment. In the UTwente MESA+ NanoLab, it was possible to experiment with the Picosun atomic layer deposition (ALD) system operated

in CVD mode, and a Tempress CVD furnace equipped with a turbo pump. In addition, molecular beam epitaxy (MBE) B-deposition was made available in a cooperation with the Institut fűr Halbleitertechnik (IHT) at the University of Stuttgart. All these methods had their own advantages and disadvantages, but they all resulted in the fabrication of diodes that could be characterized as PureB diodes, even with deposition at room temperature. An issue which is common to all these alternative deposition methods is that, for a "perfect" deposition, the surface of the Si also needs to be clean with no particle or native-oxide contamination. This was achieved in the Epsilon by diluted HF dipping, Marangoni drying, Bernoulli wand handling, etc. Here several other methods were tested and verified.

Parallel with this thesis work, the theory behind the PureB diode performance was being examined by Tihomir Knežević (University of Zagreb) using TCAD software. This work indicated that the first monolayer of B bonded to the Si would be sufficient for achieving the very low J_e. Confirming this directly via experiments by actually depositing only a monolayer of B on the Si became one of the goals for the deposition research. In fact, it did demonstrate that the thickness of the bulk B-layer could be as thin as one nanometer [18] and still deliver attractive J_e values. However, it proved very difficult to achieve a complete B-coverage of less than 1 nm thick. This is basically because the B deposition is not self-limiting, and boron atoms will inevitably attach to already deposited boron atoms before a complete first monolayer is formed. To overcome this issue, there are two possibilities: (1) to develop an extremely conformal PureB deposition that may promote a self-limiting condition, or (2) to remove the "bulk" boron without damaging the B-Si interface. In this thesis work, both methods were investigated. The simulation work was also instrumental in achieving an understanding of the effects that metallizing on the B layer may have. Many experiments had already showed that J_e would increase upon metallization if the B-layer was only a nm or so thin [18]. This was particularly problematic for the rough, low-temperature B layers. The simulations predicted that the metal would lower the barrier to electrons formed by the interfacial hole layer, if it was brought close enough to the Si surface [21]. This would be the case even without having pinholes in the B layer where the metal could actually touch the Si and form a Schottky diode. This was one of the reasons that the development of B-layer deposition methods performed here was focused almost entirely on non-metallized layers.

The original 700°C PureB technology was very rapidly developed and commercialized for use in photodiode detectors for lithography systems based on both the wavelengths 193 nm (DUV: deep ultraviolet) and 13.5 nm (EUV: extreme ultraviolet) [26, 27], where the former is challenging due to the short attenuation length (~ 4.5 nm) for the light in Si, and the latter gives a high demand on robustness due to the harsh application conditions. The success of these PureB photodiode detectors was not only due to the exceptionally low dark currents achieved with a diode where the photosensitive region extended essentially to the Si surface. Equally important was the optoelectrical stability of the critical B-to-Si interface when subjected to high-dose exposure, and the robustness of the bulk B-layer itself when subjected to aggressive cleaning procedures [28, 29]. However, for the final product, the detector processing also included that the B-layer should be covered, and thus protected, by other layers for functions such as specific wavelength absorption, filtering, or anti-reflection.

Parallel with the development of the light detectors, PureB photodiodes are also being applied in detectors for low-energy electrons used in scanning and transmission electron microscopy (SEM/TEM) systems [30, 31]. These detectors are particularly demanding with respect to the chemical resilience of the B-layer. Firstly, since electrons are absorbed by all materials, the Si surface of the photodiodes was only covered with the bulk B-layer and there was no further protection of the front-entrance window [22, 32]. Hence, the thinnest possible B-layer, 2 nm for 700°C deposition, was used for detecting electrons of only 200 eV in energy [33]. In this respect, B has the advantage of a low atomic number which minimizes the scattering of electrons [34]. Nevertheless, there was a clear interest in thinning the B entrance window even further to reach a good signal gain even for 100 eV electrons, so this also was an incentive for studying methods that might lead to a complete B-monolayer coverage of the Si. Secondly, the detectors were comprised of photodiode segments that were several millimeters large which yielded a high series resistance. To lower this, Al grids were processed directly on the B-layer surface. Importantly, the B formed a chemical barrier that protected the Si from reactions with the Al, and the Al could be removed selectively to the B by wet etching in HF [32, 35]. Thirdly, the wafers were exposed to bulk Si micromachining after the B-deposition. In the course of this work, it became clear that the B layers were resistant to Si wet etching in TMAH and KOH.

In view of the chemically resilient nature of the B-layers, including a resistance to etching in the commonly-used wet Si etchants, it became

compelling to perform experiments in the context of Si micromachining and this is also one of the topics of this thesis. For bulk Si micromachining, anisotropic wet etching is commonly achieved by using alkaline solutions such as KOH and TMAH [36]. Traditionally, thin films of materials like silicon nitride or silicon dioxide are mainly used as a hard mask since they offer high etch selectivity to Si and can be deposited with production-ripe equipment for processes such as low-pressure CVD (LPCVD) or plasma-enhanced CVD (PECVD) [37]. For SiO_2, it is also possible to thermally grow if on the Si, which has the advantage of forming a better-quality material that is highly conformal and an excellent etch barrier. However, this requires temperatures above about 900°C. For processing at 700°C, LPCVD is applicable and also has good conformality, in contrast to PECVD that can be applied below 400°C. In general, the lower the processing temperature of these materials the lower the etch selectivity and a thicker layer is needed as a hard mask. Much research has been dedicated to improving the quality of low temperature oxides and nitrides but still for wet etching of deep cavities the etch rates and/or the presence of pinholes can mean that micrometer-thick layers must be used [38, 39]. This can in turn entail problems with mechanical stress, particularly if thin membranes are to be fabricated. Sputtered metals can also offer a low temperature solution to masking. Etch selectivity is in several cases extremely high, e.g., Ta, Ti, Au, Cr, and Ag, but mask etching/removal, poor adhesion, stress and process compatibility often become issues [40]. All these issues were examined here for B-layers deposited by different CVD methods with thicknesses from a few nm to tens of nm. The B proved to be an excellent masking material, even in the case of loosely-bound low temperature layers, and considering that it is fully CMOS-compatible, it could be of great interest for micro-electromechanical systems (MEMS).

The fabrication of closed membranes was also investigated. They are of commercial interest for the systems that are already using PureB detectors. For example, in SEM systems commercial protection membranes are today made of SiN, SiC, SiO_2 and polyimide, but materials such as graphene are being studied due to the low atomic number, the monolayer thickness, the high mechanical stiffness, and high electrical conductivity which would eliminate parasitic charging effects and artifacts common for standard dielectric membranes [41, 42]. B-membranes would also have many of these advantages: B has an even lower atomic number than C and the CVD layers are conductive, albeit with very high resistivity. Also, for application as

membranes, an important advantage with respect to graphene is that B thin films are highly manufacturable [18, 43, 44]. The XUV group at University of Twente was also devoting some time to studying boron as a material for capping EUV pellicles for EUV lithography systems [45]. These pellicles are preferably made of polysilicon due to the high transmissivity and mechanical strength. To ensure resistance to EUV exposure and cleaning plasmas, coatings are necessary. Boron is one of the materials that has been proven resistant to both treatments [46]. For high-volume EUV exposure, the infrared emission needed for preventing overheating of the pellicle requires capping of the poly-Si with layers of suitable emissivity. Capping layers incorporating boron were found to have both good transmissivity [47] and emissivity [45]. To extend this to using pure B-membranes for pellicles, high demands on the mechanical strength and stiffness need to be met. Tensile stress is needed to prevent sagging but film shrink due to densification during exposure/heating gives a risk of excess tension and consequent deformation/breakage. Films with maximum material density are therefore preferred. In this thesis, the investigation is directed towards an analysis of the stress in PureB layers grown with different deposition conditions and fabrication methods for obtaining strong closed membranes.

1.1 Conventional Si p-n Photodiodes

Silicon p-n junctions are elementary “building blocks” used in semiconductor electronic devices such as diodes, transistors, etc. To establish a p-n junction inside a layer of single-crystal Si, one region is doped with acceptor impurities to form the p region and the adjacent region is doped with donor atoms to form the n region. In such a junction, the current in theory only flows in one direction when the diode is contacted as illustrated schematically in Fig. 1.1 where also the corresponding *I-V* characteristics are shown. The interface formed by the transition from a p-doped to an n-doped region is referred to as the metallurgical junction. When the diode is under forward bias, the current increases exponentially with the voltage, whereas the current almost stays constant as a saturation current in reverse bias.

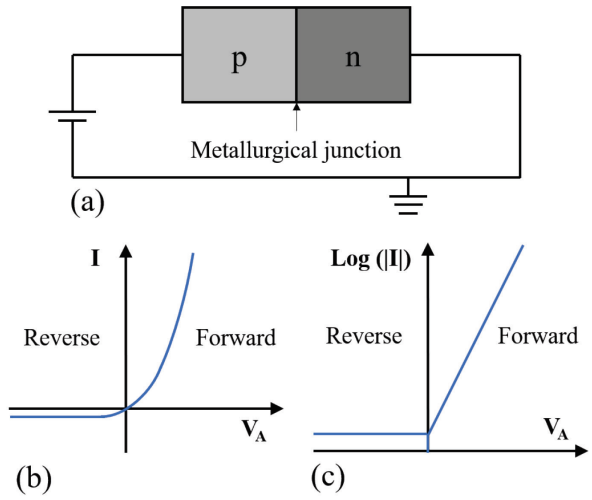

Figure 1.1. (a) Simplified geometry of a p-n diode, and corresponding idealized *I-V* characteristics; in (b) a linear, and (c) a semi-logarithmic scale.

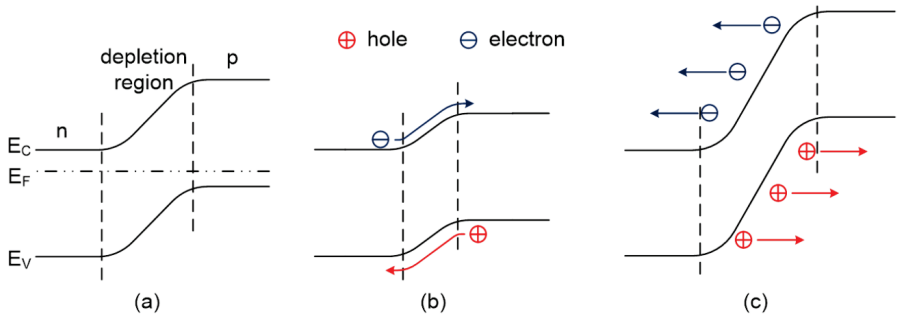

Figure 1.2. Band diagram of a p-n junction under (a) zero bias, (b) forward bias and (c) reverse bias [48].

The band diagrams of the p-n junction under zero bias, forward bias and reverse bias are shown in Fig. 1.2. If there is no voltage applied across the p-n junction, the junction is in thermal equilibrium, where a potential difference called “built-in voltage” is formed. The built-in voltage is established due to the diffusion of free holes in the p-region and electrons in n-region to cross the junction, making the p-region near the junction negatively charged and n-region positively charged, respectively. This charged region has almost no free carriers, so that it is referred to as space charge region or depletion region. The electric field created by the space charge region forms a barrier to repel the further diffusion for both holes and electrons. When under forward bias,

the holes in the p-region and the electrons in the n-region are pushed toward the junction and neutralize the depletion region, resulting in a narrower depletion width and a lower barrier height. Free holes and electrons in the neutral region are able to continuously cross the junction, forming a forward current flow. When under reverse bias, on the contrary, the holes and electrons near the depletion region are pulled away, leaving charged ions which causes the depletion region to increase, as does the barrier height. The high electric field drives minority holes and electrons that have diffused to the edge of the depletion region, into the non-depleted p- and n-regions, respectively. This gives a minimal current flow. Holes and electrons generated inside the depletion region will also be driven by the high electric field to the p and n regions, causing a generation current.

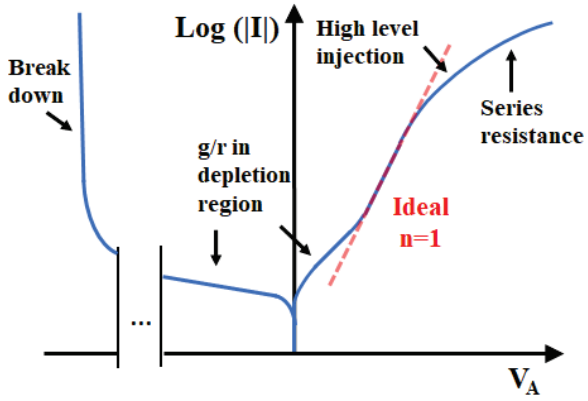

Figure 1.3. Diode *I-V* characteristics indicating the influence of parasitics.

In reality, several sources of deviations from the ideal pn junction diodes are present. This is illustrated in Fig. 1.3. For example, defects in the Si crystal structure will form generation/recombination (g/r) centers so that leakage current appears especially at small reverse/forward bias. In reverse bias, the total current is the sum of the ideal saturation current I_s and the generation current $I_{g\text{-}r}$. The I_s is independent of the reverse-bias voltage and for an ideal diode the total diode current is written as

$$I_D = I_s \left(e^{\frac{qV_D}{kT}} - 1\right), \tag{1.1}$$

where I_D and V_D are the diode current and voltage, respectively, k is Boltzman's constant, T is the temperature in Kelvin, q is the elementary charge. The $I_{g\text{-}r}$, however, is a function of the depletion width W, which in

turn is a function of the reverse-bias voltage. Thus, the actual reverse-biased current increases with the applied voltage. When the voltage increases even further, the electric field across the depletion region also increases and can become so high that sufficient energy is available for a carrier to kick out another carrier from the atomic bond. Thus, an electron-hole pair is generated and it is immediately accelerated in the depletion region, forming even more carriers. This exponential carrier creation causing avalanche breakdown consequently increases the reverse current to, in theory, infinity, but in reality, it will be limited by the series resistance of the device. At low forward bias, the parasitic g-r current may still be important because the depletion region is still wide and the ideal current level is low. At higher forward currents the ideal diode current may start to dominate. However, series resistance from the doped bulk quasi-neutral region and the diode contacts series resistance, R_s, will finally attenuate the current. If the series resistance is low enough, the diode current may also be attenuated by high injection effects because the current starts to contain so many carriers that the minority charge is comparable to the doping level of the region into which it is injected.

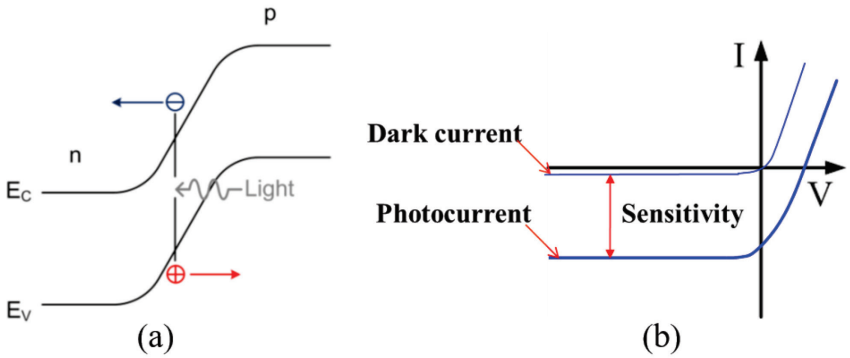

Figure 1.4. Illustration of electron-hole pair generation induced by an incident photon (a) [48] and corresponding *I-V* characteristics (b).

A generation current could also be triggered from outside by, for example, an incident photon or electron. When a photon with sufficient energy is absorbed by the diode, it can elevate a valence electron into the conduction band, creating an electron-hole pair. When the electron-hole pair is generated inside the depletion region or within about one diffusion length from the edge of depletion region, it can contribute to the light-induced current. In this way, photodetection is achieved, normally with the diode under reverse bias. Fig. 1.4 illustrates the band diagram and *I-V* characteristics

when the photocurrent is induced by incident light. The photocurrent is composed of the dark current and the photo-induced current, which is proportional to the photo flux. However, light can only be detected when the photocurrent is measurable with respect to the dark current. Thus, to achieve a photodiode with high sensitivity, the dark current should be reliably low.

In a simple 1-D approximation, the current is the sum of the electron current I_e and hole current I_h, given by

$$I_D = I_e + I_h = qAn_i^2 \left(\frac{D_n}{N_A W_p} + \frac{D_p}{N_D W_n}\right)\left(e^{\frac{qV_D}{nkT}} - 1\right), \tag{1.2}$$

where n is the ideality factor ($n = 1$ in the ideal case, but $n > 1$ is used to account for non-idealities), A is the diode area, D_n, D_p are the diffusion coefficients of electrons and holes, respectively, n_i is the intrinsic carrier concentration, N_A, N_D are the acceptor and donor concentrations on the p side and n side, respectively, W_p, W_n are the width of p-type and n-type region, respectively [49]. It is worth noting that when the minority carrier diffusion length (L) is shorter than the width, in (1.2) W_p and W_n will be replaced by L_n and L_p, respectively, which is defined as the average distance a minority carrier moves before recombining. D_n, D_p and n_i are determined by the temperature and nature of the semiconductor. Thus, the decisive parameters are N_A, N_D, W_p and W_n, which are defined by the doping process. The terms $N_A W_p$ and $N_D W_n$ are the integral doping per unit area (or "dose"), for p-type and n-type regions, respectively, when the doping concentration is uniform. When the doping concentration is not uniform, the integral doping can be calculated as

$$N_A W_p = \int_0^{W_p} N_A(x)\,dx,\ N_D W_n = \int_0^{W_n} N_D(x)\,dx. \tag{1.3}$$

The terms $N_A W_p/D_n$ and $N_D W_n/D_p$ are called the Gummel number [49] of p-region (G_A) and n-region (G_D), and are inversely proportional to the electron and hole currents, respectively, so the equation (1.2) can be written as

$$I_D = I_e + I_h = \left(\frac{qAn_i^2}{G_A} + \frac{qAn_i^2}{G_D}\right)\left(e^{\frac{qV_D}{nkT}} - 1\right). \tag{1.4}$$

Thus, the electron current is determined by the doping profile of the p-type region and hole current by that of the n-type region. To achieve a minimum saturation current, the Gummel number has to be maximized, that is, the

doping concentration and/or width of the doped region should be as large as possible.

1.2 Low-Penetration-Depth Light Detection

The interest in the development and fabrication of highly-sensitive extreme- and vacuum-ultraviolet (EUV and VUV) detectors for the wavelength range 10 nm - 200 nm has been increasing. This is mainly driven by the development of advanced lithography systems that employ these detectors to monitor beam position and/or intensity [48]. Generally, the light absorption in a material increases when the wavelength is short. And the mechanism of light penetration follows the Beer-Lambert law, given by [50]

$$I_1 = I_0 e^{-k_1 l}, \tag{1.5}$$

where I_1 is the transmitted light intensity, after being absorbed by the material, I_0 is the incident light intensity, k_1 is the absorption coefficient, l is the thickness of the material. Thus the intensity of the transmitted light decreases exponentially with the thickness of the absorbing medium.

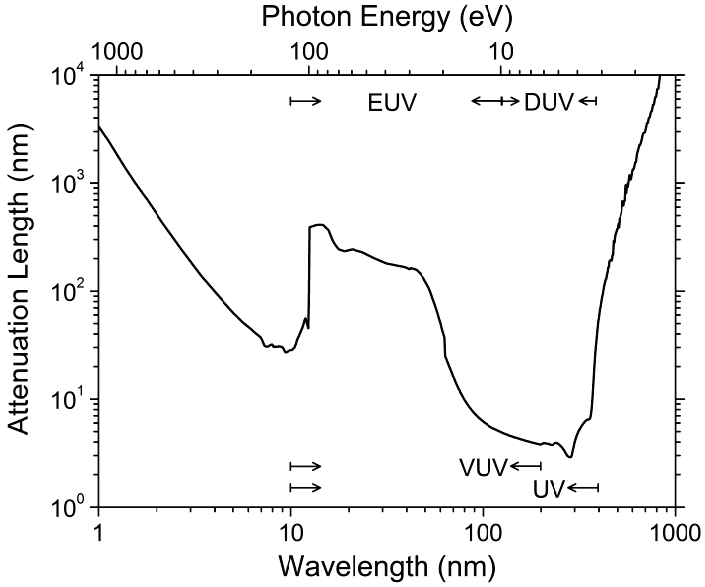

Figure 1.5. Attenuation length in Si as a function of wavelength [51, 52].

Fig. 1.5 shows the attenuation length in Si as a function of wavelength, where attenuation length is defined as the distance at which the intensity of

the beam has dropped to 1/e or about 63% of the light has been absorbed. For near-UV to deep-UV light around 190 nm to 300 nm, the attenuation length in Si is only a few nanometers. At 193 nm, used in high-volume ArF-laser lithography, the attenuation length is only about 5 nm. To detect this low-penetration-depth light in Si, the depleted region of the junction should be located very close to the Si surface, to maximize the collectable electron-hole pairs. This is extremely challenging in a conventional CMOS process, because to obtain a low saturation current a high Gummel number is also needed and this is difficult to obtain in an ultrashallow junction made by conventional doping methods. The doping concentration in Si is limited by solid solubility that is only high enough at high temperatures where also the dopant diffusivity is high, so hundreds of nanometers deep junctions are usually formed to guarantee the doping levels needed for a low saturation (dark) current. Thus, there is a trade-off between high Gummel number and junction depth.

1.3 PureB Si Photodiode Features

Leading up to the period in which PureB diodes were being investigated, there were other studies that attempted to use pure dopant depositions to make ultrashallow, low-saturation-current junctions [53- 61], but they were all focused on driving the dopants into the Si to create a counter-doping of the Si surface. One of the drive-in techniques that promised to deliver highly-doped, ultrashallow junctions was laser annealing. Attempts were made to activate well-controlled depositions of pure dopants by exposure to excimer-laser melting of the Si surface, thus reducing the dopant diffusion time to microseconds and freezing-in very high doping levels, even above 10^{20} atoms/cm^3. In this way, a highly-doped yet very shallow junction could be achieved. For example, in [62- 64] a monolayer of CVD arsenic deposited on a p-type substrate was exposed to 308-nm excimer laser annealing with energy densities from 600 to 1200 mJ/cm^2. The resulting junctions were contacted by Al/Si (1%) sputtering and diode *I-V* characteristics going from Schottky-like current levels to deep-junction-like levels were obtained as shown in Fig. 1.6.

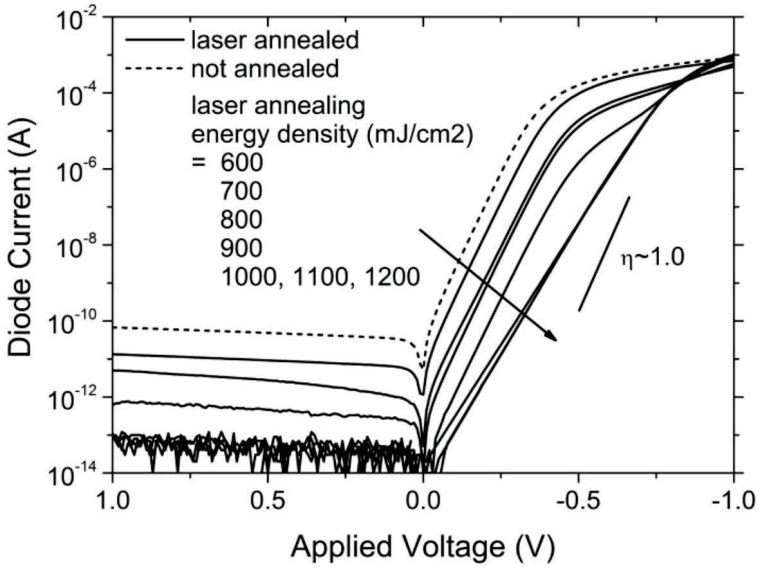

Figure 1.6. Measured *I-V* characteristics of laser-annealed diodes [62, 63].

The electron current in these diodes was the same for all anneals, being determined by the total doping of the p-type substrate that was so wide that the Gummel number was not influenced by a few-nm-deep melting and counter-doping of the Si surface. Therefore, the varying diode currents seen in Fig. 1.6 were dominated by the hole current injected from the p-Si substrate into the metal contacts for most anneals. Without laser annealing, a metal/p-Si Schottky diode was obtained and the hole injection was at its highest. With increasing laser energy levels, the saturation current of the diodes decreased. The current saturates at an anneal energy of 1000 mJ/cm^2, at which point a heavily doped n-region was created with a high doping concentration and an estimated doping depth less than 20 nm. Thus an n^+p junction diode was formed. It is interesting to note that in this experiment, anomalous *I-V* characteristics were observed at intermediate energies, which is particularly clear for the 900 mJ/cm^2 curve shown separately in Fig. 1.7. The kink in this curve, starting at about 0.4 V forward bias, marks a transition from a high current level to the same level as the n^+p diodes. This behavior was explained as having an n-doping that was so light that it was completely depleted when the bias was low enough. This was shown in simulations to pull down the barrier to holes normally set by the built-in voltage of the n^+p junction because the depletion in the metal/n-Si/p-Si junction then terminates at the metal instead of in the n^+-region.

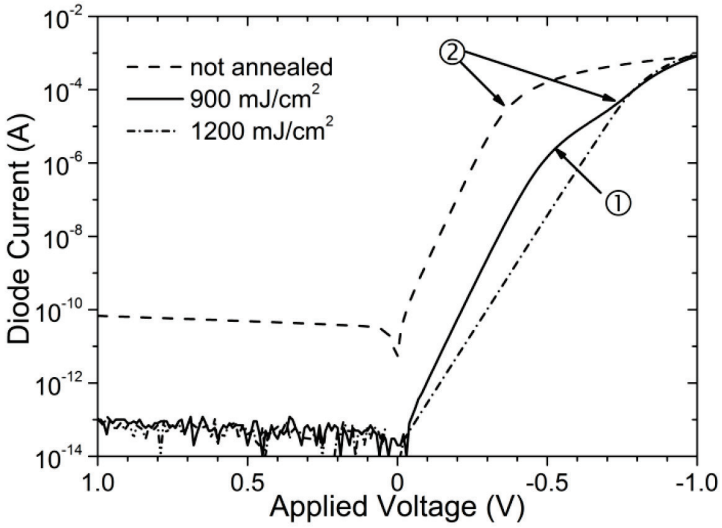

Figure 1.7. *I-V* characteristics for diodes that were either not annealed, or annealed at 900 mJ/cm^2 or 1200 mJ/cm^2 [62, 63].

In [63] an example was simulated, assuming the doping concentration N_D to be 10^{19} cm^{-3} with a doping depth of 5.1 nm. The n-region was then fully depleted under small forward bias and reverse bias, and the current in that voltage region was about 2 decades higher than that of the n^+p junctions and more than 2 decades lower than the pure Schottky case. The current increase before the kink had an ideality factor $n = 1$, because a potential barrier, which is lowered exponentially with the voltage, was formed across the depleted n-region. In Fig. 1.7, it is seen that the current saturation at point (1) is lower than at the points (2) where the series resistance starts to limit the current. This substantiated the idea that (1) was the point where the fully-depleted n^+ region started to become only partially depleted, and the diode current started to follow the n^+p diode current.

In the fabrication of photodiodes for DUV/EUV light, the use of a fully-depleted counter doping of the diode surface has been studied as a means of bringing the photo-sensitive Si region up to the surface [65]. However, the passivation of the surface was always a problem since most interfaces with Si are not stable with respect to high-dose irradiation. The high energy, particularly in EUV light, easily damages the interface, thus creating more generation/recombination sites. With respect to laser annealing of deposited dopant layers, which could have been a means of creating such extremely

shallow fully-depleted junctions on p-type Si, the technique suffers from a strong pattern dependence and surface rippling, as well as often being destructive to other structures on the wafer. Therefore, it has never really become a production technique in Si IC technology.

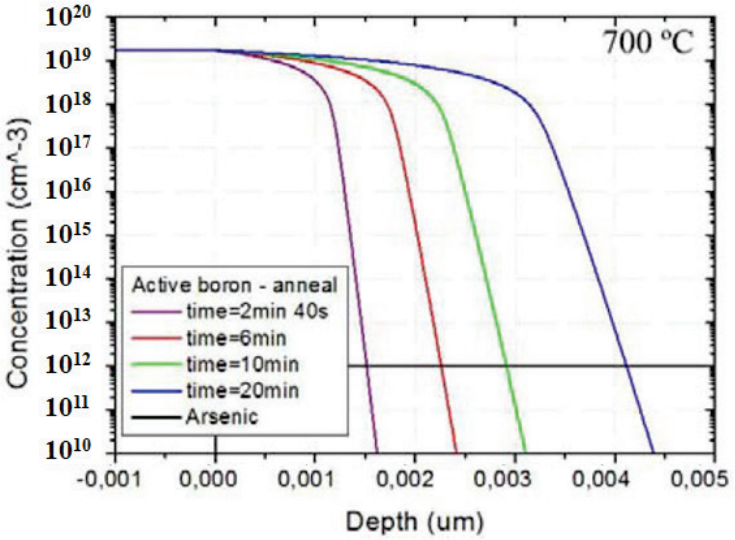

Figure 1.8. Simulated B doping profiles in c-Si for B-layer deposition at 700°C as a function of deposition time [66].

PureB technology, on the other hand, proved to be attractive on all accounts for making p^+n-like diodes, and PureB photodiodes were fabricated with extremely shallow, robust, optoelectrically stable junctions that also had low dark currents. The first diodes that were studied in depth made use of B-layers that were deposited by CVD in the ASM Epsilon at 700°C, where inevitably some of the Si became B-doped. Fig. 1.8 [66] shows a set of simulated B-doping profiles for B-deposition at 700°C, where the maximum doping level is limited by the solid solubility of ~ 2×10^{19} cm^{-3}. The diffusion coefficient in c-Si is then also very low so the resulting junction depth is small. The calculated integral doping $N_A W_A$ is in the range of ~10^{12} atm/cm^2 for a 30-min deposition time. However, there was a more than 2 decades difference between the measured and simulated Gummel numbers, as shown in Fig. 1.9 [67].

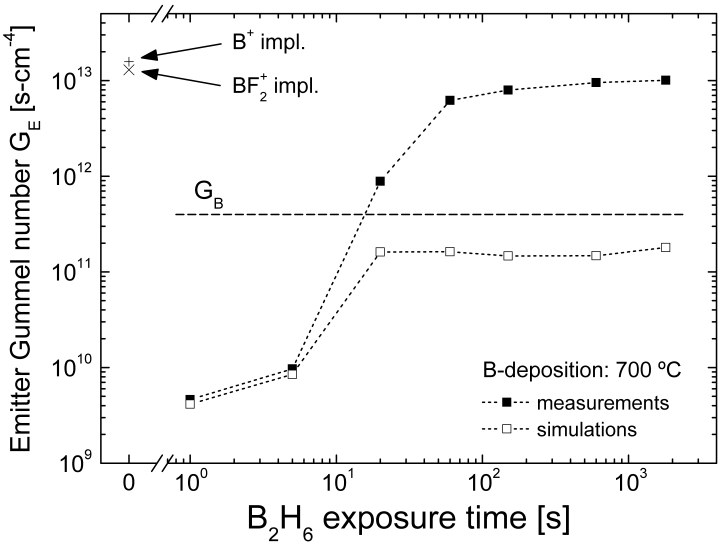

Figure 1.9. Measured and simulated emitter Gummel numbers extracted for vertical bipolar transistors fabricated with 700°C PureB emitters [67].

The actual Gummel number of a 700°C PureB emitter region was extracted from the current gain measured for a vertical bipolar transistor structure, given by

$$\frac{I_C}{I_B} = \frac{G_E}{G_B} \quad , \tag{1.6}$$

where I_C and I_B are the collector and base current, respectively, and G_E and G_B are the Gummel numbers of the PureB emitter and the base region, respectively. The G_E saturates after about 1 min deposition time, which is equivalent to an integral doping level of 10^{14} – 10^{15} atm/cm^2. In fact, despite limits set by the B solid solubility and diffusivity, these p^+n-like diodes behaved just like conventional implanted p^+n diodes with a junction depth of more than 300 nm. Therefore, the bulk doping is only contributing a negligible amount to the PureB Gummel number. More elaborate representations of the G_E, taking into account the properties of the B-layer itself and the surface recombination velocity at the metal interface, S_A, were also considered by defining it as

$$G_E = \int_{W_{QNA}} \frac{N_A(z) n_{i0}^2}{D_n(z) n_{ie}^2(z)} \, dz + \frac{N_A}{S_A} \frac{n_{i0}^2}{n_{ie\,contact}^2} \, , \tag{1.7}$$

where $W_{QNA}=W_{PureB}+W_{BxSiy}+W_{c\text{-}Si}$ is the width of p-type region composed of the B-layer, about a nanometer of B_xSi_y layer, and the B-doped c-Si. The n_{ie} is the effective intrinsic carrier concentration, given by

$$n_{ie}(z) = n_i e^{\frac{-\Delta E_G(Z)}{2kT}} , \tag{1.8}$$

where $\Delta E_G(z)$ is the bandgap difference with respect to c-Si. The silicidation process was inhibited at 500 °C, at which temperature bipolar transistors with the same current gains as the 700°C devices were fabricated, so this suggested that the B_xSi_y layer had no significant contribution to G_E [67].

Furthermore, it was not possible to connect the G_E to the bulk properties of the B-layer since the 1-min B-deposition was so thin, less than 2 nm, that it could not be attributed with a well-defined bandgap that would be constant as the layer thickness was increased. The overall consensus in the literature is also that bulk B is a narrow bandgap semiconductor, which would not promote a high G_E. The influence of a constant S_A, if it was low enough to give a high G_E, would also be reduced as the B-layer thickness increased which is not observed in the experiments. Simulations were also performed to evaluate the influence of possible B-layer electrical parameters on the G_E but did also not lead to a model that fitted with the experiments [68]. Therefore, it is assumed that almost all the p^+-like characteristics were provided by a B-Si interface interaction. Being an acceptor in Si, it was proposed that the B on the Si surface also created acceptor states that could bind an interfacial layer of fixed negative charge and thus attract holes to the interface [19, 20]. The experimentally determined G_E corresponded to a p-doping of about 5×10^{14} cm^{-2} which coincided well with the density of Si surface atoms, 6.8×10^{14} atm/cm^2, suggesting an almost fully activated 2D B-Si bonding that would be close to the physical limit.

The extremely high acceptor states in such a confined 2D space gives a unique way of achieving high Gummel numbers and bringing the metallurgical junction to a theoretical level of zero at the same time. The bulk materials (B and Si) on both sides have little influence to the electron suppression: (1), on the Si side, the bulk B doping, if there is any, only contributes approximately a factor of 1% to the effective p-doping, and (2), on the B side, a saturation of the electron suppression can be achieved when the layer reaches a certain thickness, usually less than 2 nm [18], which can also be seen in Fig. 1.9. The exact chemical origin of this behavior remains unclear but the model assuming the monolayer of acceptors states was able to

explain all the experimental data [19]. When the equilibrium is reached at the interface, the acceptor states are filled with electrons, resulting in a layer of fixed negative charge. The high charge gradient at the interface gives a very high electric field. Similar to the field under the gate of a MOS transistor, an inversion layer of holes is built up with the difference that the B layer is not isolating but conductive with very high resistivity. This model of the interface condition, illustrated by the energy band diagram in Fig. 1.10 [19], is supported by overwhelming experimental evidence [18, 19]. Later a more complete TCAD model of PureB diodes was developed and was also supported by the experimental work performed within the present thesis work [21, 68]. This will be discussed further in Chapter 5.

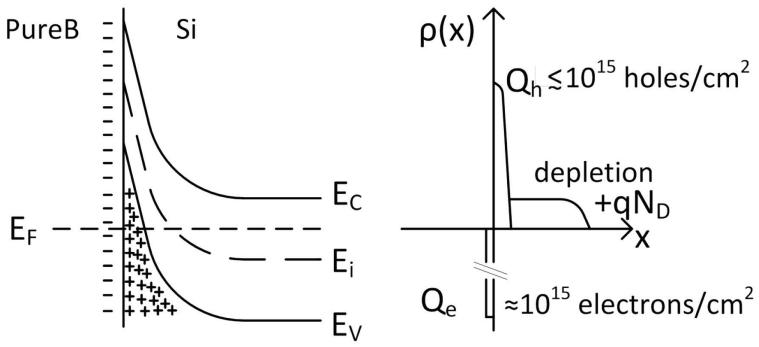

Figure 1.10. Energy band diagram (left) and charge distribution (right) illustrating the proposed model that a monolayer of acceptor states is formed at the B-Si interface. The fixed electrons at the interface are indicated with (-) and the inversion layer distribution of holes with (+) [19].

1.4 PureB Photodiode Fabrication and Applications

As described in detail in the thesis of L. Qi [48], the basic process flow used in the development of PureB photodiodes is shown in Fig. 1.11. The starting substrates were n-type (100) 1-10 Ωcm Si wafers having a doping range of about 6×10^{14} cm^{-3} to 5×10^{15} cm^{-3}. In some cases, a thick (10 µm or more), n$^-$-Si epitaxial layer was grown on the n-type starting wafer to lower the diode capacitance [69]. During photodiode operation, the epi-layer was designed to be fully depleted to avoid the series resistance being determined by the high-ohmic epi-layer. A thermal oxide was grown, either 30 nm or 300 nm thick, through which heavily-doped p$^+$ guard rings were optionally implanted and annealed at 950°C for 20 min in argon gas (Ar). The wafers

with 30 nm oxide were then covered with 300 nm LPCVD TEOS oxide. The anode/illumination window was opened in the oxide by plasma etching with soft- or wet-landing.

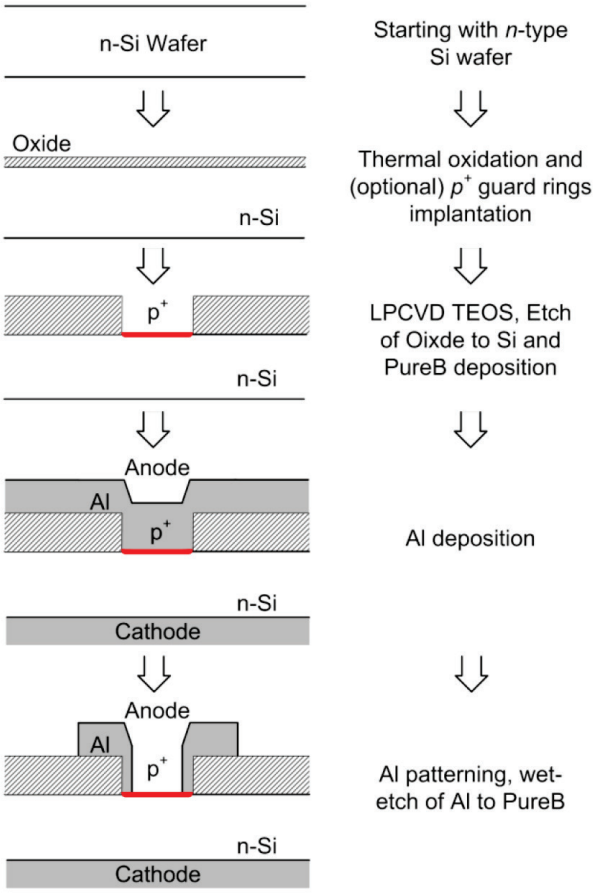

Figure 1.11. Schematic process flow for the fabrication of PureB diodes [48].

Prior to PureB deposition, the exposed Si was treated with HF dip and Marangoni drying to guarantee a clean and oxide-free Si surface [18]. The CVD deposition was performed at temperatures from 400°C to 700°C, right after which in-situ drive-in/annealing was possible in the same reactor without breaking the vacuum. For contacting, a 675-nm-thick pure Al layer was sputtered at 350 °C on the front of the wafer to form the anode contacts. On the back of the wafer Al (1%) Si was sputtered as contact to the cathode. After anode interconnect patterning, the entrance windows to the

photosensitive areas were opened first by plasma etching the Al back to 100-200 nm. This thin Al layer was then removed by wet etching in HF 0.55% for 3 min to 5 min, selectively to the PureB layer. At last, a 400 °C alloy step in forming gas was performed to passivate the Si/SiO_2 interface at the perimeter of the diodes, thus reducing perimeter leakage.

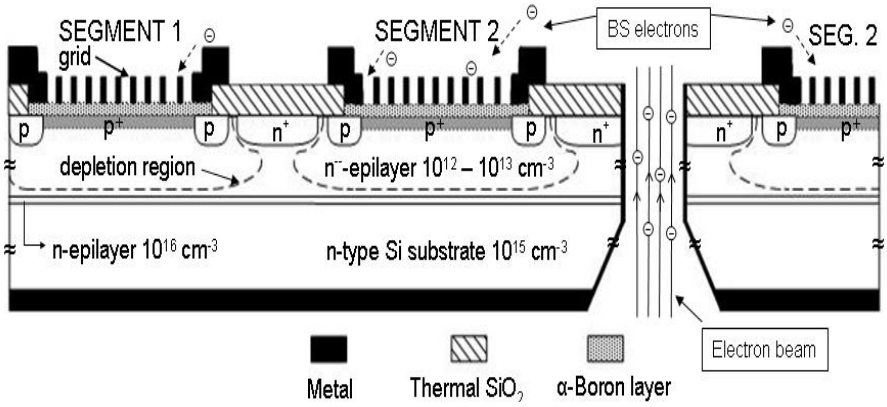

Figure 1.12. Schematic cross-section of two neighboring segments of a B-layer detector with a through-wafer hole as aperture for the electron beam. The depletion of the typically 40 μm deep n^- epitaxial layer is indicated. Segments are also isolated by the n^+-channel-stop and the undepleted n^- layer [32].

A more sophisticated PureB detector application is given in the thesis of A. Šakić [32]. The basic structure shown in Fig. 1.12 was developed and fabricated for use in advanced SEM systems to enhance performance by detecting electrons with energies below 1 keV. Record-high electron-signal-gain for electron energies as low as 200 eV was achieved with 2 nm - 3 nm thick boron layers. Several important features are indicated in the cross-section. For example, low capacitance is achieved by epitaxial growth of a very lightly-doped, tens-of-micron thick n-layers on low-ohmic substrates. Low series resistance combined with a large sensitive front-window area was achieved by patterning a fine aluminum grid directly on the boron surface. With a width of the grid of 2 μm, it covered less than 2% of the sensitive area. The series resistance dropped more than 10 times, from ~280 Ω without metal grid, to ~20 Ω with the metal grid. The combination of these features lowered the *RC* time, giving a faster response time for SEM imaging. Compact segmented anode layouts were achieved with lateral junction isolation of the segments using an n-channel stop to eliminate conductive inversion channels

and limit the lateral expansion of the depletion layer. Through-wafer apertures were etched close to the anode regions for detectors designed to monitor back-scattered electrons (BSE). To be able to micromachine the through-wafer holes from the back of the wafer, it was important that the photosensitive surface is protected from both chemical and mechanical damage. Fig. 1.13 exhibits the process flow of back-etch through-wafer apertures.

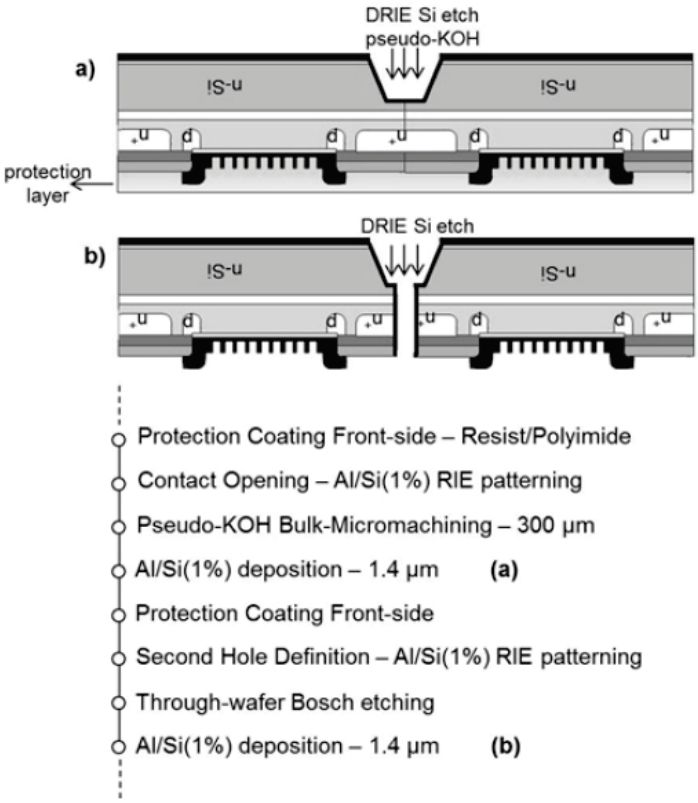

Figure 1.13. Bulk micromachining of the through-wafer aperture in two DRIE steps: a) with pseudo-KOH profile, and b) vertical sidewalls [69].

The bulk-micromachining is performed in two plasma etch steps with resist masking: the first that etches around 300 µm that mimics the anisotropic KOH profile, and the second that etches the remaining 250 µm with vertical sidewalls using a Bosch process [70]. In general, the bulk micromachining has to be performed when the front-end process is finished, which limits the choice of bulk process including etching, masking and cleaning. Since KOH

is an efficient photoresist stripper, in the first step the pseudo-KOH plasma etching was a more suitable way than wet etching, but it had the drawback of hardening the photoresist so that aggressive cleaning treatment was necessary for the removal, for which oxygen plasma stripping was used. During all this back-of-the-wafer processing, there was a risk of damaging the front-side circuitry, in particular the photosensitive anode regions. To minimize this risk, the PureB regions were protected by 100 nm Al that was left unetched during the grid patterning step. At the end of the micromachining steps, but before the final alloying step, this Al was removed by HF dip-etching. The discovery of boron layers as efficient Si anisotropic wet-etch masking layers could potentially have led to simplifications of the fabrication process. This micromachining application was investigated in detail in the present thesis work and is discussed in Chapter 4. It would be of particular interest in situations where only back-end-of-line temperatures are permitted, but both a p^+ surface region and a KOH masking layer are needed.

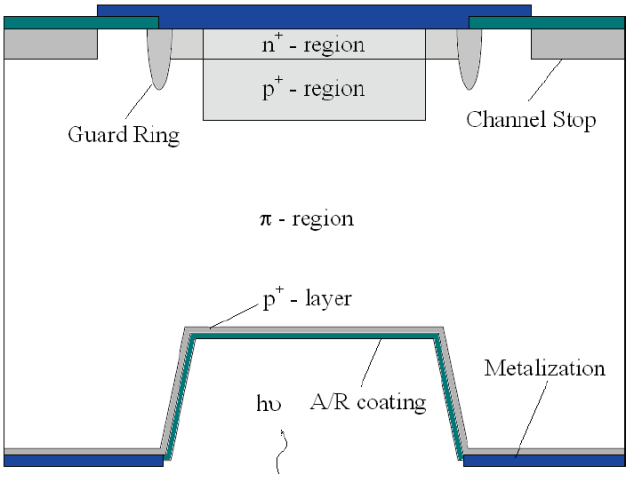

Figure 1.14. Silicon reach-through avalanche photodiode (RAPD) developed by Laser Components Inc. ® [71].

Another example of how PureB p^+-regions have been employed in UV detectors, is the silicon reach-through avalanche photodiode (RAPD) with back illumination described in [71] and illustrated in Fig. 1.14. The light-entrance window was located in a wet-etched trench at the back of the wafer. The bulk silicon was anisotropically etched so that the depth of light-absorption π region was carefully controlled. In this design, the boron layer was considered as a means of achieving both masking and p^+-region

fabrication on the non-etched regions that were metallized and served as contacts to the anode. In these types of configurations, the availability of low-temperature B deposition, the development of which is discussed in Chapter 5, can significantly simplify the process flow.

1.5 Outline of the Thesis

This thesis focuses on further exploring the applicability of pure B depositions in Si technology, among other things by investigating B deposition at lower temperatures to enhance the process compatibility, especially CMOS. Various process conditions are investigated to optimize the tradeoff between manufacturability and functionality. Several characterization techniques were developed to determine the properties of the as-deposited B-layer and to predict the performance of PureB diodes fabricated with these layers. Lastly, the application in MEMS processing was studied with the B-layer functioning as a silicon wet etch mask and membrane.

In Chapter 2, the basic principles of boron deposition by diborane decomposition are introduced. The B-Si interface properties found previously for boron deposited at high temperature (700°C) and relatively low temperature (400°C) are described, showing the trends found when going towards lower temperature deposition. An introduction to the three CVD systems used for boron deposition in this thesis is given, including the basic specifications, limitations, and advantages. The electrical and physical characterization techniques practiced in this thesis are summarized.

In Chapter 3, the electrical characterization methods are explained in more detail. The 2-diode test structure gives an easy-to-process, fast turn-around-time method of comparing process-dependent current flows when developing ultrashallow/Schottky junction technologies. Differential diode current characteristics and lateral transistor operation of the same 2-diode test structure were used to reliably identify the diode type and variations in metal-Si interfacial properties, independent of parasitic leakage currents. Test structures that required no metallization of the B-layers, such as Van der Pauw structures and sets of ring-structures, were used to measure the conductance along the B-Si interface, which gives a quick way to monitor the degree to which the desired interfacial B-Si bonds were achieved. Sets of non-metallized ring-structures were also designed to allow the extraction of the electron injection into the p-type region of PureB diodes, which also gives an important measure of the degree to which these critical bonds have been made.

In Chapter 4, the properties of nanometer-thin pure boron layers deposited by CVD were investigated for use as a barrier against tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH) etching of Si. The boron layers used were deposited from 400°C to 700°C with thickness down to 1 nm. The topographical differences of implanted and non-implanted Si after TMAH and KOH etching for various times are compared. Boron-layer patterning, fabrication of overhanging boron membranes, and layer stress evaluation are briefly introduced and will be discussed further in Chapter 6. The focus of this chapter is to validate that boron layers under certain deposition conditions are effective as anisotropic wet-etch masks on Si. The etching method is also considered as a way to quickly evaluate the bonding strength of the B-Si and B-B bonds. The former is important for PureB diode fabrication and the latter for B-membrane fabrication.

In Chapter 5, the evaluation methods mentioned in Chapter 3 and 4 are applied to B layer deposited from 450°C down to room temperature (RT) in order to characterize these layers with respect to the electrical properties when incorporated in PureB diodes, and for the physical properties when used as wet-etch masks. The lowest possible Si substrate temperatures were tested in the different deposition systems. With MBE, RT deposition was possible and this method is also advantageous in having high surface coverage and low oxygen contamination as compared to other physical vapor deposition (PVD) systems. In this chapter, an investigation is also presented of the effects of several cleaning procedures prior to deposition and annealing after deposition.

In Chapter 6, a more detailed investigation of B-layers as wet-etch masks and free-stand membranes is given. Stress measurements were performed on a set of B-layers deposited in CVD mode under different conditions (temperature, deposition rate, etc.). Thus, the correlation between processing conditions and layer stress are better understood, leading the way to stress free B-film fabrication. Overhanging B-membranes deposited from various temperatures were fabricated and studied with respect to defects and transparency. Closed B-membranes were fabricated by etching through the Si substrate, using the B-layers simultaneously as Si etch mask and membrane material. The reliability of membranes made of thick boron-layers was tested for layers grown in different reactors.

Finally, Chapter 7 summarizes the main conclusion of the work in this thesis and gives recommendations for the future work.

Chapter 2 Pure Boron Deposition Technology

This chapter focuses on the basics of boron: the B element itself, the properties already established for deposition on Si at temperatures from 400 °C to 700 °C, and the methods used in the present research to deposit B on Si and to analyze the results. The deposition equipment used here includes the Picosun and ULPCVD (ultra LPCVD) systems, which are both available in the MESA+ Nanolab at the University of Twente. In addition, the settings for B-deposition by MBE, as made available through a cooperation with the University of Stuttgart, are also described. In Section 2.5 an introduction is given to the boron film analysis techniques that received extra attention/development in order to make them suitable as cost-efficient, rapid methods for examining the B-layers fabricated here. This includes ellipsometry for film thickness measurement, electrical test structures, and wet-etch tests to compare the compactness and robustness of the layers. In addition to these methods, several standardized analysis techniques were also employed such as atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), TEM, SEM, profilometer (Dektak), secondary ion mass spectrometry (SIMS), Nomarski interference contrast microscopy (NICM), and they will be introduced as needed in connection with the results presented in the following chapters. Moreover, a more detailed treatment of the electrical test structures will be given in Chapter 3 in relationship to the development of PureB diodes, and in Chapter 4 the wet-etch tests are also put in the context of the MEMS applications of B-layers.

2.1 Background

2.1.1 Elemental boron

Boron is the fifth element in periodic table, situated between the metal beryllium and the semiconductor carbon (shown in Fig. 2.1), categorized as the lightest of the semi-metals. Boron has only three valence electrons, which would be in favor of metallicity. However, these electrons are sufficiently localized so that boron tends towards insulating behavior. This would explain the poor electrical conductivity at low temperatures. Boron forms highly delocalized bonds, sharing electron pairs among three (or more) atoms, in which the B-B bonds have high strength. Crystalline boron is the second hardest of all elements, only behind diamond, and has a melting temperature over 2000 °C [72]. Bulk boron (non-pulverous) is known to have at least

sixteen polymorphs, but only a few of the crystal structures have been identified [9], for example, the α-B_{12} (an icosahedral structure with 12 atoms in a unit cell), β-$B_{105\text{-}108}$ (rhombohedral structure), tetragonal T-192 [73] and γ-B_{28} [74]. In fact, all these crystal structures are dominated by the icosahedral B_{12} cluster (shown in Fig. 2.2), which can be interlinked by strong covalent bonds in different ways to form polymorphs [75]. Amorphous and β-rhombohedral structures are closely related with icosahedron being the sub-unit, but disorder occurs in the linking between these icosahedra. [76].

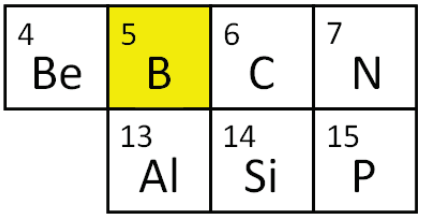

Figure 2.1. The position of boron in periodic table.

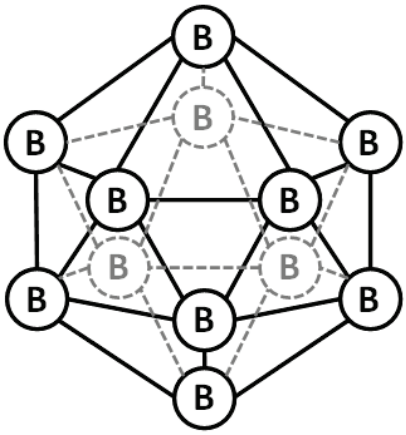

Figure 2.2. The smallest unit of the boron crystal structure icosahedral B_{12} [73].

2.1.2 Boron purification and preparation

On earth, boron mostly exists in the form of borax, also known as sodium borate, which is a salt of boric acid. Borax has been known and used in ceramic glazes and in metallurgy for centuries, but no one isolated the elements from borax until 1808, when English chemist Sir Humphry Davy used electrolysis on a borax solution and observed a brown mass forming at

one electrode [77]. In the same year, French chemists Joseph Louis Gay-Lussac and Louis Jacques Thénard reduced boric acid with iron at high temperatures [78]. Boron was identified as an element by Swedish chemist Jöns Jakob Berzelius in 1824 [79]. The earliest route towards massive boron production was established as boron oxide reduction with alkali metals such as calcium, magnesium, aluminum. However, this product is contaminated with borides of these metals [80]. Boron prepared by fused salt electrolysis is in granular form and is contaminated with the electrolyte, oxide, and possibly with high melting nonvolatile borides [80]. The demand of boron with higher purity in the semiconductor industry has enhanced the use of the reduction of gas-phase boron halides with hydrogen. Not only hydrogen is an easily purified gas, but also BCl_3, and mostly BBr_3 and BI_3, are compounds that can be made with very high purity by fractional distillation, by chromatography in gas phase, or by zone melting [79]. However, there are several disadvantages: (1) the BX_3 boron halides are characterized by very low B/BX_3 weight ratios [81], (2) the reaction product HX is corrosive [82], and (3) it requires a high substrate temperature (800°C - 1200°C) [83]. Ultrapure boron for use in the semiconductor industry is produced by the decomposition of diborane at high temperatures followed by a further purification by zone melting or Czochralski processes [84].

2.1.3 Boron doping technology in the semiconductor industry

Boron is well known as the main p-type dopant in silicon IC technology. The conventional and most mature doping techniques are either diffusion from an external source of B, or B implantation and annealing. For both methods the doping level is limited by the solubility of the B in Si, and in many situations not all dopants will be electrically activated. High temperature diffusion from a dopant-containing compound generally suffers from the lack of doping uniformity and dose control. With the continual downsizing of Si devices, the required junction depth has become smaller and smaller. The more than a micron deep diffused junctions were gradually replaced by implanted/annealed junctions with depths in the hundred nanometer range. Implantation, however, suffers from stochastic spatial distribution of the implanted ions and severe Si crystal damage. Therefore, it has always been a challenge to achieve a sufficiently damage-free, highly-doped but shallow p-region that also could meet stringent requirements for the abruptness of the doping profile. Later, p-type Si epitaxy was developed where a thin layer of p-Si is fabricated by adding gas-phase dopants during the Si deposition. For a high B doping concentration, a deposition temperature

above 1000°C is usually implemented, which inevitably causes the diffusion of dopants in both the p and n regions. Despite cross doping, a highly-doped p-region with a metallurgical junction depth as shallow as 10 nm can be achieved. However, the dopant aggregation remains a problem. Since the 80s, efforts have been dedicated to a so-called delta-doping technique [53- 60], where, for example, pure dopants are deposited and capped with another layer before being annealed in order to diffuse and incorporate the dopants. This technique is named after the delta-function-like doping profile with a sharp spike shape. In 2007, C. Ho et al. claimed the invention of monolayer doping (MLD) [61], where they replaced the pure dopants used in delta-doping with self-limiting dopant-containing molecules exposed to rapid thermal annealing (RTA), to enhance the spatial distribution and dose control.

2.2 Chemical Vapor Deposition of Pure Boron on Si

2.2.1 Surface reaction

In the semiconductor field, ultrapure amorphous boron (a-B) is mostly prepared either by CVD [25, 85], where it is common to decompose the molecule vapor of boron hydrides (B_xH_y) on the wafer surface and in the vacuum, or by PVD [86, 87], where the solid phase elemental boron target is vaporized by plasma or electron beam, and boron atoms will subsequently land on the surface. In the chemical approach, the decomposition of boranes is usually realized by plasma or pyrolysis, such as direct current (DC)/radio frequency (RF)/electron cyclotron resonance (ECR) PECVD or LPCVD. Besides the compositional and compactness difference which will be discussed in Chapter 4, chemical-based deposition can be selective with respect to substrate material, which has often been found to be an advantage in electrical device production. However, the substrate temperature needed to realize the decomposition can limit the applicability and compatibility with substrates and other processing steps that do not tolerate the required thermal budget. PVD, on the other hand, is more sensitive to surface topography since it is very directional. In this thesis, we use diborane (B_2H_6) as the precursor for CVD. B was deposited by CVD and PVD in various types of reactors. The pure boron layers can be deposited on silicon, or any other type of surface, by exposing the substrate to B_2H_6 while heating it to elevated temperatures. The activation energy of the chemical reaction is then purely provided by thermal energy. In previous studies, the deposition temperature was in the range from 400°C to 700°C, for deposition performed in a commercial Si/SiGe epitaxial

reactor ASM Epsilon [18]. Hydrogen (H_2) was used as the carrier gas to dilute the diborane source. The overall chemical reaction is:

$$B_2H_6\ (g) \longrightarrow 2B\ (s)+3H_2\ (g), \tag{2.1}$$

where (g) indicates the gas phase and (s) the solid phase. The whole point of this reaction is to release hydrogen molecules from the diborane. The dominating pathway is the generation of borane (BH_3), which is produced from B_2H_6 in a reversible reaction [88]:

$$B_2H_6\ (g) \longleftrightarrow 2BH_3\ (g). \tag{2.2}$$

At a temperature as low as 545 K, diborane is the exclusive product of borane loss, while at higher temperatures another reaction channel is built for the loss of BH_3 [89], namely

$$BH_3 \xrightarrow{\text{surface}} B\ (s)+ {}^3\!/_2\, H_2(g). \tag{2.3}$$

The silicon surface reaction mechanism will be explained more thoroughly in the following.

Crystalline silicon forms an FCC (cubic crystal system) structure, in which each Si atom is bonded to four other Si atoms. This is the most stable state for silicon because all the bonds are fulfilled. At the Si (100) surface, silicon atoms bond with two atoms below but lack two atoms above to complete the structure, leaving two available unpaired valence electrons. To achieve an energetically more favorable state, each Si atom is spontaneously bonded to another atom with one electron, forming a row of silicon pairs, namely dimers. This leaves the surface atoms with one available valence electron, which will form electrically active interface traps, known as dangling bonds. BH_3 is a strong Lewis acid, since it is an electron-deficient compound with a low-lying unoccupied orbital, resulting in a facile surface dimer buckling with Si daggling bonds [90]. Low temperature deposition processes are generally controlled by surface reactions, where boron atoms in boron hydrides either form direct bonds with Si surface, or Si-B dimers with Si adatoms and trapped by the following growth of B to become part of the lattice [91]. The silicon surface is usually treated with HF solution dipping prior to boron deposition to remove the native oxide and to terminate the dangling bonds with hydrogen. This hydrogen termination is of great importance because it passivates the dangling bonds of surface silicon atoms to prevent unwanted reactions with other species, especially from carbon and

oxygen contamination. Assuming Si-H are hydrogen terminated silicon atoms and Si° are silicon atoms with dangling bonds, a simplified model of surface reaction was proposed by [92] as shown in Fig. 2.3 [93], where BH_3 is the dominant reactant. The mechanism is:

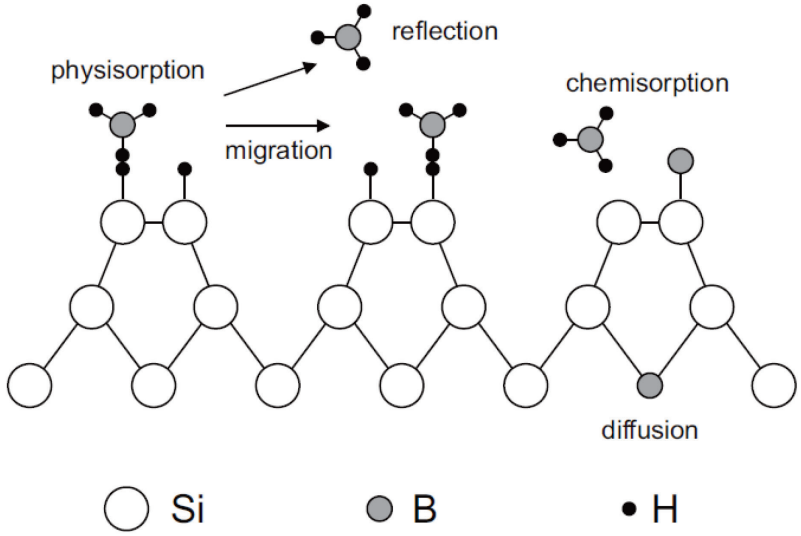

Figure 2.3. Reaction model of Si surface and BH_3 [93].

(1) Physisorption and reflection $Si\text{-}H+BH_3 \longleftrightarrow Si\text{-}HBH_3$ (2.4)
(2) Migration $Si\text{-}HBH_3+Si\text{-}H \longrightarrow Si\text{-}H+Si\text{-}HBH_3$, (2.5)
(3) Recombination $Si\text{-}HBH_3+Si\text{-}HBH_3 \longrightarrow 2Si\text{-}H+B_2H_6$, (2.6)
(4) Chemisorption $Si°+BH_3 \longrightarrow SiBH+H_2$, (2.7)
(5) Diffusion $SiB \longrightarrow Si°+B$ (diffused). (2.8)

After chemisorption between Si° and BH_3, the incomplete release of hydrogen makes the surface boron naturally passivated. Same mechanism also applies to BH_3 decomposition at boron surface, where in both cases the chemical bond formation between boron atoms and surface dangling bonds (either Si° or B°) is essential. Those dangling bonds will be exposed by

$$H(g)+Si\text{-}H(s) \longleftrightarrow H_2(g)+°Si(s), \quad (2.9)$$

$$H(g)+B\text{-}H(s) \longleftrightarrow H_2(g)+°B(s), \quad (3.0)$$

where the presence of hydrogen will suppress the forward reaction [85]. In reality, higher orders of boron hydrides (B_3H_6, B_4H_{10}, B_5H_{11}, etc.) were found

by mass spectrometry in the gas phase, meaning the mechanism of intermediate reactants and their reactions are rather complex [94]. In the deposited layer, possible cross linking happens between adjacent B-H bonds [85]:

$$\text{B-H(s)+B-H(s)} \longleftrightarrow \text{B-B(s)+ } H_2\text{(g)}. \qquad (3.1)$$

Thus, boron deposition is a process that eventually releases the hydrogen with respect to a serial reaction of gas-phase and surface reaction.

2.2.2 Relationship to electrical behavior of PureB diodes

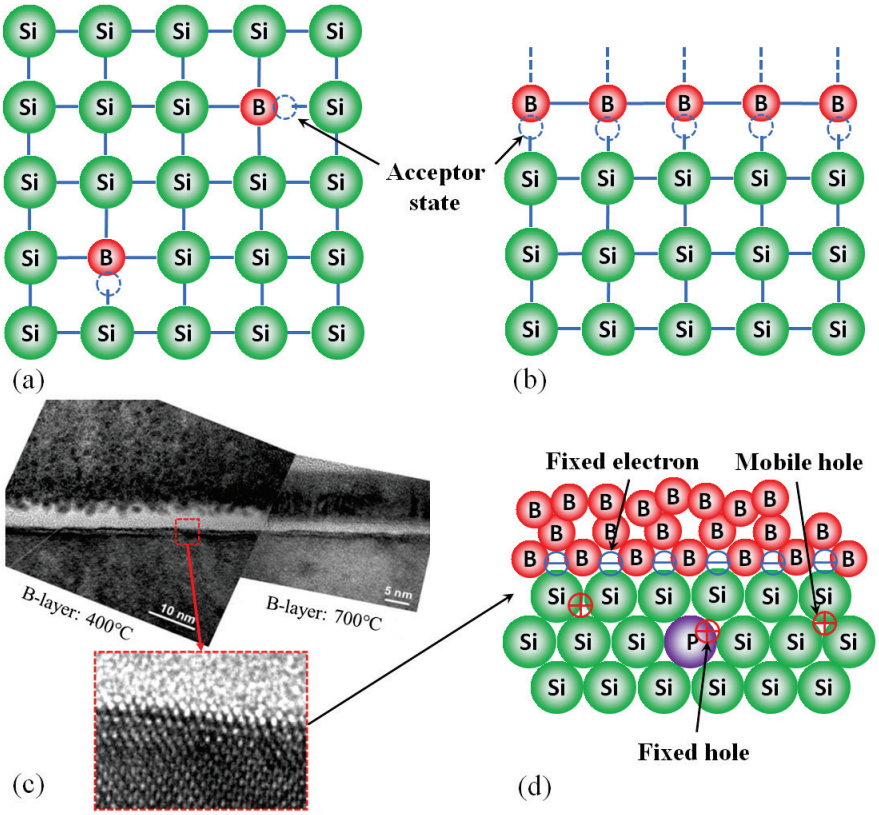

Figure 2.4. (a) Schematic of B-doping in a Si lattice. (b) Simplistic model showing how acceptor states between the B and Si dangling bonds possibly could be formed at the Si surface. (c) HRTEM images of CVD B-layers deposited at 400°C and 700°C [24]. (d) Interfacial B-Si acceptor states filled with negative charge attracting holes from an n-doped Si substrate.

The chemical mechanisms discussed in Section 2.2.1 focus on the creation of covalent bonds between the B and Si surface atoms, and do not give any information on the formation of acceptor states that could be created at or near the B-Si interface and possibly account for the electrical behavior. In an earlier study, the density of a complete monolayer (ML) of boron on Si (100), 6.78×10^{14} cm^{-2} [25], corresponded well with the p-doping concentration at the surface that would be needed to fit the 700°C PureB diode characteristics to simulations. Fig. 2.4 (b) gives a very simplistic, speculative model of B-Si interface bonding, where every B-atom connects to a Si-atom by binding the Si dangling bond in much the same way as it would if it was incorporated in the bulk Si lattice as a dopant atom, as shown in Fig. 2.4 (a). A hole that can move freely in the Si lattice is then created. For 700°C B-deposition there is significant penetration of the B into the Si, with an about a 1-nm-thick B_xSi_{x-1} layer being observed [25]. Therefore, it seems plausible that the observed high surface concentration of fixed negative charge is a result of a high surface concentration of disordered but "normal" B-doping of the Si. However, at 400°C where no bulk doping of the Si is expected, TEM images also showed that the B-Si interface is flat. This is seen in the TEM images of Fig. 2.4 (c) where CVD boron deposited on Si at 400°C is compared to a 700°C deposition [24]. In the 400°C case the B is seen to be deposited epitaxially with the first few atoms following the crystalline structure of Si. In the course of this work, more information was gained about the electrical performance of such low temperature B-deposition. In addition, the challenge of achieving a complete surface coverage with the desired B-Si bonds at these temperatures was given attention. In the past, researchers have presented different views on whether boron would form a complete surface coverage of silicon or nucleate as isolated islands regardless of deposition conditions [85, 95]. In any case, it would always be a challenge to guarantee the surface coverage when the layer is extremely thin (< 1 nm). The exposed surface of silicon would eventually be oxidized in air and this has been found to be detrimental to the electrical performance of PureB diodes. Electrically, the oxidized regions become generation/ recombination sites that are a source of leakage current, while mechanically, they are weak spots when B is exposed to chemicals, which will be discussed in detail in Chapter 4. Thus, the critical boron thickness for surface coverage is of great importance especially for low temperature deposition where the boron atom migration over the substrate surfaces is negligible. Then the immediate surroundings, with the available Si or B bonding possibilities, of the deposited B-atoms will be decisive for the final deposition location. Therefore, depending on the application, it may be

favorable to deposit excessive boron (> 2 nm thick), either to extend boron islands until they finally meet, or to overgrow the unsaturated silicon surface until it is fully covered and protected.

2.3 Boron Layer deposited at 400°C or 700°C

This section gives a review, based on the reference [43] that was published as part of the present thesis research, of the properties of boron layers that are known from earlier work on PureB diode fabrication. So far, the 400°C and 700°C depositions in the Epsilon reactor have been the most interesting layers for electrical applications. They both form diodes with similar p^+n-junction-like characteristics but the 700°C layers are chemically more robust while the 400°C layers have the advantage of being suitable for integration in post-metal back-end-CMOS process modules [18]. In Fig. 2.5 [43] the main structural and electrical differences between the layers are illustrated. Both layers were deposited in the ASM Epsilon CVD reactor. Five regions have been identified:

(1) A uniform, compact layer of amorphous boron is seen to be deposited directly on the Si surface.
(2) The surface of the compact B layer is covered with a rough increasingly incomplete layer of non-compact B. This layer is quite thick for 400°C layers but barely noticeable for 700°C layers. At this temperature uniform layers with low surface roughness are formed as a result of the high diffusion length of the boron atoms along both Si and SiO_2 surfaces [85, 96]. As the deposition temperature is lowered the mobility along the surface diminishes and the layers become rougher.
(3) For the 700°C layer the Si surface is roughened, and some mixing of the B and Si is visible in a region less than 1 nm wide at the interface. The 400°C deposition leaves the Si surface flat.
(4) At 700°C the boron can diffuse a few nm into the bulk Si, doping it to the solid solubility of 2×10^{19} cm^3. At 400°C no bulk doping is expected.
(5) For both the 400°C and 700°C depositions, it is speculated that a layer of fixed negative charge is formed at the B-to-Si interface. The layer of holes that thereby is induced at the interface is responsible for the attractively low saturation current of the diode *I-V* characteristics [18]. It also determines the sheet resistance along n-type Si surfaces covered with B deposited at temperatures that give no significant doping of the Si, i.e., 400°C - 500°C [19]. The resistivity of the amorphous boron layer itself is very high with values above 500 Ω-cm [95]. In the literature, other CVD

layers of B have been reported to be semiconductors with a p-type doping in the 10^{16} - 10^{18} cm^3 range [98, 99].

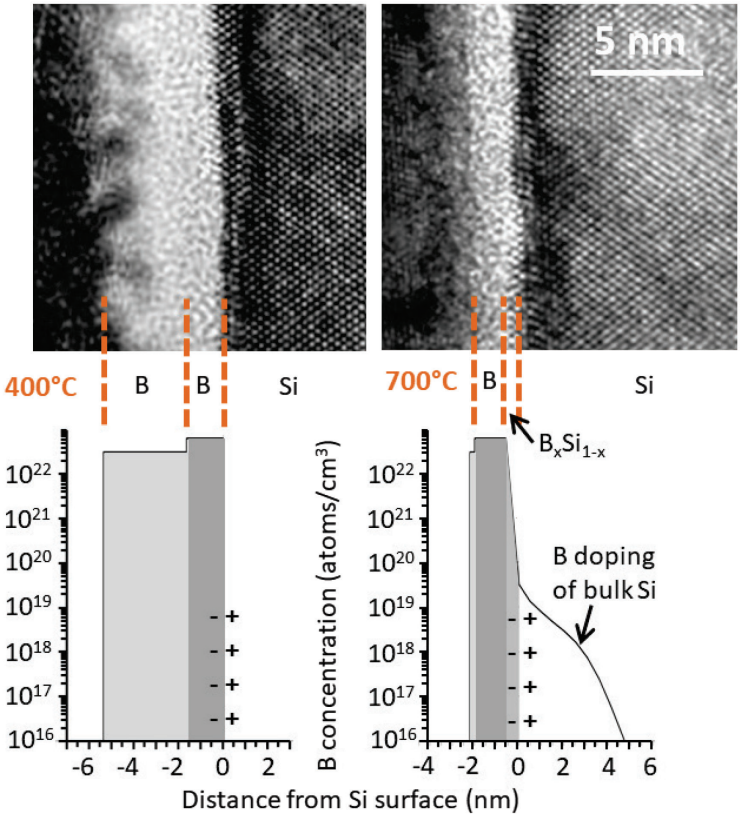

Figure 2.5. Top: HRTEM images of B layers grown at 400°C (left) and 700°C (right). Bottom: corresponding graphs of the B concentration. The dark grey regions represent compact bulk boron, the concentration in which was determined by SIMS [25]. The light grey regions on the B layer surface represent the non-compact surface regions, the indicated thickness of which is equal to the roughness extracted from ellipsometry measurements. The profile of the B-doping of the bulk Si is taken from simulations [18]. At the B-to-Si interface the minus and plus signs represent respectively the fixed negative charge and the associated hole accumulation. The medium grey region at the Si interface of the 700°C deposition represents a mixing of the B and Si at this interface.

2.4 Deposition Equipment and Pre-deposition Procedures

2.4.1 Deposition reactors

(a) ASM Epsilon CVD reactor

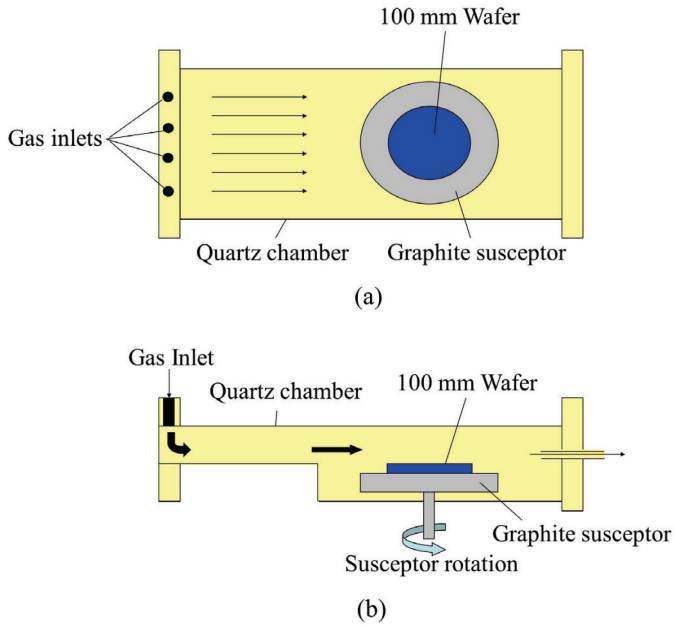

Figure 2.6. A schematic diagram of the (a) top view and (b) side view of the Epsilon CVD reactor [100].

ASM Epsilon CVD systems, Epsilon One and Epsilon 2000, are single-wafer systems with a quartz chamber and a rotating graphite susceptor, used here for boron layer deposition on 100/200 mm wafers with diborane as precursor. The B_2H_6 precursor is 0.2% diluted by H_2, and can be further diluted by introducing extra carrier gas of the system either as N_2 or H_2. They are equipped with integrated heating lamps to grow layers at temperatures from 400°C up to 1200°C, at atmospheric pressure (AP), i.e., 760 Torr, or reduced pressure (RP) down to 1 mTorr [85]. The gas flow in the chamber is laminar, parallel to the surface of the rotating wafer. Besides, the temperatures in the middle and at the edge of the wafer are separately monitored by the integrated thermocouple of the susceptor and can be controlled by the heating lamps. Thus, a thickness deviation of less than 3% can be routinely achieved.

The schematic diagram of the CVD reactor is shown in Fig. 2.6 [100]. These systems benefit from having a load-lock that lessens the risk of bringing oxygen/water contamination into the system with the wafer. It was also possible to perform a hydrogen bake at temperatures above 700°C to remove native oxide and/or organic contaminants from the wafer surface.

(b) Picosun ALD reactor

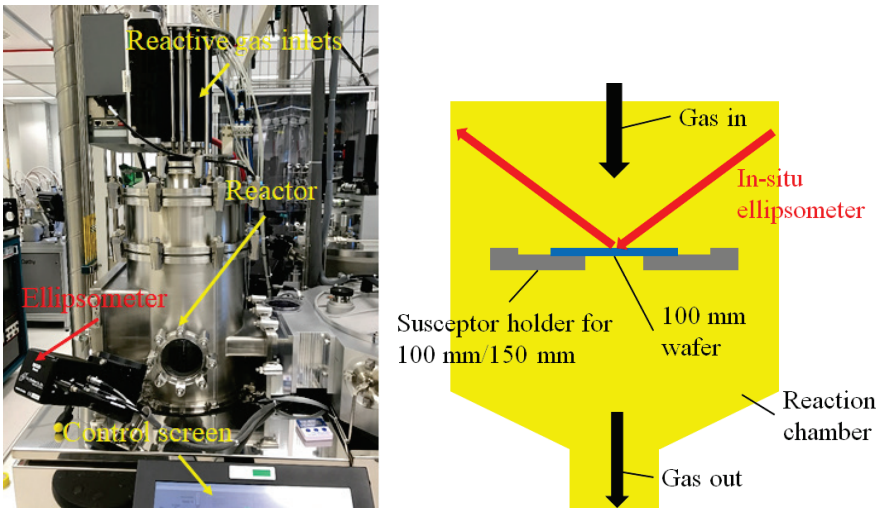

Figure 2.7. An image of Picosun system (left) and a schematic of the side view of Picosun reactor (right) [101].

Picosun is a single wafer (100 mm or 150 mm) system originally designed for atomic layer deposition (ALD). Here it was operated in CVD mode for boron layer deposition with a constant diborane flow. The B_2H_6 precursor is 5% diluted by Ar, and can be further diluted by introducing extra carrier gas of the system either as N_2 or Ar. The Picosun is equipped with a loadlock, which takes about 20 min to pump down to a pressure of 10^{-6} mbar before transferring the wafer to the reactor. It is also possible to load smaller substrates placed on a wafer tray. A Woollam M2000 in-situ ellipsometer is attached to the reactor, which has basically two functions: (1) to make sure the substrate temperature has been stabilized before the deposition; and (2) to monitor the film growth during the deposition. The temperature range of the reactor is from RT to 550°C, and the working pressure can be tuned from 1 mbar to 10 mbar. The range of the precursor mass flow meter is up to 200 sccm, thus the gas flow is only readable between 0 to 200 sccm. Fig. 2.7 shows the schematic of Picosun system, in which the gas flow is introduced

from the top, facing the wafer surface to lessen the precursor depletion over the wafer. However, due to the stationary wafer susceptor, thickness variations were larger than for deposition in the Epsilon, and Fig. 2.8 shows the B thickness mapping over a 100 mm silicon wafer with thickness variation around 10%.

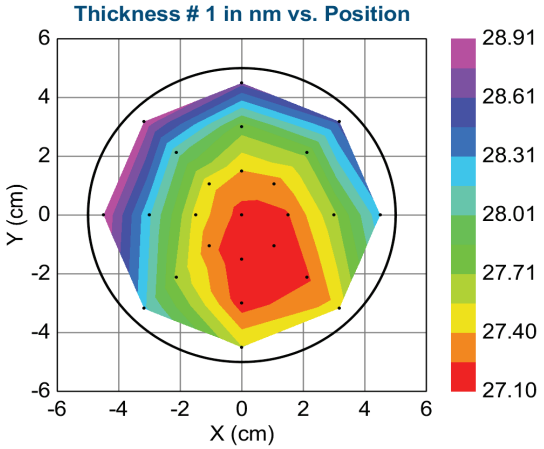

Figure 2.8. Boron thickness as a function of wafer positioning, deposited under 400°C for 10 min, with B_2H_6 flow of 200 sccm and Ar 500 sccm.

(c) ULPCVD furnace system

The ULPCVD furnace is a customized batch furnace system that enables boron layer deposition of up to 112 100-mm wafers. The precursor is the same with Picosun, 5% B_2H_6 in Ar. It contains a quartz chamber and wafers are loaded in a 28-cm-long quartz boat. The temperature can be tuned from room temperature (RT) up to a maximum of 850°C due to limitations of the O-ring seal design. The turbo pump would take about 30 min to pump down the chamber to a level of 10^{-7} mbar to minimize the oxygen and water contaminants brought by the wafers. During the deposition, the working pressure is kept at 0.0013 mbar. Due to the lack of a loadlock, it is impossible to operate under atmospheric pressure. The schematic of the ULPCVD furnace system is shown in Fig. 2.9. The gas flow is facing the wafer surface, and parallel to wafer positioning. The quartz boat should be always fully loaded, either by target wafers or dummy wafers, to prevent any deposition in the notches that support the wafers. Thus, the precursor is inevitably depleted from the front wafer (near the gas inlet) to the back wafer (near the gas outlet), which is shown in Fig. 2.10. The depletion has less effect on the

individual wafers, where at the edge the film is about 10% thicker than in the center.

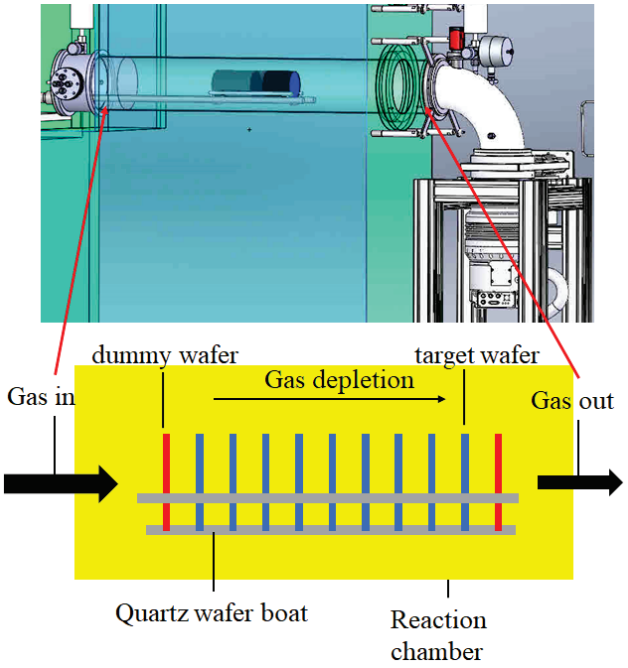

Figure 2.9. A drawing (top) and a schematic cross section (bottom) of ULPCVD furnace system [101].

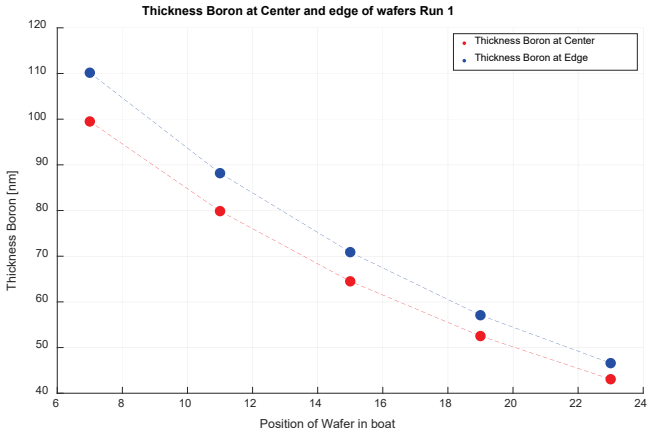

Figure 2.10. B-layer thickness as a function of wafer positioning, for deposition at 400 °C for 150 min, with a B_2H_6 flow of 43 sccm.

(d) MBE system

In a cooperation with Institut für Halbleitertechnik (IHT) at the University of Stuttgart, MBE samples were made available for this study. Different than the 3 machines mentioned above that use B_2H_6 pyrolysis, the boron layer is deposited from a Knudsen effusion cell of elemental boron. One of the most important aspects of MBE is the extremely low deposition rate (few nm per hour) that allows the layers to grow layer by layer. The deposition takes place in ultra-high vacuum from 10^{-8} – 10^{-10} mbar, to avoid the contaminants. Thus, the layer uniformity and purity are guaranteed. Due to the physical deposition nature, the layer can be deposited at temperatures down to room temperature [102].

2.4.2 Surface cleaning prior to deposition

For nm-thin layers the integrity of the B deposition will be disrupted by any native oxide, particle contamination or other residues on the Si surface. Therefore, before loading into the CVD reactor, the wafers were immersed in a diluted HF solution to remove native oxide and H-passivate the surface against native oxide formation. This was followed by spin rinse drying or Marangoni drying [103], which is an effective substitute as the formation of drying spots is avoided [104]. After drying, the samples were immediately transferred in the reactor, either in the load-lock of the reactor where they are continuously purged by oxygen-free N_2 gas, or in the process chamber where the system is pumped down. Depending on the different clean room facilities and protocols, the specific method could vary. Table 2.1 gives the core cleaning steps for the samples deposited at TU Delft (Epsilon) and UTwente (Picosun, ULPCVD). The summary of the deposition machines mentioned in 2.4.1 is listed in Table 2.2.

TABLE 2.1 SAMPLE CLEANING PRIOR TO DEPOSITION AT TU DELFT AND UTWENTE

Facility	TU Delft	UTwente
Organic/metal removal	HNO_3 99% + HNO_3 65% 110°C	Ozone steam
Native oxide removal	0.55% HF dip	1% HF dip
Sample Drying	Marangoni drying	Spin drying

2.4.3 Deposition machines summary

TABLE 2.2 MAIN DEPOSITION REACTOR PROPERTIES

Reactors	Epsilon	Picosun	ULPCVD	MBE
Precursor	0.2% B_2H_6 in H_2	5% in B_2H_6 in Ar	5% in B_2H_6 in Ar	/
Carrier gas	H_2 or N_2	Ar and/or N_2	/	/
Temperature range	400°C - 700°C	RT - 550°C	RT - 850°C	≥ RT
Loadlock	Yes	Yes	No	No
Pressure range	10^{-3} mbar - AP	1 - 10 mbar	10^{-3} mbar	10^{-8} - 10^{-10} mbar
Special features	Rotating susceptor	In-situ growth monitoring	Batch process	Independent of temperature

Standard sample cleaning steps incorporated with table 2.1:

Yellow: TU Delft; Green: UTwente; Grey: U Stuttgart

2.5 Analysis Techniques

2.5.1 Ellipsometry for thickness measurement

Spectroscopic ellipsometry (SE) is a non-destructive optical technique to measure the change in polarization state of the beam induced by the reflection from the sample (film). The polarization change is characterized by the magnitude of the reflectivity ratio Psi (Ψ) and phase difference Delta (Δ), which are acquired as a function of wavelength. The phase information Delta is particularly sensitive, enabling the measurement of sub-nanometer thickness levels. Based on wavelength-dependent Psi and Delta, a complex dielectric function can be extracted, providing the wavelength-dependent values of the refractive index (n_R) and the extinction coefficient (k_E). The polarization change is dependent on the optical properties and thickness of the measured sample. Ellipsometry is commonly used to determine the optical constants and thickness of the film. However, in order to obtain both the optical constants and thickness information, an optical model must be built for the specific material. Though for some of the standard materials like Si or SiO_2, optical constants are already given in the modeling software library, it is necessary to establish an optical model for other materials, especially when the material is amorphous or inhomogeneous. For ultra-thin films, this

technique is fast, non-destructive and cheap compared with TEM. In this thesis, we focus on the thickness measurement of B-layers with in-situ and ex-situ Woollam M2000 spectroscopic ellipsometry. All the thickness measurements were performed quantitively by ex-situ SE, due to its ease of calibration. The in-situ SE is used in two ways. On one hand, in-situ SE enables the monitoring of the thickness in real time deposition qualitatively, which is important for observing the influence of the deposition conditions, e.g., reactive gas flow, total pressure. It is also particularly useful to determine if there is any surface reaction at all under critical conditions, e.g., low temperatures. On the other hand, with SE the substrate temperature (T_s) can be measured by using the known temperature dependence of optical constants of certain materials, such as a Si (100) wafer. Although there is a deviation between the temperature value measured by SE and the system thermocouple, we consider the T_s has reached the chamber temperature at the point when SE signal becomes stable.

The SE modeling software used in this thesis is CompleteEASE®, where in theory both the optical constants and thickness of the film can be extracted based on the measured Psi and Delta. In reality, however, in order to determine the thickness of B layer, an optical model has to be established and calibrated. From previous reports [18], we learned that the physical properties of B deposited at 400°C and 700°C are different, hence it is logical to establish separate optical models. The optical constants are obtained by fitting with the SE oscillator Tauc-Lorentz with known thickness. The B-layer is modeled with two regions: the first region directly on the Si containing a compact homogeneous boron film and a surface region of incomplete (non-compact) boron coverage commonly referred to as the roughness layer [105].

2.5.2 Electrical characterization with test structures

The chemical B-to-Si bonding at the interface is of great importance for the electrical characterization of PureB diodes and is determined by the exact B-layer processing, including pre-cleaning, B deposition and post-processing. To investigate the influence of the processing, several dedicated electrical test structures were implemented to anticipate the performance of the PureB devices using knowledge of the as-deposited B that reflects the electrical properties of B-Si interface. Test structures were designed and fabricated in a way that pre-processed samples could be stored and be ready for deposition after the cleaning procedure. Moreover, directly after the B-deposition, the samples could be electrically measured without making any metal contacts.

The probes were placed in the heavily implanted p^+ areas as contacts. Thus, the process-analysis turnaround time is short. In this thesis work, three electrical test methods were applied and will be discussed in detail in Chapter 3. Each method serves a unique purpose.

The 2-diode test method was designed to quickly discern if metallized diodes act as p^+n or Schottky junctions. The method compares the hole injection to the electron injection. The hole injection should be the same for all p^+n-type diodes, but can be cut off in the case of high work function Schottky diodes such as many Al-Si Schottky junctions. Moreover, the hole current level can be determined independent of generation-recombination currents from defects formed near the metallurgical junction. For PureB diodes this gave a method of comparing different pre-deposition procedures and deposition techniques while confirming that a p^+n-type diode was realized.

The standard Al metallization of PureB diodes was seen to degrade the diode characteristics if the B-layer was too thin or grown on contaminated Si surfaces. Therefore, test structures were designed to allow electrical characterization without processing metal contacts. One type was used to measure the conductivity along the B-Si interface, which not only gave direct information related to the series resistance of PureB photodiodes, but also could be used to monitor the quality of B-Si bonding. The B-layer itself has very high resistivity so the bulk layer does not contribute significantly to the sheet resistance of the interfacial hole layer. The complete surface coverage of B on Si was also identified as the point where a further increase of the layer thickness no longer lowered the sheet resistance [23]. The interface conductivity was also dependent on any B-doping from diffusion into the Si substrate, as well as the substrate n-doping. According to previous studies, for n-Si with 10^{15} cm^{-3} substrate doping, the sheet resistance for 400°C deposition is 35 kΩ/sq, and 10 kΩ/sq for 700°C [74, 98]. These two numbers became important as references for evaluating the PureB diode quality.

To also extract the electron current component from the *I-V* characteristics of non-metallized B-layers, a series of PureB and implanted p^+n diodes were designed, where the hole current in all the devices can be assumed to be the same if the PureB diode functions as a pn-type junction. This also gave information on the quality of the B-Si bonding because the suppression of the electron injection is determined by the concentration of the interfacial hole layer induced by the negative fixed charge associated with the

B-Si bonding. This test procedure gave a low turnaround time and non-destructive way of evaluating different deposition methods in terms of diode characteristics.

2.5.3 Wet-etch tests of bulk B-layers

Unlike the electrical characterization which focuses on evaluating the bonding at the B-Si interface, the wet etch tests are more focused on the integrity and quality of "bulk" boron layer itself. The bulk boron is important not only for protecting the B-Si interface from degradation, e.g., oxidation, but also for MEMS applications. For example, a nanometer-thin boron layer was capable of protecting the Si from the anisotropic Si etchants TMAH and KOH. However, this was only possible when the layer is free of pinholes and weak spots, which were more prevalent when the layer was thin. Thus, by immersing the sample in TMAH or KOH and observing the effect on the Si, the quality of the boron layer was evaluated. The surface before and after etching was examined by NICM with which the non-uniformities on the Si surface become visible. For a higher resolution surface investigation, SEM and AFM were used. The etching depth and roughness are measured by height measurement with a DEKTAK surface profiler. In this thesis, 25 % TMAH by weight at 85°C and 25% KOH by weight were used to give an etch rate of Si of approximately 30 μm/hour.

It was possible to pattern B-layers using resist masks and standard aluminum etchant (80% phosphoric acid, 16% acetic acid and 4% nitric acid). The etch rates varied a lot depending on the boron deposition conditions. It is believed that the lower the etch rate, the higher the B/B bonding and layer compactness. The temperature of the solution ranged from room temperature to 65°C, and the thickness/roughness of the layer was measured by ellipsometry.

2.6 Conclusion

In this chapter an overview was given of the basic physical structures of elemental boron, and the theoretical mechanism of borane decomposition/interaction with the Si surface. The fundamental structure of pure boron polymorphs is the B12 structure. The formation of a complete boron coverage on silicon is particularly important for PureB applications because any unoccupied sites may electrically will become the source of unwanted leakage current, and with respect to processing could become weak spots for etchants to penetrate. Both 400°C and 700°C depositions were

proven to make excellent PureB diodes. As mentioned in Section 2.3, the 700℃ layers were chemically more robust while the 400℃ layers have broader process compatibility. No bulk doping is expected for B under 500℃.

The four types of deposition systems used in this thesis to grow B have different advantages. The Epsilon CVD system produces the best overall B-layer quality; the Picosun is capable of in-situ growth monitoring; the ULPCVD furnace makes batch deposition possible; MBE allows room temperature deposition with great uniformity and contamination control. In this thesis, the boron layer thickness is measured both in-situ and ex-situ with ellipsometry, which is known to be non-destructive, fast and reliable. The techniques and test structures developed for as-deposited B analysis were summarized briefly, and will be further discussed in Chapter 3 and 4.

Chapter 3 Electrical Test Structures

In this chapter, a review will be given of the electrical test structures that have been used to characterize the different B-layer deposition methods and the structures that have repeatedly been used in this thesis work will be described in detail. As a starting point, a number of test structures dedicated to the characterization of PureB diodes had already been designed. Mainly the aim was to develop short turnaround-time process-flows so that many process-parameter variations could be studied as efficiently as possible. The main goal was to measure and analyze the individual electron and hole current flows in the different types of PureB diodes and compare them to the conventional deep diffused B-doped junctions. The most suitable test structures for doing this are vertical pnp's with the PureB region as emitter. In these devices, to best separate the electron/hole currents, it is also desirable to have a low collector resistance, a thin base region that nevertheless has a low base resistance and does not readily punch-through, as well as small external base-collector diode areas. Several results obtained with such vertical pnp's are reported in [48, 67]. However, the fabrication of vertical pnp's with these properties demanded processing steps that were not readily available in the MESA+ Nanolab. Therefore, they have not been used in the present study. Instead, effort was put into evaluating how useful it would be to work with lateral pnp structures. These can be made in a 2-mask-step process and not only bipolar transistor measurements can be performed but also 2-diode measurements like those reported earlier in [63] are possible. In that work the degree to which a CVD deposited arsenic layer was able to dope the Si surface when activated by excimer laser annealing was studied. The diode *I-V* characteristics are shown in Fig. 3.5 and 3.6. With the 2-diode technique equally simple measurements made it possible to determine how significant the hole injection from the p-substrate into the n-Si/metal contact region was with respect to the electron injection from this region into the substrate. In the present thesis work, a more in-depth analysis using PureB diodes was made to better establish the usefulness of this method [106, 107] and this is reviewed in Section 3.1.3.

The vertical and lateral pnp bipolar transistors, were all fabricated with Epsilon B-layers at TU Deflt. They had aluminum contacts to the emitter, base and collector regions mainly in the form of sputtered Al/1%Si but also as pure Al. For the low-temperature B-depositions that are a main focus of this thesis, earlier work had already made clear that the B-bonding was much

looser than for the high-temperature B-layers. This meant that thin layers when metallized with pure Al displayed shorting of the Al to the Si leading to Schottky-like high PureB diode currents. This impeded the study of the interface of the B with the Si that was found to be the important region for obtaining low saturation currents. Therefore, test structures without metallization were developed [21, 106, 108] with which PureB diode characteristics and the sheet resistance, R_{sh}, along the B-Si interface could be measured. These test structures have been expanded in the present study to also make the measurement of the electron injection, I_e, into the PureB p-type region possible. This is described in Section 3.2.3. Most of the electrical experiments performed in this thesis use these test structures to evaluate the different B-layers in terms of R_{sh} and I_e. Combined with the short turnaround-time etch tests described in Chapter 4, these measurements give a good indication of what the corresponding PureB diode performance would be.

3.1 Metallized Diode Test Structures

3.1.1 Vertical pnp transistors

As already discussed in connection with Fig. 1.9, vertical pnp's with PureB emitters were reported in [67] where B-layer deposition was performed at 500°C and 700°C. Both layers resulted in a high G_E, comparable to that of implanted p^+n diodes with deep junctions. The basic design of the transistors was as shown in Fig. 3.1 where also the current gain of pnp's made at the 2 temperatures are compared. The current gain increases as the B-layer thickness increases. The 500°C deposition had a longer incubation time but otherwise the behavior was very similar to the 700°C deposition.

In the thesis work of Lin Qi [48], vertical pnp's were also studied with PureB emitters deposited at 400°C. An example of the results is shown in Fig. 3.2 where a comparison to 700°C devices is made. The base current of the 400°C devices is more than 3 decades higher than for the 700°C devices. Experiments where the metal on the central part of large diodes was removed before alloying, made clear that it was the presence of the Al on the emitter that was the cause of the high currents. It was concluded that the high roughness and loose bonding of the B would not entirely protect the Si surface from being reached by the Al, locally giving Schottky-like current levels. This prohibited the use of very thin B-layers at this low temperature when metallization was necessary.

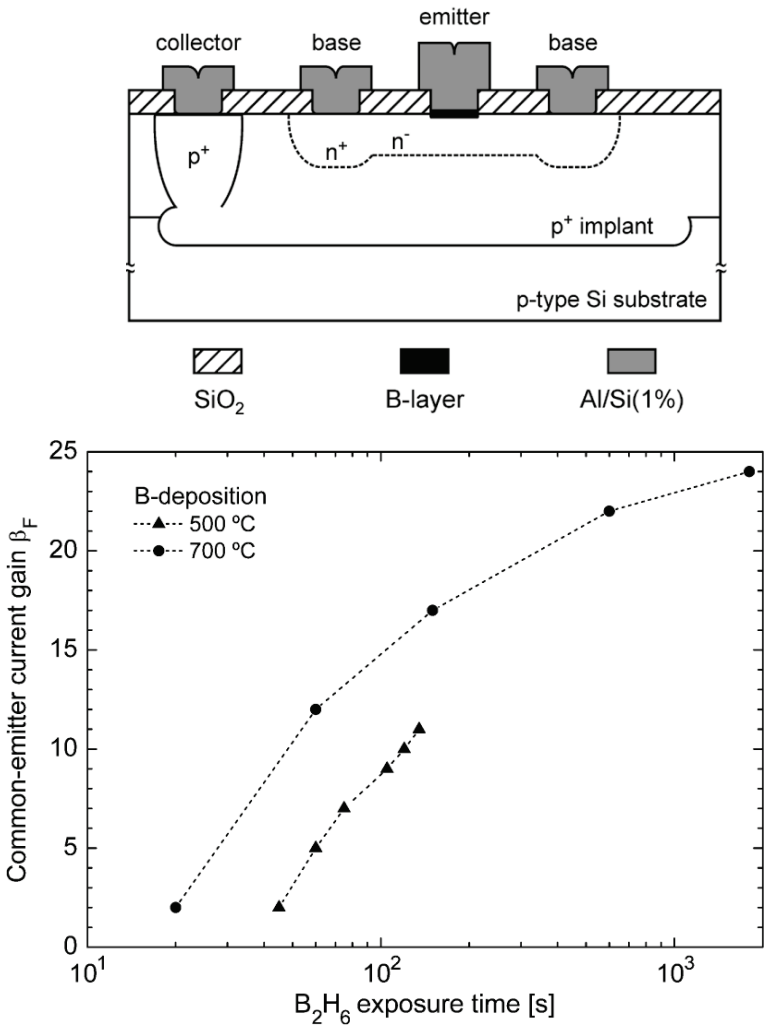

Figure 3.1. Top: Schematic cross section of vertical pnp bipolar transistors. Bottom: Common-emitter current gain of pnp bipolar transistors as a function of B_2H_6 exposure time at V_{EB} = 0.45 V for an emitter area of 40 × 10 μm^2. The emitter region has been fabricated with B-deposition at either 500°C or 700°C. The base region has been formed by phosphorus implantations of 1 × 10^{12} and 1.5 × 10^{12} cm^{-2} at 40 and 180 keV, respectively [67].

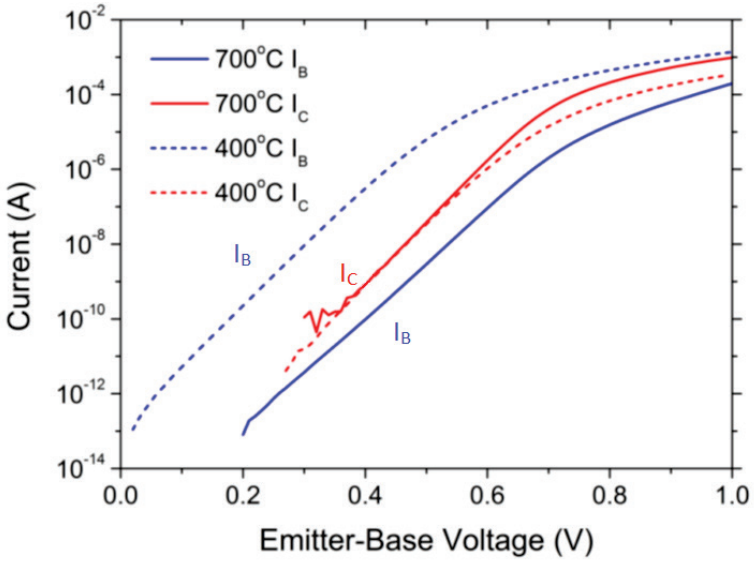

Figure 3.2. Gummel plot of PureB vertical pnp bipolar transistors. The emitter area is 40×1 μm^2 [48].

3.1.2 Lateral pnp transistors

At the start of this thesis project, a number of wafers were available with PureB diodes fabricated on n-type Si substrates in a very simple process flow as shown in Fig. 3.3 [106]. Also shown is the basic layout of a 2-diode test structure indicating that, when operated as a pnp transistor, the n-substrate forms the base region and the 2 diodes are contacted as either emitter or collector terminals. The W_B is the distance between the emitter and collector, and the W_E and L_E are the emitter width and length, respectively. The biasing of the structure when operated as a pnp is shown in Fig. 3.4 along with the expected electron and hole current flows. Two other biasing techniques are also illustrated: the single-diode and the parallel-diode biasing. All 3 biasing methods were used to study the emitter diode properties. A comparison is also made to the current-flow situation where the PureB emitter is replaced by an Al-Si Schottky diode emitter.

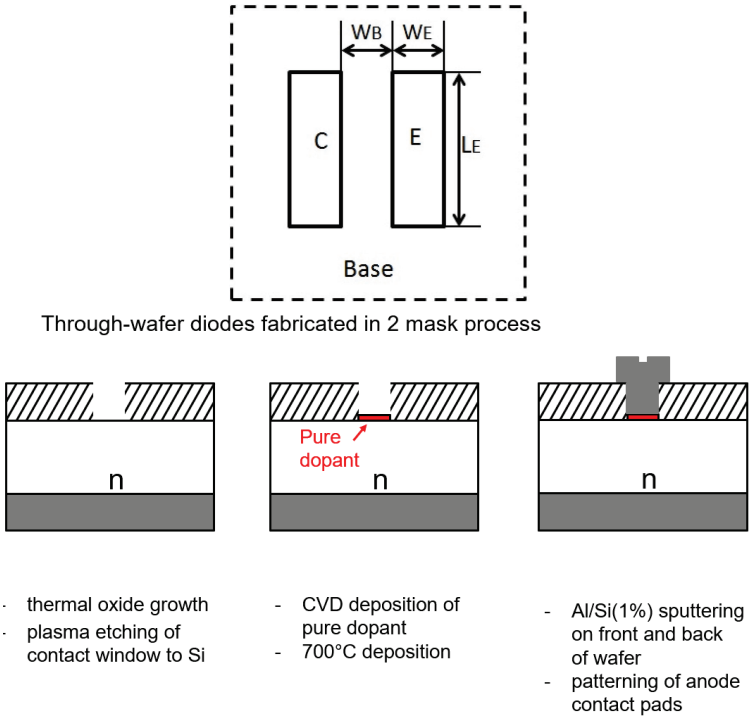

Figure 3.3. Top: Basic layout of a 2-diode test structure with equally sized rectangular emitter and collector windows. Bottom: Basic process flow for fabrication of a single diode with metal contacting of the deposited region and the back of the n-type Si substrate. The studied depositions include pure B, As, or P, and B-doped Si [106].

In the lateral pnp case, Fig. 3.4 (a) and (b), the emitter and collector are biased as a lateral bipolar transistor in forward active mode with the substrate as base so $I_E = I_B + I_C$. The I_C is governed by the effective base Gummel number, G_B, that for ideal pn junctions is determined by the distance and integral doping between the E and C contacts. For the Schottky case, the level of hole injection depends on the effective Schottky barrier height (SBH) of the junction. If it is very low, the electron current is very high and the supply of holes may become limited [109]. This means that at a certain forward bias voltage, the hole current will saturate and no longer increase exponentially with the voltage. This effect may be difficult to identify in the measurements because the high current also means that the series resistance has a large impact and can attenuate the current already at low forward voltages [110, 111].

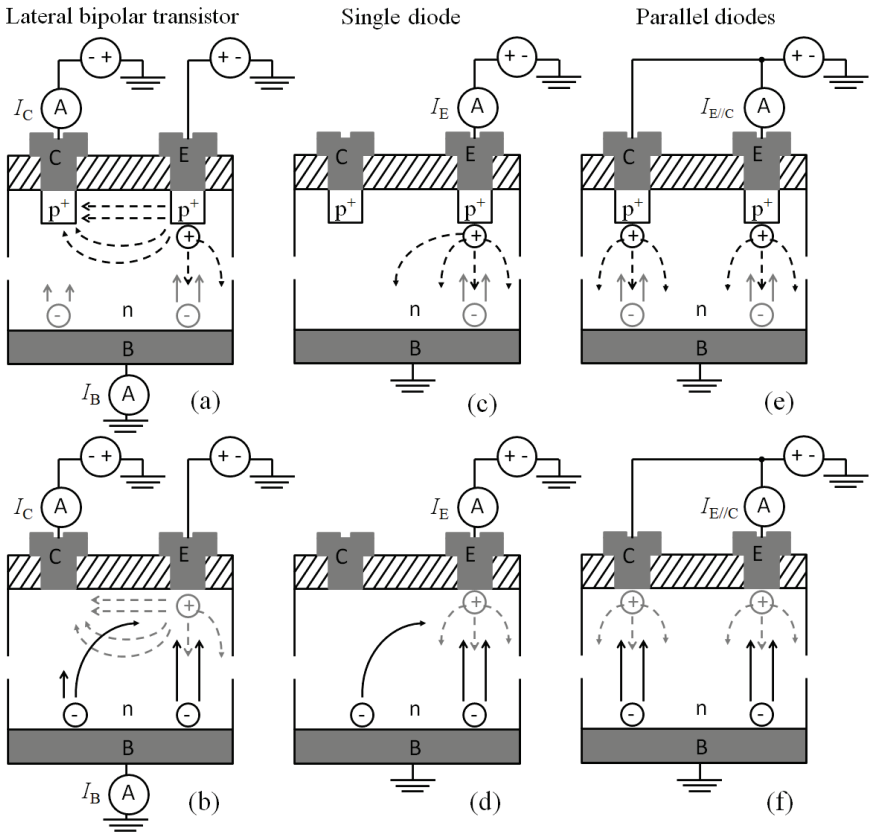

Figure 3.4. Schematic cross-section of the 2-diode test structure for 3 different biasing methods. The expected current flows are indicated by black arrows for the dominant carrier flows and light grey arrows the other carrier-type flows. The hole flows are represented by dashed lines and the electron flow by solid lines. The top row is for p^+n-like diodes and the bottom row for Schottky-like diodes.

In Fig. 3.5, examples of Gummel plots for a PureB-emitter and three different Schottky-emitter pnp's are compared. The latter are made with the same base-collector structure as the PureB device, but with or without exposures at 700°C to arsine or phosphine instead of diborane. They all have decades higher base current than the PureB device. The I_B is highest for the phosphorus (P) deposition, presumably because the surface doping with P, which is possible to about 2×10^{20} cm^{-3}, lowers the Schottky barrier height. The arsenic (As) deposition prevents native oxide growth but does not n-dope the Si surface. For the device without any deposition to protect the Si surface

against native-oxide formation, the I_B is 2 decades lower and non-ideal, indicating that oxide was present at the interface and increased the effective G_E. The I_C of the other devices is of the same level at low voltages. While the PureB I_C curve is ideally exponential up to about 0.6 V forward bias, the two Schottky curves are already attenuated by series resistance at 0.3 V. In contrast, the I_C for the "no-depo" Schottky is decades lower. This suggests that the effective G_B was also increased by the presence of oxide at the interface, i.e., there is no longer a "clean" metal-Si interface.

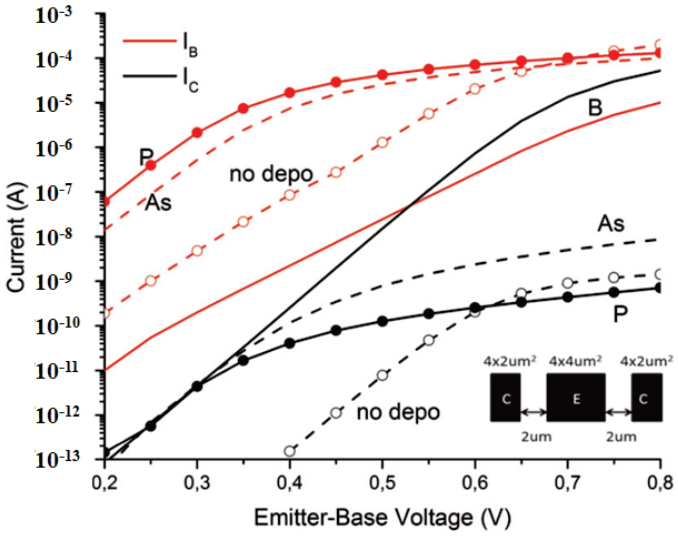

Figure 3.5. Gummel plots for test structures without and with a surface deposition of either B, As, or P, I_B is in red and I_C in black. The substrate doping is 10^{15} cm^{-3}. The schematic top view layout (insert) gives the dimensions of the measured 2-diode structure [106].

The I_B of all the lateral pnp's will for a great part be dominated by the emitter-base diode current which, depending on the exact geometry of the device, will flow directly between the emitter and the base contact on the back of the wafer. Therefore, unlike for the vertical pnp's, the I_B does not give any direct means of calculating G_E. Interpretation of the measurements in terms of G_E would in some situations be facilitated if a comparison to a deep p^+n diffused junction could be made.

3.1.3 2-diode measurement techniques

A fundamental difference between the electron and hole current injection is found in the volume of the region into which they are injected. The emitter region is limited in size to the designed area of the contact windows, give or take some variations that may be caused by the actual processing. Therefore, the injected electron current is proportional to the emitter area. In contrast, the holes injected into the substrate can spread in all directions into the substrate [112]. In the present case with a low-doped 525-µm-thick substrate, the perimeter hole current per micrometer readily becomes much higher than the laterally uniform current density being vertically injected through the surface area of the contact. The spreading of the holes will be attenuated by any hole injection from other diodes being operated in the vicinity.

For single-diode operation, illustrated in Fig. 3.4 (c) and (d), only the emitter diode under investigation is connected and forward biased. In the PureB diode case, hole injection into the substrate dominates because electron injection into the emitter is suppressed by a high G_E. In the Schottky diode case, electron injection dominates. In the parallel-diode case, Fig. 3.4 (e) and (f), both the emitter and collector are connected and biased in forward and the current flow through the emitter is defined as $I_{E//C}$. The spreading of the holes injected from the emitter is limited by the holes spreading from the collector, making $I_E > I_{E//C}$.

The *I-V* characteristics of an As-deposited Schottky diode and a PureB diode with $N_{sub} = 10^{15}$ cm^{-3} are shown in Figure 3.6, along with the extracted ΔI_E. The visible differences between I_E and $I_{E//C}$ are typical for the two types of diodes: for the PureB diode, the relative current discrepancy, $\Delta I_E/I_E$, is large in the low current exponential (i.e., low injection) region because the spreading of the hole current is restricted by the current flow from the adjacent diode. As the current increases with voltage, the discrepancy becomes small relative to I_E because the current increase becomes attenuated by series resistance. The opposite is true for the Schottky case because in principle the electron current is proportional to the diode area, unaffected by the spreading through the substrate. The spreading is, however, restricted when the collector is contacted and this increases the effective series resistance through the substrate. This is seen as an increasingly large discrepancy when high current levels are reached. For the PureB case, dominated by hole injection, $\Delta I_E/I_E$, with $\Delta I_E = I_E - I_{E//C}$, will be large but for the Schottky case, it will depend on the height of the Schottky barrier. To avoid the influence of series resistance

on Schottky diodes with low SBH and thus very high electron injection, it is advantageous to have the smallest possible emitter dimensions. Nevertheless, the current level in the devices we studied was mainly so high that the low voltage region, where hole injection of the same level as in the PureB diodes is expected, was not measurable.

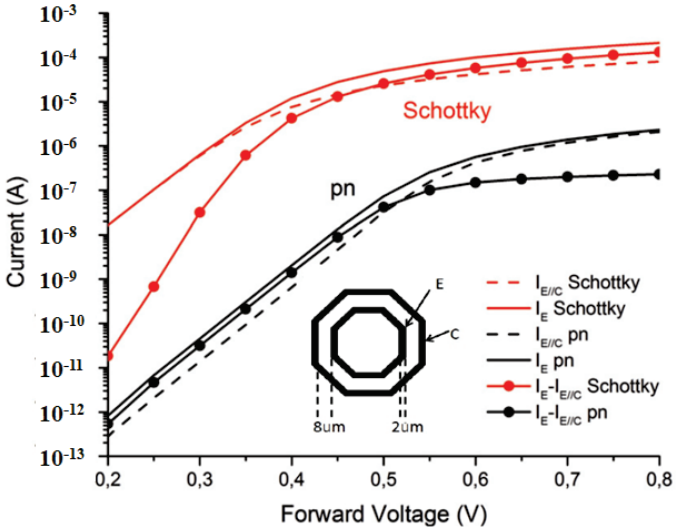

Figure 3.6. I_E, $I_{E//C}$ and ΔI_E as a function of forward voltage for Schottky diode (in red) and a PureB diode (in black). The substrate doping is $10^{15}cm^{-3}$. The schematic gives the dimensions of the measured 2-diode structure; the emitter is 431 µm long [106].

The emitter current can be expressed as follows:

$$I_E = J_A A_E + J_P P_E + I_{leak} = I_{SE}\left(e^{\frac{qV}{kT}} - 1\right) + I_{leak}, \qquad (3.1)$$

where A_E is the emitter area in which a laterally uniform current density J_A flows, P_E is the on-mask perimeter, J_P is the current per micrometer that then accounts for the current not included in $J_A A_E$, and I_{leak} is the non-ideal current component. In view of the limited processing, it can be expected that the leakage component originates from defects in or near the depletion region over the emitter junction and not in the bulk of the substrate. This leakage is therefore the same whether or not the collector is connected. By using an emitter area, A_E, that covers a laterally uniform current-flow region in both contacting situations, we can write:

$$I_{\mathrm{E}} = J_{\mathrm{E}}A_{\mathrm{E}} + J_{\mathrm{PE}}P_{\mathrm{E}} + I_{\mathrm{leak}} = I_{\mathrm{SE}}\left(\mathrm{e}^{\frac{qV}{kT}} - 1\right) + I_{\mathrm{leak}}. \quad (3.2)$$

$$I_{\mathrm{E||C}} = J_{\mathrm{E}}A_{\mathrm{E}} + J_{\mathrm{PE||C}}P_{\mathrm{E}} + I_{\mathrm{leak}} = I_{\mathrm{SE||C}}\left(\mathrm{e}^{\frac{qV}{kT}} - 1\right) + I_{\mathrm{leak}}. \quad (3.3)$$

Therefore ΔI_{E} follows the ideal *I-V* characteristic:

$$\Delta I_{\mathrm{E}} = J_{\mathrm{PE}}P - J_{\mathrm{PE||C}}P = (I_{\mathrm{SE}} - I_{\mathrm{SE||C}})\left(\mathrm{e}^{\frac{qV}{kT}} - 1\right). \quad (3.4)$$

The above formulations are only valid for low currents where the series resistance through the Si substrate and the emitter contact are not playing a role and that both components have the same ideality factor. The PureB $\Delta I_{\mathrm{E}}(V)$ characteristic shown in Fig. 3.6 has an $n = 1$ in the low voltage region as would be expected from (3.4). This is not the case for the Schottky diode that has $n <$ 1 in this region, confirming that the I_{E} is so high that series resistance effects dominate the whole curve.

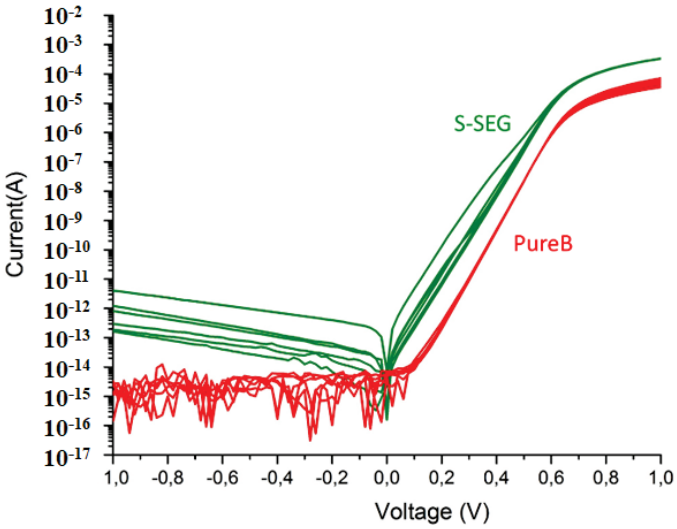

Figure 3.7. Across-the-wafer measurements of diode *I-V* characteristics for PureB and SEG diodes with area 20×1 μm^2. The B layer thickness is about 3 nm [107].

In Fig. 3.7 the *I-V* characteristics of a set of PureB diodes is compared to those of SEG (selective-epitaxial-growth) diodes that have a deposition of B-doped Si in the contact windows, grown by selective epitaxy. The PureB

diodes display uniformly low saturation current and an ideality factor $n = 1$. The SEG diodes have about 2 decades higher current with a decade spread and consistently have varying values of $n > 1$.

Despite the lower saturation current of the PureB diodes the attenuation at high forward voltage due to series resistance is higher than for the SEG diodes. This is because the resistivity of the B layer is very high (> 500 Ω-cm [84]), so for a low series resistance a less than 3-nm-thick tunneling layer should be used. This is made clear in Fig. 3.8 where the *I-V* characteristics of devices with different PureB thickness are displayed. In this figure the differential current ΔI_E is also shown, revealing behavior characteristic of p^+n diodes where the hole injection into the substrate dominates. At low voltages the curves are equal with an $n = 1$. At high forward voltage the attenuation from series resistance is highest for the thickest PureB layer as would be expected. Even for the lowest series resistance the deviations in ΔI_E typical of high electron current ($n < 1$) are not seen indicating that the electron injection in the emitter is much lower than the hole injection. The series resistance with the 2-nm-thick PureB layer is so low that the attenuation is not larger than what is seen for the SEG samples.

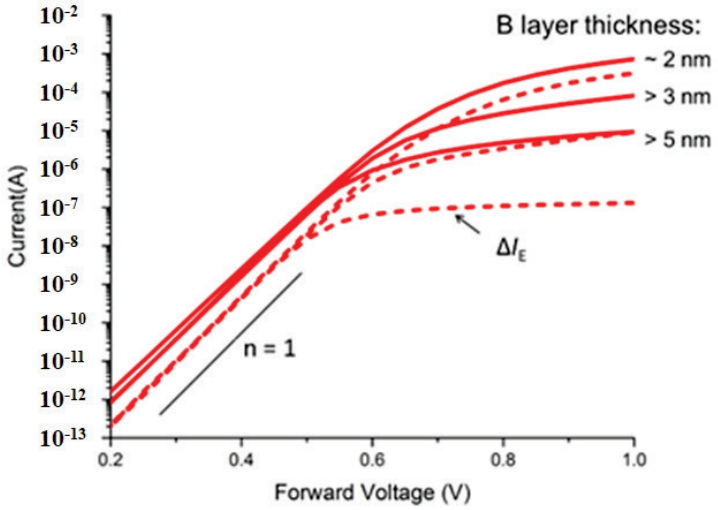

Figure 3.8. *I-V* characteristics of diodes with different PureB layer thickness showing the emitter current I_E (solid line) and the differential current ΔI_E (dashed line). The anode area is 20x1 μm^2 [107].

The *I-V* characteristics of 2 SEG diodes are shown in Fig. 3.9. At low voltages these diodes show the same ΔI_E level as is measured in the PureB diodes, i.e., the hole current is the same in both cases. The non-ideal diode leakage current does not appear in the differential current indicating that it is related to defects in the p^+ SEG region as expected. The effects of series resistance become visible when the current level increases with an $n < 1$. This is typical for high electron injection, i.e., the high SEG diode saturation current comes from high electron injection into the SEG emitter. A much higher integral doping in the SEG region would be needed to suppress this injection. The examples given in Fig. 3.8 and 3.9, underline the difference between have a high series resistance through either the emitter region or the n-substrate. The ΔI_E region with $n < 1$ is only seen when the substrate resistance is dominating due to the high electron current level.

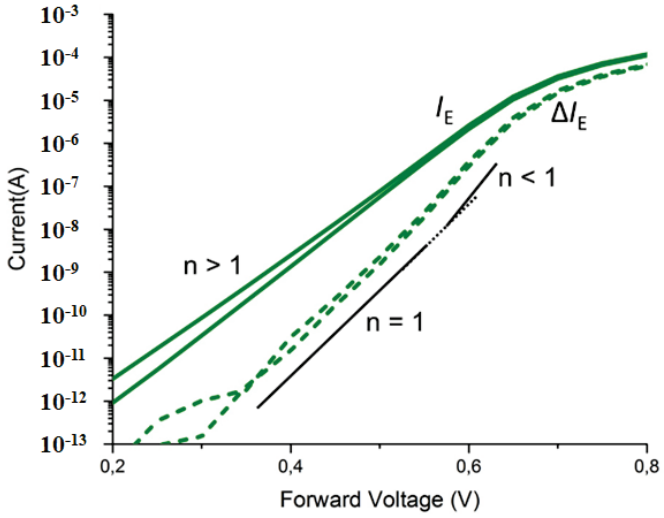

Figure 3.9. *I-V* characteristics of 2 SEG diodes showing the emitter current I_E (solid line) and the differential current ΔI_E (dashed line). The anode area is 20x1 μm^2 [107].

In [106] a number of different E-C configurations were studied which showed that the 2-diode measurement technique was more robust than the pnp measurements. The latter are sensitive to punch-through if the distance between the E and C is too small, and if it becomes very large or the substrate doping becomes too high, the collector current becomes so small that the vertical E-B and C-B diode currents dominate. In contrast, the 2-diode measurement of ΔI_E was unaffected by E-C punch-through and gave clear

results for E-C distances as high as 80 μm. The same was true when doping levels up to 10^{18} cm^{-3} were tested.

3.2 Non-metallized Test Structures

From the work with the PureB pnp test structures it became clear that the metallization of the B-layers could be detrimental for the current levels for very thin B-layers and this effect became more prominent for layers grown at low temperatures, and emitter perimeter was then particularly vulnerable to leakage currents. This complicated the study of the electrical behavior of the B-layer itself. From experiments where the Al metallization was locally removed it was possible to estimate the sheet resistance of the p-type surface layer created by the B deposition but there were cases where this Al removal also appeared to degrade the quality of the PureB diodes [18]. A first measurement without having put metal on the B-layer was reported in [25] by using structures where the B-layer was covered with a PECVD oxide before metallization. Later it was found that the plasma processing could dramatically degrade the properties of the low temperature B-layers. Therefore, to study the very thin layers, a method was needed to enable measurement of the as-deposited layers. This led to the development of the sheet resistance test structures described in [19, 23] where the B-layer was biased via the Si by directly contacting implanted p^+-regions. In this thesis work, the applicability of these structures was extended to determine the electron current injection into the PureB p-like regions as described in Section 3.2.3.

In Fig. 3.10 the basic process flow for the fabrication of non-metallized test structures is shown. The starting substrates were (100) 1-10 Ωcm n-type Si wafers. After standard cleaning, a thermal oxide layer of 235 nm is grown by dry oxidation. Then p^+ regions for probe contacting were created by B^+ implantation through the oxide followed by annealing at 950 °C, to give a surface doping concentration of 10^{19} cm^{-3} and a junction depth of about 0.5 μm. The windows to the p^+ regions and the Si where a thin-film was to be deposited, were opened by wet etching in buffered HF (BHF). Just before the deposition, a diluted HF dip-etch step was performed to remove native oxide. Thus, the whole process only required 2 masks.

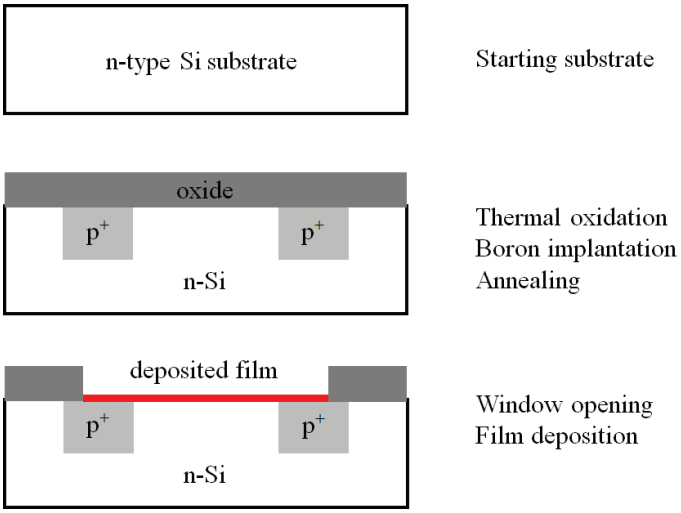

Figure 3.10 Basic process flow of the non-metal test structures.

3.2.1. Sheet resistance measurements: van der Pauw structures

Van der Pauw structures were designed as shown in Fig. 3.11. These structures are very popular for measuring the sheet resistance, R_{sh}, of the central region because only a single measurement is needed. In the present situation, they are also attractive because it is a currentless measurement that eliminates the influence of the often high series resistance from having to contact Si directly rather than via a metal. In principle the R_{sh} can be calculated as [113]

$$R_{sh} = 4.53 \times V/I. \tag{3.5}$$

However, this formulation is only correct if the current flows entirely through the deposition region. This is only approximately the case because all the pn regions will have some diode leakage. When this becomes of the same size as the current I, a much lower R_{sh} will be extracted. In these Van der Pauw structures, there are two reasons why one should be wary of this effect. For the first, the R_{sh} was often in the 100 kΩ range, and second, the perimeter of the deposition region was often prone to imperfections that led to g-r currents that added significantly to the leakage and also destroyed the symmetry of structures. For these reasons, the ring-shaped structures discussed in the next section were used if I and the leakage current were comparable.

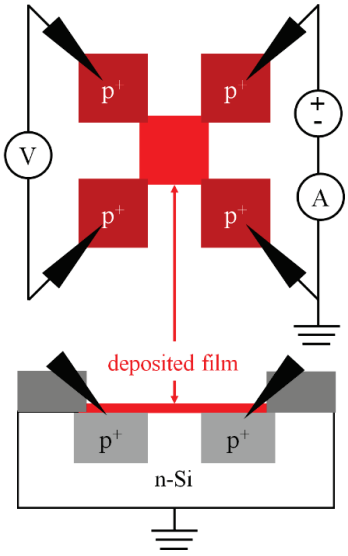

Figure 3.11. Van der Pauw sheet resistance test structure (left) and top view contact method (right).

3.2.2. Sheet resistance measurements: ring structures

Sets of ring structures were designed as illustrated in Fig. 3.12 [108]. Each ring structure had a fixed radius r_g =164 μm so the total perimeter, P = 2061 μm, was always the same despite the different width, L, of the rings. Sets of each 5 ring structures are designed with L = 10 μm, 20 μm, 40 μm, 100 μm, and 200 μm. The ring area where the B-layers are deposited and measured is called Deposition Under Test (DUT) ring. Five of such sets were designed. Sets S2 and S3 had a p^+-guard ring covering the whole perimeter region. This option was included for 2 reasons: for the first, any perimeter leakage due to a deficient B-coverage coverage at the edge of the oxide window was then eliminated, and, secondly, if the R_{sh} was very high, the low-ohmic p^+-guard ring would nevertheless ensure a rotational symmetric current flow from the inner to outer p^+ ring. In set S1 the p^+-guard ring was absent. In the sets S4 and S5, the p^+-region extends under the whole ring that in S4 was also covered with the B-deposition.

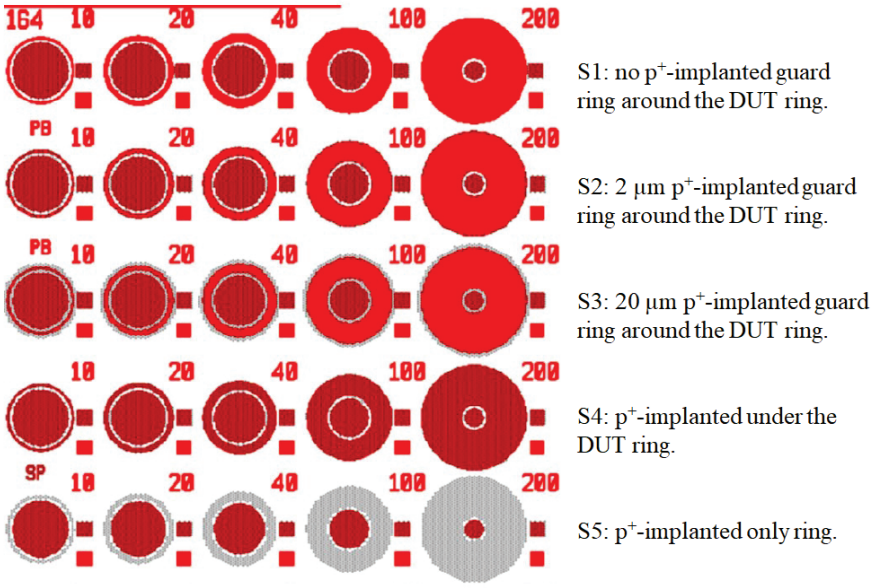

Figure 3.12. Set of ring-shaped test structures where the PureB-only regions are red, implanted p^+-regions are grey, and the overlap of both regions is dark red. In each row the perimeter of the PureB-only region is constant and equal to $4\pi r_g$ while the width of the ring has varying values L_i [108].

In Fig. 3.13 the biasing of the ring structure for measurement of the R_{sh} is illustrated. The R_{sh} increased as the ring width, L, increases. Due to the curvature of the rings, the $R_{sh}(L)$ is not linear, and a radial correction factor must be applied [114], where the indices $i = 1, ..., 5$ refer to each specific test structures in the given set of structures., and $L_i < L_{i+1}$, $i < j$.

$$\alpha_{ij}^{edge} = \frac{1}{2\pi} \ln \left[\frac{\left(r_g - \frac{1}{2}L_i\right) \cdot \left(r_g + \frac{1}{2}L_j\right)}{\left(r_g + \frac{1}{2}L_i\right) \cdot \left(r_g - \frac{1}{2}L_j\right)} \right]. \tag{3.6}$$

The R_{sh} is extracted as the slope of the plot of R_{mij} as a function of α_{ij}^{edge},

$$R_{mij} = R_{sh}\, \alpha_{ij}^{edge}. \tag{3.7}$$

In the study of these structures, it was found that the exact sheet resistance of the substrate could have a significant influence on the determination of the R_{sh}. For example, if the nominal sheet resistance of a B-layer was 35 kΩ/sq and $N_{sub} = 10^{15}$ cm^{-3}, then variations in N_{sub} from 10^{14} cm^{-}

^{3} to 10^{15} cm^{-3} cause a spread in R_{sh} from 32 kΩ/sq to 47 kΩ/sq. Therefore, when comparing different B-layer deposition methods this had to be taken into account.

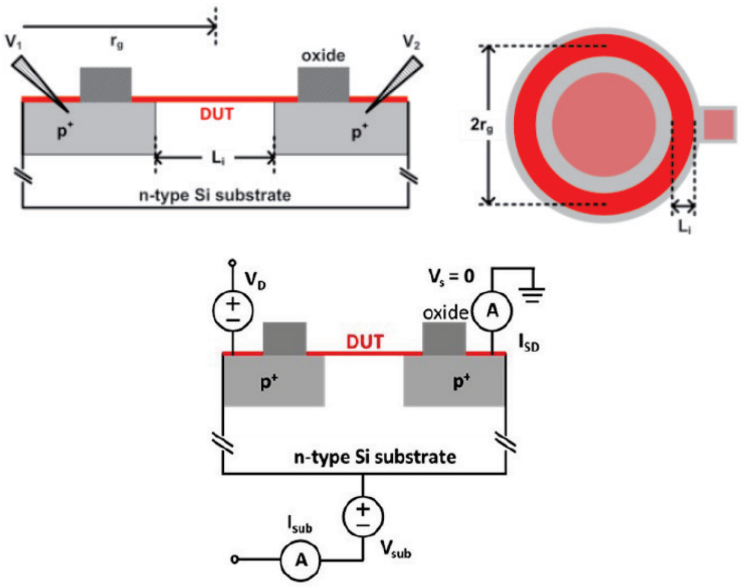

Figure 3.13. Schematic cross section (top left) and layout (top right) of the ring-shaped measurement structures. In each set the perimeter of the deposition-only region is constant and equal to $4\pi r_g$ while the width of the ring has varying values *Li*. (bottom) Schematics of the measurement configuration for voltage dependent JFET-like source-to-drain measurements used to extract the R_{sh} [48].

3.2.3. Extraction of electron current

The ring structures of Fig. 3.12 were also used to extract the electron current injection, I_e, into the PureB region. This is a parameter that can become decisive for the dark current of PureB diodes if the hole injection current, I_h, into the n-type region is of the same order or even smaller. When the hole and electron injection currents become of the same order, the structures can be used to determine the electron injection following the principles discussed in connection with Figure 3.2. The Gummel number of the n- and p-type regions determine the minority carrier injection currents. For the n-type region it is proportional to the integral doping of the wafer as determined by the wafer thickness (525 µm) and resistivity (1-10 Ωcm). This

gives an integral n-doping of 10^{12} – 10^{13} cm^{-2}, and for a ring structure with a ring width = 1031 µm and length = 200 µm, the I_h will be about 1 nA. The implanted p$^+$-regions have an integral doping of about 10^{15} cm^{-2} which means that the I_e into these regions will be in the range of 10 to 100 times lower than I_h. For 700°C boron depositions the I_e was also much lower than I_h, and could therefore not be determined accurately from diode *I-V* measurements. For low temperature B deposition, the I_e increased and it became possible to extract it. For diodes with the same L, the measured diode currents on S3 I_{dDUT}, and S5, I_{dp+}, structures are related as

$$I_{dDUT} = I_h + I_{eDUT}, \tag{3.8}$$

$$I_{dp+} = I_h + I_{ep+}. \tag{3.9}$$

Therefore, if I_{ep+} can be neglected

$$I_{eDUT} = I_{dDUT} - I_{dp+}. \tag{3.10}$$

There is a compromise to be made in the radius of the ring structures. The larger the r_g and the L, the higher the measured currents, which increases the accuracy when differential extractions need to be made. Moreover, the larger the inner radius of the rings, the smaller the influence on the radial current spreading into the substrate. However, the larger the structures, the higher probability that imperfections in the processing will cause leakage currents that inhibit the extraction of I_{eDUT}. One advantage of using I_e to compare different depositions is that, unlike the R_{sh}, it is independent of the substrate doping.

3.3 Conclusions

The electrical measurement techniques presented in this chapter were developed to study the currents flowing through PureB diodes in fast turnaround time process flows. In this thesis, in particular, the non-metallized test structures have been used to electrically characterize low temperature B-layer depositions of different types. The important optimization parameters were the electron current injection into the emitter and the sheet resistance of the interfacial hole layer formed at the Si surface under the B-layer. Both parameters are important for assessing whether the B-layer would have suitable electrical properties for use in a specific PureB diode application. For R_{sh} measurement, van der Pauw structures and set of ring structures were applied that complemented each other: the van der Pauw measurements

tolerated high contact resistance, but were susceptible to perimeter leakage, while the opposite was true for the ring structures. The ring structures were also used for extracting the I_e of all the low-temperature PureB diodes, which was possible because the electron injection into implanted p^+n regions was much lower than into the B-layer p-type regions.

Chapter 4 Material Analysis Using TMAH/KOH Wet-Etching

Boron and aluminum are both group III elements that act as acceptors in Si, but in the course of research on PureB diodes it became clear that the properties of interest for IC and MEMS processing are very different. In contrast to Al, B-layers were found to be resistant to etching in diluted HF solutions. The HF-resistance was essential for their successful integration in complex micromachined photodiode detectors [85]. Furthermore, Agata et al. [35] discovered that pure B-layers as thin as 3 nm deposited at 700°C could act as diffusion barriers for Al metallization to prevent spiking of the Si. However, the same article also demonstrated that the 1.8 nm B-layer was inadequate as a diffusion barrier, and a distribution of cavities in the Si was observed after Al removal by HF. This problem was caused by the poor uniformity of the B-layer at such low thickness, and increasing the deposition time to achieve thicker layers was a way to solve the problem. Although 400°C B-layers were not mentioned in that study, it would be reasonable to infer that their higher roughness and lower compactness would mean that a thicker layer would be needed to achieve the same performance as a barrier. For all CVD deposition temperatures from 400°C to 700°C, the B-layer has very good adhesion to Si, which has allowed the deposition and selective removal of Al layers with diluted HF [115].

In the course of the past development of PureB diodes, 700°C B-layers were also found to be resistant to TMAH, that is widely used in Si anisotropic etching. In this thesis work, this property was found to give a convenient way of characterizing the compactness and uniformity of B-layers deposited on Si. Similar to the effects of Al on B barrier-layers, exposure to TMAH can be used to check for any penetration through the B-layer because this causes visible Si cavities. This gives information on the reliability and robustness of the PureB detectors which is important for application in harsh environments as, for example, high-dose EUV or electron irradiation. This is even more important when developing PureB detectors with extremely thin B-layers. Even though electrical characterization can be used to test the integrity of the B-layer, reliably good diode characteristics are not sufficient to guarantee the physical robustness [35]. In a previous study [23], the increase of R_{sh} after several post-process steps could be related to the physical degradation of the bulk B-layer. However, more evidence is needed to confirm this. In this

chapter, an investigation is presented of a series of nanometer-thin B-layers deposited by CVD and their properties with respect to the TMAH and KOH wet-etching of Si. Deposition temperatures in the range 400°C - 700°C were applied where some samples were treated with extra processing steps like those discussed in [23]. The aim was to develop a wet-etch method to quickly evaluate the robustness of as-deposited B-layers, as well as to find the potentials and limitations of using the layers as a patterning ("hard mask") material for Si micromachining. Situations where the latter could have been useful were in the past encountered in connection with the fabrication of photodetectors and silicon-on-glass varactors [18, 115-117]. Both involved microstructuring of the Si using conventional dielectric masking layers, to either reduce resistance/capacitance parasitics [118-120] or to fabricate through wafer apertures [115]. In the course of this past research the robustness of the B-layers used for diode fabrication with respect to etching in TMAH or KOH became apparent and it had to be taken into account when designing process flows.

4.1 Conventionally Used Si Anisotropic Wet-Etch Masks

Crystalline silicon is widely used to fabricate micro-developed Si processing systems (MEMS) due to the well-developed Si processing methods and equipment that allow accurate patterning and controllable etch rates during wet and dry etching [121]. For bulk silicon micromachining, anisotropic wet etching is commonly achieved by using alkaline solutions, such as KOH and TMAH. For patterning, thin films of materials like silicon nitride or silicon dioxide are mainly used since they offer high etch selectivity to Si and can be deposited with production-ripe equipment for processes such as LPCVD or PECVD. For SiO_2, it is also possible to thermally grow a layer on the Si, which has the advantage of forming a better-quality material that is highly conformal and forms an excellent etch barrier. However, this requires temperatures above about 900°C. For processing at 700°C, LPCVD is applicable and also has good conformality, in contrast to PECVD that can be applied below 400°C. In general, the lower the processing temperature of these materials the lower the etch selectivity and a thicker layer is needed. Much research has been dedicated to improving the quality of low temperature oxides and nitrides but still for wet etching of deep cavities the etch rates and/or the presence of pinholes can mean that micrometer-thick layers must be used [38, 39]. This can in turn entail problems with mechanical stress, particularly if thin membranes are to be fabricated. Sputtered metals

can also offer a low temperature solution to masking. Etch selectivity is in several cases extremely high, e.g., Ta, Ti, Au, Cr, and Ag, but hard mask etching/removal, poor adhesion, stress and process compatibility often become issues [40].

4.2 Wet Chemical Etch Mechanism for Silicon in TMAH or KOH

The etch rate of anisotropic wet etching of silicon in TMAH or KOH depends on the crystal orientation. For example, the etch-rate ratio between the <100>, <110> and <111> direction is reported to be 20:35:1 [117] for TMAH. KOH, on the other hand, has stronger anisotropy, meaning the etch-rate ratio is larger. However, because KOH solutions contain potassium ions, it is not CMOS compatible. On (100) wafers patterned with a masking layer, the huge difference in etch-rate will lead to the etching of inverted pyramids with 54.74° side walls. The reaction sequence starts with hydroxyl ions releasing four electrons at the silicon surface that subsequently react to reduce the water: [122]

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-, \tag{4.1}$$

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2. \tag{4.2}$$

The intermediate reactant $SiOH_2^{2+}$ can then react with OH^- to form a soluble silicon complex and water

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O. \tag{4.3}$$

The overall reaction is

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2. \tag{4.4}$$

For these reactions it is clear that the generation of electrons is essential for achieving an etching of the silicon. In p^+-Si regions, the etch rate is slow down due to the high hole concentration that promotes recombination of the electrons and limits the generation of hydroxyl ions [124]. Therefore, it could be expected that the doped bulk Si under the 700℃ B-layers and the induced hole layer found at the interface of both 400℃ and 700℃ B-depositions could retard the etching of the Si, which will be discussed in Section 4.5.1. The exact composition and temperature of the Si etchants influences the etch rates.

4.3 Experimental Procedures

4.3.1 Sample overview

The basic TMAH/KOH etch experiments were performed on n-type Si (100) wafers with a resistivity of 1-10 Ωcm. The B-layers in this chapter were deposited from B_2H_6 in the Epsilon at either 400°C, 500°C and 700°C with varying deposition times. After cleaning, the samples were immediately put in the load-lock of the reactor where they were continuously purged by oxygen-free N_2 gas. On some of the wafers, as an extra measure to assure a contamination-free surface, a 4 min in-situ H-bake at 800°C was performed before the deposition.

In Table 4.1, a list of the different types of patterned samples is given. Wafers with B-layer thickness from 1 nm to 6 nm were prepared with a deposition temperature of 400°C. The wafer B[400,4A] was treated with Al-metallization and removal as described in [23, 35], where the pure Al was sputtered and selectively removed in HF 0.55%. At a deposition temperature of 500°C, 2 types of wafers were examined: B[500,2.4H] with H-bake and 2.4 nm layer thickness and B[500,5A] without H-bake before deposition of 5 nm B-layer followed by Al-metallization and removal. For all depositions at 700°C a H-bake was performed before the deposition

TABLE 4.1 NOMENCLATURE OF PATTERNED SAMPLES WITH PROCESSING CONDITIONS

Sample name	B deposition		Extra treatment	
	Temp. (°C)	Thickness (nm)	H_2 prebake	Al sputtering and removal
B[400,1]	400	1	no	no
B[400,2]	400	2	no	no
B[400,3]	400	3	no	no
B[400,4]	400	4	no	no
B[400,5]	400	5	no	no
B[400,6]	400	6	no	no
B[400,4A]	400	4	no	yes
B[500,2.4H]	500	2.4	yes	no
B[500,5A]	500	5	no	yes
B[700,2.4HA]	700	2.4	yes	yes
B[700,5.5H]	700	5.5	yes	no

4.3.2 Analysis techniques

The B layer thickness was measured by ellipsometry as described in Section 2.5.1. The etch experiment were performed on both patterned and non-patterned wafers. The patterned wafers were fabricated with the ring structures described in Chapter 3, the layout of which is illustrated in Fig. 4.1.

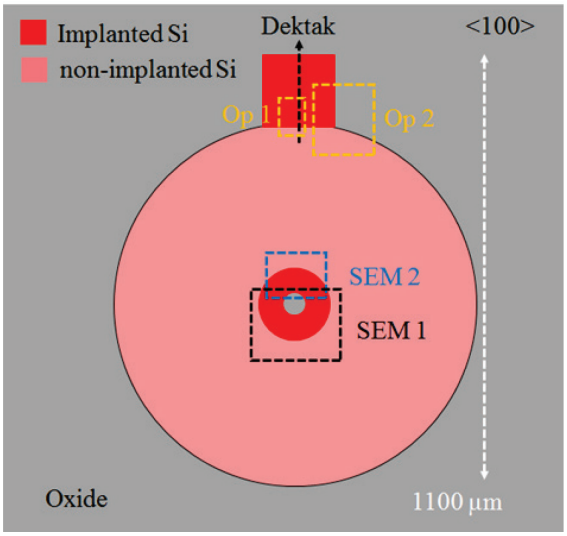

Figure 4.1. Schematic layout of the fabricated ring structures; regions used for material analysis are indicated with dashed lines.

4.4. Silicon Cavity Etching on Patterned Wafers

4.4.1. Dependence on B-deposition temperature

Several samples with 700°C B-layers of a thickness from 2.4 nm up to about 5.5 nm were immersed in TMAH or KOH. Hour-long exposures were tested but the optical inspection of the surfaces after this wet processing revealed no change of the topography. Ellipsometry measurements revealed that the etch rate of boron was less than 0.1 nm per hour. The selectivity with respect to Si is therefore extremely high, much greater than 10^4. In Fig. 4.2, an optical microscope image of the sample with the thinnest layer, B[700,2.4HA] that also was exposed to Al sputtering and removal, is shown. Despite this post-deposition processing, both the non-implanted and implanted regions remained intact. Also, for the 500°C samples B[500,2.4H] and B[500,5A], the non-implanted Si regions were undamaged by the exposure to the wet Si-

etchant, but on the implanted p^+-regions cavities appeared. This also applies to 400°C B-depositions, in which the B[400,2] is shown in Fig. 4.2 as an example.

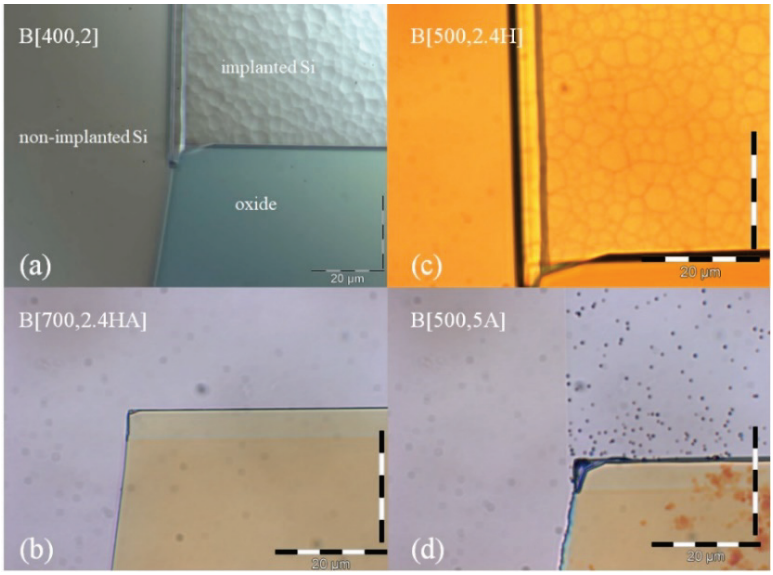

Figure 4.2. Optical microscope image of sample B[400,2] (a), B[700,2.4HA] (b), B[500,2.4H] (c), and B[500,5A] (d), showing the p^+- implanted and non-implanted regions indicated (rotated 90°) by Op 2 in Fig. 4.1, after exposure to Si etchants.

4.4.2 Dependence on thickness for 400°C B-deposition

The 400°C boron depositions are of particular interest because the low processing temperature makes deposition on fully-metallized wafers possible. This does, however, mean that a high temperature H-bake step would not be possible before the deposition. At 400°C H-baking is not effective. Therefore, a series of 400°C samples was fabricated without the bake, and the etch behavior for a B-layer thickness increasing from 1 nm to 6 nm was studied in detail. In Fig. 4.3, images are shown of samples after etching for 6 min in TMAH (left) or KOH (right), respectively. Just like for the 500°C and 700°C samples, the non-implanted n-Si region appeared to be unaffected by the etchants. However, like the 500°C samples, a cavity was etched where the p^+-implantation had been performed.

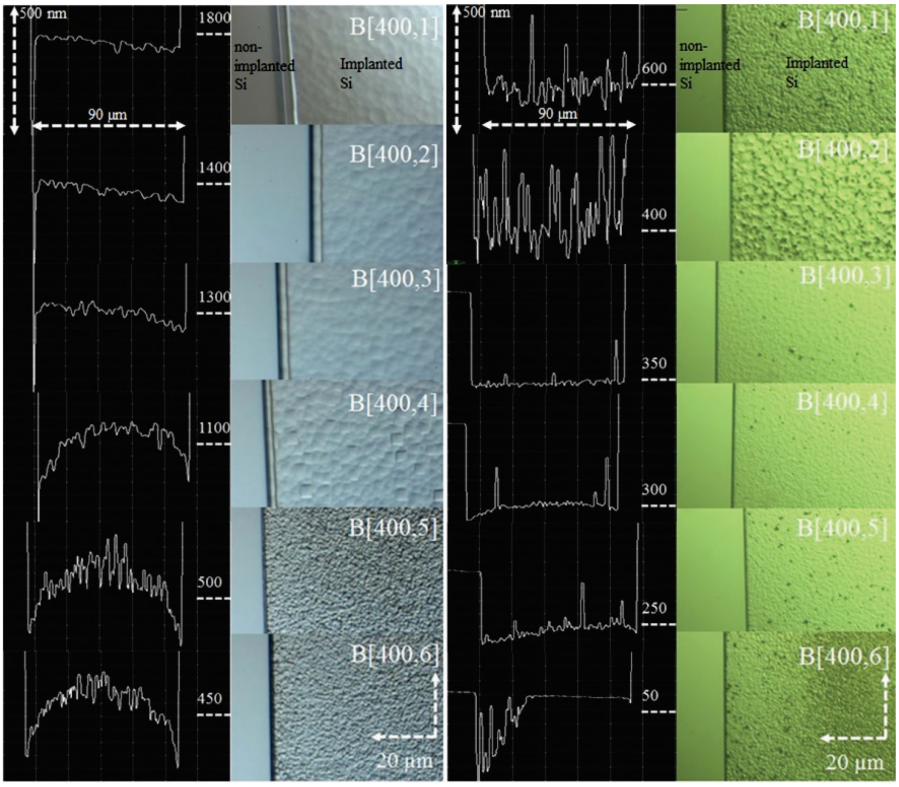

Figure 4.3. DEKTAK surface profiles beside optical microscope images of regions indicated as Op1 in Fig. 4.1, for 400ºC samples after 6 min etching in TMAH (left) and KOH (right). The numbers on the right side in the surface profile plots indicate the distance to the non-etched B-layer surface.

In Table II the depth of the cavities is listed. For the etchant conditions chosen here, the Si etch rate of the KOH is much lower than that of the TMAH. Therefore, the KOH samples give a picture of the begin situation where the etch behavior is more erratic than when much larger etch depths are reached, such as for the TMAH samples. For these, the thicker the B-layer the shallower the cavity and the higher the roughness. For the thickest layers, 5 nm and 6 nm thick, only 400 nm to 450 nm was etched with a high roughness of 80 nm as compared to 1800-nm etch-depth and 15-nm roughness for the 1-nm-thick B-layer. This suggests that the etchant is finding weak spots in the B-layer that are more numerous for the thin layers. As opposed to this, on a clean silicon (100) surface the etching would proceed more uniformly.

TABLE 4.2 ETCH DEPTH AND ROUGHNESS OF P^+- SI REGIONS AFTER 6 MIN ETCHING IN TMAH OR KOH

Sample	TMAH		KOH	
	Depth (nm)	Roughness (nm)	Depth (nm)	Roughness (nm)
B[400,1]	1800	15	600	80
B[400,2]	1400	20	400	80
B[400,3]	1300	30	350	15
B[400,4]	1100	60	300	15
B[400,5]	500	80	250	20
B[400,6]	450	80	50	10

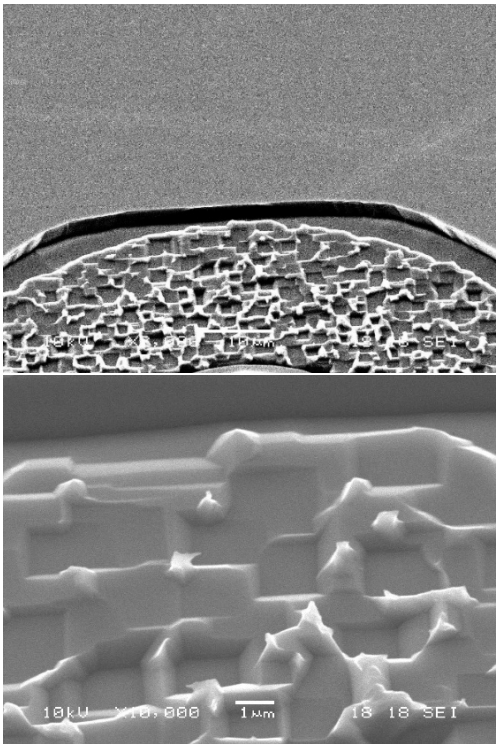

Figure 4.4. SEM images of the sample B[400,4A] at the position indicated as SEM 2 in Fig. 4.2, after etching for 6 min in TMAH.

The topography of the etched p^+-surface of sample B[400,4A] is shown in the SEM image of Fig. 4.4. The etchant has penetrated the B-layer at some

points forming cavities that eventually connect to each other. The process of lateral etching along the (111) Si surfaces is significantly enhanced by the presence of defects [121], in this case caused by residual implantation damage. Remnants of the B-layer are still visible on some of the peaks of Si but upon deeper etching the narrow peaks were etched away and the boron-layer was "lifted off". The etched surface then became less rough. This process is illustrated in Fig. 4.5.

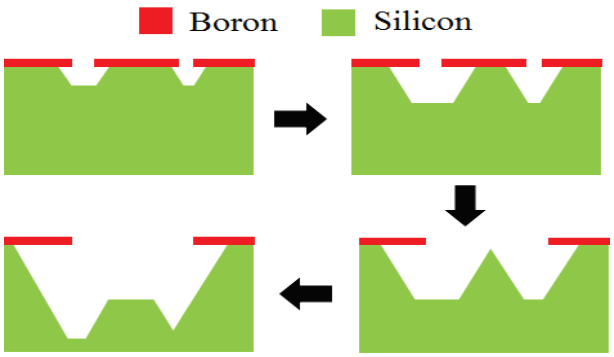

Figure 4.5. Schematic of p^+-region etched through weak spots in the B-layer.

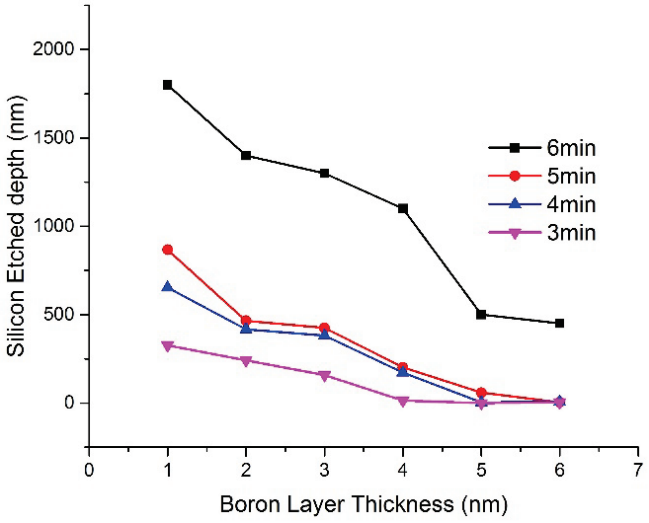

Figure 4.6. Depth of cavity etched with TMAH in implanted p^+-Si as a function of the B-layer thickness and the etching time for samples with 400°C deposition.

In Fig. 4.6, the TMAH etch depths on p^+-regions are plotted as a function of the 400°C B-layer thickness for different etch times. Not only was the etch depth significantly reduced for the thicker layers, but also for etch times of less than 6 min, the effect of the etching was hardly visible. This suggests that the weak spots that exist on the implanted regions are overgrown and protected from the etchant as the boron deposition time is increased. A few hour-long immersions in the etchants confirmed this. These results show that while a complete, etch-resistant B-coverage of the Si was readily achieved on the non-implanted Si, the implanted regions somehow prevented this for the low temperature depositions.

The influence of the H-bake step always performed for the 700°C samples, was tested but did not improve the etch resistance of the 400°C p^+-Si regions. Another suspect is the native oxide growth which is known to be more aggressive on highly-doped regions and will therefore be thicker on the implanted regions. However, the dip-etch step was developed to remove oxide also on such regions. Hence the most probable reason for the deficient B-coverage is the fact that the implantation is performed through a thick oxide. Co-implantation of oxygen atoms may lead to defect structures on the surface that prevent boron atoms from bonding to the Si. At 700°C any such point defects will rapidly be overgrown due to the high mobility of the boron atoms along the surface. At the lower temperatures the lower mobility and the preference of the boron to deposit on boron rather than Si, will slow down the process of overgrowth. The 700°C samples also have the advantage of a significant p-doping of a few nm of the Si but there was no clear evidence that this doped layer was influencing the final results.

The depth profiles and SEM images also revealed that at the perimeter of the implanted region the etch depth was much higher than in the central region. This can be correlated to the fact that the 950°C anneal of the implanted regions will leave end-of-range residual implantation damage that at the perimeter will extend up to the Si surface. Such defected regions are more vulnerable to etching.

4.4.3. Non-implanted regions with 1-nm-thick B-layers

Of a number of B[400,1] samples etched for 6 min or longer, only one was observed to have pin-holes in the non-implanted region when using optical microscopy. However, SEM imaging, as shown in Fig. 4.7, revealed that this 1-nm-thick B-layer was probably too thin to completely protect the

non-implanted Si from being etched. The SEM images show that after 6 min etching in TMAH, pin-holes appear on the non-implanted Si surface. From the AFM analysis also shown in Fig. 4.7, it is clear that these are inverted pyramids with areas of up to a few hundred nanometer. The density of these small pyramids was too low to lead to a connected fully-etched surface area. Therefore, it appears that even at 400°C the coverage with boron is almost complete after deposition of the first few atom layers. The large spread in size and shape of the pin-holes suggests that the weak spots in the B-coverage that allow the etchant to reach the Si, also have structural differences. They are, however, not visible in the optical or SEM images.

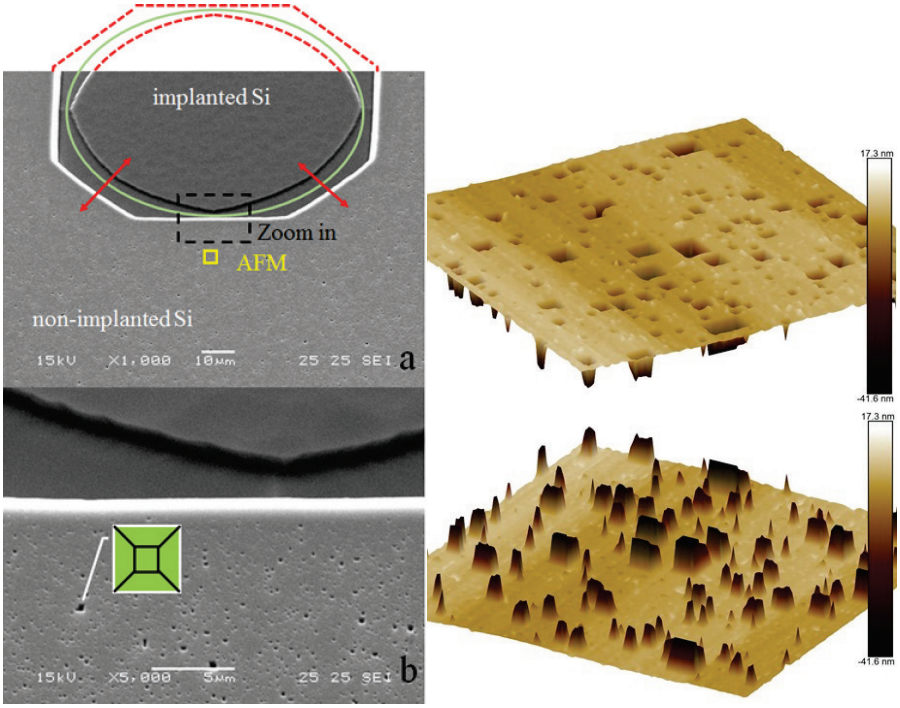

Figure 4.7. SEM images (left) of the implanted and non-implanted region indicated by region, (a) SEM1 in Fig. 4.2 in a structure without the central oxide island, (b) the zoom in labeled by dash line. The sample is B[400,1] with a 1-nm-thick B-layer after 6-min etching in TMAH. The AFM (right) is of the region designated by the yellow line with area 3 µm × 3 µm.

In the SEM image of Fig. 4.7, the sample was tilted at 45 degrees. Apart from the small cavities in the non-implanted Si region, a wide ditch around the otherwise circular p^+-Si region can be seen. This is the result of the high

etch-rate at the defected perimeter of these regions. The different etch-rates in the <100>, <110>, and <111> directions gave the outer etch boundary an octagonal shape while the inner boundary acquires a rounded square shape. Both are intermediate shapes that eventually converge and the square of an inverted pyramid that is typical of Si etching [121].

The presence of pits in the non-implanted region of sample B[400,1] corresponds well with the results of the electrical measurements [23] that showed a decrease in the conductance along the B-to-Si interface in this case. For the thicker 400°C layers that all had no pits, the conductance was at the value found to be optimal at this deposition temperature. For the sample B[400,4A] that was exposed to Al-sputtering and removal, the conductance measurement did differ from the optimal value by being almost halved. For the B[500,5A] sample a slight decrease was also monitored. An overview of all the measured sheet resistance values is given in Fig. 4.8 that is reproduced from [23]. Despite this measured increase in sheet resistance, the non-implanted regions of these samples did not show any signs of becoming more susceptible to the etchants, i.e., the degradation of the electrical interface properties does not directly correspond to the creation of weak spots for etching.

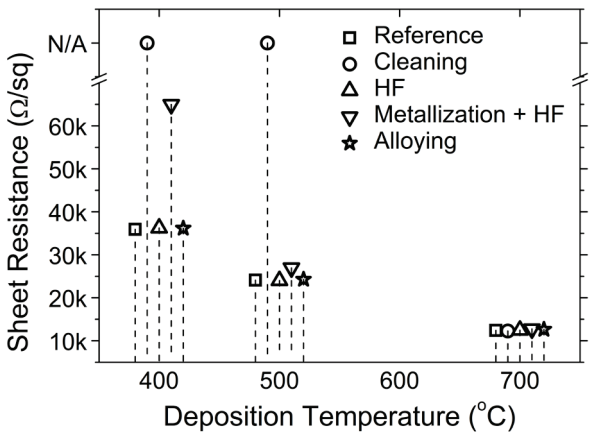

Figure 4.8. Measured sheet resistance of a 20-min B-deposition at 400°C, 500°C and 700°C with different post processing steps: the cleaning is performed in a standard metal clean with HNO_3 99%; the HF is a 0.55% HF dip-etch step; the metallization + HF is the same as B[400,4A] and alloying is at 400ºC in forming gas [23].

The results summarized in Fig. 4.8 also made clear that the standard metal cleaning step in HNO_3 99% will completely remove the B-Si interface conductivity for 400°C and 500°C B-layers while the 700°C layer remains intact. This can be correlated to the high surface roughness and probably low compactness of the lower temperature layers, which allows the oxidation of Si surface by fuming HNO_3. This diminished chemical resistance may make integration of the low-temperature layers more difficult than is the case for the 700°C layers. However, as Saitoh et al. claimed [125], the reason that various acid solutions (including hot HNO_3) have almost no effect on the sheet resistance of 700°C boron on silicon, is because that the R_{sh} is determined by B doping in Si, which was not influenced by those acid etchants.

4.5 Patterning with B-Layers

4.5.1 Si etching after B removal

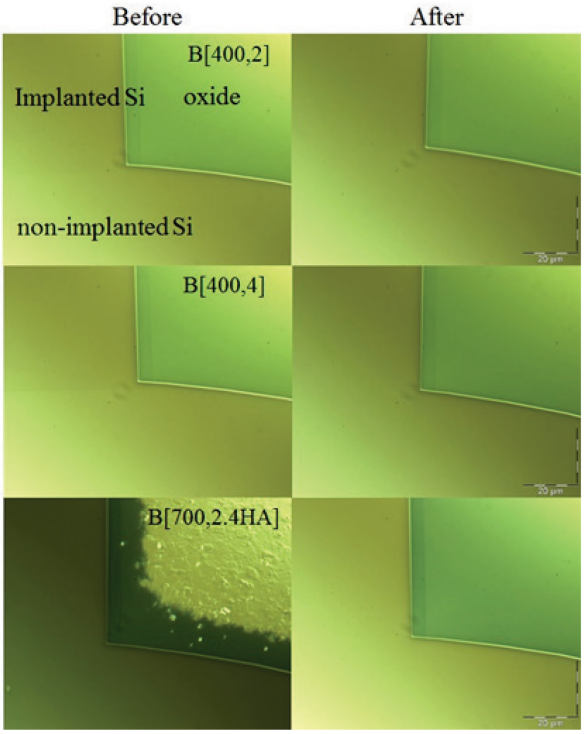

Figure 4.9. Optical microscope images taken at position Op1 in Fig. 4.2, before and after 10-min exposure of samples to Al-etchant at 45°C.

Aluminum metal etchant was found to be efficient for patterning of the B layers. For the experiments, a standard Al etchant with 80% phosphorus acid, 16% acetic acid and 4% nitric acid was applied [124]. Samples of B[400,2], B[400,4] and B[700,2.4HA] were etched at 45°C for 10 min. As shown in Fig. 4.9, there was no visible difference before and after etching except on the oxide surface of the B[700,2.4HA] sample. The coarseness seen before etching is due to the post-deposition processing with Al-deposition and removal in HF. Presumably the Al is less readily removed from the oxide than the B due to, for example, reactions with the Si component of the oxide. This visible Al-residue is also removed by the Al-etchant.

Subsequently, these samples were etched in TMAH for 6 min which resulted in successful etching of the silicon as seen in Fig. 4.10. Since the etching rate of thermal oxide in TMAH and KOH is only a few nanometers per hour, which is negligible compared with that of silicon, the oxide level was taken as a reference for determining the etch depth in the silicon. The etch depths are given in Table 4.3. The etch rate on the p^+-implanted region is slower due to the fact that the very low concentration of electrons in the p^+-region slows down the reaction [124]. Otherwise, the etch depths are comparable with values of 2250 ± 100 nm for the non-implanted Si region and 1400 ± 100 nm for the implanted region. The 700°C sample does, however, appear to have an etch depth that is lower by a small amount of about 100 - 200 nm. This could be connected to the bulk B doping from the B-deposition that at this temperature can be up to 2×10^{19} cm^{-3}. This is enough to significantly retard the TMAH reaction [124] but since this extra doping is only a few nm deep it does not in itself form an efficient etch-stop.

TABLE 4.3 ETCH DEPTH OF SI AFTER BORON REMOVAL AND 6-MIN ETCHING IN TMAH

Sample	Non-implanted Si (nm)	Implanted p^+- Si
B400[2]	2317	1417
B400[4]	2367	1525
B700[2.4HA]	2125	1302

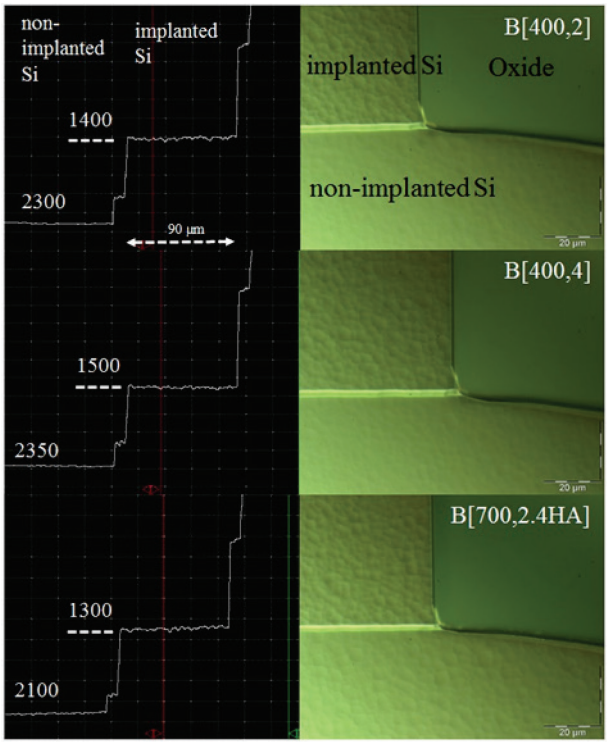

Figure 4.10. DEKTAK surface profiles (left) and optical microscope images taken at position OP1 in Figure 4.2 (right), for samples after etching in Al-etchant for 10 min and TMAH for 6 min. The numbers on the left side in the surface profile plots indicate the distance to the non-etched B-layer surface.

4.5.2. Localized B-layer removal

Localized B-layer removal was performed with standard positive photoresist lithography and samples with a blanket B-layer deposited at either 400°C or 700°C. The photoresist adhesion was enhanced by spin-coating of HDMS and after applying a 1 min bake step at 120°C. The patterning was non-critical, performed manually, with about 10 µm minimum feature size which left very rounded corner in the square structures and some uncertainty in the exact size of the resist windows. Samples were immersed in Al etchant at 45°C for 20 min and the remaining photoresist was removed by acetone. There was no pattern visible on the wafer before and after the B-layer patterning due to the very limited absorption in the nm-thin B-layer. Nevertheless, a visual confirmation that windows had been etched could be

seen as a patterned reflection in layers of residual water on the wafer during the drying process as shown in Fig. 4.11.

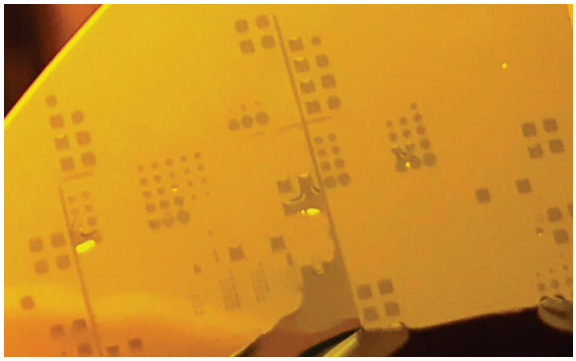

Figure 4.11. Patterns seen in a thin layer of water on a wafer where windows were etched in the 400°C B-layer; after resist removal, cleaning, and photographed during drying.

TABLE 4.4 AVERAGE OF MEASURED ETCH DISTANCES AND CORRESPONDING ETCH RATES OF SI IN LATERAL <110> AND VERTICAL <100> DIRECTION

Etchant	TMAH		KOH	
Boron deposition temperature	400°C	700°C	400°C	700°C
<110> undercut (μm)	1.76	2.46	1.21	0.81
<111> etch rate (μm/min)	0.012	0.017	0.008	0.006
<100> etch depth (μm)	53.9	70.4	56.7	58.6
<100> etch rate (μm/min)	0.45	0.59	0.47	0.49
<100>/<111> etch-rate ratio	37.5	34.7	58.8	86

Deep cavity etching was performed on wafers with B depositions from 2 nm to 6 nm thick. All these layers proved resistant to both TMAH and KOH etchants. To enable the determination of the etch rate in <100> direction, patterned samples were first etched in either the TMAH or KOH for 10 min. The size of the resulting squares etched in the Si could then serve as an initial value for determining the undercut after deep cavity etching. The lateral undercut, δ, along the <110> directions was measured by optical microscopy and the vertical etch depths, d, in <100> direction with the Dektak. The samples were then etched for another 2 hours and remeasured. Optical microscope images of the resulting cavities for one of the samples are shown in Fig. 4.12 and measured etch distances are listed in Table 4.4 along with the

calculated etch rates in <100> and <111> directions. Inspection of several cavities on each sample was performed to ensure that there were no irregularities due to poor B adhesion or Si substrate quality that could give defect-enhanced etching. Such irregularities were not found but due to the small undercut, measurements on 3 different square windows on the same wafer were averaged to reduce measurement uncertainty.

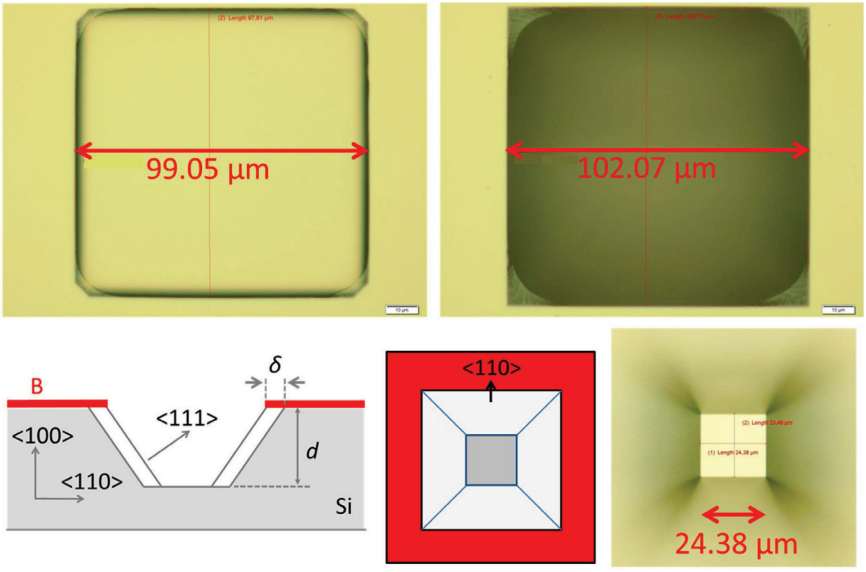

Figure 4.12. Schematic showing the undercut δ in <110> direction and cavity depth d in vertical <100> direction along with optical microscope images of square windows after TMAH etching: after 10 min (left) and 2 h 10 min (right). The images above are taken with focus on the Si surface and the one below with focus on the bottom of the cavity. The B-layer was deposited at 700°C to a thickness of 5 nm and the on-mask size of the square window was 90 × 90 µm^2.

For TMAH etching the <100>/ <111> etch-rate ratio is about 35 for both the 400°C and 700°C B-layers while the values are higher and clearly different for KOH etching. The 700°C layer ratio is 86 while for 400°C it is only 59. Whether this difference can be accorded to differences in the interface formation and related adhesion of the B to the Si cannot be concluded from the present experimental material and requires further investigation. Ellipsometry measurements of the B layers before and after the 2 h 10 min etch-cycle revealed that the etch rate of boron was less than 0.1

nm per hour. Moreover, inspection of the surface morphology with optical microscopy, NICM and SEM imaging, confirmed that there was no visible change in the appearance of the surface. The selectivity with respect to Si is therefore extremely high, much greater than 10^4. Since the integrity of the B-layer is very important for such thin layers, extra experiments were performed to test the reliability of the wafer cleaning before deposition. For the samples that received an 800°C H-bake step in the CVD reactor just before deposition it can be expected that all native oxide is removed. The 400°C boron deposition is of particular interest because the low processing temperature makes deposition on fully-metallized wafers possible but a high temperature pre-bake is then not possible. Both 400°C and 700°C were tested with and without H-baking and no differences in the resistance to the etchants were detected. This confirms that the HF-dip plus Marangoni cleaning is an efficient procedure for native oxide and particle removal for this application.

4.6 Overhanging B-Membranes

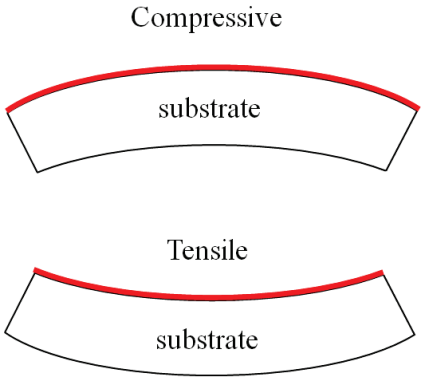

Figure 4.13. Wafer bow due to film deposition. The curvature depends on whether the film stress is tensile (positive) or compressive (negative).

The stability of membranes fabricated with etch-resistant layers like the B-layers will be very dependent on the stress in the layer. In general, the nature of the film stress can be verified by comparing the substrate bowing with and without the film. A compressive film tends to expand upon release while a tensile film tends to contract upon release (Fig. 4.13). Values for the stress were found here by applying the Stoney equation to the curvature measurement by Dektak:

$$\sigma = \frac{4}{3} \times \frac{E_s}{1\text{-}\nu_s} \times \frac{t_s^2}{t_f} \times \frac{\partial_c}{d_{sc}^2} \tag{4.5}$$

where σ is the residual stress, E_s is Young's modulus for silicon, ν_s is Poisson's ratio for silicon, t_f is the film thickness, t_s the substrate thickness, d_{sc} the scan length and ∂_c the curvature difference of the substrate as measured with and without the B layer.

TABLE 4.5 PARAMETERS USED FOR STRESS CALCULATION AND THE RESULTING VALUES

B deposition	400°C Picosun	700°C Epsilon
Substrate orientation	<110>	<100>
E_s (Gpa)	169	130
ν_s	0.064	0.28
t_f (nm)	30	5.5
t_s (μm)	380	675
d_{sc} (μm)	80000	80000
∂_c (nm)	2700	-400
σ (MPa)	490	-1250

The applied parameters [126, 127] and the resulting stress values are listed in Table 4.5 for two films deposited at 400°C in the Picosun and 700°C in the Epsilon, respectively. The stress is comparable to what is found for other commonly-used masking layers and it changes from 490 MPa tensile for the 400°C to 1250 MPa compressive for the 700°C deposition. This suggests that the stress could be tuned by changing the deposition conditions.

In the corners of the square cavities shown in Figure 4.12, the resist was rounded and the undercut in the <100> direction leaves membranes of boron overhanging the corners. This undercutting process that leads to inverted pyramids being etched from irregular windows in the masking layer, is more clearly seen for circular windows such as the ones used to form cavities in the SEM images of Fig. 4.14. These B-layers were 6-nm- and 13.5-nm-thick and deposited in the Picosun at 400°C and the Epsilon at 700°C, respectively. With a SEM electron beam-energy of 8 kV, the nm-thin membranes are transparent, absorbing only a small fraction of the electron beam and they appear to be quite uniformly suspended. In the optical microscope images of Figure 4.14, the actual membrane morphology is more clearly seen. For thinner layers than the ones shown in Fig. 4.14, the membranes would often

be broken but they all displayed a very clear wrinkling pattern. For the 700°C Epsilon deposition the membranes are buckled with folds pointing towards the center of the square window (Fig. 4.14 bottom right), suggesting that they were stretched over a compressed wafer before release. In contrast the 400°C Picosun membranes appear to be stretched tightly (Fig 4.14 bottom left) over the corners showing folds perpendicular to the diagonals of the square window. This is in accordance with the stress measurements that showed compressive stress for the 700°C Epsilon and tensile stress for the 400°C Picosun deposition. The influence of B-layer stress with respect to deposition conditions will be discussed further in Chapter 6.

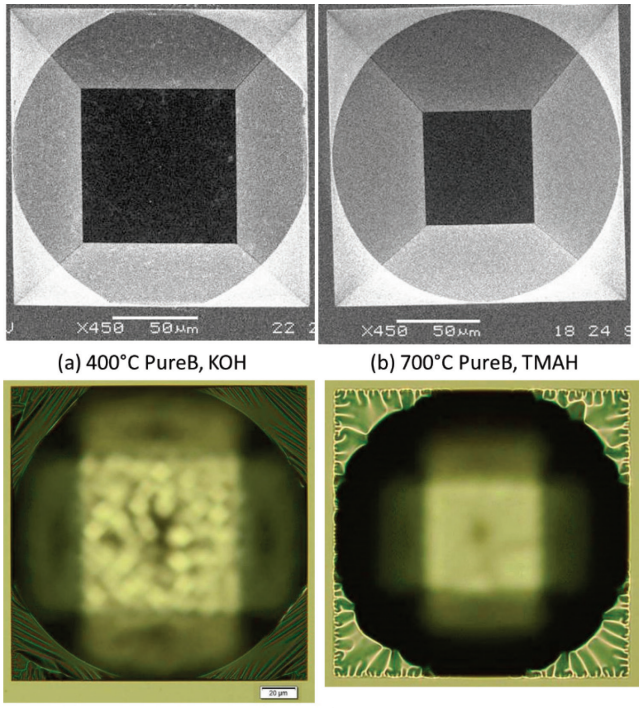

Figure 4.14. Top-view images of cavities etched for 2 h 10 min in circular windows with an on-mask diameter of 180 µm; (a) 400°C Picosun B-deposition with thickness 6 nm and roughness 1.5 nm, etched in KOH, and (b) 700°C Epsilon B-deposition with thickness 13.5 nm, etched in TMAH. Top: SEM images. Bottom: optical microscope images with focus on the overhanging membranes.

4.7 Conclusions

The suitability of nm-thin B-layers as masking layer for TMAH and KOH etching of Si was demonstrated for patterning of the layers with photoresist and Al etchant. The TMAH/KOH etch test also gave an easy way of evaluating the B-layer compactness and robustness. For boron deposition temperatures from 400ºC-700ºC, all layers that were 2-nm to 6-nm thick showed high resistance to etching when deposited on non-implanted Si surfaces. The selectivity was extremely high, much greater than 10^4. Pitting of the Si was only observed for a 400ºC sample with a very thin 1-nm-thick B layer. The 700ºC layers offer the best surface coverage and displayed good etch resistance also on implanted p^+-Si regions. In contrast, all the 400ºC and 500ºC layers displayed good etch resistance on non-implanted regions but cavities were etched on p^+-implanted Si surfaces. The overall results indicate that in these cases, weak spots were present but these could be overgrown by increasing the layer thickness by a few nm. The boron adhesion to the Si was good giving low undercut during cavity etching with <100>/<111> etch-rate ratios as high as 86 and 38 for KOH and TMAH, respectively. The stress in the layers was found to be 490 MPa tensile for 400°C Picosun and 1250 MPa compressive for the 700°C Epsilon depositions.

Just like diffused or epitaxially-grown p^+-regions that are conventionally used as etch-stop for cavity etching into the back of a wafer, the B-layer is fully CMOS compatible with front-end CMOS. In addition, it is back-end CMOS compatible when 400°C deposition is used. The B-layers can also be simultaneously incorporated in a device structure as a masking layer for Si micromachining and as a region with an induced hole-carrier layer junction that can act as a p^+-region for electrical purposes. Particularly the 400°C B-layer is of interest in this respect since it can be integrated as a post-metallization step.

Chapter 5 Low Temperature Boron Depositions

In this chapter, several B-layers, deposited particularly in the temperature range from 50°C to 450°C, will be evaluated with respect to their material and electrical properties. They are of particular interest for applications where PureB diode modules should be back-end CMOS compatible. In the first section the Si surface preparation before B-deposition will be examined more extensively than was done in Section 2.4.2, and be put in the context of how it affects the PureB diode characteristics. All deposition methods described in Section 2.4.1 are investigated and compared in order to establish which conditions are important for achieving ideal PureB diodes with minimum electron injection and sheet resistance of the p-type layer. In many cases, the electrical results were supplemented with the results of physical analysis techniques used to assess the compactness of the layers and the presence of possible contamination. However, as described in Section 4.4.3, the electrical properties of the interface and the physical B-layer compactness/robustness do not directly correspond. Thus, the integrity of the layer has been tested both with electrical analysis and etch methods. Both methods are effective indicators of the quality of the B-layer, especially when the thickness is only around 2 nm. A minimum deposition temperature was also sought for each deposition method, partly to increase the flexibility of integrating B-layers, and partly to seek a method to deposit as thin a layer as possible. The back-etching of bulk B-layers was also tested with the goal of achieving close to a monolayer B-thickness without destroying the B-Si bonds that are responsible for creating the negative fixed charge that attracts a substantial layer of holes to the interface.

5.1 Si Surface Preparation Before B-Deposition

As discussed in Sections 2.4.2 and 3.2, the interface conditions and associated B-coverage could be efficiently monitored by electrical characterization. Any imperfections may cause an increase in the sheet resistance, R_{sh}, along the interface and the electron injection, I_e, into the B-layers. As already discussed in Chapter 4, the capability of B-layer used as a Si anisotropic etch mask is highly dependent on the material integrity. Pin-holes or weak spots are more likely to appear when the deposition temperature or the layer thickness is low, and then the perfection of the Si surface becomes even more important. The standard Si surface cleaning procedures prior to

deposition described in Section 2.4.2 have proven to be reliable and effective. In this section, several Epsilon B samples deposited with extra pre-cleaning or post-annealing were tested to see if any of them would improve the electrical performance. All the 450°C B-depositions were performed at Lawrence Semiconductor Research Lab (LSRL) in an ASM Epsilon 2000 system. The temperature of 450°C was chosen because it is usually the maximum temperature that is considered to be CMOS back-end compatible.

TABLE 5.1 ELECTRICAL CHARACTERIZATION AND ETCH TEST WITH VARIOUS DEPOSITION CONDITIONS [124]

Sample	Pre-dep. step	Dep. temp (°C)	Post-dep. step	Thick. + rough. (nm)	R_{sh} (kΩ/sq)	I_e at 0.3 V forw. (nA)	TMAH etched Si with no p^+	TMAH etched Si with p^+
B[400]	-	400	-	4.0+2.5	37	2.2	no	yes
B[450]	-	450	-	2.9+2.0	30	1.9	no	no
B[H,450]	800°C	450	-	2.8+3.0	48	12.3	yes	yes
B[HCl,450]	HCl	450	-	2.7+3.1	42	17.1	no	yes
B[700]	-	700	-	2.2+0.4	13	<0.2	no	no
B[450,H]	-	450	850°C	3.1+0.6	0.58	<0.2	no	no

In CVD reactors, H_2 baking at temperatures above 800°C is commonly used to guarantee a contamination-free surface. At lower temperatures, gaseous HCl cleaning is also a possibility. Here it was tested at 500°C, even though little effect is expected at such a low temperature [126-129]. A list of all studied samples and their treatments is given in Table 5.1, along with the main electrical and wet-etch results. The samples B[400] and B[700] had B-layers deposited at 400°C and 700°C without any extra cleaning steps, and are used here as a reference to evaluate the 450°C B-layers B[*x*,450,*y*], where *x* and *y* represent pre- and post-deposition steps, respectively.

Sample B[H,450] received an 800°C H-bake for 4 min prior to deposition, B[HCl,450] was cleaned with HCl, and B[450,H] was exposed to H_2 annealing at 850°C for 5 min. As the deposition temperature goes from 700°C down to 400°C, both R_{sh} and I_e increase. At 700°C, the R_{sh} is dominated by B-doping of the bulk Si and I_e by a high density of the electrically active B-Si bonds, giving very low values for both parameters. Likewise, the B-layer of the sample B[450,H] improves from the 850°C post-deposition anneal, and

has unmeasurably low I_e and R_{sh} = 580 Ω/sq. For B-deposition below about 500°C, no bulk doping is expected and the electrical properties are determined by the interfacial B-Si bonding. The R_{sh} and I_e of B[400] are slightly higher than those of B[450], suggesting that less of the desired B-Si bonds were formed either because less energy is supplied for the activation and/or because the deposited B is less mobile making it more difficult to achieve a perfect B-coverage. The 450°C samples that received extra cleaning steps in the deposition chamber show a significant increase for both R_{sh} and I_e. For B[H,450], the degradation of the interface could be explained by the fact that the baking step will cause the phosphorus (P) dopant atoms in the Si substrate to segregate on the surface [117] and where a P-atom is present the B adsorption is possibly prevented. In Fig. 5.1, *I-V* characteristics are compared for B[450], B[H,450] and B[450,H].

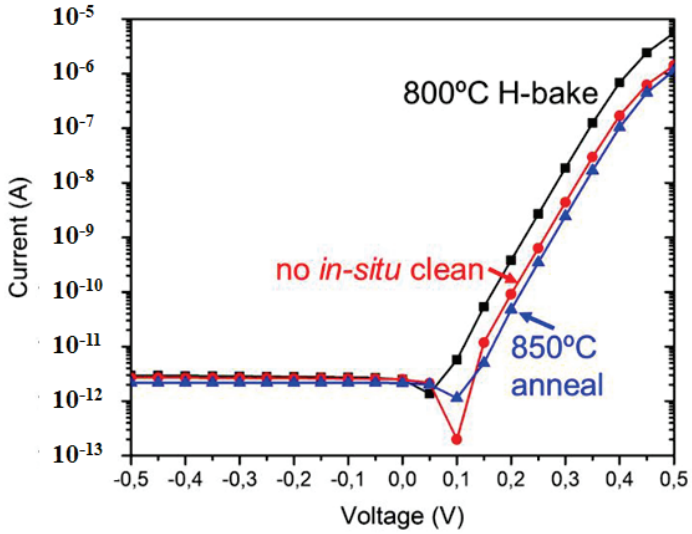

Figure 5.1. *I-V* characteristics for PureB diodes deposited at 450°C for 2 different cleaning methods compared to a diode that has had an 850°C post-deposition anneal [130].

For B[HCl,450], the HRTEM in Fig. 5.2 exhibits a slight roughening of the interface to the Si. This would possibly lead to a less perfect B-coverage and Si surface defects, which could explain the high electron current injection and high sheet resistance.

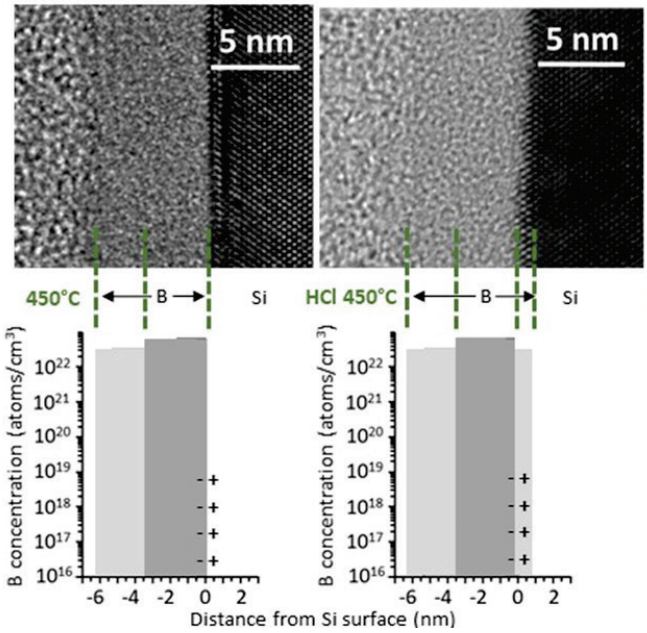

Figure 5.2. HRTEM images and schematic plots of approximated boron concentration through B-layers deposited on bare Si wafers for a 450°C deposition without any in-situ cleaning step (left) and with a HCl clean (right) [130].

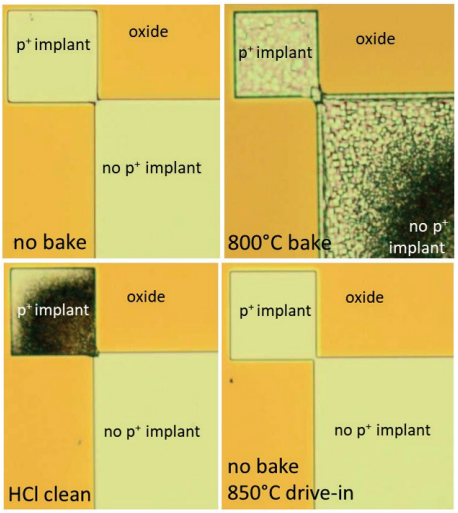

Figure 5.3. Optical images (from top left to bottom right) of B[450], B[H,450], B[HCl,450] and B[450,H], after immersion in TMAH [130].

The material integrity of the different B layers was tested on the patterned samples by immersing them in TMAH. The results for the 450°C depositions are displayed in the optical images of Fig. 5.3 and listed in Table 5.1 together with the effect on the 400°C and 700°C samples. The samples that were deposited without extra cleaning steps in the deposition chamber show optimal resistance to TMAH etching. Only the 400°C-deposition showed etching of the Si on the p^+-implanted region. This is also the case for the p^+-pad of the B[HCl,450] sample. The sample B[H,450] where P-segregation to the Si surface is expected was attacked by the TMAH on both the implanted and non-implanted regions. Therefore, from this etch test, it can also be concluded that the perfection of the B-coverage is degraded due to the extra cleaning steps. It is more likely that the TMAH etching of the Si is occurring through weak-spots in the bonding structure of the B atoms that occurs more frequently when the initial deposited layer is incomplete and the temperature is so low that the B-atom mobility is low along the Si and B surfaces.

Despite of the cleaning procedures that remove the oxide prior to deposition, oxygen could also be incorporated under non-optimal conditions during deposition. This was evaluated by XPS analysis. An example is shown in Fig. 5.4 (bottom) where the atomic composition of B[450] and B[HCl,450] is compared with a 450°C layer kept in load-lock for extra N_2 purging. The red line represents the sample that was deposited shortly after being transferred from the load-lock. The corresponding bonding energy spectrum is also shown in Fig. 5.4 (top). The green line represents the sample that received an extra HCl cleaning step in the chamber before the deposition. The blue line is for the sample that was kept in the load-lock and N_2 purged for about 5 hours.

The one with extensive N_2 purging in load-lock displays negligible oxygen content while the others have about 4% - 5% through the whole layer. The consistent oxygen level indicates that this O-contamination is captured homogeneously during the deposition, because the oxygen and moisture caught in the open air will only give a high O-signal at the surface. As a result, a significant incorporation of oxygen was only observed when the wafers were not kept in the load-lock long enough, which indicates that the killer oxygen source was from the moisture transported onto the deposition chamber with the wafer.

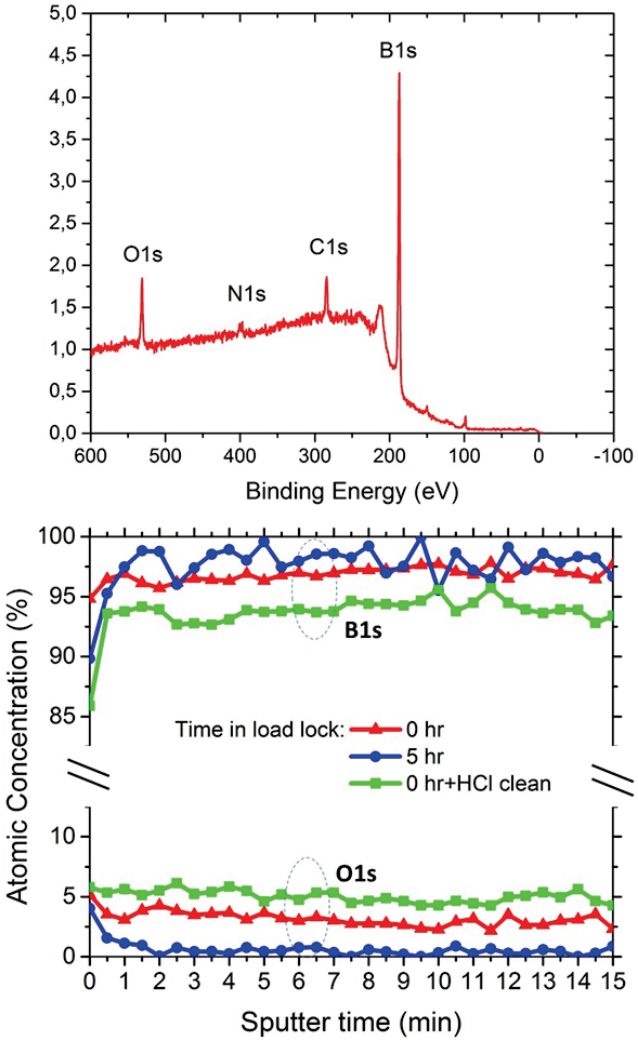

Figure 5.4. XPS analysis of 450°C B-deposition in the ASM Epsilon 2000 on bare Si wafers. Top: XPS survey spectrum of a sample without any in-situ cleaning step that went straight form the load-lock to the deposition chamber. Bottom: boron and oxygen concentrations extracted for samples with and without a HCl clean for different times in the load-lock [130].

5.2 Picosun B-Layers

The CVD boron discussed in Chapter 3 and 4 were all deposited in an ASM Epsilon 2000 system, which was originally designed for Si-epitaxy. The Epsilon is an excellent system for deposition in a board temperature range from 400℃ to 1200℃ and for good control of contamination with oxygen. In order to explore the versatility of CVD B, the research was continued to develop low-temperature deposition of B in the ALD Picosun system in the MESA+ Nanolab, focusing on deposition below 450℃. The precursor is composed of 5% B_2H_6 in Ar gas. According to a previous study [86], at low temperatures the mobility of the B atoms along the surface is low, which reduces the probability of adsorption to a Si atom because the boron atoms preferably attach to other boron atoms. Therefore, vertical growth of boron is promoted. For high growth rates undesirable voids in the first monolayer of the film will be readily overgrown. Due to the flexibility of the ALD system, the boron deposition can be controlled in several ways. The simplest way is to change the precursor concentration by adjusting the flow rate of diborane and Ar carrier gas. The temperature also has a large impact since the deposition rate is around 2 nm per 30 min at 250 ℃, 5 nm per 30 min at 300℃ and as high as a few nanometers per minute at 400℃ when the diborane flow is 200 sccm and that of the extra Ar carrier gas 500 sccm. To achieve low growth rates at 400℃ and above, a low diborane concentration is required. With the Picosun system, it is possible to modulate the process from conventional CVD mode (constant flow) to pulsed CVD mode in which the pulses of diborane are introduced discretely during a constant flow of Ar purging gas. In the pulse CVD mode, the purging gas can be replaced by H_2, which is known to inhibit the decomposition of diborane. In this way the decomposition rate can also be reduced.

During the deposition, the pressure in the chamber is around 1 mbar. In this situation, there is a risk of contamination with oxygen, which readily reacts with the intermediate reactants during diborane decomposition and forms B_xO_y. Apart from the oxygen that could possibly be brought along with the wafer as mentioned in previous section, oxygen atoms are always present to some degree, coming from oxygen and water molecules that are part of the background pressure. The incorporation of oxygen is expected to be higher when the boron deposition rate is low. Thus, the boron deposition should be fast enough to prevent oxygen contamination but slow enough to allow a good first coverage of the B-to-Si interface. The effect of background pressure can

be overcome by introducing extra Ar carrier gas, in order to dilute the contamination molecules. Another suspected source of oxygen contamination is the moisture absorbed in the sample carrier that transports the wafer (pieces) into the Picosun. It is coated with Al_2O_3 and always stored outside the vacuum system. To improve the cleanliness of the carrier, a dedicated 100 mm Si wafer was fabricated with an etched cavity for positioning the wafer pieces.

TABLE 5.2 SHEET RESISTANCE OF AS-DEPOSITED B-LAYERS, MEASURED ON VAN DER PAUW STRUCTURES

Temp. (°C)	B_2H_6 (sccm)	Ar (sccm)	Time (min)	Thickness (nm)	*R*sh (kΩ/sq)
200	180	500	30	1	603
200+400	180	500	30+2	-	69.9
250	200	500	30	1.5	49
250+400	200	500	30+1	-	52.8
300	200	500	6	1.5	46.6
400	50	500	6	12	39.6

A great number of boron depositions were performed in the Picosun in the temperature range 250°C - 450°C. They all created diodes with characteristics that show behavior similar to that of p^+n diodes, i.e., the diode current component from electron injection into the PureB region is much lower than for comparable Schottky diodes. Examples are listed in Table 5.2. The measured sheet resistance displays the trend that higher deposition temperature enhances the boron coverage of the Si and desirable bond formation. For B deposited below 250°C, the growth of the layer appears to stagnate at around 1 nm to 1.5 nm, as determined by in-situ ellipsometry. As opposed to higher temperature deposition [130], possibly the conditions at 250°C resulted in a preference for the B to adsorb on Si sites rather than B-sites, leading to an almost self-limiting deposition [21].

SIMS analysis of these samples was carried out and the resulting B concentration is shown in Fig. 5.5. At 200°C the integral B concentration is 4.6×10^{14} atoms/cm^2 while at 250°C it is 1.5×10^{15} atoms/cm^2. The number of Si atoms on the surface is 6.78×10^{14}cm^2 so the boron coverage in both cases is in the range of one monolayer. From the very high sheet resistance of the 200°C sample, 603 kΩ/sq, it seems plausible that the B coverage was incomplete in this case, while at 250°C the much lower sheet resistance suggests a reasonably good coverage. Adding a 400°C deposition brought the

sheet resistance of the 200°C sample down to 70 kΩ/sq while the 250°C sample was not significantly changed. Fig. 5.6 displays the *I-V* characteristics of 250°C PureB diode compared to a deep implanted p^+n diode. Apart from a very small non-ideal leakage current in the PureB device, the two curves are almost identical [21].

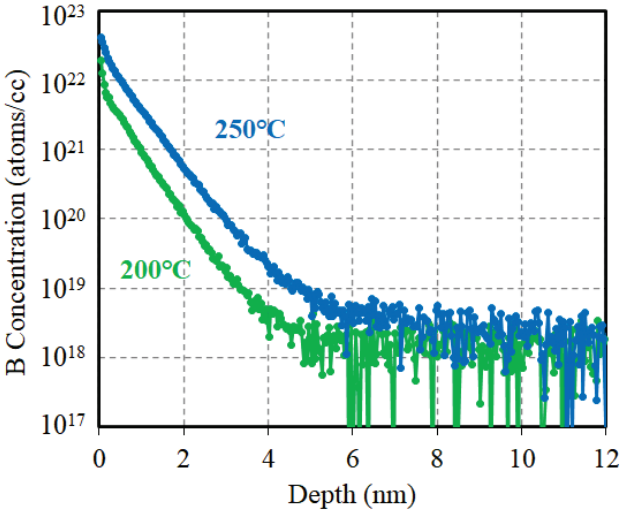

Figure 5.5. SIMS profiles for boron layers deposited at 200°C and 250°C.

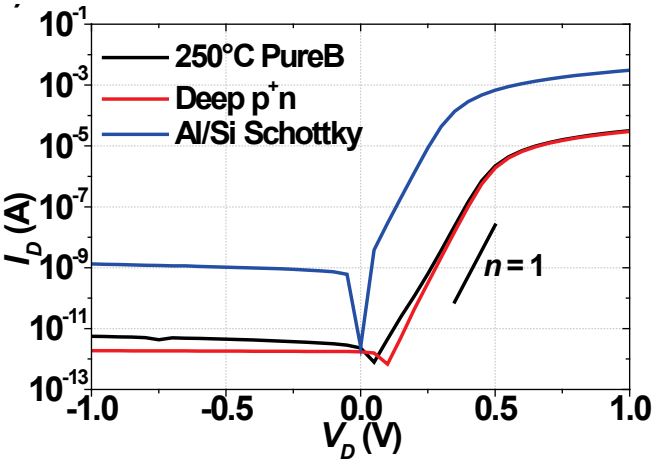

Figure 5.6. *I-V* characteristics of a PureB diode fabricated with a ~ 1 nm thick 250°C B-layer, a deep implanted p^+n diode, and an Al-to-Si Schottky diode [21].

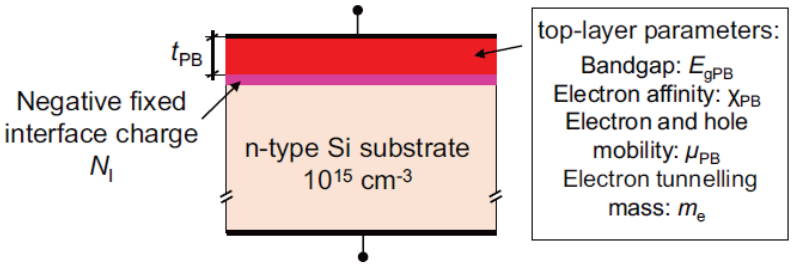

Figure 5.7. Cross section of the simulated structure with indicated material parameters of the B-layer [68].

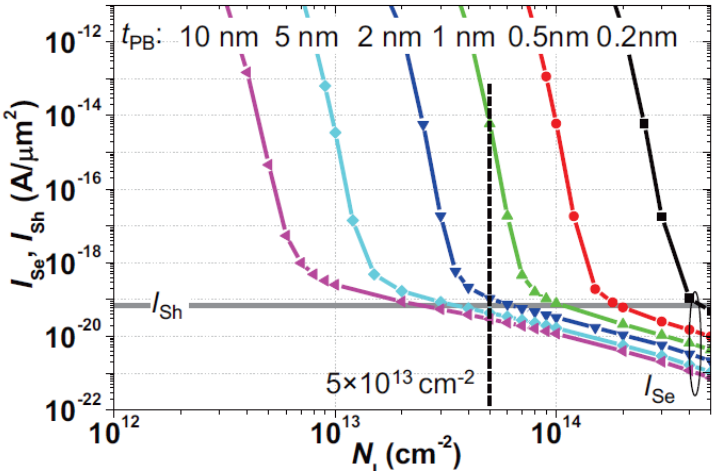

Figure 5.8. Electron and hole saturation current densities obtained from TACD simulations as a function of N_I extracted for a device with an Al/B-layer contact and t_{PB} = 0.2 nm, 0.5 nm, 1 nm, 2 nm, 5 nm and 10 nm [68].

Parallel with the experiments, an in-depth investigation on the electrical modelling of PureB diodes was performed by Tihomir Knežević [21, 68] using Sentaurus Device TCAD software. The basic structure shown in Fig. 5.7 was simulated for varying thickness of the deposited B-layer, t_{PB}. The thickness of the n-Si substrate was set to 500 µm with doping concentration of 10^{15} cm^{-3}. A fixed negative interface charge, N_I, was defined between the bulk Si and the B layer in the range of 10^{12} cm^{-2} to 5×10^{14} cm^{-2}. An Al-metal contact with a work function of 4.1 eV was defined as contact to the B-layer. The doping of the B-layer was set to 10^{18} cm^{-3}. B diffusion into Si was neglected. The relations between the saturation current density (I_{Se} for

electrons; I_{Sh} for holes) and N_I with respect with varied t_{PB} are shown in Fig. 5.8. Due to the Schottky-induced depletion of the B surface, the associated band bending would influence the hole accumulation at the B-Si interface. All the B-layers were so thin that the presence of the metal increases the I_{Se} with respect to the non-depleting case. For N_I less than 10^{13} cm^{-2}, the effective suppression of I_{Se} was lost even for t_{PB} as thick as 10 nm. For N_I around 5×10^{14} cm^{-2}, 0.2-nm B-layers were still efficient. Since the atomic size of B is around 0.2 nm, it suggested that with a near fully-activated B-Si bonding (6.78×10^{14} cm^{-2}) at the interface, a monolayer of B would be sufficient in suppressing the electron injection.

The 30 min B deposition at 250°C was by far the best in achieving monolayer-like thin layers with the desirable electrical characteristics, as discussed in connection with mentioned in Table 5.2 and Fig. 5.6. Even though the ellipsometry gave the layer thickness of 1.5 nm, it could be explained by either an inaccuracy of the ellipsometry for such low layer thickness, or a disturbing effect of other molecules that could be present on the Si surface. In this sense, the actual thickness calculated by integral doping concentration of SIMS of 1.5×10^{15} atoms/cm^2 would be more accurate, and this is about 2 monolayers. The excellent electrical characteristics of this 250°C B layer indicated that: (1) only the interfacial B-to-Si bonding and not the bulk boron layer is of importance, (2) 250°C is sufficient to form a high density of negative interfacial charge layer.

5.3 MBE Boron Deposition

The advantage of MBE could be that the amount of B that is actually deposited on the silicon, being physically limited, is independent of the Si substrate temperature. Therefore, even room-temperature deposition can be achieved. The incorporation of atoms from the gas-phase only happens at the target surface, and a precise control of the thickness of each layer is feasible. This might make it possible to achieve uniform layers with a lower thickness than is possible with CVD. With MBE the contamination level is kept small by using a high vacuum (10^{-8}- 10^{-12} mbar). As a drawback, in situations with surface topography, the MBE deposition is not conformal. Depositions were performed at room temperature, 200°C, 300°C, and 400°C, on both blanket wafer pieces and pieces patterned with sheet resistance test structures, for a thickness of about 1.5 nm. The B layer is deposited from a Knudsen effusion cell of elemental B. The base pressure in the MBE was 10^{-11} mbar. The deposition was first made on Si samples without heating the substrate which

resulted in heating of the sample to 50°C due to radiation emission from the B effusion cell.

The *I-V* characteristics of the MBE PureB diodes are shown in Fig. 5.9. They are all close to the characteristics of implanted p^+n diodes for which the current is dominated by hole injection into the substrate [102]. All characteristics displayed a small non-ideality that was similar for all devices including the implanted ones. Such leakage was not observed for the samples processed with CVD B. In the MBE case a slightly different pre-deposition processing could have caused excessive thinning of the SiO_2 and in addition, unlike with CVD, the MBE boron is non-selectively deposited over the whole substrate.

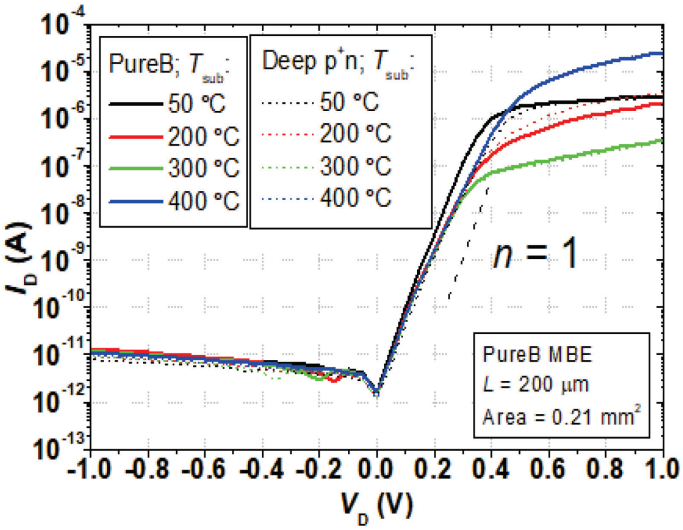

Figure 5.9. *I-V* characteristics of a non-metallized ring-shaped diodes with *L* = 200 µm (see Fig 3.13) fabricated using MBE deposited B layer at temperature at 50°C, 200°C, 300°C and 400°C, compared to implanted p^+n diodes [102].

The electrical characteristics were measured using sheet resistance and diode structures and the extracted R_{sh} and I_e are compiled in Fig. 5.10 [99], together with the values found for CVD B-layers. The CVD B-deposition was performed in the temperature range from 250°C to 400°C in the Picosun and from 400°C to 700°C in the Epsilon. In Fig. 5.10, the I_e at 0.2V forward bias is plotted. For the 600°C and 700°C devices, the B bulk Si doping contributes to reducing I_e. Below 450 °C the I_e appears to saturate at ~ 45 pA for the CVD

samples, which corresponds to a saturation current density of 9.6×10^{-20} A/μm^2. Devices with MBE boron deposited at T_{sub} = 300 °C and 400°C follow the same trend and almost the same suppression of electron injection is achieved. However, decreasing the deposition temperature down to 200°C and 50°C increases electron current to 330 pA and 2.45 nA which correspond to saturation current densities of 7×10^{-19} A/μm^2 and 5.2×10^{-18} A/μm^2, respectively. The large increase in electron injection at 50°C suggests that the interface bonding between the B and Si that leads to hole accumulation at the interface is still taking place, albeit not very effectively. The low temperature deposition probably does not provide enough energy to form and sustain a high concentration of negative fixed charge at the B-Si interface.

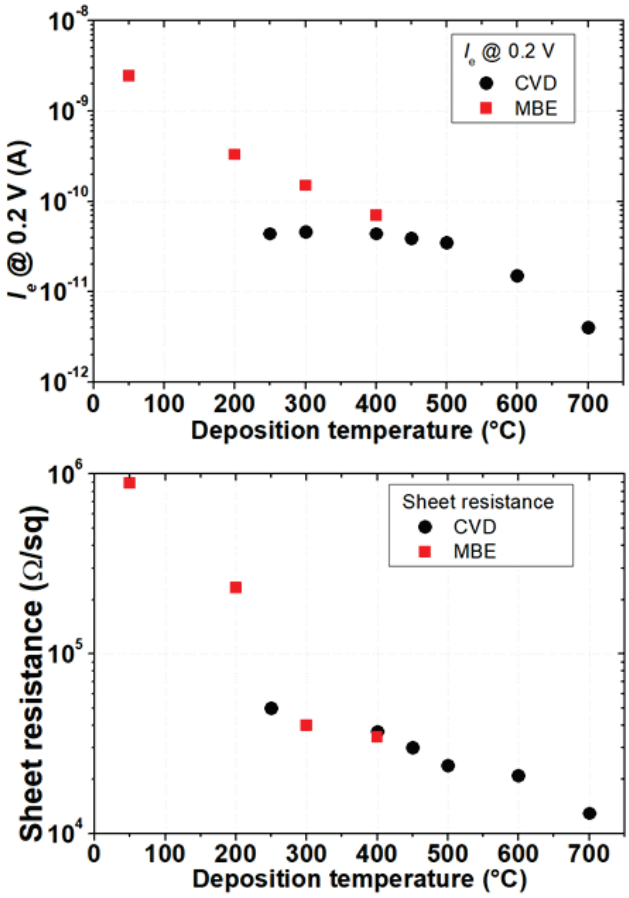

Figure 5.10. Electron current (top) and sheet resistance (bottom) as a function of deposition temperature for devices with MBE and CVD B layers [102].

The CVD layers from 250°C to 400°C were deposited in the Picosun as listed in Table 5.2. The Epsilon layers were deposited from 400°C to 700°C.

The same conclusion could be drawn from the sheet resistance measured along the B-Si interface on the same samples and also plotted in Fig. 5.10. In contrast to the I_e that has a more or less constant value from 400°C to 250°C, the R_{sh} continues to increase as the deposition temperature is decreased. It becomes, just like the I_e, extremely high for the 200°C and 50°C depositions. These high values could also indicate that, besides a lower hole concentration, a higher density of interface defects or a weak B-Si bond could also be playing a role for degrading the R_{sh} [102].

TABLE 5.3. THICKNESS AND ROUGHNESS EXTRACTED FROM ELLIPSOMETRY MEASUREMENT FOR MBE B SAMPLES ETCHED IN AL ETCHANT AT ROOM TEMPERATURE FOR DIFFERENT ETCH TIMES [102]

Dep. Temp.	Before etch	30s	2min	5min	15min
	$t_B + R_B$	$t_B + R_B$	$t_B + R_B$	$t_B + R_B$	$t_B + R_B$
RT	1.54+2.31	1.31+2.17	1.16+2.18	1.03+2.21	0.88+1.90
200°C	1.58+2.12	1.35+1.95	1.18+2.05	1.04+2.10	0.92+1.98
300°C	1.56+1.83	1.43+1.50	1.28+1.71	1.13+1.95	1.00+2.07
400°C	1.62+1.64	1.50+1.51	1.40+1.62	1.28+1.88	1.15+2.22

The quality of the MBE B-layers was evaluated by monitoring the removal in Al etchant at room temperature. Normally Al etchant is used in an elevated temperature, for example 45°C, to achieve a reasonably high etch rate. In order to investigate the effect of Al etchant on the 1.5-nanometer thin MBE boron films, the etching was performed at room temperature to moderate the etch rate. The results are shown in Table 5.3, in which the layer thickness (t_B) and roughness (R_B) are indicated. The etch rate was slowest for the highest substrate temperatures, indicating a higher compactness of these layers. This was also confirmed by immerging the samples in TMAH at 85°C. After 20 min, inspection with the optical microscope revealed no visible pinholes, similar to what was observed for the CVD B-layers discussed in the previous sections. After a prolonged 2 hours immersion, a high density of pinholes was observed on the samples deposited at RT, as shown in Fig. 5.11. At 400°C, the pinholes were much less dense, and appeared to be related to mechanical damage of the sample surface [88]. The MBE B-layers deposited

at higher temperature were more resistant to TMAH, indicating that the thermal energy enhances the strength and/or number of the B-to-B bonds.

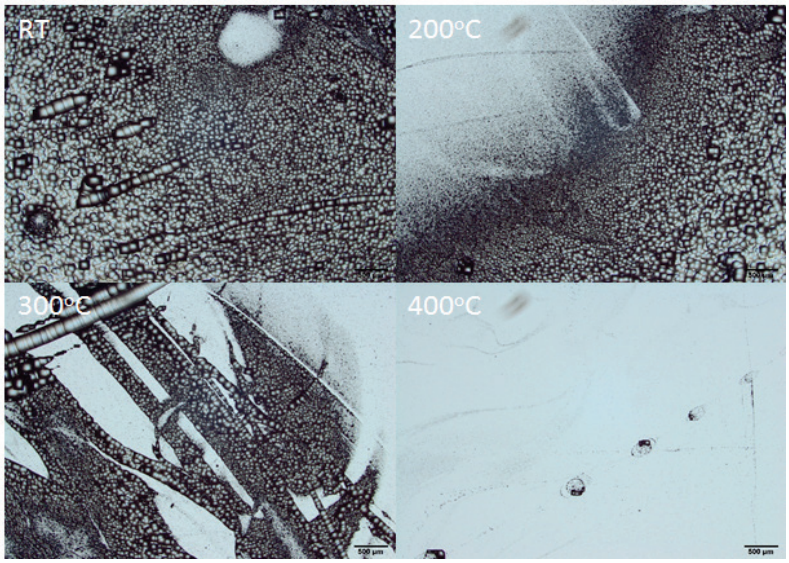

Figure 5.11. Optical microscope images of MBE B deposited on Si at substrate temperature of RT, 200°C, 300°C and 400°C after TMAH etching at 85°C for 2 hours [102].

5.4 B-Deposition in the ULPCVD System

The customized furnace in the MESA+ facility of the University of Twente enables batch processing of up to 29 wafers. With a turbo pump, the pressure in the process chamber can be brought down to 10^{-7} mbar and the processing pressure is less than 10^{-3} mbar. Prior to deposition, samples were cleaned with 1% HF to remove the native oxide and to build H-termination. To minimize the risk of H-desorption and subsequent oxidation, it was chosen to load the samples at the deposition temperature, followed immediately by pumping down of the system to the 10^{-5} mbar to 10^{-6} mbar range. Temperature stabilization was then performed in N_2 at a pressure of 1 mbar to bring the sample temperature to the set point quicker, after which the system was again pumped down and the B_2H_6 flow was turned on. Although Ar carrier gas was used for ULPCVD deposition, the associated incubation time was found to vary considerably for this system. For example, great variations were seen when stabilization times from 30 min to 1 h were applied. Yet the temperature stabilization time cannot be prolonged indefinitely because it increases the

risk of possible oxygen contamination. The 1 h stabilization time was used and several samples deposited from 300°C to 400°C were analyzed by XPS. For all samples, the oxygen content was very low, in the 0.5% to 2% range, with no clear peak at the Si surface. Moreover, with 1 h stabilization, the layer thickness was proportional to the deposition time, which confirms that the sample temperature was stabilized after that time.

In addition to the ULPCVD furnace samples, a wafer with B deposited in an LPCVD furnace in the former DIMES cleanroom at TU Delft was available [131]. The major difference with respect to the ULPCVD deposition was that the precursor in LPCVD furnace was 0.2% B_2H_6 in H_2 gas, and the processing pressure was around 1 mbar. For B-deposition in both furnaces on patterned wafers, the thickness of the B-layer would presumably be more uniform because the deposition on thermal oxide has a much longer incubation time [132], probably because there are too few nucleation centers for B-adsorption. Therefore, gas depletion, which is responsible for thickness non-uniformity, will be reduced. The PureB diode *I-V* characteristics for the LPCVD and ULPCVD furnace depositions at 400°C are shown in Fig. 5.12 (a) and (b), respectively [133]. The LPCVD results were measured across the wafer on 50 dies and were found to be very uniform with a J_{SE} value $1.00 \pm 0.05 \times 10^{-12}$ A/cm^2 that was identical to what was achieved with Epsilon PureB diodes. There was more spread in the corresponding R_{sh} values, the lowest of which were 35 kΩ/sq, just as for the comparable Epsilon PureB diodes, but several were in the 40 - 50 kΩ/sq range and a couple as high as 75 kΩ/sq. Such higher values could indicate a small amount of native oxide contamination of the Si surface [133]. The *I-V* characteristics of the ULPCVD PureB diodes displayed a large spread in current, showing a non-ideal leakage as seen in Fig. 5.12b. This effect is found to be more evident with thicker layers. The incubation time was not well-defined at 400°C so attempts to grow a few nanometer-thin layers was not optimized. With a 10 nm B-layer on Si, the boron deposition on the oxide was already enough to form an electrically connected layer that degraded the electrical isolation between devices. By measuring the current across a ring of oxide, the resistivity of the B-layer on the oxide was estimated to be about 10^3 Ω-cm, whereas the theoretical value is from 500 to 10^4 Ω-cm. Nevertheless, it is possible to reasonably estimate the J_e because the implanted p^+ diodes suffer from the almost the same poor isolation. Therefore, the parasitic current across the oxide can largely be eliminated by using the differential I_e subtraction method described in Section 3.2.3. It is clear from the current

values above about 0.3 V forward bias that, when the leakage is subtracted, the I_e is practically the same for both diodes and close to the values for the LPCVD and Epsilon PureB diodes [133].

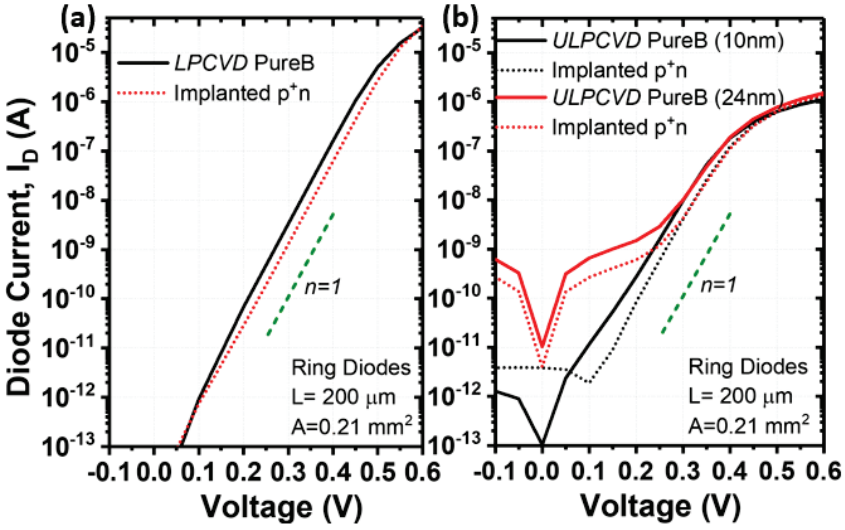

Figure 5.12. Measured *I-V* characteristics for PureB diodes and the corresponding implanted p^+n diodes for (a) a 5-nm-thick LPCVD B-deposition, and (b) 10-nm- and 24-nm-thick ULPCVD B-deposition. Ring-shaped diodes with L = 200 μm and A = 0.21 mm^2 (see Fig 3.13) [133].

5.5 Back-Etching of B-Layers to the B-Si Interface

The interface quality of B-Si bonding is the critical feature of interest for PureB diode applications. The experimental results discussed in Chapter 4 show that Al etchant can etch B with high selectivity with respect to Si. However, whether the Al etchant will also remove the B atoms that have made the desired bonds to Si atoms at the interface is not clear. Even for 600°C - 700°C high temperature depositions, where there is some B doping of the bulk Si, the special B-Si bonds are still the decisive element for obtaining low I_e. Thus, the *I-V* characteristics of as-deposited PureB diodes, regardless of deposition temperatures, is dependent on the integrity of the B-Si interface. In this section, the focus is put on the removal of the bulk B with Al-etchant to see if this can be done without damaging the interface. This would perhaps then be a method of making the thinnest possible functional 2D boron layer.

Having such a thin layer is, whether achieved by growth or thinning down, would be of direct interest for low-energy electron detection for eliminating the bulk boron dead-layer, but also for nanoscale devices such a compact p-type region would find applications.

Three samples with a B-layer thickness of approximately 10 nm were deposited in the Epsilon by LSRL on bare Si wafers at 350°C in N_2 (N350), 400°C in N_2 (N400) and 700°C in H_2 (H700). A long-duration immersion in Al etchant is applied to N350 and N400 for 8 hours at 45°C, and to H700 for more than 4 hours at 65°C. The etch speed in all cases was larger than 1 nm/min. Standard ellipsometry measurements, the results of which are given in Table 5.4, indicate that a thin layer remained on the Si. It is thicker than a native oxide layer on an unprocessed wafer. The ellipsometry might not be able to accurately describe the actual situation on the surface, yet it at least shows that the B deposition/removal process somehow changed the conditions at the Si surface. For 700°C deposition, the roughening and mixed B-Si at the interface together result a higher final value of thickness and roughness. For 350°C and 400°C depositions, however, there was no expected diffusion of B into Si, so the extra thickness and roughness could be the result of, either a remaining B-layer after exposure to Al-etchant, or a thicker native oxide.

TABLE 5.4 ELLIPSOMETRY MEASUREMENT OF B-ON-SI AFTER >4 HOURS AL ETCH

Sample	Thickness (nm)	Roughness (nm)
N350	0.63	1.59
N400	0.63	1.61
H700	0.73	2.23
Native oxide	0.49	1.38

TABLE 5.5 THE INTEGRAL BORON CONCENTRATION AFTER >4 HOURS AL ETCH

Sample	Integral boron concentration (atoms/cm^2)
N350	1.88×10^{13}
N400	1.82×10^{13}
H700	3.78×10^{14}

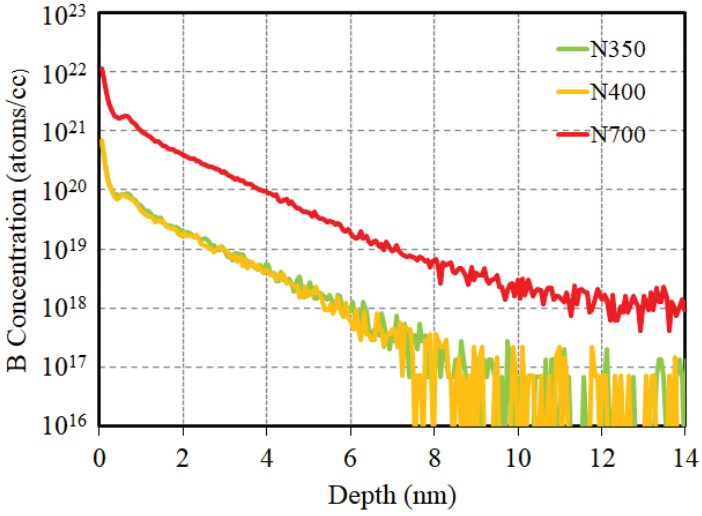

Figure 5.13. Boron atomic concentration after prolonged immersion in Al etchant, measured by SIMS.

The SIMS measurement shown in Fig. 5.13 confirms the presence of boron residues after etching, but the integral boron concentration presented in Table 5.5 suggests that the boron left on the Si surface is less than a monolayer which is 6.78×10^{14} cm^{-2} for the Si surface. This means that only some of the B-Si bonds are strong enough to withstand the extensive Al etch. In addition, at both temperatures the remaining B atoms are much less than a monolayer, however, the starting point of the SIMS B concentration measurement is much higher than the solubility of Si (2×10^{19} /cm^{-3} at 700°C). Both these pieces of evidence suggest that the remaining B atoms are on the surface for low temperature depositions. For 700°C deposition, the integrated B concentration is more than 10 times higher than for the low temperatures, and most of the boron atoms appear to be very near to the surface. There are some uncertainties on the absolute numbers extracted from the SIMS measurement, but the relative numbers are reliable. The HRTEM in Fig. 2.5 indicates the existence of a 1-nm B-Si mixed layer near the surface which could exceed the Si solubility, and can explain this high concentration at the surface. This could suggest a larger quantity of B atoms remaining on the surface, which means a stronger bonding with Si. The influence of electrical properties after Al etch is needed for further experimental investigations.

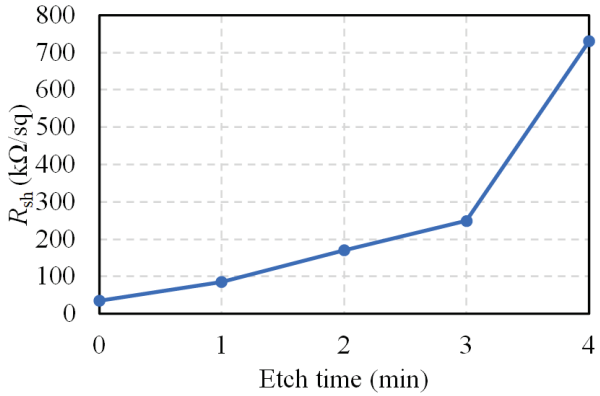

Figure 5.14. The sheet resistance as a function of 45°C Al-etchant exposure time for sample B[400,4].

The samples called B[400,4], discussed in Chapter 4, were patterned with sheet resistance test structures and had a 4-nm-thick B-layer grown in the Epsilon at 400°C. One of these was immersed in 45°C Al-etchant. The relationship between Al-etchant exposure time and sheet resistance is shown in Fig. 5.14. The conductance along the interface gradually decreased as the exposure time was increased. This means that the Al-etchant deteriorated the interface and compromised interface conductance. The diode characteristics were monitored on B[400,4] deposited on ring structures with L = 200 µm mentioned in Fig. 3.12 before and after a 10 min exposure to Al-etchant at 45°C. As seen in Fig. 5.15, from being optimal PureB diodes, the etching causes high leakage currents in the diodes. Therefore, the remaining B atoms on the surface are not numerous enough to sufficiently suppress the electron injection. The unoccupied sites are promoting generation/recombination, and they are possibly overgrown with native oxide. The diode without guard ring (Fig. 5.15 a) appears to have degraded a bit more than the one with guard ring (Fig. 5.15 b), which is not surprising since the B-coverage of the perimeter is always a point of concern for the low temperature B-depositions (Fig. 5.9). For the diode where the B deposition windows were p-type implanted (S4 set in Fig. 3.12), the leakage is much less significant (Fig. 5.15 c), because the Al etchant does not influence the bulk p^+-Si. The leakage in the S4 (Fig. 3.12) diode could possibly be due to moisture on the wafer, however the exact origin is not known. Further analysis was stopped because the etched wafers degraded due to the native oxide growth after a month. In future studies, precautions need to be taken to protect the surface after etching.

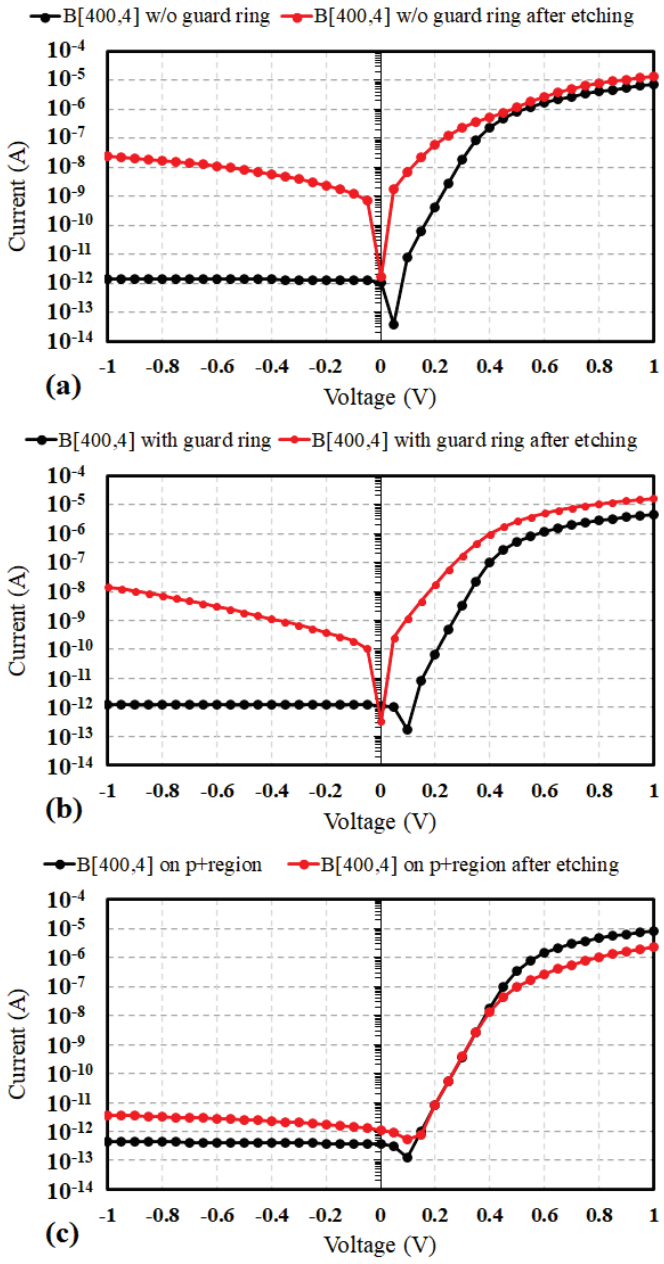

Figure 5.15. Diode characteristics before and after 10 min exposure to Al etchant at 45°C for B [400,4] in ring 200 structures, (a) without guard ring, (b) with guard ring and (c) B on a p^+-implanted region.

5.6 Conclusions

TABLE 5.6 COMPARISON OF B DEPOSITION METHODS

Equipment	Epsilon CVD	Picosun	ULPCVD furnace	MBE
Equipment availability	-	++	++	-
Selectivity	++	+-	+-	-
Conformality	++	++	++	+-
Thickness control	++	+-	-	++
High-volume production	-	-	++	-
Low oxygen contamination	+-	+-	/	++
Optimal 400°C *I-V*	++	+	+	+
RT deposition	-	-	-	++

In Table 5.6 an overview is given of the advantages and disadvantages with respect to PureB diode fabrication of the four different deposition techniques discussed in this chapter. All deposition machines show promising electrical *I-V* characteristics of the PureB diodes. In general CVD depositions have better selectivity and conformality on Si. MBE deposition has poor selectivity due to its physical nature, however this feature could be beneficial for B deposition on an arbitrary substrate or larger, e.g., SiO_2. The Epsilon and MBE systems are especially developed for good control of layer uniformity and deposition rate. Both were originally designed for Si/Ge epitaxy, specifically for SiGe heterojunction bipolar transistors (HBTs) that require nm-thin highly-uniform layers. In the Epsilon, the low process pressure and use of H_2 instead of N_2 carrier gas lowers the deposition rate, which is especially advantageous at high temperatures. MBE enables atomic layer-by-layer deposition and can have an even lower deposition rate. The availability of these two machines is mostly limited by their high price. The Picosun, on the contrary, is more accessible due to its broader range of functionality and relatively low price. The ULPCVD furnace would be advantageous for massive production, while the other machines can only process one wafer at a time.

Chapter 6 B-Membrane Development and Reliability

In Chapter 4, B-layers as masks for the anisotropic wet-etching of Si were introduced, and the experiments also revealed their potential as a membrane material. In this chapter, experiments are presented that were designed to gain knowledge of B-layer properties for different deposition temperature/rate with respect to the layer compactness and the resulting stress. For lower deposition temperatures, the Epsilon system was unsuitable because maintaining good control of the temperature of the deposition chamber becomes difficult below 350 °C. Therefore, low temperature B-deposition was now developed in the Picosun. Focus was also put on the development of closed B-membranes using several through-wafer back-etch methods.

6.1 Membranes on Semiconductors

In SEM systems commercial protection membranes are today made of SiN, SiC, SiO_2 and polyimide, but materials such as graphene are being studied due to the low atomic number, the monolayer thickness, the high mechanical stiffness, and high electrical conductivity which would eliminate parasitic charging effects and artifacts common for standard dielectric membranes [41, 42]. B-membranes are shown here to also have many of these advantages: B has an even lower atomic number than C and the CVD layers are conductive. Although the resistivity is very high [86] charging effects were not observed on the membranes presented here. An important advantage with respect to graphene is that B thin films are highly manufacturable [18, 43].

Boron has also been studied as a material for capping EUV pellicles for EUV lithography systems [45]. These pellicles are preferably made of polysilicon due to the high transmissivity and mechanical strength. To ensure resistance to EUV exposure and cleaning plasmas, coatings are necessary. B is one of the materials that has been proven resistant to both treatments [46]. For high-volume EUV exposure, the infrared emission needed for preventing overheating of the pellicle requires capping of the poly-Si with layers of suitable emissivity. Capping layers incorporating boron were found to have both good transmissivity [47] and emissivity [45]. To extend this to using

pure B-membranes for pellicles, high demands on the mechanical strength and stiffness need to be met. Tensile stress is needed to prevent sagging but film shrink due to densification during exposure/heating gives a risk of excess tension and consequent deformation/breakage. Films with maximum material density are therefore preferred.

For all the above-mentioned membrane applications, the robustness of the membrane is of major importance. More generally, for many applications employing Si structures shaped by micromachining, the structuring is simplified by having masking and membrane layers fabricated at low temperature and with low stress. In particular, layers deposited below 400°C, can be more easily integrated in complex process flows that include partially or fully-processed CMOS circuits. As presented in Chapter 4, B-layers with excellent adhesion, conformality and etch selectivity (> 10^4) were achieved at SiN_x-like stress levels: 490 MPa for 400°C and -1250 MPa for 700°C B-deposition. As opposed to conventional PECVD SiO_2 or SiN_x masking layers that often require several micrometer thickness [38, 39], low strain could be realized because a B-layer thickness as low as 2 nm was sufficient for masking purposes. Moreover, B-layer membranes of only 4 nm in thickness were fabricated. Patterning of the boron was straightforward, being achieved by standard resist masking and removal by aluminum etchant [43].

Although our work was the first to demonstrate the use of B-layers as TMAH-resistant material, B has always played an important role in Si micromachining in the form of heavily-B-doped p-type Si regions that function as etch-stops for wet Si etching. The selectivity of these regions is poor compared to B-layers, with values only reaching up to about 10^2 [134-136]. More recently there has also been an increasing interest in B in the form of the 2D material borophene, the synthesis of which has been reported to have been achieved by CVD [7-11] among others on silver or copper. Extended one-atom-thick boron sheets were constructed from planar hexagonal 36-atom clusters of B [137]. These layers were metallic and they have also been predicted to have high electrical and heat conductivity, and to be more flexible and stronger than graphene [9]. Moreover, borophene has high reactivity which may be attractive for battery application but this is a disadvantage for application as protection membranes since a rapid oxidation of the borophene in open air has been reported [9]. Unlike B, this and the many other manufacturability challenges mean that borophene is very far from entering any products.

6.2 Experimental procedures

TABLE 6.1. LIST OF MAIN DEPOSITION PARAMETERS FOR THE STUDIED SAMPLES.

Sample	Deposition System	Temperature (°C)	Carrier Gas
E2[400,N2]	CVD Epsilon	400	N_2
Ex[450,N2]	CVD Epsilon	450	N_2
Ex[550,N2]	CVD Epsilon	550	N_2
Ex[590,H2]	CVD Epsilon	590	H_2
Ex[625,H2]	CVD Epsilon	625	H_2
Ex[675,H2]	CVD Epsilon	675	H_2
E2[700,H2]	CVD Epsilon	700	H_2
PC[300,Ar]	ALD Picosun	300	Ar
PC[400,Ar]	ALD Picosun	400	Ar
PC[500,Ar]	ALD Picosun	500	Ar

* "x" can be either 1 or 2 and refers to Epsilon run 1 or run 2.

For patterning of the B-layers, removal of B was achieved by wet etching in standard aluminum etchant at a temperature of 45°C. Wet etching of Si was performed in 25% TMAH at 85°C TMAH. The etch rate in the <100> direction was approximately 0.6 μm/min.

Samples were prepared by CVD either in the Epsilon or Picosun. An overview of the deposition parameters is listed in Table 6.1. For the Epsilon depositions, 150 mm p-type <100> silicon wafers were used and the deposition temperature was varied from 400°C to 700°C using deposition parameters as described in Section 4.3.1 Below 550°C, the carrier gas was changed from hydrogen to nitrogen because at such low temperatures the H-coverage of the Si surface impedes the B-adsorption and the B_2H_6 decomposition is also hindered so that the bulk B deposition rate becomes very low [94]. Two runs E1 and E2 were performed. For the second run effort was made to maintain about the same deposition rate and resulting B-layer thickness for all deposition temperatures.

The second group of B-layers was deposited on 100-mm p-type <100> double-side polished silicon wafers from 200°C to 500°C in Picosun. From 200°C to 500°C, B_2H_6 flow rates were from 10 sccm to 200 sccm. At 500°C, one sample was also made in a pulsed CVD mode with 0.2 s B_2H_6 and 5 s Ar

purge, in order to reduce the growth rate. The total pressure in the reactor was 1 mbar. At this pressure the incorporation of oxygen atoms due to back ground contamination, mostly moisture, was difficult to completely eliminate and it may have some negative influence on the final compactness of the B-layers. However, in this study the oxygen contamination was not explicitly monitored since the results were consistent with respect to the applied deposition conditions. For deposition at temperatures of 200°C and 250°C we were not successful in building up a bulk B-layer but at 300°C several nm-thick layers were realized and these will be discussed in the following sections.

6.3 Stress Measurements

6.3.1 Epsilon B-layer samples

The stress of the B-layers deposited in the Epsilon runs was determined and the results are shown in Fig. 6.1 as a function of the deposition temperature. The first run E1 gave an indication that a zero-stress condition may exist at about 600 °C. In the second run E2, effort was made to achieve about the same deposition rate and layer thickness at all temperatures, using ellipsometry measurements to estimate the thickness.

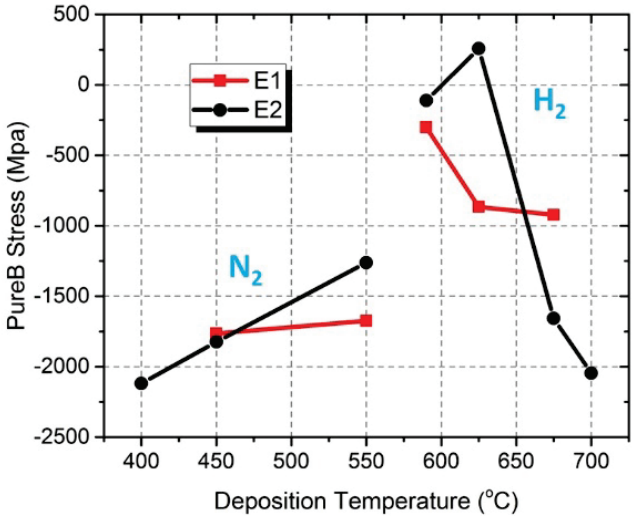

Figure 6.1. B-layer stress as a function of deposition temperature, for the E1 and E2 deposition runs [44].

The resulting values are listed in Table 6.2. The layer group grown in H_2 has about a 30% lower deposition rate than the N_2 group but within the two

groups the deposition rate is so similar that it can be eliminated as a parameter in evaluation of the stress. Also in the E2 run, a zero-stress point appears at a deposition temperature of about 600℃.

Since the deposition rate is eliminated within the two groups, it is clear that the resulting stress level is highly dependent on deposition temperature with both the highest and lowest temperature having the highest compressive stress. For the higher temperatures, the B-H molecules readily decompose and it is known that the B atoms can move with high mobility along the surface [85, 96]. From this viewpoint, it is understandable that lowering the temperature will move the stress towards tensile values since lower decomposition rates and mobility will plausibly lead to more H incorporation and less strong B-B bonding in the film, i.e., the B-layer will become less compact. Switching to N_2 carrier gas will enhance the decomposition of B-H molecules [85], improving the compactness with respect to what could be achieved in H_2 carrier gas. However, when going from 400 ℃ to 550 ℃ there appears to be a slight decrease in the stress. It is likely that more parameters such as the expansion coefficients of the Si and the specific B-layers, would have to be considered to entirely understand the resulting stress behavior. Nevertheless, it is clear that the deposition temperature is a means of tuning the B-layer stress for a given set of deposition parameters. An evaluation of the B-B bonding strength was achieved by measuring the rate at which the layers were etched in Al etchant.

TABLE 6.2. DEPOSITION RATE OF E2 SERIES.

Sample	Thickness (nm)	Roughness (nm)	Deposition rate (nm/min)
E2[400,N2]	13.65	2.89	0.95
E2[450,N2]	13.57	1.7	0.92
E2[550,N2]	11.38	3.22	1.07
E2[590,H2]	15.6	4.46	0.73
E2[625,H2]	10.7	2.32	0.65
E2[675,H2]	14.58	1.93	0.62
E2[700,H2]	14.47	2.06	0.67

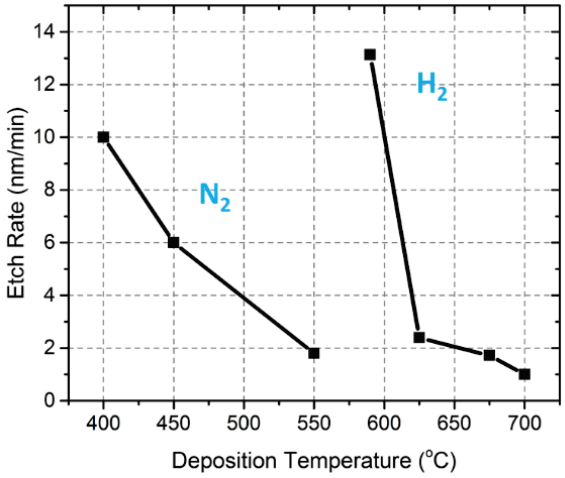

Figure 6.2. B-layer etch rate in Al-etch as a function of deposition temperature, for the E2 deposition run [44].

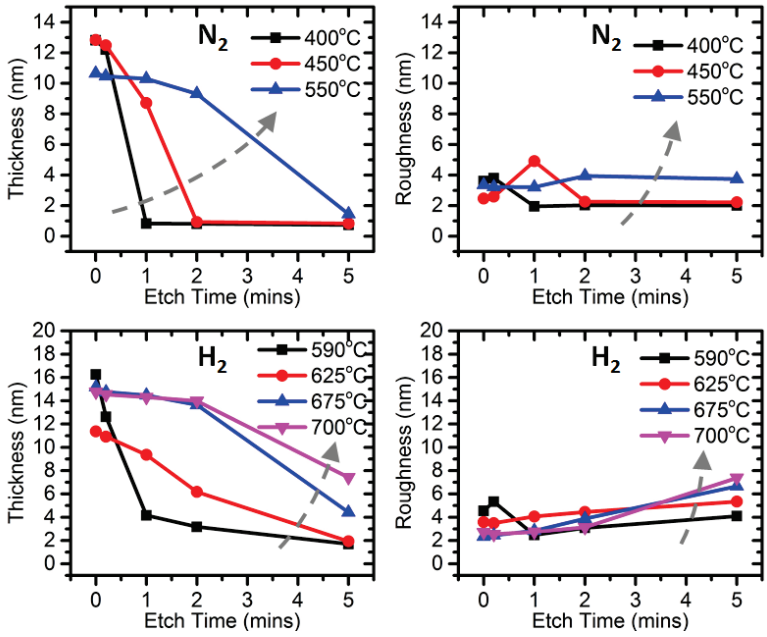

Figure 6.3. B-layer thickness and roughness values extracted from ellipsometry measurements, for the E2 samples listed in Table 2.1 as a function of etch time in Al etchant [44].

The etch rate of the B as a function of deposition temperature is plotted in Fig. 6.2. The thickness and roughness of the layers are plotted in Fig. 6.3 as a function of the etch time. The graphs are shown separately for the H_2 and N_2 carrier gas groups. Within the two groups the same trends are evident. For the first, it is clear that the etch rate increases as the deposition temperature decreases, a first indication that the compactness within each group improves with temperature.

The etch rate was found to be slow, less than 2.4 nm/min, for the highest deposition temperatures in each group, and E2[700,H2]. The roughness of these layers is noticeably increased by a nm or more upon B-removal. For E2[675,H2] and E2[700,H2] it is clear that the 5 min total etch time is too low for full B-removal. At the intermediate etch times an increase in roughness indicates that the etching is not entirely uniform. Obviously, some spots were more susceptible to etching than others.

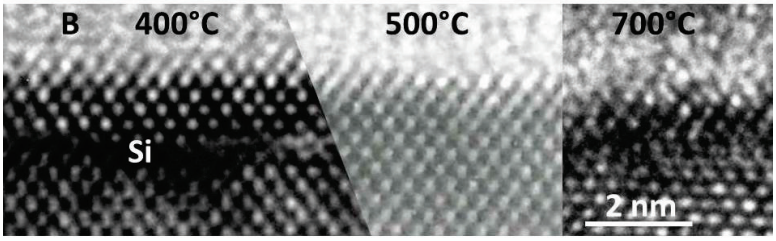

Figure 6.4. HRTEM images of the B-to-Si interface for layers grown at 400°C, 500°C and 700°C taken from [19].

For the E2[400,N2] and E2[450,N2] layers the thickness and roughness stabilizes at 0.8 nm and 2 nm, respectively, after 2 min etch time. This corresponds to a flat Si surface, which gives evidence that the B does not penetrate into the Si at such low temperatures. For E2[550,N2], E2[590,H2] and E2[625,H2] the bulk B is also removed but the surface remains slightly rough. At these high deposition temperatures, the Si was roughened because it reacts with the B during the initial exposure to B_2H_6 used for layer growth. Such a roughening is visible in the high-resolution transmission-electron-microscope (HRTEM) images of the B interface with Si shown in Fig. 6.4 [19]. For the 700 °C B-layer about a 1-nm-thick B-Si intermixed layer is visible, while for the 500 °C layer, the interface is much more uniform but still not as flat as for the 400 °C layer. The roughness measured before B-removal includes both the B surface roughness and the B-to-Si interface roughness. The former increases with decreasing temperature while the latter

decreases. Therefore, for the lowest temperature depositions, E2[400,N2] and E2[450,N2], the initial roughness before etching is high but quickly becomes less than 2 nm after etching. The initial etch rate of these samples was also very high, more than 6 nm/min. The lowest temperature deposition with H_2 as carrier gas, E2[590, H2] behaves in exactly the same manner with respect to etch speed. Therefore, as far as compactness is concerned, E2[590,H2] bears more resemblance to these two N_2-samples than to the other higher-temperature H_2 samples. This is one more confirmation that using H_2 carrier instead of N_2 gas impedes the formation of strong B-B bonds [90, 138].

6.3.2 Picosun B-Layer Samples

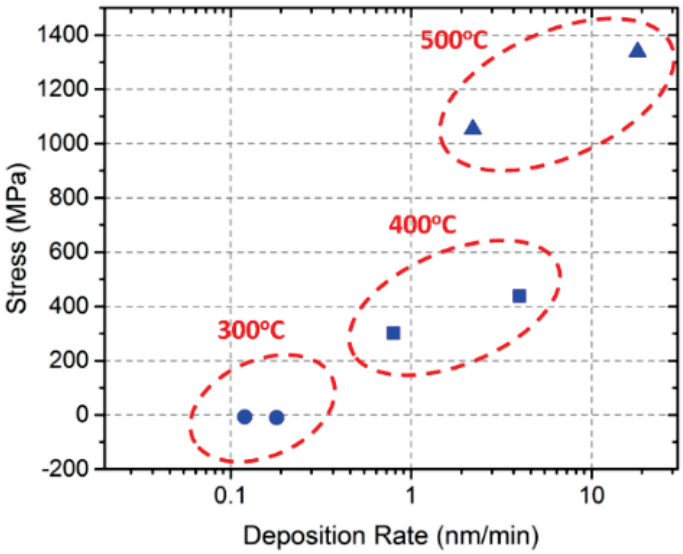

Figure 6.5. Stress as a function of deposition rate for Picosun samples deposited of the types PC[300,Ar], PC[400,Ar] and PC[500,Ar] [44].

For the group of B-layer samples deposited in the Picosun, the correlation between B-layer stress and deposition rate is shown in Fig. 6.5. All samples have tensile stress that shows a clear dependence on the deposition temperature and rate. The higher the temperature and the higher the deposition rate, the higher the tensile stress. The dependence on the deposition rate is understandable since, with the very low mobility of the boron atoms at these temperatures, there will be a faster vertical building up of the layers as the rate increases and more empty sites will be left in the final structure. This leads to a more tensile stress. For the 300 °C sample, there is

no measurable stress which indicates that the layer is very loosely bonded. The deposition rate was very low because with our gas settings it was not possible to achieve rates more than about 0.1 nm/min - 0.2 nm/min. Plausibly the low temperature also slows down the processes that break up the B_2H_6 and other B-H molecules, so not only will the number of strong B-B bonds be less likely to be formed, but also B-H molecules of different types may become incorporated in the B-layer [88, 138-140]. The low compactness of all these Picosun B-layers was confirmed by etch rates in Al etchant that were too fast to monitor. Fig. 6.6 illustrates the possible correlation of built-in stress and deposition conditions.

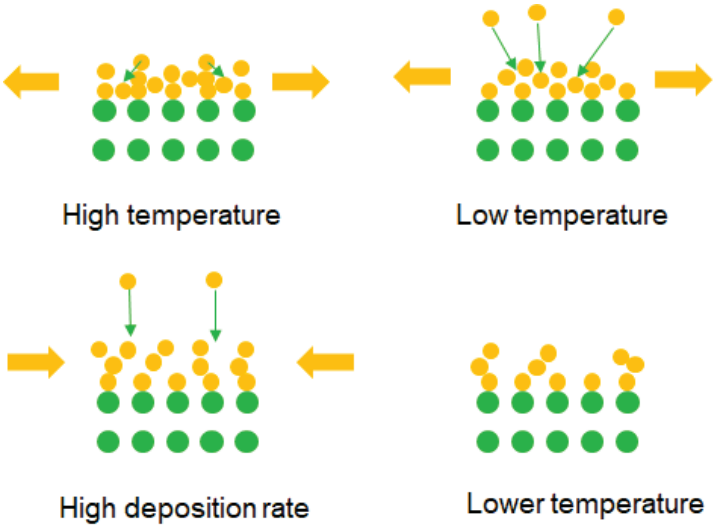

Figure 6.6. Illustration of deposition-related stress. The yellow arrows indicate the direction of the force on the deposited layer. High temperature represents E2[700,H2]; low temperature Ex[400,N2]; high deposition rate PC[500,Ar], lower temperature PC[300,Ar].

6.4 Overhanging Membranes

In Chapter 4, overhanging membranes were fabricated with B-layers deposited at 400 °C in the Picosun and 700 °C in the Epsilon under conditions that led to, respectively, tensile (490MPa) and compressive stress (-1250MPa). Membranes of these materials were fabricated by etching cavities through circular patterns in the deposited B, as shown in Fig. 6.7.

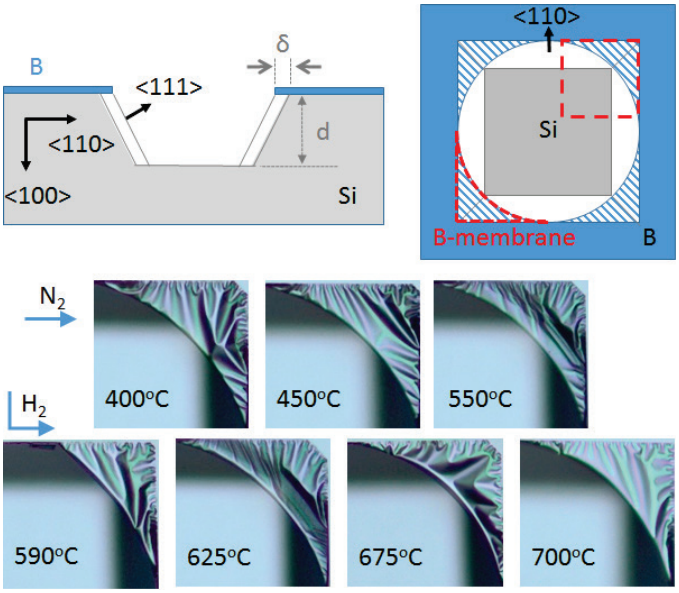

Figure 6.7. Top: schematic cross-section and top view of a cavity after TMAH etching through a circular window in a B-layer mask; the overhanging B-membranes are indicated as the hatched regions in the cavity corners. Bottom: optical microscope images of B-membranes for samples in the E2 run after etching in TMAH for 100 min. The etch window diameter was 200 μm and the focus is placed on membranes overhanging the cavity corners [44].

Visual inspection of the membranes through an optical microscope revealed stretching of the tensile and buckling of the compressive membranes, behavior that fitted well with the respective type of stress. The same type of patterning was used to fabricate membranes of all layers in the E2 series, optical images of which are included in Fig. 6.7. They all display patterns that appear buckled. This is, however, a little less pronounced for E2[625,H2] that was characterized by having a very low tensile stress. In the same manner, membranes were also fabricated with a 15-nm-thick B-layer deposited at 300 °C in the Picosun using a deposition rate of 0.12 nm/min. The result is shown in Fig. 6.8 where transparency of the membranes is evident. This was not seen for even much thinner Epsilon layers that, even for 400 °C deposition, have a metallic look. This gives additional confirmation of the very low compactness of the 300 °C layer. Such a high transparency of amorphous B-layers grown at 300 °C was also observed by infrared spectroscopy in [41]. Despite their loosely-bound nature, the membranes were undamaged, showing no pin-holes and they were mechanically strong enough to withstand the etch procedure.

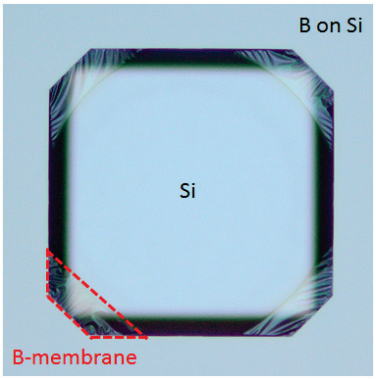

Figure 6.8. Optical microscope image of a cavity etched with TMAH for 80 min through a circular window in a 15-nm-thick B-layer deposited at 300 °C. The focus is placed on membranes overhanging the cavity corners. The etch window diameter was 200 µm [44].

With the same method as described in Section 4.6, the under-etching of Si with 300 °C B-layers as etch mask was measured in the optical microscope, as shown in Fig. 6.9. Top view optical microscopy images taken before and after cavity etching in TMAH at 85°C for 1 h and 20 min. The cavity depth in <100> direction is calculated with Fig. 6.9 (b) and (c) as approximately 30 µm, and the <110> undercut is 3 µm according to Fig. 6.9 (a) and (b). Thus, the etch-rate ratio of <100>/<111> is about 12.5, and under-etching in the <110> direction is very limited, showing that the B-Si adhesion is good, though lower than 400°C and 700°C B-layers with etch-rate ratios > 30.

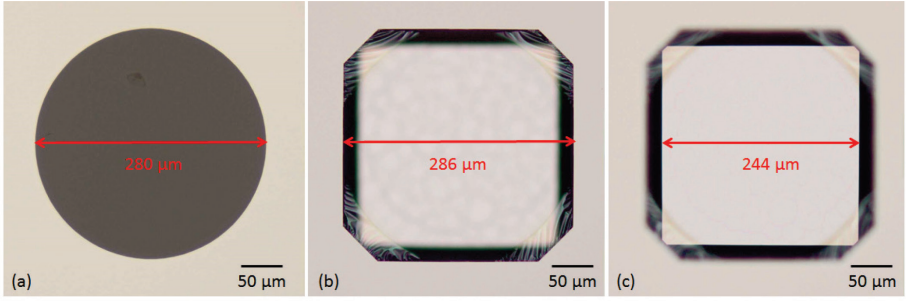

Figure 6.9. Optical microscopy images of a 300°C B-layer on silicon: (a) circular opening made with photoresist mask and Al etchant B-removal; after TMAH etching, the images were taken with focus on the Si surface (b) and bottom of the cavity (c).

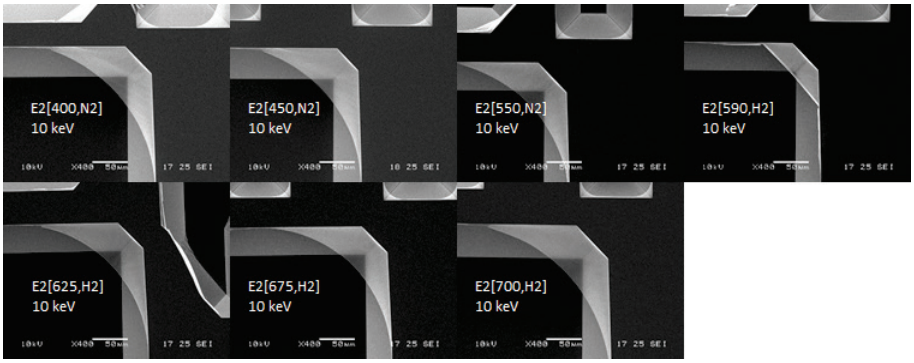

Figure 6.10. SEM images of B overhanging membranes for the Epsilon E2 samples, taken with electron acceleration energies of 10 keV.

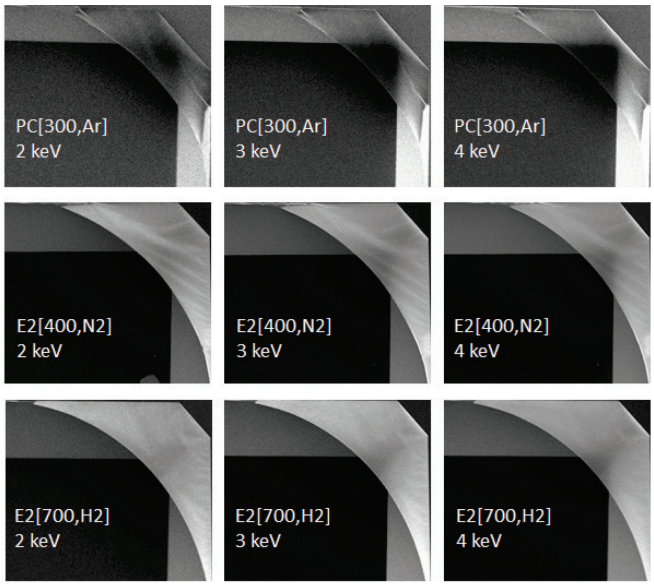

Figure 6.11. SEM images of B overhanging membranes for the samples PC[300,Ar], E2[400,N2], and E2[700,H2], taken with electron acceleration energies of 2 keV, 3 keV and 4 keV [44].

The overhanging membranes were imaged by SEM with electron acceleration energies from 1 keV up to 10 keV. At 10 keV all the Epsilon membranes had high transmissivity, giving a clear image of the cavity beneath the membrane in all cases as seen in Fig. 6.10. As the energy was lowered the membranes became more and more opaque. At 2 keV the cavity

was only visible for the 300°C Picosun sample. This is seen in Fig. 6.11 where a 15-nm-thick PC[300,Ar] membrane is compared to 14-nm-thick E2[400,N2] and E2[700,H2] membranes, for SEM images taken with 2 keV, 3 keV and 4 keV electrons. The 300 °C sample is transparent at 2 keV while the Epsilon samples are opaque. At 3 keV, the 400 °C samples become slightly transparent while the 700 °C one remains opaque until 4 keV. At higher electron energies, all images of the Epsilon samples resembled each other as far as transparency was concerned. Therefore, although the very loose bounding of the 300 °C sample is clearly identified, this method is not as sensitive as the etch tests. Since the electron transmissivity is determined by the number of B atoms that are traversed, it is concluded that the 300 °C Picosun layer is considerably less dense than the Epsilon layers that only marginally decrease in density as the temperature is decreased.

6.5 Closed Membranes

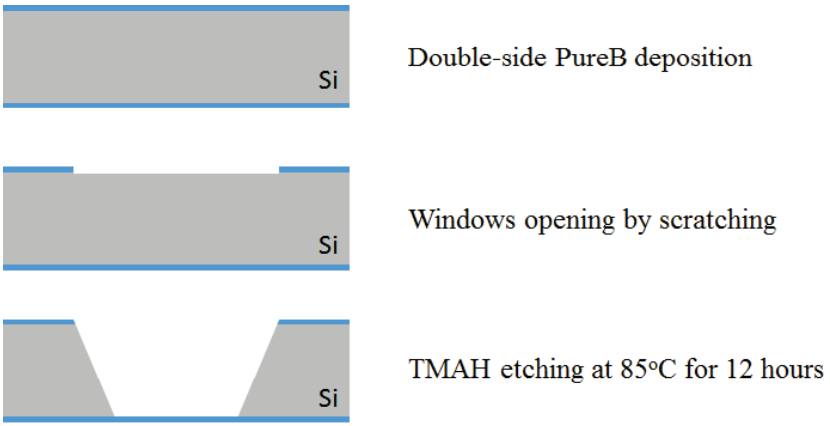

Figure 6.12. Schematic process flow for the fabrication of closed B-membranes [44].

Closed B-membranes were fabricated by wet etching through the silicon substrate as illustrated in Fig. 6.12. A 40 nm B-layer was deposited in the Picosun on both sides of a double-side-polished (DSP) wafer at 400°C and at a deposition rate of 7 nm/min. Openings of few hundred micrometers were made on the back of the wafer by scratching to damage the B-layer. The wafer was etched in TMAH for more than 12 hours until cavities reached the front of the wafer. Membranes of several sizes were produced, examples of which are shown in Fig. 6.13 (a) – (d). A few residues of Si are evident as yellowish regions within the membranes but these could be removed if the etch time

were to be prolonged. The SEM image in Fig. 6.13 (d) shows that parts of these residues are glowing which means that they have very low conductivity and are being charged by the electrons. Obviously, these are very thin Si residues that have formed a thin layer of native oxide below the B. In contrast, the B does not charge, confirming that it is conductive enough to prevent excessive charging under the normal electron flux used for SEM imaging.

Damage that led to holes in the membranes is seen to cause some wrinkling of the membranes but otherwise they were stretched perfectly over the cavities. Moreover, such damage to the membranes did not cause them to break or detach. The holes seen in the membrane to the right in Fig. 6.13 (c) are most likely due to isolated cavities having been etched through weak spots in the B-layer on the front of the wafer. Such weak spots can be the result of particle contamination of the wafer surface before or during B-deposition and the long etch time will enhance the probability of TMAH penetration to the Si surface.

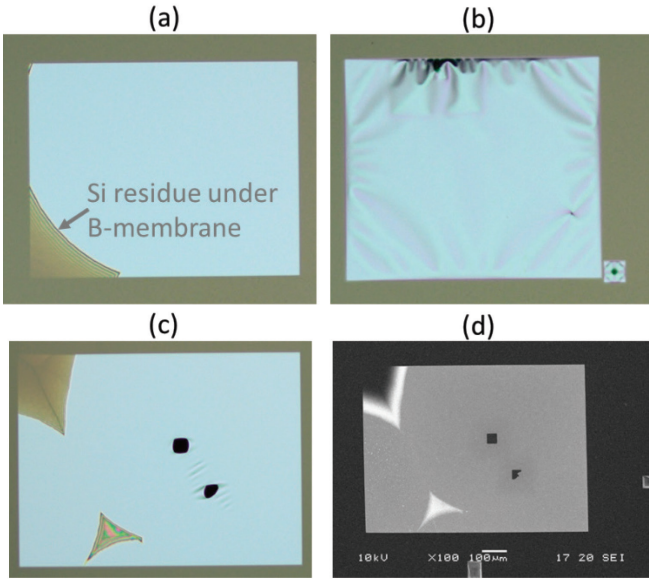

Figure 6.13. (a) – (c) Optical microscope images of closed rectangular membranes of 40-nm-thick PC[400,Ar] B-layers fabricated by TMAH etching through the Si wafer, and (d) a SEM of the film shown in (c). The sides are about 400 μm long [44].

In order to fabricate a larger closed boron membrane, another method was attempted to minimize the exposure to the wet-etchant as shown in Fig. 6.14. In this way, the weak spots that presumably would lead to holes in the membrane would be less likely to be penetrated by TMAH. The boron openings were made by photolithography and Al etchant. Then the sample was put in the Oxford Estrelas dry etcher to remove most of the silicon with a directional Bosch etch process using C_4H_8 and SF_6. The photoresist was intentionally thickened to 3.5 μm in step 2 so that it also could be used as a dry etching mask. In the last step, the remaining silicon was etched by TMAH.

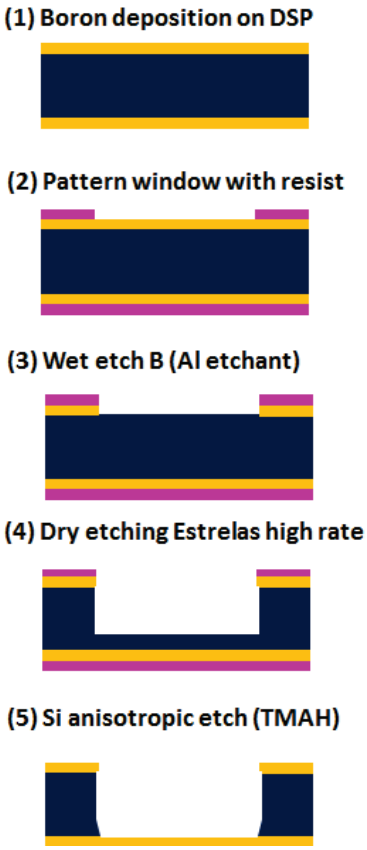

Figure 6.14. Schematic process flow for fabricating boron membranes by etching through the wafer.

A 60 nm B-layer was deposited on a DSP wafer in the Picosun at 400°C and at a deposition rate of 2 nm/min (50 sccm B_2H_6 & 500 sccm Ar). Compared with the membrane shown in Fig. 6.13, this layer was deposited

thicker and at a lower rate to eliminate the etch-susceptible weak spots and to reduce the stress level. After the process described in Fig. 6.14, a membrane of size 7 × 7 mm^2 was produced as shown in Fig. 6.15. The stress level in theory should be around 400 MPa tensile. The ripples in the membrane were possibly caused by the stretching during the wet treatment or from movements in the air.

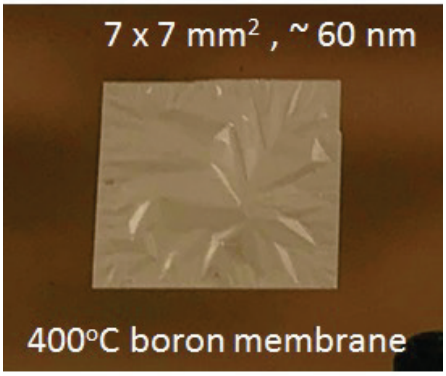

Figure 6.15. Optical image of closed rectangular membranes of a 60-nm-thick B-membrane fabricated by dry & wet etching through a DSP wafer.

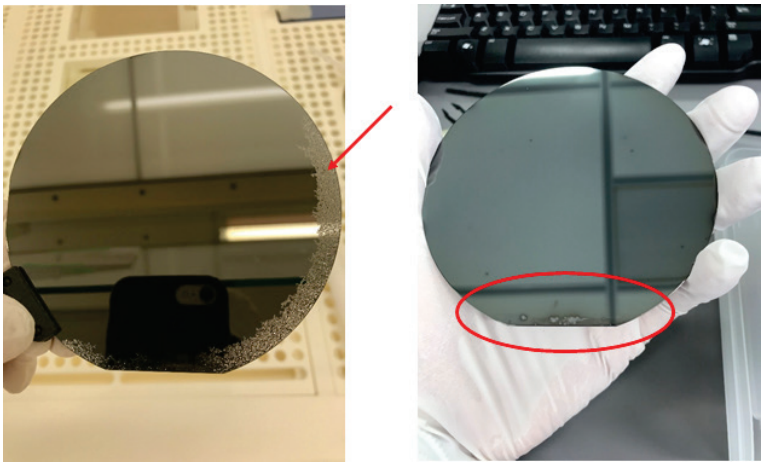

Figure 6.16. Optical images of ULPCVD furnace layers: 500°C, 880 nm (left) and 400°C, 320 nm (right).

Attempts to make thicker layers up to several hundreds of nanometers were carried out in the ULPCVD furnace, which has the advantage of enabling batch processing with low oxygen contamination. Up until tens of

nanometers thick, the layer remained intact similar to Epsilon and Picosun layers. However, flaking was found as the layer became thicker as seen in Fig. 6.16. For 500°C deposition using 50 sccm B_2H_6 for 3 hours at a rate of approximately 300 nm/h, the layer spontaneously broke from the edge and boron flakes fell off. Presumably the very fast deposition rate deteriorated the layer compactness and built up tremendous stress. Another sample was deposited at 400°C using 25 sccm B_2H_6 for 6 hours at a rate of approximately 50 nm/h. Though more stable than the 500°C layers, this layer was still mechanically fragile with flaking appearing where the wafer was carried around by tweezers.

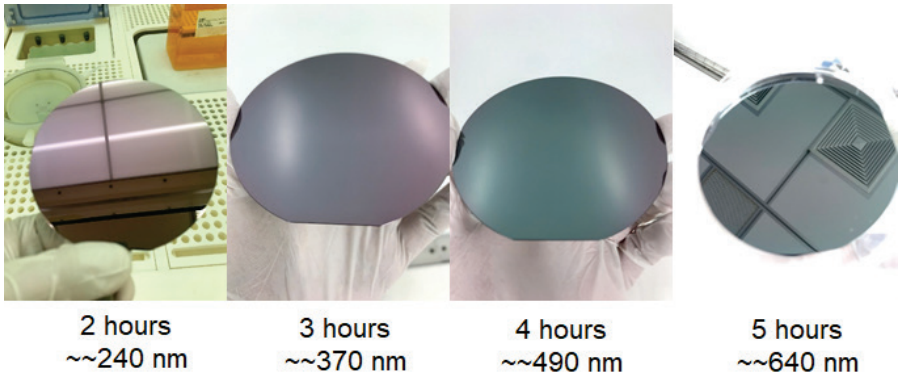

Figure 6.17. Optical images of Picosun B deposition at a total time of 2 hours, 3 hours, 4 hours and 5 hours

The lack of extra carrier Ar gas in the ULPCVD furnace made it more difficult for the ULPCVD furnace to deposit B-layers at a low rate. However, the high deposition rate is not enough to explain the vulnerability of the ULPCVD layers. Another thick layer deposition was performed in the Picosun at 400°C at a rate of ~120 nm/h using 50 sccm B_2H_6 and 500 sccm Ar. In view of the ULPCVD results, it was suspected that such a thick layer would be fragile. Optical images and ellipsometry measurements were taken after 2 hours of deposition, after which the sample was put back in the reactor and the deposition was continued for another hour. The images of the samples with a total deposition time of 2 hours, 3 hours, 4 hours and 5 hours are shown in Fig. 6.17. The corresponding thickness was approximately 240 nm, 370 nm, 490 nm and 640 nm, respectively. Even after relatively extensive physical contact with tweezers, the bottom of the wafer remained intact, unlike the ULPCVD layer deposited at 400°C.

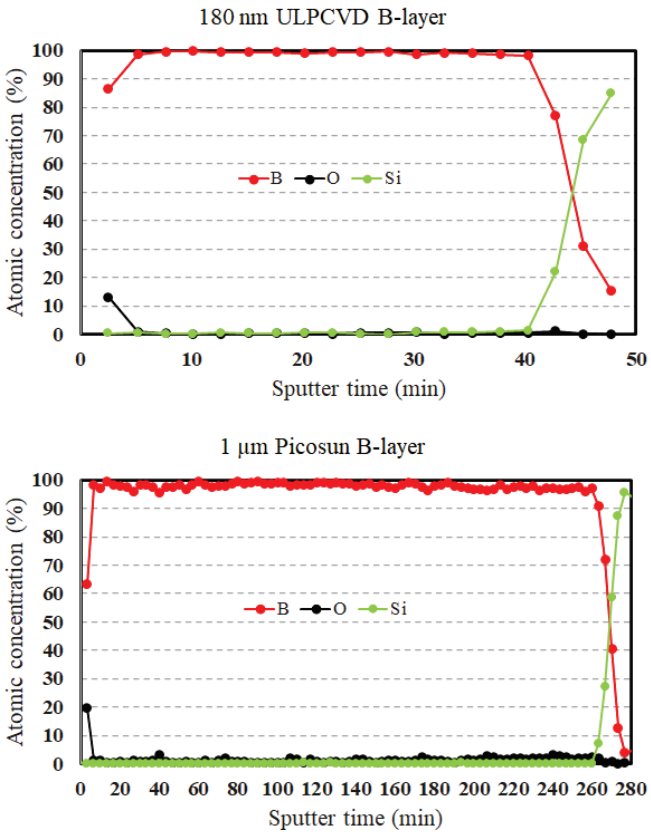

Figure 6.18. XPS measurements of 180 nm ULPCVD B (50 nm/h) and 1 µm Picosun B (120 nm/h). The oxygen content in the bulk boron is 0.5% and 1%, respectively.

XPS compositional analysis was performed on the ULPCVD and Picosun samples grown by the recipe as used for the layers shown in Fig. 6.16 (right) and Fig. 6.17. The results showed that the oxygen content in the bulk boron was 0.5% and 1%, respectively, as seen in Fig. 6.18. Most of the oxygen came from exposure to the air and stayed at the layer surface after deposition. Due to the high thickness (> 200 nm) of both layers, the XPS result is considered to accurately describe the oxygen in the bulk, because the tailing effect only has an influence up to a depth of about 20 nm in the material.

The Picosun deposition described in Fig. 6.17 continued for 8 hours and the layer thickness was measured to be 1 µm by ellipsometry. Free-standing membranes were made using the method shown in Fig. 6.14. Through the

optical images of boron-on-Si sample and membrane showed in Fig. 6.19, the self-sustained integrity indicates a much better mechanical property comparing with ULPCVD boron. And the reason in such a difference is probably the oxygen content, which seems strength the covalent bonds between boron atoms. The explanation could be found in the study of boron suboxide. For example, the B_6O, with a rhombohedral structure similar to β-boron, has been reported to exhibit high hardness with low density, high mechanical strength, oxidation resistance and high chemical inertness [141]. The presence of a high electronegativity interstitial in the structure may enhance the strength of bonding, and the shortened covalent bonds are in favor of higher elastic constants and hardness values [129]. The boron suboxide with lower oxygen content $B_{22}O$, with a crystal structure of the grains similar to β-rhombohedral boron, has even higher hardness that can easily wears down the (001) face and scratches the (111) face of diamond [142]. It is not yet clear whether the oxygen in Picosun layer forms crystal structure, however from the experimental point of view, the higher oxygen content seems to enhance the mechanical property of the boron film. The cross section of the 1 μm boron film was observed under SEM (Fig. 6.19 right). The thin bright layer at the surface is the electron charging effect caused by the oxygen-rich non-conductive layer. Even the XPS analysis in Fig. 6.18 suggests a high oxygen content at the boron surface, it cannot be easily concluded the degree of the boron oxidation.

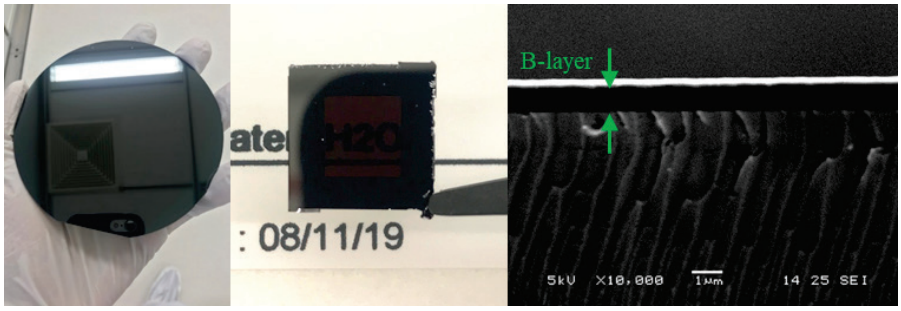

Figure 6.19. Optical image of a 1-μm-thick Picosun B-layer on Si (left), a free-standing membrane of 7 × 7 mm^2 (middle), and SEM image of the cross section (right) with the thickness of the B-layer indicated.

6.6 Conclusions

In this chapter, a tuning of the stress of CVD B-layers by varying the deposition temperature has been demonstrated for depositions from 400°C to

700°C in Epsilon, and from 300°C to 500°C in Picosun. The former were characterized by compressive stress that approached zero at about 600 °C, while the latter had tensile stress that decreased with temperature to values so low that at 300 °C they were not measurable. Furthermore, the conditions in the Picosun promoted a higher tensile stress as the deposition temperature and/or rate were increased. The type of carrier gas had a large impact on the B-layer compactness, which was evaluated by monitoring the etch rate of the material in Al etchant. The etch rate was decreased by switching from H_2 to either N_2 or Ar at temperatures below 550 °C. It is evident that there was a relation between the compactness, the etch rate, and the stress of the B-layer since clear trends were seen within specific groups of B-layers where a limited number of deposition parameters were varied. The conclusion that the B was more loosely bound as the deposition temperature was decreased was also confirmed by observing the electron transmissivity of the different layers. However, to obtain a more complete understanding of the relationship to stress, more knowledge is needed of the exact composition of the B-layers with respect to B and H bonding structures, as well as knowledge of the expansion coefficients of the specific layers.

The layers down to a deposition temperature of 300°C, were shown here to be suitable for masking of TMAH Si etching and for membrane fabrication. Weak spots in the layers that may lead to undesirable pinholes to the Si were readily avoided for depositions in the Epsilon even for a few nm-thin layers. In contrast, for low-temperature deposition in the Picosun, residues of native oxide or particle contamination are more difficult to eliminate, and the layers also have low compactness. Although the presence of weak spots with low resistance to TMAH etching were more likely for deposition in the Picosun, the results show that any such weak spots could be overgrown, and even for the very loosely-bound 300°C layers, layers as thin as 15 nm were suitable for masking and membrane fabrication.

A 60-nm-thick B-membrane of 7 × 7 mm^2 in size was made with a Picosun deposition at 400°C and through-wafer etching. However, the thick layers were prone to be very fragile and could spontaneously break. This was more likely to happen when the deposition rate was high and the layer was pure. Therefore, it could be beneficial to intentionally introduce oxygen contamination in order to make the membrane less brittle.

Chapter 7 Conclusions and Recommendations

7.1 Conclusions

This thesis was focused on further explorations to extend the applicability and availability of PureB technology. In particular, B-layer depositions at temperatures below 500°C were developed to enhance the CMOS compatibility. Several types of deposition equipment in different configurations were used to fabricate B-layers on Si, and the influence of deposition conditions were evaluated with respect to the properties of the B-layer itself as well as to the integration of the layer in PureB diodes. The main conclusions of this thesis are summarized as follow:

Electrical characterization of the interfacial hole layer

For the B-layer development, non-metalized electrical test structures proved very useful in that they allowed an electrical evaluation of the as-deposited layers in fast turnaround time process flows. The B-Si interfacial sheet resistance (R_{sh}) and the electron current (I_e) in the PureB diodes were routinely monitored. Both parameters are important for assessing whether the B-layer would have suitable electrical properties for use in a specific PureB diode application. For R_{sh} measurement, van der Pauw structures and set of ring structures were applied that complemented each other: the van der Pauw measurements tolerated high contact resistance, but were susceptible to perimeter leakage, while the opposite was true for the ring structures. The ring structures were also used for extracting the I_e of all the low-temperature PureB diodes, which was possible because the electron injection into implanted p^+n regions was much lower than into the B-layer p-type regions.

TMAH/KOH etch test for B-layer compactness/integrity

The Si anisotropic etchants, TMAH/KOH, were successfully used to evaluate the compactness of thin B-layers grown on Si under different process conditions. It was clearly shown that as the CVD layers were deposited at higher temperatures, better uniformity, selectivity and compactness, were achieved. At low temperatures, thicker layers were needed to overgrow weak spots in the layer structuring. For example, at 400°C, one-nm-thick Epsilon B-layers left the Si riddled with cavities after exposure to these etchants,

whereas 4-nm-thick B-layers were a perfect masking layers with high etch selectivity.

Surface cleaning procedures before deposition

For the low-temperature B-depositions, the Si surface cleaning before deposition was of crucial importance. The traditional native oxide removal by HF dip-etching was found to be the most reliable cleaning method. Extra cleaning steps were investigated by studying the PureB diode characteristics and B-layer etch behavior, and they mainly had a negative effect on the perfection of the Si surface. For example, high-temperature baking in H_2 would bring dopant impurities to the surface, and low-temperature *in-situ* HCl etching roughened the surface. Moreover, it was an advantage to keep the Si wafer in the load-lock for prolonged N_2 purging in order to reduce the oxygen/moist brought into the deposition system and thus reduce oxygen incorporation in the B-layer.

Low temperature boron deposition

Low temperature depositions under 450°C were performed in Picosun. The deposition rate was reduced as the temperature was decreased. PureB diodes were fabricated at temperatures down to 200°C where R_{sh} and I_e were high. At this temperature, and also at 250°C, the thickness of the layer saturated at 1 nm to 1.5 nm. However, at 250 °C the *I-V* characteristics were similar to those of thick layers grown at 400 °C, showing that the B-coverage obtained at the lowest temperature was quite good even though vertical growth was not obtained. To enable deposition below 200 °C, MBE B-deposition was investigated. Even at room temperature, PureB diodes were fabricated, albeit with very high R_{sh} and I_e. At 300°C to 400°C, the MBE results were very similar to the CVD results, both electrically and with respect to layer compactness. The latter clearly decreased significantly as the substrate temperature decreased down to 50 °C and the frequency of the aspired B-Si acceptor states decreased accordingly. The furnace ULPCVD system enabled batch processing, but with poorer selectivity than observed for Epsilon and Picosun deposition. Already for 10-nm-thick B-deposition an electrically connected layer was deposited on the oxide. For thinner ULPCVD layers deposited at 400 °C, about the same electrical and etch results were obtained as for the other deposition methods. Therefore, the substrate temperature appears to be the most important parameter for obtaining the B-layer properties of interest.

B-layer back-etching to the interface

The Al etchant cannot completely remove B atoms on Si. Even for 200 °C Picosun deposition where no bulk doping is to be expected, the concentration of B atoms left after extensive etching was 1.88×10^{13} /cm^2, while a complete monolayer would be 6.78×10^{14} /cm^2. The exposed Si surface will oxidize so electrically the back-etch diodes are not PureB-like.

B-membranes

While requirements for low series resistance and high transmissivity mainly will dictate that the B-layers in PureB (photo)diodes be but a few nanometers thick, for masking and membrane fabrication much thicker layers can be desirable. This in turn means that stress can become a critical parameter. Both Epsilon and Picosun B-layers were shown to have deposition conditions that gave low stress. In particular, negligible stress was found for Picosun deposition at 300°C where the compactness was very low. Nevertheless, etch tests showed that this layer was suitable as a masking layer. At 400°C the Picosun layers were slightly tensile and several millimeter large membranes with tens-of-nanometer to a micrometer thickness were successfully fabricated. It is suspected that a slight oxygen content could have been beneficial for improving the physical strength of these B-membranes.

7.2 Recommendations for Future Work

1. Another interesting CVD B-layer deposition method that would be worth investigating is hot-wire/plasm-assisted deposition. The substrate can then be kept at a low temperature while the extra energy is used to enable the B_2H_6 pyrolysis. There would, however, be some risk that the reactive radicals damage the Si surface. In this respect, the atomic radicals created by a hot wire would possibly be less destructive than a plasma.
2. For achieving a complete monolayer coverage of B on Si, it would be of interest to implement an ALD process. Self-limiting precursors would then be needed such as BBr_3 and BCl_3 in combination with H radicals produced by hot wire or plasma. A problem could arise because a byproduct of hydrogen halides could potentially contaminate the process.
3. The metal contacting of the low-temperature PureB diodes has not been studied in this thesis but it will be an important aspect of many integration schemes. It has been shown in other studies that if the B-layer is too thin, sporadic Schottky contacting of the metal to the Si may significantly

increase the diodes currents. Therefore, the trade-offs between series resistance, B-layer thickness, and diodes current levels and reliability, would have to be investigated for each type of B-deposition and metallization scheme.

4. Back-etching of the B-layer in PureB diodes is potentially at method of achieving very thin B-layers but only one low temperature case was studied electrically in this thesis. It would be interesting to also study a 700°C B-layer in this respect since there is more chance that a B/Si interface would survive the etching with the desired electrical properties still intact.
5. The relationship between process conditions and B-layer stress needs to be investigated more extensively. The 400°C B-layer grown in the Picosun with very low stress in Picosun would be a good starting point.
6. In this thesis, Al etchant was used to remove B layer. The chemical resistance of B towards other etchants is also interesting to investigate. For example, 99% HNO_3 and boiling HNO_3, to see if they are more efficient to remove B-layers. In addition, one of the isotropic Si wet etch HNO_3 + HF is worth trying. If B and Al are comparable in this sense, then the guess would be boiling HNO_3 can remove B quite easily, while 99% HNO_3 will passivate the surface from further etching. Still, the assumption needs experiments to confirm.

Bibliography

[1] L. Zou, L. Wang, Y. Wu, C. Ma, S. Yu, and X. Liu, "Trends analysis of graphene research and development," *Journal of Data and Information Science*, vol. 3, 1, pp. 82–100, 2018.

[2] L. K. Nanver, T. Knežević, X. Liu, S. D. Thammaiah, M. Krakers, "On the many application of nanometer-thin pure boron layers in IC and MEMS technology," *Journal of Nanoscience and Nanotechnology,* vol. 21, 4, pp. 1-11, 2020.

[3] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, and D. Akinwande, "Silicene field-effect transistors operating at room temperature," *Nature Nanotechnology*, vol. 10, pp. 227-230, 2015.

[4] J. Beilstein, "Silicene, germanene and other group IV 2D materials," *Journal of Nanotechnology*, vol. 9, pp. 2665–2667, 2018.

[5] H. J. Conley, B. Wang, J. I. Ziegler, R. F. Haglund, Jr., S. T. Pantelides, and K. I. Bolotin, "Bandgap engineering of strained monolayer and bilayer MoS_2," *Nano Letters*, vol. 13, 8, pp. 3626-3630, 2013.

[6] H. Liu, A.T. Neal, Z. Zhu, D. Tomanek, P.D. Ye, "Phosphorene: A new 2D material with high carrier mobility," *ACS Nano*, vol. 8, pp. 4033-4041, 2014.

[7] Z. Wang, T. Lv, H. Wang, Y. Feng and J. Zheng, "Review of borophene and its potential applications", *Frontiers of Physics*, vol. 14, 33403, 2019.

[8] J. Mannix., X. Zhou, B. Kiraly, et al., "Synthesis of borophenes: anisotropic, two-dimensional boron polymorphs", *Science*, vol. 350, 6267, pp. 1513-1516, 2015.

[9] Z. Zhang, E.S. Penev, B. I. Yakobson, "Two-dimensional boron: structures, properties and applications", *Chemical Society Reviews*, vol.46, 22, pp. 6746-6763, 2017

[10] G. Tai, T. Hu, Y. Zhou, et al. "Synthesis of atomically thin boron films on copper foils", *Angewandte Chemie International Edition*, vol. 54, 51, pp. 15302-15302, 2015.

[11] S. Xie, Y. Wang, X. Li, "Flat boron: a new cousin of graphene", *Advanced Materials*, vol. 31, 36, pp. 1900392, 2019.

[12] L. Yuan, J. Ge, X. Peng, et al., "A reliable way of mechanical exfoliation of large scale two dimensional materials with high quality", *AIP Advances*, vol. 6, 12, pp. 125201, 2016.

[13] C. Wu (2017), *Inorganic Two-dimensional Nanomaterials: Fundamental Understanding, Characterizations and Energy Applications*, Royal Society of Chemistry 1st Edition.

[14] J. Moore, "The birth of topological insulators", *Nature*, vol. 464, pp. 194-198, 2010.

[15] M. Yang, J. Wang, Y. Zhao, et al., "Three-dimensional topological insulator Bi_2Te_3/organic thin film heterojunction photodetector with fast and wideband response from 450 to 3500 nanometers", *ACS Nano*, vol. 13, 1, pp. 755-763, 2018.

[16] H. Zhang, X. Zhang, C. Liu, S. Lee and J. Jie, "High-responsivity, high-detectivity, ultrafast topological insulator Bi_2Se_3/silicon heterostructure broadband photodetectors", *ACS Nano*, vol. 10, 5, pp. 5113-5122, 2016.

[17] W. Tian, W. Yu, J. Shi, Y. Wang, "The property, preparation and application of topological insulators: a review", *Materials*, vol. 10, 7, 814, 2017.

[18] L. K. Nanver, L. Qi, et al., "Robust UV/VUV/EUV PureB photodiode detector technology with high CMOS compatibility", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, 6, pp. 306-316, 2014.

[19] L. Qi and L. K. Nanver, "Conductance along the interface formed by 400 ℃ pure boron deposition on silicon," *IEEE Electron Device Letters*, vol. 36, 2, pp. 102-104, 2015.

[20] L. K. Nanver et al., "Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices," *ECS Transactions*, vol. 49, 1, pp. 25-33, 2012.

[21] T. Knežević, X. Liu, E. Hardeveld, T. Suligoj, and L. K. Nanver, "Limits on thinning of boron layers with/without metal contacting in PureB Si (photo)diodes," *IEEE Electron Device Letters*, vol. 40, 6, pp. 858–861, 2019.

[22] L. Shi, S. Nihtianov, L. Haspeslagh, F. Scholze, A. Gottwald, and L. K. Nanver, "Surface-charge-collection-enhanced high-sensitivity high-stability silicon photodiodes for DUV and VUV spectral ranges," *IEEE Transactions on Electron Devices*, vol. 59, 11, pp. 2888-2894, 2012.

[23] L. Qi and L. K. Nanver, "Sheet resistance measurement for process monitoring of 400 ℃ PureB deposition on Si," *Proceedings of the 2015 International Conference on Microelectronic Test Structures (ICMTS)*, pp. 169-174, Tempe, AZ, USA, Mar. 23-26, 2015.

[24] V. Mohammadi, L. Qi, N. Golshani, K. R. C. Mok, W. B. de Boer, A. Sammak, J. Derakhshandeh, J. van der Cingel and L. K. Nanver, "VUV/low-energy electron Si photodiodes with postmetal 400 ℃ PureB deposition," *IEEE Electron Device Letters*, vol. 34, 12, pp. 1545-1547, 2013.

[25] F. Sarubbi, T. L. M. Scholtes and L. K. Nanver, “Chemical vapor deposition of α-boron layers on silicon for controlled nanometer-deep p^+n junction formation,” *Journal of Electronic Materials*, vol. 39, 2, pp. 162-173, 2010.

[26] F. Sarubbi, L. K. Nanver, T. L. M. Scholtes, S. N. Nihtianov and F. Scholze, “Pure boron-doped photodiodes: A solution for radiation detection in EUV lithography,” *38th European Solid-State Device Research Conference (ESSDERC)*, pp. 278-281, Edinburgh, UK, 15-19 Sept. 2008.

[27] F. Sarubbi, L. K. Nanver, T. L. M. Scholtes and S. N. Nihtianov, “Extremely ultra -shallow p+-n boron-deposited silicon diodes applied to DUV photodiodes,” *2008 Device Research Conference*, pp. 143-144, Santa Barbara, CA, 23-25 June 2008.

[28] L. Shi, F. Sarubbi, S. N. Nihtianov, L. K. Nanver, T. L. M. Scholtes and F. Scholze, “High performance silicon-based extreme ultraviolet (EUV) radiation detector for industrial application,” *2009 35th Annual Conference of IEEE Industrial Electronics (IECON)*, Porto, Portugal, 3-5 Nov. 2009.

[29] L. Shi, L. K. Nanver, A. Šakić, S. Nihtianov, A. Gottwald and U. Kroth, “Optical stability investigation of high-performance silicon-based VUV photodiodes,” *2010 IEEE Sensors*, pp. 132-135, Waikoloa, HI, USA, 1-4 Nov. 2010

[30] A. Šakić et al., "Silicon photodiodes for high-efficiency low-energy electron detection," *2010 Proceedings of the European Solid State Device Research Conference (ESSDERC)*, pp. 102-105, Sevilla, Spain, Sept. 14-16, 2010.

[31] A. Šakić et al., “Boron-layer silicon photodiodes for high-efficiency low-energy electron detection,” *Solid-State Electronics*, vol. 65-66, pp. 38-40, 2011.

[32] A. Šakić et al., “Versatile silicon photodiode detector technology for scanning electron microscopy with high-efficiency sub-5 keV electron detection”, *2010 International Electron Devices Meeting*, San Francisco, CA, USA, pp. 31.4.1-31.4.4, Dec. 6-8, 2010.

[33] L. Qi, S. Sluyterman, K. Kooijman, K. R. C. Mok and L. K. Nanver, “PureB single-photon avalanche diodes for low-energy electron detection down to 200 eV,” *Optics Letters*, vol. 40, 3, pp. 300-303, 2015.

[34] B. J. Inkson, (2016), *Material Characterization Using Nondestructive Evaluation (NDE) Methods*, Sheffield, United Kingdom: Woodhead Publishing, pp. 17–43.

[35] A. Šakić, V. Jovanović, P. Maleki, T. L. M. Scholtes, S. Milosavljević, and L. K. Nanver, “Characterization of amorphous boron layers as diffusion barrier

for pure aluminum," *The 33rd International Convection MIPRO*, Opatija, Croatia, pp. 26–29, May 24-28, 2010.

[36] I. Zubel, I. Barycka, K. Kotowska and M. Kramkowska, "Silicon anisotropic etching in alkaline solutions IV," *Sensors and Actuators A: Physical*, vol. 87, 3, pp. 163-171, 2001.

[37] A. Stoffel, A. Kovács, W. Kronast and B. Müller, "LPCVD against PECVD for micromechanical applications," *Journal of Micromechanics and Microengineering*, vol. 6, 1, pp. 1-13, 1996.

[38] V. Dao, V. Nguyen, J. Heo, et al., "Effect of N_2O/SiH_4 flow ratios on properties of amorphous silicon oxide thin films deposited by inductively-coupled plasma chemical vapor deposition with application to silicon surface passivation", *Vacuum*, vol. 84, 3, pp. 410-414, 2009.

[39] A. Y. Kovalgin, G. Isai, J. Holleman and J. Schmitz, "Low-temperature SiO_2 layers deposited by combination of ECR plasma and supersonic silane/helium jet," *Journal of The Electrochemical Society*, vol. 155, 2, 2007.

[40] M. Elwenspoek and H. V. Jansen, (1998), *Silicon Micromachining*. Cambridge, U.K.: Cambridge University Press.

[41] J. D. Stoll and A. Kolmakov, "Electron transparent graphene windows for environmental scanning electron microscopy in liquids and dense gases", *Nanotechnology* vol. 23, 50, pp. 505704, 2012

[42] Y. Han, K. Nguyen, Y. Ogawa, H. Shi, J. Park and D. A. Muller, "Electron microscopy in air: Transparent atomic membranes and imaging modes", *Microscopy and Microanalysis,* vol. 21, 3, pp. 1111-1112, 2015.

[43] X. Liu, L. K. Nanver and T. L. M. Scholtes, "Nanometer-thin pure boron layers as mask for silicon micromachining", *Journal of Microelectromechanical Systems*, vol. 26, 6, pp. 1428–1434, 2017.

[44] X. Liu, J. Italiano, R. Scott and L. K. Nanver, "Silicon micromachining with nanometer-thin boron masking and membrane material", Material Research Express, vol. 6, 11, pp. 116438, 2019.

[45] P. J. van Zwol, M. Nasalevich, E. Kurganova, P. Voorthuijzen, D. Vles, M. Péter, W. Symens, W. van der Zande, A. Notenboom, J. Klootwijk, R. W. van de Kruijs and A. Giesbers, "Pellicle films supporting the ramp to HVM with EUV", *Proceedings of SPIE*, vol. 10451, pp. 1-9, 2017.

[46] L. Shi, S. N. Nihtianov, L. K. Nanver and F. Scholze, "Stability characterization of high-sensitivity silicon-based EUV photodiodes in a detrimental environment", *IEEE Sensors Journal*, vol. 13, 5, pp. 1699-1707, 2013.

[47] B. L. Henke, E. M. Gullikson and J. C. Davis, "X-ray interactions: photoabsorption, scattering, transmission, and reflection at E= 50-30,000 eV, Z=1-92", *Atomic Data Nuclear Data Tables*, vol. 54, pp. 181–342, 1993.

[48] L. Qi, Jan 18th, 2016, "Interface properties of group-III-element deposited-layers integrated in high-sensitivity Si photodiodes", *Ph.D. dissertation*, Delft University of Technology, Delft, the Netherlands.

[49] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd edition, Hoboken, New Jersey, USA: John Wiley & Sons, Inc.

[50] A. Beer, "Bestimmung der Absorption des rothen Lichts in farbigen Flüssigkeiten," *Annalen der Physik und Chemie*, vol. 162, 5, pp. 78-88, 1852.

[51] F. Scholze, H. Rabus and G. Ulm, "Mean energy required to produce an electron-hole pair in silicon for photons of energies between 50 and 1500 eV," *Journal of Applied Physics*, vol. 84, 5, pp. 2926-2939, Sept. 1998.

[52] F. Scholze, H. Henneken, P. Kuschnerus, H. Rabus, M. Richter and G. Ulm, "Determination of the electron-hole pair creation energy for semiconductors from the spectral responsivity of photodiodes," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 439, 2-3, pp. 208-215, 2000.

[53] R. L. Headrick, B.E. Weir, A.F.J. Levi, D.J. Eaglesham, L.C. Feldman, "Buried, ordered structures: Boron in Si (111) and Si (100)," *Journal of Crystal Growth*, vol. 111, 1-4, pp. 838-842, 1991.

[54] E. F. Schubert, "Delta doping of III–V compound semiconductors: Fundamentals and device applications," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 8, 3, pp. 2980-2996, 1990.

[55] B. E. Weir, L.C. Feldman, D. Monroe, H. J. Grossmann, R. Headrick, T. Hart, "Electrical characterization of an ultrahigh concentration boron delta-doping layer," *Applied Physics Letters*, vol. 65, 6, pp. 737-739, 1994.

[56] B. E. Weir, R. Headrick, Q. Shen, L. C. Feldman, M. Hybertsen, M. Needels, M. Schlüter and T. Hart, "Growth and structural analysis of an ordered boron monolayer in Si (100)," *Physical Review B,* vol. 46, 19, pp. 12861-12864, 1992.

[57] B. S. Meyerson, F. K. LeGoues, T. N. Nguyen, and D. L. Harame, "Nonequilibrium boron doping effects in low-temperature epitaxial silicon films," *Applied Physics Letters*, vol. 50, 2, pp. 113-115, 1987.

[58] R. L. Headrick, B. E. Weir, A. F. J. Levi, B. Freer, J. Bevk, and L. C. Feldman, "Ordered monolayer structures of boron in Si (111) and Si (100)," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 9, 4, pp. 2269-2272, 1991.

[59] R. L. Headrick, B. E. Weir, A. F. J. Levi, D. J. Eaglesham, and L. C. Feldman, "Si (100) - (2x1) boron reconstruction: self-limiting monolayer doping," *Applied Physics Letters*, vol. 57, 26, pp. 2779-2781, 1990.

[60] N. L. Mattey, M. Hopkinson, et al., "P-type delta doping in silicon MBE," *Thin Solid Films,* 184, no. 1-2, pp. 15-19, 1990.

[61] J. Ho, R. Yerushalmi, Z. Jacobson, et al., "Controlled nanoscale doping of semiconductors via molecular monolayers," *Nature Materials*, vol. 7, 1, pp. 62-67, 2007.

[62] G. Lorito, L. Qi, and L. K. Nanver, "Arbitrarily shallow arsenic deposited junctions on silicon tuned by laser annealing," *Proceedings of 10th IEEE International Conference on Solid-State and Integrated Circuit Technology*, pp. 572–574, Shanghai, China, Nov. 1-4, 2010.

[63] L. Qi, G. Lorito and L. K. Nanver, "Lateral-transistor test structures for evaluating the effectiveness of surface doping techniques," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, 4, pp. 581-588, 2012.

[64] M. Popadicć, L. K. Nanver, C. Biasotto, V. Gonda, and J. van der Cingel, "Ultrashallow doping by excimer laser drive-in of RPCVD surface deposited arsenic monolayers", *Proceedings of the 16th IEEE International Conference on Advanced Thermal Processing of Semiconductors,* pp. 141-146, Las Vegas, NV, USA, Sep. 30-Oct. 3, 2008.

[65] L. R. Canfield, J. Kerner, and R. Korde, "Stability and quantum efficiency performance of silicon photodiode detectors in the far ultraviolet," *Applied Optics*, vol. 28, 18, pp. 3940, 1989.

[66] L. Shi et al., "Series resistance optimization of high-sensitivity Si-based VUV photodiodes," *2011 IEEE International Instrumentation and Measurement Technology Conference*, pp. 1-4, Binjiang, China, May 10-12, 2011.

[67] F. Sarubbi, L. K. Nanver and T. L. M. Scholtes, "High effective Gummel number of CVD boron layers in ultrashallow p^+n diode configurations", *IEEE Transactions on Electron Devices*, vol. 57, 6, pp. 1269-1278, 2010.

[68] T. Knežević, T. Suligoj and L. K. Nanver, "Impact of ultra-thin-layer material parameters on the suppression of carrier injection in rectifying junctions formed by interfacial charge layers," *42nd International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, pp. 24-29, Opatija, Croatia, 20-24 May, 2019.

[69] A. Šakic, T. L. M. Scholtes, W. de Boer, N. Golshani, J. Derakhshandeh and L. K. Nanver, "Arsenic-doped high-resistivity-silicon epitaxial layers for integrating low-capacitance diodes," *Materials*, vol. 4, pp. 2092-2107, 2011.

[70] A. Šakić, Nov 28th, 2012, "Silicon technology for integrating high-performance low-energy electron photodiode detector", *Ph.D. dissertation*, Delft University of Technology, Delft, the Netherlands.

[71] D. Grubišić and A. Shah, "New silicon reach-through avalanche photodiodes with enhanced sensitivity in the DUV/UV wavelength range," *36th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, pp. 48-54, Opatija, Croatia, May 20-24, 2013.

[72] "Boron," *Britannica encyclopedia,* https://www.britannica.com/science/boron-chemical-element

[73] M. Vlasse, R. Naslain, J. S. Kasper and K. Ploog, "Crystal structure of tetragonal boron related to α-AlB_{12}," *Journal of Solid State Chemistry*, vol. 28, 3, pp. 289-301, 1979.

[74] A. R. Oganov, J. Chen, C. Gatti, et al., "Ionic high-pressure form of elemental boron," *Nature*, vol. 457, 7231, pp. 863-867, 2009.

[75] A. Polian, S. V. Ovsyannikov, M. Gauthier, et al., "Boron and boron-rich solids at high pressures," *NATO Security through Science Series B: Physics and Biophysics*, vol. 0, pp. 241-249, 2010.

[76] R. G. Delaplane, U. Dahlborg, W. S. Howells and T. Lundström, "A neutron diffraction study of amorphous boron using a pulsed source," *Journal of Non-Crystalline Solids*, vol. 106, 1-3, pp, 66-69, 1988.

[77] H. Davy (1809), *An Account of Some New Analytical Researches on the Nature of Certain Bodies, Particularly the Alkalies, Phosphorus, Sulphur, Carbonaceous Matter, and the Acids Hitherto Undecomposed: with Some General Observations on Chemical Theory*, Philosophical Transactions of the Royal Society of London. 99: 39–104.

[78] J. L. Gay-Lussac and L. J. Thenard, "Sur la décomposition et la recomposition de l'acide boracique," *Annales de Chimie*. vol. 68, pp. 169–174, 1808.

[79] J. Berzelius, "Untersuchungen über die Flußspathsäure und deren merkwürdigste Verbindungen", *Poggendorff's Annalen der Physik und Chemie,* vol. 78, pp. 113-150, 1824.

[80] C. F. Powell, C. J. Ish and J. M. Blocher, "The preparation of high purity boron by hot wire techniques," In: J. A. Kohn, W. F. Nye and G. K. Gaulé (eds.), *Boron Synthesis, Structure, and Properties. Springer, Boston, MA*, pp. 7-14, 1960.

[81] V. I. Matkovich, G. V. Samsonov, P. Hagenmuller, T. Lundstrom (1977), *Boron and Refractory Borides*, Springer-Verlag Berlin Heidelberg.

[82] W. S. Rees Jr. (1996), *CVD of Nonmetals*, Wiley-VCH.

[83] P. Hagenmuller (1972), *Preparative Methods in Solid State Chemistry*, Academic Press.

[84] L. I. Berger (1996), *Semiconductor Materials*, CRC Press.

[85] V. Mohammadi, W. B. de Boer, and L. K. Nanver, "Temperature dependence of chemical-vapor deposition of pure boron layers from diborane," *Applied Physics Letters*, vol. 101, 11, pp. 111906, 2012.

[86] M. Audronis, P. Kelly, A. Leyland, A. Matthews, "A new approach to the deposition of elemental boron and boron-based coatings by pulsed magnetron sputtering of loosely packed boron powder targets," *Plasma Processes and Polymers,* vol. 4, 1, pp. 160-165, 2007.

[87] E. Oks, A. Anders, A. Nikolaev and Y. Yushkov, "Sputtering of pure boron using a magnetron without a radio-frequency supply," *Review of Scientific Instruments,* vol. 88, 4, pp. 043506, 2017.

[88] K. Sato, N. Kanda, T. Ogata and Y. Kumashiro, "Structure of the main precursors and initial decomposition products of diborane chemical vapor deposition: an experimental and ab initio molecular orbital study," *Chemical Physics Letters*, vol. 235, 4, pp. 453-456, 2000.

[89] G. W. Mappes, S. A. Fridmann, and Thomas P. Fehlner, 'The absolute rate of association of borane molecules,' *The Journal of Physical Chemistry*, vol. 74, 18, pp. 3307-3316, 1970.

[90] R. Konecny and D. J. Doren, "Adsorption of BH_3 on Si (100) – (2 × 1)," *The Journal of Physical Chemistry B*, vol. 101, 51, pp. 10983-10985, 1997.

[91] I. Lengyel and K. F. Jensen, "A chemical mechanism for in situ boron doping during silicon chemical vapor deposition," *Thin Solid Films*, vol. 365, 2, pp. 231-241, 2000.

[92] Y. Kiyota and F. Yano, "Role of hydrogen during rapid vapor-phase doping analyzed by x-ray photoelectron spectroscopy and Fourier-transform infrared-attenuated total reflection," *Journal of Vacuum Science & Technology A,* vol. 16, 1, pp. 1-5, 1998.

[93] F. Sarubbi, 18th Jan, 2010, "Characterization of pure boron depositions integrated in silicon diodes for nanometer-deep junction applications", *Ph.D. dissertation*, Delft University of Technology, Delft, the Netherlands.

[94] A. B. Baylis, G. A. Pressley, and F. E. Stafford, "Mass spectrometric investigation of the pyrolysis of boranes. IV. Diborane," *Journal of the American Chemical Society*, vol .88, 11, pp. 2428-2433, 1966.

[95] H. Tseng, F. Pan and C. Chang, “Characterization of boron silicide layer deposited by ultrahigh-vacuum chemical-vapor deposition,” *Journal of Applied Physics*, vol. 80, 9, pp. 5377-5833, 1996.

[96] V. Mohammadi, N. Golshani, K. R. C. Mok, W. B. de Boer, J. Derakhshandehand L. K. Nanver, “Temperature dependency of the kinetics of PureB CVD deposition over patterned Si/SiO_2 surfaces,” *Microelectronic Engineering*, vol. 125, 1, pp. 45-50, 2014.

[97] V. Mohammadi, S. Ramesh and L. K. Nanver, "Thickness evaluation of deposited PureB layers in micro-/millimeter-sized windows to Si," *2014 International Conference on Microelectronic Test Structures (ICMTS),* pp. 194-199, Udine, Italy, Mar. 24-27, 2014.

[98] K. Kamimura, T. Nagaoka, T. Shinomiya, M. Nakao, Y. Onuma and M. Makimura, “Preparation and properties of boron thin films,” Thin Solid Films, vol. 343-344, pp. 342-344, 1999.

[99] Y. Kumashiro, T. Yokoyama and Y. Ando, “Thermoelectric properties of boron and boron phosphide CVD wafers,” *17th International Conference on Thermoelectrics. Proceedings ICT98 (Cat. No.98TH8365),* pp. 591-594, Nagoya, Japan, 28-28 May, 1998.

[100] A. Sammak, 20th Dec, 2012, “Silicon-based integration of groups III, IV, V chemical vapor depositions in high-quality photodiodes”, *Ph.D. dissertation*, Delft University of Technology, Delft, the Netherlands.

[101] MESA+ website, https://mesaplusnanolab.ewi.utwente.nl/mis/MISHomePage.php

[102] T. Knežević, T. Suligoj, X. Liu, L. K. Nanver, et al., “Back-end-of-line CMOS-compatible diode fabrication with pure boron deposition down to 50 °C,” *49th European Solid-State Device Research Conference (ESSDERC*), pp. 242-245, Cracow, Poland, 23-26 Sep. 2019.

[103] A. F. M. Leenaars, J. A. M. Huethorst and J. J. van Oekel, “Marangoni drying: a new extremely clean drying process,” *Langmuir*, vol. 6, pp. 1701 – 1703, 1990.

[104] K. A. Reinhardt and R. F. Reidy, *Handbook for Cleaning for Semiconductor Manufacturing: Fundamentals and Applications*. Hoboken, NJ, USA: Wiley, 2011.

[105] D. Lehmann, F. Seidel, and D. R. T. Zahn, “Thin films with high surface roughness: Thickness and dielectric function analysis using spectroscopic ellipsometry,” *SpringerPlus*, vol. 3, 82, pp. 1-8, 2014.

[106] X. Liu and L. K. Nanver, "Comparing current flows in ultrashallow pn-/Schottky-like diodes with 2-diode test method," *2016 International Conference on Microelectronic Test Structures (ICMTS*), pp. 190-195, Yokohama, Japan, Mar. 28-31, 2016.

[107] X. Liu, S. D. Thammaiah, T. L. M. Scholtes, L. K. Nanver, "Comparison of selective deposition techniques for fabricating p^+n ultrashallow silicon diodes," *Proceedings of ICT.OPEN-2016, Semiconductor Advances for Future Electronics and Sensors (SAFE),* Mar. 21, 2016.

[108] L. K. Nanver, X. Liu and T. Knežević, "Test structures without metal contacts for DC measurement of 2D-materials deposited on silicon," *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS*), pp. 69-74, Austin, TX, USA, Mar. 19-22, 2018.

[109] M. A. Green and J. Shewchun, "Minority carrier effects upon the small signal and steady-state properties of Schottky diodes," *Solid-State Electronics*, vol. 16, 10, pp. 1141-1150, 1973.

[110] G. Gupta, S. D. Thammaiah, L. K. Nanver and R. J. E. Hueting, "Investigation of Pd/MoO_x/n-Si diodes for bipolar transistor and light-emitting device applications," *Journal of Applied Physics,* vol. 128, 5, pp. 055703, 2020.

[111] G. Gupta, S. D. Thammaiah, R. J. E. Hueting and L. K. Nanver, "In search of a hole inversion layer in Pd/MoO_x/Si diodes through I- V characterization using dedicated ring-shaped test structures," *2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)*, pp. 12-17, Kita-Kyushu City, Fukuoka, Japan, Mar. 18-21, 2019.

[112] P. J. Chen, K. Misiakos, A. Neugroschel, and F. A. Lindholm, "Analytical solution for two-dimentional current injection from shallow p-n junctions," *IEEE Trans. Electron Devices*, vol. 32, no. 11, pp. 2292-2296, Nov. 1985.

[113] L. J. van der Pauw, "A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape," *Philips Technical Review*, vol. 20, pp. 220-224, 1958.

[114] S. B. Evseev, L. K. Nanver and S. Milosavljevic, "Ring-gate MOSFET test structures for measuring surface-charge-layer sheet resistance on high-resistivity-silicon substrates," *2006 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, pp. 3-8, Austin, TX, USA, Mar. 6-9, 2006.

[115] A. Sakic et al., "High-efficiency silicon photodiode detector for sub-keV electron microscopy," *IEEE Transactions on Electron Devices*, vol. 59, 10, pp. 2707-2714, 2012.

[116] L. Shi, S. Nihtianov, S. Xia, L. K. Nanver, A. Gottwald, and F. Scholze, "Electrical and optical performance investigation of Si-based ultrashallow-junction p+-n VUV/EUV photodiodes," IEEE Transactions on Instrumentation and Measurement, vol. 61, 5, pp. 1268–1277, 2012.

[117] K. Buisman, L. K. Nanver, T. L. M. Scholtes, H. Schellevis, and L. C. N. de Vreede, "High-performance varactor diodes integrated in a silicon-on-glass technology," *Proceedings of 35th European Solid-State Device Research Conference* (ESSDERC 2005), pp. 117-120, Grenoble, France, Sep. 16, 2005.

[118] L. K. Nanver *et al.*, "Improved RF devices for future adaptive wireless systems using two-sided contacting and AlN cooling," *IEEE Journal of Solid-State Circuits*, vol. 44, 9, pp. 2322–2338, 2009.

[119] K. R. C. Mok, L. Qi, A. H. G. Vlooswijk, and L. K. Nanver, "Self-aligned two-layer metallization with low series resistance for litho-less contacting of large-area photodiodes," *Solid-State Electronics*, vol. 111, pp. 210–217, 2015.

[120] T. Knežević, L. K. Nanver, and T. Suligoj, "Silicon drift detectors with the drift field induced by PureB-coated trenches," *Photonics*, vol. 3, 4, p. 54, 2016.

[121] R. Ghodssi, P. Lin (2011), *MEMS Materials and Processes Handbook*, Springer Science & Business Media.

[122] M. A. Gosalvez, 2003, "Atomistic modeling of anisotropic etching of crystalline silicon", *Ph.D. dissertation,* Helsinki University of Technology, Espoo, Finland.

[123] P. Sullivan, B. W. Offord, M. E. Aklufi, "Tetra-methyl ammonium hydroxide (TMAH) preferential etching for infrared pixel arrays," SPAWAR System Center, pp. 1–13, San Diego, CA, USA, Technical Report 3097, 2000.

[124] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing- Part II," *Journal of Microelectromechanical Systems*, vol. 12, 6, pp. 761–778, 2003.

[125] N. Saitoh, T. Akamine, K. Aoki, and Y. Kojima, "Composition and growth mechanisms of a boron layer formed using the molecular layer doping process," *Japanese Journal of Applied Physics*, vol. 32, 10R, pp. 4404-4407. 1993.

[126] Y. Bogumilowicz, J. M. Hartmann, J. M. Fabri and T. Billon, "Selective chemical vapour etching of $Si_{1-x}Ge_x$ versus Si with gaseous HCl," *Semiconductor Science and Technology*, vol. 21, 12, pp. 1668-1674, 2006.

[127] A. Hikavyy, A. Kruv, T. Van Opstal, B. De Vos, C. Porret and R. Loo, "Investigation of Cl_2 etch in view of extremely low temperature selective epitaxial processes," *Semiconductor Science and Technology*, vol. 32, 11, pp. 114006, 2017.

[128] H. Habuka, H. Tsunoda and T. Otsuka, “Change in microroughness of a silicon surface during in situ cleaning using HF and HCl gases,” *Journal of The Electrochemical Society*, vol. 145, 12, pp. 4264-4271, 1998.

[129] H. Habuka, T. Otsuka and M. Katayama, “In situ cleaning method for silicon surface using hydrogen fluoride gas and hydrogen chloride gas in a hydrogen ambient,” *Journal of Crystal Growth*, vol. 186, 1, pp. 104-112, 1998.

[130] L. K. Nanver, K. Lyon, X. Liu, J. Italiano and J. Huffman, “Material reliability of low-temperature boron deposition for PureB silicon photodiode fabrication,” *MRS Advances*, vol 3, 57-58, pp. 3397-3402, 2018.

[131] K. R. C. Mok, A. H. G. Vlooswijk, et al., “Furnace deposition of PureB layers from B_2H_6 for solar cell applications,” *29th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC)*, Amsterdam, the Netherlands, pp. 863-866, Sep. 22-26, 2014.

[132] R. O. Apaydin, A. J. Onnink, X. Liu, A. A. I. Aarnink, M. P. de Jong, D. J. Gravesteijn, A. Y. Kovalgin, “Comparative study of thermal and radical-enhanced methods for growing boron nitride films from diborane and ammonia,” *Journal of Vacuum Science & Technology* A, vol. 3, 38, pp. 033411, 2020.

[133] S. D. Thammaiah, X. Liu, T. Knežević, K. M. Baternburg, A. A. I. Aarnink, “PureB diode fabrication using physical or chemical vapor deposition methods for increased back-end-of-line accessibility,” *Solid-State Electronics*, pp. 107938, 2020.

[134] E. Steinsland, M. Nese, A. Hanneborg, R. W. Bernstein, H. Sandmo and G. Kittilsland, "Boron etch-stop in TMAH solutions," *Proceedings of the International Solid-State Sensors and Actuators Conference - TRANSDUCERS '95*, pp. 190-193, Stockholm, Sweden, June 25-29, 1995.

[135] R. Charavel and J. P. Raskin, “Tuning of etching rate by implantation: silicon, polysilicon and oxide,” *AIP Conference Proceedings*, vol. 866, 1, 2006.

[136] R. Charavel, J. Laconte, and J. P. Raskin “Advantages of p^{++} polysilicon etch stop layer versus p^{++} silicon,” *Proceedings of SPIE 5116, Smart Sensors, Actuators, and MEMS*, 2003.

[137] Z. A. Piazza, H. Hu, W. Li, J. Li and L. Wang, “Planar hexagonal B_{36} as a potential basis for extended single-atom layer boron sheets,” *Nature Communications,* vol. 5, 1, pp. 1-6, 2014.

[138] R. J. Hamers and Y. Wang, “Atomically-resolved studies of the chemistry and bonding at silicon surfaces,” *Chemical Reviews*, vol. 96, 4, pp. 1261-1290, 1996.

[139] C. W. Ong, K. P. Chik and H. K. Wong, “Properties of a-boron films prepared by low pressure chemical vapour deposition,” *Journal of Non-Crystalline Solids*, vol. 114, 2, 2, pp. 783-785, 1989.

[140] K. Shirai and S. Gonda, “Characterization of hydrogenated amorphous boron films prepared by electron cyclotron resonance plasma chemical vapor deposition method,” *Journal of Applied Physics*, vol. 67, 10, pp. 6286-6291, 1990.

[141] R. Machaka, B. W. Mwakikunga, E. Manikandan, T. E. Derry, I. Sigalas and M. Herrmann, “Mechanical and structural properties of fluorine-ion-implanted boron suboxide,” *Advances in Materials Science and Engineering*, vol. 2012, pp. 1-11, 2012.

[142] A. R. Badzian, “Superhard material comparable in hardness to diamond,” *Applied Physics Letters*, vol. 53, 25, pp. 2495-2497, 1988.

List of Abbreviations and Variables

List of Abbreviations

AFM	atomic force microscopy
Ag	silver
Al	aluminum
ALD	atomic layer deposition
Ar	argon
ArF	argon fluoride
Au	gold
B	boron
BBr_3	boron tribromide
BCl_3	boron trichloride
B_xH_y	boron hydrides
BH_3	borane
B_2H_6	diborane
BHF	buffered HF
BI_3	boron triiodide
BSE	back-scattered electrons
Bi_2Se_3	bismuth selenide
BX_3	boron halides
C	carbon
CMOS	complementary metal oxide semiconductor
Cr	chromium
CVD	chemical vapor deposition
DC	direct current
DUT	deposition under test
DUV	deep ultraviolet
ECR	electron cyclotron resonance
EUV	extreme ultraviolet
FCC	cubic crystal system
H_2	hydrogen
HCl	hydrochloric acid
HF	hydrofluoric acid
HNO_3	nitric acid
HRTEM	high-resolution transmission electron microscopy
IC	integrated circuit
JFET	junction-gate field-effect transistor
KOH	potassium hydroxide
LPCVD	low pressure chemical vapor deposition

MBE	molecular beam epitaxy
MEMS	micro-electromechanical systems
MLD	monolayer doping
MOS	metal-oxide-semiconductor
MoS_2	molybdenum disulfide
N_2	nitrogen
NICM	Nomarski interference contrast microscopy
O_2	oxygen
PECVD	plasma-enhanced chemical vapor deposition
PVD	physical vapor deposition
RAPD	reach-through avalanche photodiode
RF	radio frequency
RP	reduced pressure
LSRL	Lawrence Semiconductor Research Laboratory
RT	room temperature
RTA	rapid thermal annealing
SBH	Schottky barrier height
SE	spectroscopic ellipsometry
SEG	selective-epitaxial-growth
SEM	scanning electron microscopy
Si	silicon
SiC	silicon carbide
SiGe	silicon-germanium
SIMS	secondary ion mass spectrometry
SiN	silicon nitride
SiO_2	silicon dioxide
Ta	tantalum
TEM	transmission electron microscopy
TEOS	SiO_2 made out of tetraethyl orthosilicate
Ti	titanium
TCAD	technology computer-aided design
TMAH	tetramethylammonium hydroxide
ULPCVD	ultra low-pressure chemical vapor deposition
XPS	X-ray photoelectron spectroscopy

List of Variables

J_e	electron current density
R_{sh}	sheet resistance
I_s	saturation current
$I_{g\text{-}r}$	generation current
k	Boltzman's constant
q	elementary charge
R_s	series resistance
T	temperature
W	depletion width
I_D	diode current
V_D	diode voltage
A	diode area
n	ideality factor
D_n	diffusion coefficients of electrons
D_p	diffusion coefficients of holes
n_i	intrinsic carrier concentration
W_p	width of p-type region
W_n	width of n-type region
N_A	acceptor concentration
N_D	donor concentration
L_n	diffusion length of electrons
L_p	diffusion length of holes
G_A	Gummel number of p-region
G_D	Gummel number of n-region
I_0	incident light intensity
I_l	transmitted light intensity
k_l	absorption coefficient
l	thickness of the absorbing medium
I_e	electron current
I_h	hole current
I_C	collector current
I_B	base current
G_E	Gummel number of emitter
G_B	Gummel number of base
S_A	surface recombination velocity at the metal interface
W_{QNA}	total width of p-region
W_{PureB}	width of B layer
W_{BxSiy}	width of B and Si mixture layer at the B-Si interface
$W_{c\text{-}Si}$	width of B-doped crystalline Si
n_{ie}	effective intrinsic carrier concentration

ΔE_G	bandgap difference with respect to c-Si
Ψ	reflectivity ratio
Δ	phase difference
k_E	extinction coefficient
n_R	refractive index
T_s	substrate temperature
I_E	emitter current
I_C	collector current
I_B	base current
$I_{E//C}$	current flow through the emitter when both the emitter and collector are connected and biased in forward
ΔI_E	difference of emitter current with and w/o collector connected and biased
N_{sub}	substrate doping concentration
A_E	emitter area
P_E	on-mask perimeter of emitter
J_P	perimeter current density
I_{leak}	leakage current
J_A	area current density
J_E	emitter current density
I_{SE}	emitter saturation current
$I_{SE//C}$	saturation current of emitter when both the emitter and collector are connected and biased in forward
J_{PE}	perimeter current density of emitter
$J_{PE//C}$	current density of emitter when both the emitter and collector are connected and biased in forward
r_g	ring structure radius
P	ring structure total perimeter
L	width of the ring structure
R_{mij}	measured resistance between two contacts in ring structure
α_{ij}^{edge}	radial correction factor
I_{dDUT}	ring structure diode current with guard ring and the test region is deposited with B
I_{dp+}	ring structure diode current where the test region is heavily implanted
I_{eDUT}	electron current of ring structure diode with guard ring and the test region is deposited with B
σ	residual stress
E_s	Young's modulus for silicon
v_s	Poisson's ratio for silicon

t_f	film thickness
t_s	substrate thickness
d_{sc}	scan length
∂_c	curvature difference of the substrate as measured with and without the B layer
δ	lateral undercut
N_I	fixed negative interface charge
I_{Se}	saturation current density for electrons
I_{Sh}	saturation current density for holes
t_{PB}	boron layer thickness

Summary

In this thesis, the research on silicon-based PureB technology was extended from the original work performed by depositing pure boron in a state-of-the-art commercial Si/SiGe ASM Epsilon epitaxy system, to other deposition methods and less optimal deposition conditions. This included lower substrate temperatures, much faster deposition rates, and higher susceptibility to oxygen contamination. To study the effects on the B-layer and PureB diode properties, several electrical characterization and chemical analysis techniques were developed to evaluate the usability of the as-deposited B-layers. In addition, the B-layer was established to be attractive both as a masking layer for Si anisotropic etching and as a membrane material.

The properties of PureB diodes are discussed in relationship to the behavior of conventional diffused p-n diodes and their application as photodiodes. PureB diodes with a nanometer-thin pure B layer as the anode region on n-type Si, were in the past shown to have deep-junction-like *I-V* characteristics. The physical model proposed to explain this behavior was that a high density of acceptor states is formed at B-Si interface. These fill with negative charge that attracts an inversion layer of holes and this interfacial hole layer functions in the same manner as would be expected for a B-doped p^+-region. While this interface bonding is largely responsible for the electrical characteristics, the capping layer of bulk B provides a robust protection of the interface.

In the past, the 400°C and 700°C chemical-vapor deposition (CVD) of B in the Epsilon was given most attention, the latter being electrically and chemically very robust and former having the advantage of being back-end CMOS compatible. Both displayed *I-V* characteristics that were similar to conventional deep diffused p^+n junction diodes. In this thesis, B-deposition in three other ways was investigated. CVD was performed in the Picosun ALD system using 5% B_2H_6 in Ar, where in-situ growth monitoring was possible. Batch furnace low-pressure and ultra-low-pressure CVD systems (LPCVD and ULPCVD) systems were compared. These systems allowed deposition temperatures down to about 200°C. For room-temperature deposition a molecular-beam-epitaxy (MBE) system was used with the advantage that the layer thickness was independent of the substrate temperature. The B-layer

thickness and uniformity, as the key parameter in this research, was monitored by ellipsometry.

In Chapter 3, several electrical test structures were developed to study the current flow in PureB diodes with respect to different fabrication procedures. Vertical pnp transistors with emitter regions made with PureB diodes are ideal for measuring the electron injection into the B-region but demand several diffused regions. Lateral pnp's with emitter and collector region made with PureB diodes much more are straightforward to process but parasitic base current prevents the extraction of the electron injection into the B-regions. A 2-diode measurement technique making use of the lateral pnp structures, was studied. It made use of the interaction of hole currents spreading into the substrate to help distinguish whether the diodes were pn-like or Schottky-like. These transistor test structures had Al-metallization of the contacts, which for thin B-layers sometimes degraded the interface that was important for the PureB diode characteristics. Therefore, to enable an electrical evaluation of the as-deposited B-layers, non-metallized test structures were developed, making use of implanted p^+ regions to contact the B-layer. Test structures for measuring the sheet resistance, R_{sh}, along the B-Si interface were used to evaluate the degree to which the electrically active B-Si bonds were created. A method was also found for extracting the electron injection, I_e, into PureB regions fabricated at low temperatures where it became comparable to the hole injection, I_h, into the n-substrate.

Chapter 4 introduced the B-layer as masking layer for wet anisotropic Si etching in TMAH or KOH. The etch rate in these etchants was also used to evaluate the compactness and integrity of the B-layer. For Epsilon B-layers deposited at 400°C or 700°C, layers as thin as 2nm were resistant to the Si etchants, but some pre-depositions treatments were found to weaken the integrity of the layers in this respect. For example, 400°C B-deposition on implanted p^+-regions the Si under the B-layer was attacked by the etchants. The appearance of separated cavities after exposure to an etchant suggested that isolated weak spots were present in the B-layers. Among several 1 nm 400°C B-layers, cavities on non-implanted region were found in one sample after 6 min TMAH etch at 65 °C. The density of these small pyramid-shape cavities was too low to lead to a connected fully-etch surface area, meaning at 400°C the coverage was almost complete after deposition of first few atom layers. The B-layers were found to be effectively etched by standard Al etchant, so patterning with photoresist was possible. After long-time Si etching on patterned B samples, a very low lateral undercut was observed,

demonstrating a good adhesion of B and Si. B-membranes were left across the corners cavities etched through circular openings in B-masks. The topography of these B-membranes, as observed by optical microscopy, revealed that the stress in the membranes varied a lot depending on deposition conditions.

In Chapter 5, a number of B-depositions from 450°C down to room temperature were studied using the electrical characterization techniques and etch tests developed in Chapter 3 and 4. The Si surface cleaning before deposition was shown to be crucial for establishing the desired B-Si bonding at the interface. The most reliable cleaning method was found to be the traditional native oxide removal by HF dip-etching. Several extra cleaning treatments were investigated with the purpose of guaranteeing the free oxide surface, such as exposure to high-temperature H_2 annealing or vapor HCl. However, these extra steps appeared to have a negative impact on the perfection of Si surface. Moreover, in the Epsilon it was found that keeping the substrate in the load-lock for N_2 purging could reduce the oxygen/moist brought into the system and significantly lower the oxygen incorporation in the layer during the deposition. Post-deposition annealing at higher temperatures also improved the electrical properties by doping the Si with B.

B-layer depositions under 450°C were performed in the Picosun, the ULPCVD furnace and the MBE system. In the Picosun, depositions from 450°C to 200°C were performed, and the growth of the layers showed a supposedly self-limiting behavior with the 250°C B-layer thickness measured to be 1 nm to 1.5 nm by in-situ ellipsometry. The presence of a B-coverage at 200°C and 250°C was confirmed by SIMS, and B-concentration was higher at 250°C. The 250°C B-layer gave I_e and R_{sh} values close to those of 400°C PureB diodes while the 200°C layers gave a very high R_{sh}. Adding a 400°C deposition brought the sheet resistance of the 200°C sample down to the same order with 400°C while the 250°C sample was not significantly changed, showing that the potential B-Si bonding at these low temperatures is about the same. MBE PureB diodes with ~ 2-nm-thick B-layers were made with deposition temperatures from 50°C to 400°C. The electrical results were similar to the CVD layers except for the very low temperature MBE B-depositions at 200°C and 50°C that had a much higher gave I_e and R_{sh} values.

The furnace ULPCVD system enabled batch processing, but with the disadvantage that the selectivity and thickness control of thin layers was poor. A 10 nm deposition on Si was already enough to grow an electrically

connected layer on oxide. The back-etching of the B-layers in Al etchant was investigated as a means of chemically thinning the layers. Even after extensive etching, the Al etchant could not completely remove B atoms on Si. SIMS analysis showed that for low temperature deposition without bulk doping, the number of B atoms left after extensive etching was about a decade less than expected for a complete monolayer. Hence, oxidation of the etched samples was imminent and high I_e and R_{sh} were found.

As discussed in Chapter 6, B-layer research in other groups had led to the realization that these layers had a transmissivity and emissivity that made them potentially suitable for use in EUV pellicles. If stand-alone B-membranes were to be applied, the requirements on the robustness and flatness of the membrane would be high. Several B-deposition conditions were studied with this in mind. At 400°C the Picosun layers were slightly tensile and several millimeter large membranes, tens-of-nanometer to a micrometer in thickness were successfully fabricated. The B-layers grown in the Epsilon from 400°C to 700°C were characterized by compressive stress that approached zero at about 600 °C. The Picosun B-layers grown from 300°C to 500°C had tensile stress that decreased with temperature to values so low that at 300°C they were not measurable. This tensile stress increased as the deposition temperature and/or rate increased. With respect to the masking of TMAH Si etching, all layers were suitable. However, while the Epsilon B-layers gave sufficient protection when only a few nm thick, the low-temperature Picosun B-layers needed to be thicker due their low compactness and more susceptibility to Si surface contamination. With a Picosun deposition at 400°C, a 60-nm-thick B-membrane, 7×7 mm^2 in size, was made by through-wafer etching. These thick layers were, however, more prone to break spontaneously or to be very fragile. This was particularly true B-layers grown in the ULPCVD furnace, and if the deposition rate was high. There were also indications that it could be beneficial for the strength of the membrane to intentionally introduce a bit of oxygen contamination. In this way a 1-µm-thick B-membrane with an area of 3×3 mm^2 was successfully demonstrated.

Samenvatting

In dit proefschrift wordt het onderzoek naar silicium (Si) gebaseerde pure boor (PureB) technologie uitgebreid ten opzichte van het originele werk waarbij PureB was gedeponeerd in een state-of-the-art commercieel Si/SiGe ASM Epsilon epitaxie systeem: andere depositie methodes, ook onder minder optimale depositie omstandigheden, worden bestudeerd. Dit omvat lagere substraattemperaturen, aanzienlijk snellere depositiesnelheden en een hogere gevoeligheid voor zuurstofverontreiniging. Om de effecten op de B-laag en de eigenschappen van de PureB diode te onderzoeken, zijn er verschillende elektrische karakteriseringtechnieken en chemische analysetechnieken ontwikkeld om de bruikbaarheid van de gedeponeerde B-lagen te evalueren. Daarnaast is vastgesteld dat de B-laag aantrekkelijk is als zowel een maskeerlaag voor het anisotropisch etsen van Si, als een membraan materiaal.

De eigenschappen van PureB diodes worden bestudeerd en gerelateerd aan het gedrag van conventionele gediffundeerde p-n diodes en de toepassing als fotodiodes. In het verleden is aangetoond dat PureB diodes met een nanometer-dikke PureB laag als anode materiaal op n-type Si, vergelijkbare stroom-spanning (*I-V*) karakteristieken hebben als diepe juncties. Het voorgestelde fysische model om dit gedrag te verklaren is dat een hoge dichtheid van acceptor toestanden wordt gevormd aan het B-Si raakvlak. Deze vormen negatieve lading dat vervolgens een gaten inversielaag aantrekt. Deze inversielaag van gaten functioneert zoals dat verwacht kan worden van een B-gedoteerde p^+-gebied. Hoewel de raakvlakverbindingen grotendeels verantwoordelijk zijn voor de elektrische eigenschappen, zorgt de afdeklaag van bulk B voor een robuuste bescherming van het raakvlak.

In het verleden is de meeste aandacht uitgegaan naar de 400°C en 700°C Chemical-Vapor Deposition (CVD) van B in de Epsilon reactor, waarbij de laatste elektrisch en chemisch zeer robuust is en de eerste het voordeel heeft dat het back-end CMOS-compatibel is. Beiden vertoonden *I-V* karakteristieken vergelijkbaar met die van conventionele diep gediffundeerde p^+n junctie diodes. In dit proefschrift zijn drie andere manieren van B-deposities onderzocht. CVD is uitgevoerd in het Picosun atomaire laagdepositie (ALD) systeem met 5% diboraan (B_2H_6) in argon (Ar), met in-situ groeimonitoring mogelijkheden. Aansluitend zijn lagedruk en ultra-lagedruk batch-oven CVD-systemen (LPCVD en ULPCVD) vergeleken.

Deze systemen maken depositietemperaturen tot ongeveer 200°C mogelijk. Voor kamertemperatuur deposities is een Molecular-Beam-Epitaxy (MBE) systeem gebruikt, met als voordeel dat de laagdikte onafhankelijk is van de substraattemperatuur. De B-laagdikte en uniformiteit, de belangrijkste parameters in dit onderzoek, zijn gemonitord met ellipsometrie.

In Hoofdstuk 4 zijn verschillende elektrische teststructuren ontwikkeld om de stroom te bestuderen in PureB diodes uit verschillende fabricageprocessen. Verticale pnp transistoren met PureB diodes als emittergebieden zijn ideaal voor het meten van de elektroneninjectie in het B-gebied, maar vereisen meerdere gediffundeerde gebieden. Laterale pnp's met PureB diodes in zowel emitter als collector gebieden zijn gemakkelijker te fabriceren, maar een parasitaire basisstroom verhindert de extractie van de elektroneninjectie in de B-gebieden. Een 2-diode meting waarbij gebruik wordt gemaakt van de laterale pnp structuren werd onderzocht. Het maakt gebruik van de interactie tussen gatenstromen die zich spreiden in het substraat om te onderscheiden of de diodes pn-achtig of Schottky-achtig zijn. Deze transistor teststructuren hadden aluminium (Al)-gemetalliseerde contacten. Dergelijke contacten kunnen soms het raakvlak bij dunne B-lagen aantasten, wat belangrijk is voor de PureB diode eigenschappen. Om desondanks toch de B-lagen elektrisch te karakteriseren, zijn er niet-gemetalliseerde teststructuren ontwikkeld die gebruik maken van geïmplanteerde p^+ gebieden voor het contacteren van de B-laag. Teststructuren om de vierkantsweerstand R_{sh} te meten langs het B-Si oppervlak zijn gebruikt om te bepalen in hoeverre de elektrisch actieve B-Si bindingen aanwezig zijn. Bovendien is er een methode gevonden om de elektroninjectie, I_e, te extraheren in PureB gebieden van diodes die geproduceerd zijn op lage temperaturen, waar de injectie vergelijkbaar wordt met de gateninjectie, I_h, in het n-substraat.

Hoofdstuk 4 introduceerde de B-laag als maskeerlaag voor nat anisotropisch Si etsen in TMAH of KOH. De etssnelheid in deze etsmiddelen is ook gebruikt om de compactheid en integriteit van de B-laag te bestuderen. Voor Epsilon B-lagen gedeponeerd bij 400°C of 700°C, waren lagen zo dun als 2 nm bestand tegen de Si etsmiddelen, maar enkele pre-depositiebehandelingen bleken de integriteit van de lagen aan te tasten. Voor bijvoorbeeld een 400°C B-depositie op geïmplanteerde p^+ gebieden, werd het Si onder de B-laag aangetast door het etsmiddel. De aanwezigheid van afgezonderde uitsparingen in het Si na blootstelling aan een etsmiddel suggereert dat geïsoleerde zwakke plekken aanwezig zijn in de B-laag. Onder

verschillende 1-nm 400°C B-lagen zijn er slechts op één monster uitsparingen aangetroffen op niet-geïmplanteerde gebieden na een 6 min TMAH-ets op 65°C. De dichtheid van deze kleine piramidevormige uitsparingen was zo laag dat een verbonden uitsparing van het oppervlak niet kon vormen, wat betekent dat de dekking bij 400°C bijna volledig was na de depositie van een paar atoomlagen. De B-lagen blijken efficiënt geëtst te worden door een standaard Al etsmiddel, dus patronen aanbrengen met fotoresist is mogelijk. Na een langdurige Si ets op B monsters met patronen, was er een zeer kleine laterale onderets zichtbaar, wat een goede adhesie van B op Si aantoont. B-membranen bleven staan op de hoeken van uitsparingen geëtst door cirkelvormige openingen in de B-maskers. De topografie van deze B-membranen, waargenomen met optische microscopie, onthult dat de spanning in de membranen sterk varieert afhankelijk van de depositieomstandigheden.

In Hoofdstuk 5 zijn een aantal B-deposities van 450°C tot kamertemperatuur bestudeerd met behulp van de elektrische karakterisatietechnieken en etstesten ontwikkeld in Hoofdstukken 3 en 4. Het is aangetoond dat de Si oppervlakreiniging vóór depositie cruciaal is voor het creëren van de gewenste B-Si bindingen op het raakvlak. De meest betrouwbare schoonmaakmethode blijkt het traditionele korte etsen te zijn in fluorwaterstofzuur (HF) voor het verwijderen van het natuurlijk gevormde oxide. Andere schoonmaakmethoden zijn onderzocht met als doel een oxide-vrij oppervlak te garanderen. Voorbeelden hiervan zijn blootstelling aan waterstof (H_2) onder hoge temperaturen of aan zoutzuur (HCl) damp. Deze extra stappen blijken echter een negatieve invloed te hebben op de kwaliteit van het Si oppervlak. Bovendien bleek dat door het substraat in de laadsluis van de Epsilon reactor te houden voor een stikstof (N_2) behandeling, de hoeveelheid zuurstof/vochtigheid dat in het systeem gebracht wordt verminderd werd. Dit verlaagt de hoeveelheid zuurstof dat wordt opgenomen in de laag tijdens de depositie aanzienlijk. Post-depositie gloeien op hogere temperaturen verbeterde de elektrische eigenschappen dankzij B dotering van het Si.

B-laag deposities lager dan 450°C zijn uitgevoerd in de Picosun, de ULPCVD-oven, en het MBE-systeem. In de Picosun zijn deposities uitgevoerd van 450°C tot 200°, waarbij de groei van de lagen een vermoedelijk zelflimiterend gedrag is waargenomen. De dikte van de 250°C laag is vastgesteld op 1 nm tot 1.5 nm met in-situ ellipsometrie. De aanwezigheid van een B-dekking bij 200°C en 250°C is bevestigd door secundaire ion massaspectrometrie (SIMS), waarbij de B-concentratie hoger

was bij 250°C. De 250°C laag gaf een I_e en R_{sh} dicht bij de waardes van 400°C PureB diodes, terwijl de 200°C lagen een aanzienlijk hogere R_{sh} hadden. Een extra 400°C depositie bracht de vierkantsweerstand van de 200°C lagen terug tot waardes in de buurt van de 400°C PureB diodes, de waardes van de 250°C lagen daarentegen vertoonden geen aanzienlijke verandering. Dit toont aan dat de elektrisch actieve B-Si bindingen op deze lage temperaturen ongeveer gelijk zijn. MBE PureB diodes met ~2 nm dikke B-lagen zijn gemaakt met depositietemperaturen van 50°C tot 400°C. De elektrische resultaten zijn vergelijkbaar met die van diodes gerealiseerd met CVD lagen, maar de lage MBE B-depositie temperaturen van 200°C en 50°C gaven hogere I_e en R_{sh} waardes.

Het ULPCVD-oven systeem maakt batchverwerking mogelijk, maar heeft het nadeel dat de selectiviteit en controle over de dikte van dunne lagen slecht is. Een 10 nm depositie op Si was al genoeg om een elektrische verbonden laag te groeien op oxide. Het terugetsen van de B-lagen in Al etsmiddel is onderzocht als een manier om de dikte van de lagen chemisch te verminderen. Zelfs na lang etsen, was het Al etsmiddel niet in staat om alle B atomen te verwijderen van het Si. SIMS-analyse laat zien dat voor deposities op lage temperatuur zonder bulk dotering, het aantal overgebleven B atomen na lang etsen ongeveer tien keer lager was dan verwacht voor een volledige monolaag. Hierdoor is oxidatie van de geëtste structuren onvermijdelijk, en zijn er hoge waarden voor I_e en R_{sh} geconstateerd.

Zoals beschreven in hoofdstuk 6, heeft onderzoek naar B-lagen in andere groepen geleid tot het besef dat de doorlaatbaarheid en emissiviteit van deze lagen mogelijk geschikt zijn voor gebruik als EUV pellicles. Als op zichzelf staande B-membranen hiervoor toegepast zouden worden, zouden de vereisten hoog zijn met betrekking tot de robuustheid en vlakheid. Met dit in het achterhoofd zijn verschillende B-deposities bestudeerd. Bij 400°C waren de Picosun lagen enigszins onder trekspanning en zijn er verschillende membranen van millimeters groot gefabriceerd, met diktes variërend van tientallen nanometers tot een micrometer. De B-lagen gegroeid in de Epsilon van 400°C tot 700°C waren onder drukspanning, die nul benaderde rond 600°C. De Picosun B-lagen gegroeid van 300°C tot 500°C hadden een trekspanning die afnam met de temperatuur tot onmeetbaar kleine waardes rond 300°C. Deze trekspanning neemt toe als functie van depositietemperatuur en/of snelheid. Met betrekking tot de maskering van TMAH Si etsen waren alle lagen geschikt. Hoewel de Epsilon B-lagen voldoende bescherming boden met een dikte van een paar nanometer,

moesten de lage temperatuur Picosun B-lagen dikker zijn vanwege hun lage compactheid en gevoeligheid voor Si oppervlaktevervuiling. Met een Picosun depositie bij 400°C is een 60-nm dik B-membraan, van 7×7mm^2 groot, gefabriceerd door gebruik te maken van het etsen door de hele plak. Deze dikke lagen waren echter vatbaarder, kon spontaan breken of waren erg fragiel. Dit was vooral het geval voor B-lagen gegroeid in de ULPCVD-oven en wanneer de depositiesnelheid hoog was. Ook zijn er aanwijzingen dat het voor de sterkte van het membraan gunstig is om bewust een beetje zuurstofvervuiling te introduceren. Op deze manier is een 1-µm dik B-membraan met een oppervlakte van 3×3 mm^2 succesvol gedemonstreerd.

List of Publications

Journals

- L. K. Nanver, T. Knežević, **X. Liu**, S. D. Thammaiah, M. Krakers, "On the many application of nanometer-thin pure boron layers in IC and MEMS technology," *Journal of Nanoscience and Nanotechnology*, vol. 21, 4, pp. 1-11, 2021. https://doi.org/10.1166/jnn.2021.19112
- S. D. Thammaiah, **X. Liu**, T. Knežević, K. M. Baternburg, A. A. I. Aarnink, "PureB diode fabrication using physical or chemical vapor deposition methods for increased back-end-of-line accessibility," *Solid-State Electronics*, pp. 107938, 2020. https://doi.org/10.1016/j.sse.2020.107938
- R. O. Apaydin, A. J. Onnink, **X. Liu**, A. A. I. Aarnink, M. P. de Jong, D. J. Gravesteijn, A. Y. Kovalgin, "Comparative study of thermal and radical-enhanced methods for growing boron nitride films from diborane and ammonia," *Journal of Vacuum Science & Technology* A, vol. 3, 38, pp. 033411, 2020. https://doi.org/10.1116/6.0000132
- **X. Liu**, J. Italiano, R. Scott and L. K. Nanver, "Silicon micromachining with nanometer-thin boron masking and membrane material", Material Research Express, vol. 6, 11, pp. 116438, 2019.
- T. Knežević, **X. Liu**, E. Hardeveld, T. Suligoj, and L. K. Nanver, "Limits on thinning of boron layers with/without metal contacting in PureB Si (photo)diodes," *IEEE Electron Device Letters*, vol. 40, 6, pp. 858–861, 2019. https://doi.org/10.1109/LED.2019.2910465
- L. K. Nanver, K. Lyon, **X. Liu**, J. Italiano and J. Huffman, "Material reliability of low-temperature boron deposition for PureB silicon photodiode fabrication," *MRS Advances*, vol 3, 57-58, pp. 3397-3402, 2018. https://doi.org/10.1557/adv.2018.506
- **X. Liu**, L. K. Nanver and T. L. M. Scholtes, "Nanometer-thin pure boron layers as mask for silicon micromachining", *Journal of Microelectromechanical Systems*, vol. 26, 6, pp. 1428–1434, 2017. https://doi.org/10.1109/JMEMS.2017.2764322
- L. K. Nanver, L. Qi, **X. Liu**, T. Knežević, "Nanolayer boron-semiconductor interfaces and their device applications," Solid-State Electronics, vol. 186, pp. 108041, 2021.

Conferences

- T. Knežević, T. Suligoj, **X. Liu**, L. K. Nanver, et al., "Back-end-of-line CMOS-compatible diode fabrication with pure boron deposition down to 50 °C," *49th European Solid-State Device Research Conference (ESSDERC*), pp. 242-245, Cracow, Poland, Sep. 23-26, 2019. https://doi.org/10.1109/ESSDERC.2019.8901810
- L. K. Nanver, **X. Liu** and T. Knežević, "Test structures without metal contacts for DC measurement of 2D-materials deposited on silicon," *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS*), pp. 69-74, Austin, TX, USA, Mar. 19-22, 2018. https://doi.org/10.1109/ICMTS.2018.8383767
- **X. Liu** and L. K. Nanver, "Comparing current flows in ultrashallow pn-/Schottky-like diodes with 2-diode test method," *2016 International Conference on Microelectronic Test Structures (ICMTS*), pp. 190 - 195, Yokohama, Japan, Mar. 28 - 31, 2016. https://doi.org/10.1109/ICMTS.2016.7476205

Workshops

- **X. Liu**, S. D. Thammaiah, T. L. M. Scholtes, L. K. Nanver, "Comparison of selective deposition techniques for fabricating p^+n ultrashallow silicon diodes," *Proceedings of ICT.OPEN-2016, Semiconductor Advances for Future Electronics and Sensors (SAFE),* Mar. 21, 2016.
- **X. Liu,** R. O. Apaydin, S. Banerjee, A. A. I. Aarnink, A. Y. Kovalgin and L. K. Nanver, "Electrical measurement of the conductance along the interface of negatively-charged CVD/ALD depositions on silicon," EuroCVD 21 – Baltic ALD 15, Linköping, Sweden, June 11–14, 2017.
- **X. Liu,** A. A. I. Aarnink, K. M. Baternburg and L. K. Nanver, "Low temperature CVD pure boron layers for Si micromachining," EuroCVD 22 – Baltic ALD 16, Luxembourg, June 24-28, 2019.

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