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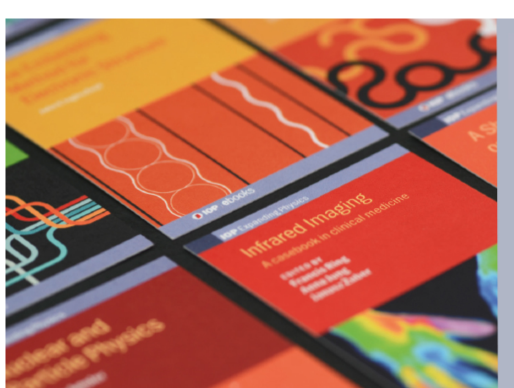

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Sacrificial grid release technology: a versatile release concept for MEMS structures

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Abstract

Micro-electro-mechanical-systems (MEMS) structures with different in-plane dimensions often need to be released simultaneously from the bulk of the wafer and a single dry etching or wet etching technique cannot fulfill all release requirements. In this paper we present a universally applicable solution to release MEMS structures with different surface areas in a controlled and uniform way, which combines isotropic etching of a sacrificial silicon support structure by xenon difluoride with a predefined etch surface made by deep reactive ion etching. Two applications of this Sacrificial Grid Release Technology are presented, in which MEMS devices are released in silicon-on-insulator wafers. The demonstrated applications involve the release of microstructures with in-plane dimensions ranging from tens of micrometers to a few millimeters. The sacrificial silicon structure provides mechanical support which allows freedom in process flow design for fragile MEMS structures. The release technique can also be used to separate the chips from the wafer.

Keywords: sacrificial grid release technology, free-hanging MEMS structures, sacrificial grid structures, release etch

(Some figures may appear in colour only in the online journal)

1. Introduction

Most micro-electro-mechanical-systems (MEMS) devices contain structures that need to be released from the bulk substrate, e.g. for thermal isolation [1] or to allow for mechanical movement [2]. Often, MEMS structures with different in-plane dimensions need to be released from the backside simultaneously, as indicated in figure 1(d). Backside release poses the least amount of restrictions on the MEMS structures, however, this requires that large and small cavities all should reach the same depth.

Backside release processes make use of bulk silicon micromachining techniques including wet chemical etching, such as potassium hydroxide (KOH) etching, plasma etching, such as reactive ion etching (RIE) and deep reactive ion etching (DRIE) using sulfur hexafluoride (SF_6), and gas or vapor phase chemical etching using e.g. xenon difluoride (XeF_2) [3]. Wet chemical etching is severely limited by the risk of stiction due to capillary forces [4–8] and results in relatively large openings at the backside of the wafer.

Plasma, gas, and vapor phase etching techniques also have limitations when used individually. RIE can be used to release larger MEMS structures isotropically, but, similar to wet etching, through-wafer release from the backside of the wafer will result in large areas of semi-circular sideway under-cuts. DRIE can be used to create directional release profiles such as holes or trenches with tunable aspect-ratios [9]. However, there are several practical problems when only DRIE is used: (1) wafer clamping and helium backside cooling are required during processing and gives pressure differences across the wafer, which might damage fragile structures on the wafer, (2) the helium backside cooling cannot be used if the MEMS

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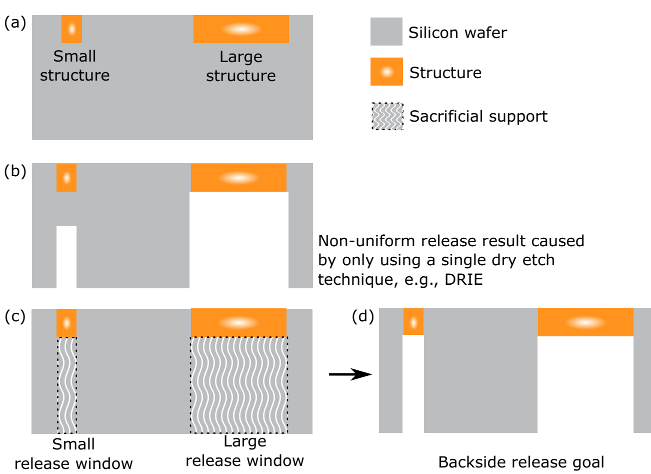

Figure 1. Schematic cross-sectional view of (a) a silicon wafer that contains both large and small structures. (b) Using a single etch technique like DRIE, the small structure is not released or requires significant over etching due to the different sizes of the release openings. (c) Employing a sacrificial silicon structure provides mechanical support during processing wafer with large or fragile structures, and (d) eventually achieving the goal of releasing both large and small structures from the backside of the wafer simultaneously.

Table 1. XactiX XeF_2 pulsed isotropic etching recipe (XeF_2 pressure* is the expansion chamber pressure).

	Setting
Temperature expansion chamber	40 °C
Temperature etch chamber	35 °C
Base pressure	0.3 Torr
Loading/unloading	3 purges with nitrogen
XeF_2 pressure*	5 Torr
Etch time	10 s
Number of cycles	Depend on the grid design

structures result in openings through the entire wafer, and (3) the etch rate of DRIE depends on the release window sizes due to the RIE-lag effect [9], as illustrated in figure 1(b). XeF_2 is an isotropic silicon etchant which does not require wafer clamping or helium cooling. XeF_2 has high selectivity for silicon over other commonly used MEMS materials such as silicon dioxide (SiO_2) and silicon nitride (Si_xN_y) [10]. However, etching silicon with XeF_2 is a surface-area controlled process and has etch rates depending on the mask openings [10], which complicates the release of MEMS structures of different sizes.

This problem can be avoided by first creating sacrificial structures with specific patterns and subsequently removing these sacrificial structures to achieve accurate control over the etch profile. SiO_2 is often used as the sacrificial material and removed by hydrogen fluoride (HF). For example in [11], high aspect ratio kinoform silicon x-ray lenses were fabricated by DRIE using the Bosch process. However, the optical performance is highly sensitive to tapering and bowing of the sidewall profiles if only DRIE is used. In order to gain accurate control over the vertical profile, high aspect-ratio sacrificial silicon pillars and walls were first etched using DRIE and followed by thermal oxidation and removal in buffered HF.

In another example [12], hermetic packaging of silicon MEMS devices often creates ultra-clean and low-pressure cavities following the epi-seal process. Gaps in silicon are etched by DRIE, then filled with SiO_2 using low pressure chemical vapor deposition (LPCVD) or pressure-enhanced chemical vapor deposition (PECVD). After the deposition of poly-crystalline silicon (poly-Si), the sacrificial SiO_2 is eventually removed by vapor HF. However, refilling the relatively wide gaps with SiO_2 suffers from stresses accumulated from multiple cycles of LPCVD or the non-conformal profile of PECVD. Chen *et al* [12] adjusted the epi-seal process so that deep trenches were etched using DRIE and refilled with SiO_2 using LPCVD along the edges of the desired wide gap locations. The silicon between the SiO_2 beams was removed by XeF_2 to create wide gaps. Eventually, after poly Si final sealing, the sacrificial SiO_2 beams were removed by vapor HF.

However, in both of these examples [11, 12], the creation of sacrificial SiO_2 requires a high temperature oxidation or deposition process which is not universally applicable, for example when temperature sensitive elements are present on the wafer. Therefore, a release process that does not require a high temperature oxidation or deposition step is preferred. In [13], silicon was used as the sacrificial material to release large (3 mm by 3 mm) thin film aluminum mirrors. A backside release mask with circular stripe patterns was used during Bosch-based DRIE to obtain high aspect ratio trenches underneath the mirror. The sacrificial silicon beams were subsequently removed by isotropic SF_6 etching. However, as mentioned earlier, in the Bosch-based DRIE process, SF_6 plasma etching requires wafer clamping and backside helium cooling, which might damage fragile MEMS structures.

In this paper, as an extension to the method reported in [13], we propose a universal release method called Sacrificial Grid Release Technology (SGRT). Different from the circular stripe-shaped mask, we designed a mask layout with a regular grid pattern. With that, a uniform etch depth over the wafer is obtained by directional DRIE. Subsequently, other than the isotropic enchant SF_6 used in [13], the sacrificial silicon grid structure is removed by pulsed isotropic etching with XeF_2, the recipe is shown in table 1. The directional and isotropic etch steps can be separated in the fabrication process. For instance, the grid structure can be etched before having any sensitive structures at the frontside that could get damaged. The grid structure can act as mechanical support during further processing, before it is removed when this support is no longer needed.

The work is organized as follows. First, in section 2 the proposed release process is explained. Next, in sections 3 and 4 we will present two applications of this technology, the release of microfluidic channels and thin film resonators, respectively.

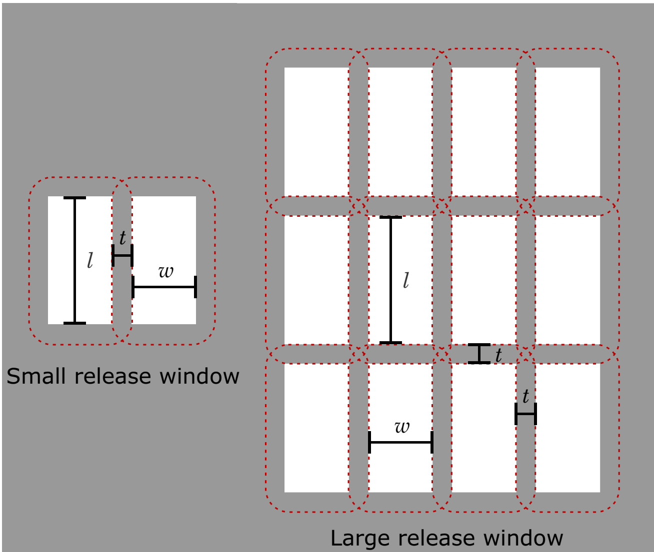

Figure 2. Schematic drawing of a small and a large release window that each consist of an array of rectangular openings with fixed width w and length l. In between the rectangular openings sacrificial silicon beams with width t remain that form a supporting grid for the structures that need to be released. At the end of the process this grid is removed by isotropic XeF_2 etching. The dashed lines indicate the release area, where some over-etching is used to allow complete removal of the silicon at the crossing of two grid beams.

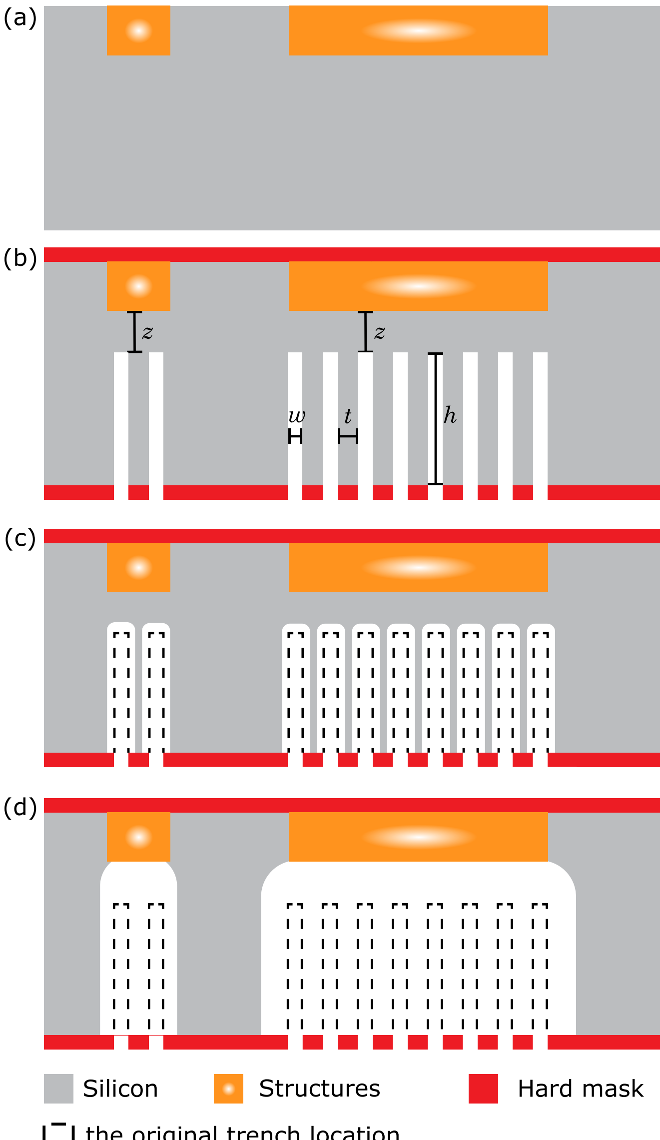

Figure 3. A cross-sectional schematic illustration shows that SGRT uses sacrificial grid structures and two-step dry etching techniques for the backside release of (a) both large and small MEMS structures on the silicon wafer. (b) Step 1, etch deep trenches until silicon remaining underneath the structures of depth h using Bosch-based DRIE process. The sacrificial silicon grid walls of depth h and width depth t are formed. The grids provide mechanical support when processing fragile structures on the frontside of the wafer. (c), (d) Step 2, isotropic XeF_2 etch to remove all the sacrificial silicon grid walls underneath each structure.

2. Sacrificial grid release technology

2.1. Process description

In the proposed SGRT process, the backside release openings are defined by an array of rectangular openings with fixed length l, width w, and spacing t, as indicated in figure 2. The final released area is indicated by the dashed red lines.

An outline of the SGRT fabrication process is shown in figure 3. Figure 3(a) shows the locations of the MEMS structures that need to be released. Note that these structures can be created prior to the release process, but also later after realizing the grid pattern. Figure 3(b) shows that the arrays of rectangular openings are etched by DRIE until a thickness z is left underneath the MEMS structures.

This results in a grid of sacrificial silicon walls with height h and thickness t. Because all rectangular openings have the same dimensions, RIE-lag [9] is avoided and the etching process can be optimized to achieve uniform depth over the whole wafer. Next, in figure 3(c), the sacrificial grid walls are etched using XeF_2 until the silicon is completely removed underneath the MEMS structures as shown in figure 3(d). The dashed lines indicate the original trench locations.

If required, further processing steps can be performed in between the steps in figures 3(b) and (c) since the grid structures provide mechanical support. After figure 3(c) no harsh processing steps should be performed that can cause damage to fragile MEMS structures. Doing this step last has many advantages. A wafer with many large holes is fragile and might also bend due to stress originating from the fabricated structures. Not doing any harsh processing steps not only protects the structures, but the whole wafer.

2.2. Chip separation by SGRT

SGRT can also be used as a method to separate chips from the wafer. This will be illustrated in section 3, in which we will discuss an example application that involves the release of large areas of suspended microfluidic channels.

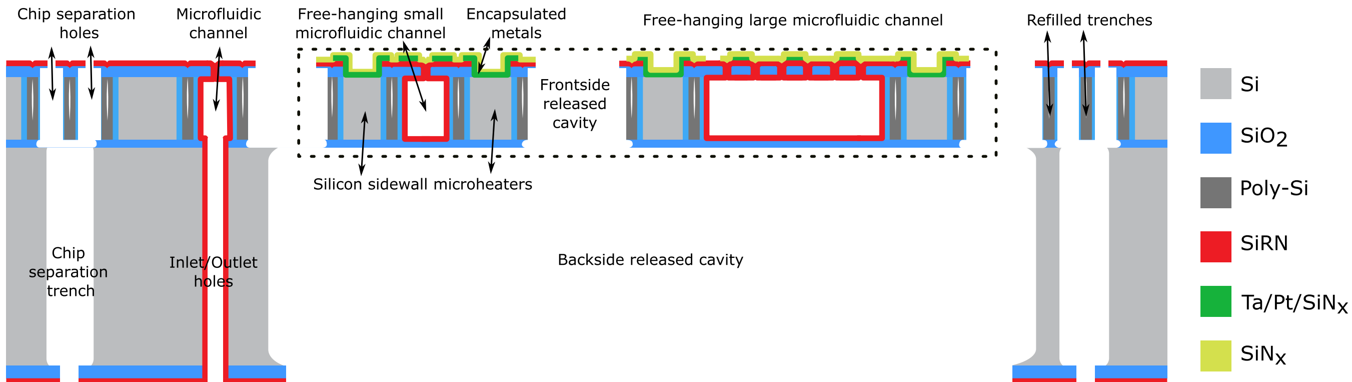

Figure 4. Schematic cross-sectional view of microfluidic channels fabricated by Trench-Assisted Surface Channel Technology. Narrow trenches refilled by SiO_2 and poly-Si are used as channel sidewall outlines and as protection of silicon sidewall heaters. Simultaneously, with the backside release cavities, trenches are created around each chip in order to separate the chips from the wafer.

3. Application: the release of large microfluidic structures by SGRT

3.1. Introduction

In [14], we presented the design of a micro-scale combustor containing large areas of suspended microfluidic channels with in-plane dimensions ranging from tens of micrometers to a few millimeters. These microfluidic channels need to be free-hanging to maintain a good thermal isolation from the substrate. Figure 4 shows a schematic cross-section of such microfluidic channels. Trench-Assisted Surface Channel Technology (TASCT) [15, 16] was designed to fabricate these microfluidic channels using refilled trenches as channel wall outlines. Besides having frontside cavities etched using conventional isotropic RIE, backside cavities underneath the microfluidic channels are realized using the SGRT approach to ensure complete release of the channels.

3.2. Fabrication process

The complete release process of large areas of microfluidic channels using the SGRT approach at the backside of the wafer is schematically illustrated in figures 5(a)–(f).

Wafers were processed by Trench-Assisted Surface Channel Technology [15, 16] to reach the status shown in figure 5(a). Silicon-on-insulator (SOI) wafers with a 50 μm thick device layer, a 200 nm thick buried oxide layer (BOX), and a 475 μm thick handle layer are used. In the device layer, the microfluidic channels are confined between two trenches refilled with silicon dioxide (SiO_2) and poly-crystalline silicon (poly-Si). All the channel walls have LPCVD SiRN inner surfaces. A thin film platinum layer (Pt) on top of the channels is used for electrical connections and to realize temperature sensors. A tantalum (Ta) adhesion layer is used and the metal layers are protected by a silicon nitride (SiN_x) encapsulation. In the device layer, the refilled trenches also outline an array of chip separation holes along the chip edges. This results in a gentle chip separation method similar to the technique proposed by [17] and [18]. In the handle layer, backside inlet and outlet holes are already connected to the frontside microfluidic channels.

Firstly, as shown in figure 5(a), a 20 μm thick dry film photoresist (DuPont MX5020 foil) was laminated on the backside of the wafer to prevent process contamination in the backside inlet and outlet holes. The grid release pattern was transferred into the dry film photoresist using UV photolithography and then the backside hard mask layers were etched using RIE. In the backside grid pattern, the grid beams are $t = 60$ μm wide. Each rectangular grid release window is $w = 200$ μm wide and $l = 1000$ μm long. Also, there is a 200 μm wide chip separation trench along the chip edge. When the backside trench is etched through the handle layer and connected to the frontside chip separation holes after vapor-HF etching of the BOX layer, the chips can be separated from the substrate without applying mechanical force. To prevent RIE-lag [9], all backside separation trenches are designed to have the same aspect-ratios as the grid patterns.

Secondly, 200 μm wide frontside release windows were patterned into the hard mask layers by UV photo-lithography and directional RIE, as shown in figure 5(b).

Next, at the backside of the wafer, as shown in figure 5(c), $h = 445$ μm deep grids and trenches were etched into the handle layer using a Bosch-based DRIE. A silicon layer of $z = 30$ μm remained underneath the BOX layer, together with the $w = 60$ μm wide sacrificial grid beams. This sacrificial silicon provides mechanical support for wafer handling and subsequent process steps. Fluorocarbon residuals from the DRIE was removed by an *in-situ* oxygen plasma step [19], which allows a uniform XeF_2 isotropic removal silicon later.

As shown in figure 5(d), the silicon in the device layer can be etched using selective isotropic etching, e.g. using XeF_2, at the frontside release windows and the chip separation holes. Because the refilled trenches have SiO_2 outer surfaces which serve as an etch stop for XeF_2, over-etching is allowed to guarantee a complete frontside release.

As shown in figure 5(e), the remaining silicon grid structure in the handle layer was completely etched using XeF_2. Because of the uniform surface areas and regular spacings created in the sacrificial grid pattern, XeF_2 etches the silicon beams in the grid uniformly. Lastly, as shown in figure 5(f), vapor HF is used at the frontside of the wafer to remove the BOX layer. In this way, chips were separated from the wafer

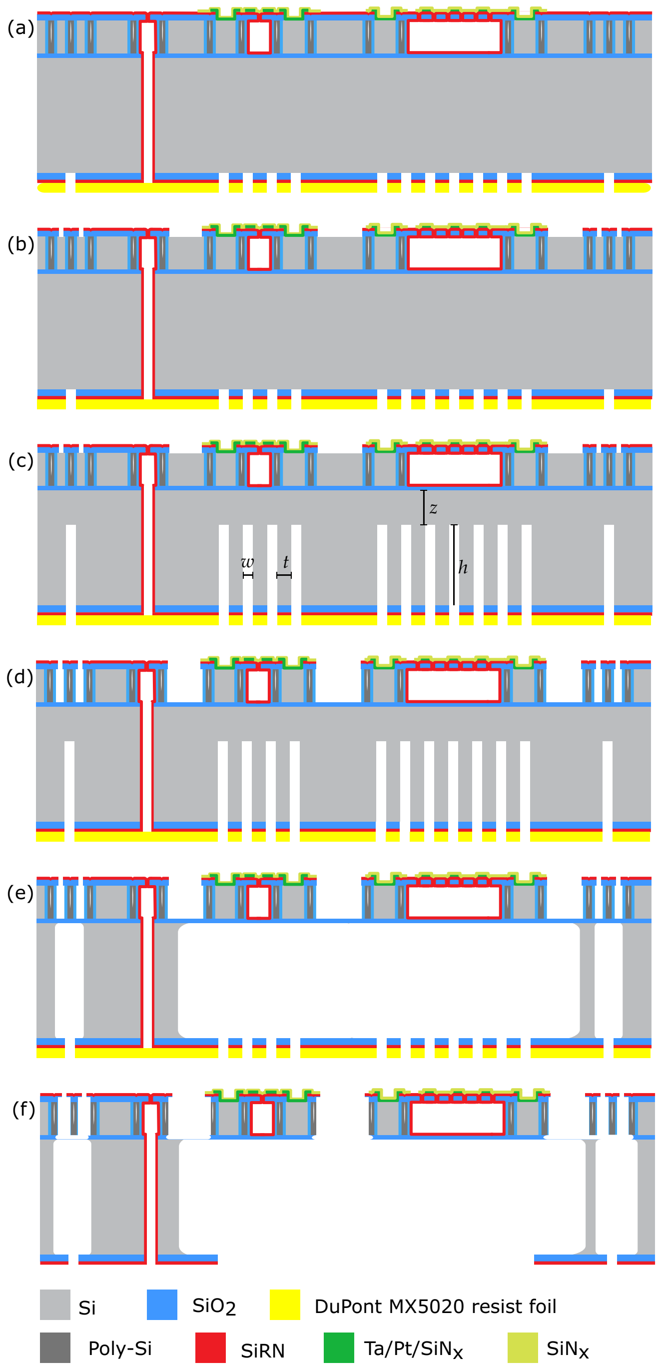

Figure 5. Outline of the SGRT release process to obtain free-hanging microfluidic channels with large in-plane areas in an SOI wafer. In combination with frontside cavities the SGRT release principle is also used to gently separate the chips from the wafer.

and the microchannels were fully released and become free-hanging. The dry film photoresist can be removed manually by an adhesive tape.

3.3. Results

Successful release results of large areas of microfluidic channels by SGRT are demonstrated on three microfluidic chips fabricated from a single wafer. Figures 6 and 7 show the top views of chips 1 and 2, respectively. Chip 1 has four spiral shaped microfluidic channels connecting to a microcombustor chamber in the center. Chip 2 has meander shaped microfluidic channels connected to a 'pizza' shaped microcombustor chamber. In figures 6(a) and 7(a), after the frontside release etch, frontside cavities separate all the channels from the device layer silicon, which corresponds to the fabrication step in figure 5(d). After the complete SGRT release etch, figure 6(b) shows that the grid pattern in the backside hard mask layers can be seen clearly below the microchannels. Figure 7(b) shows a photograph of the fully released chip 2. Figures 6(b) and 7(b) correspond to the fabrication step in figure 5(e). These grid-shaped hard mask layers can be easily removed with adhesive tape as shown in the fabrication step in figure 5(f).

Figure 8 shows a microscope photograph of the backside of the fully released chip 3, which corresponds to figure 5(e). The handle layer silicon underneath the microfluidic channels is completely removed. This microscopic image is focused on

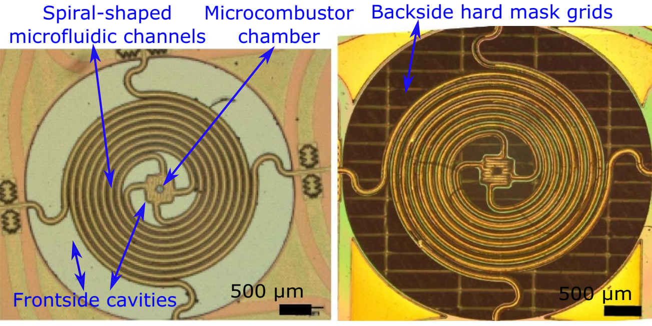

Figure 6. Microscopic top view of large areas of free-hanging microfluidic channels in chip 1 released by SGRT. (a) Four spiral shaped microfluidic channels are connected to the microcombustor chamber in the center. After the frontside release, all the channels are separated from the device layer bulk silicon by the frontside cavities. (b) After the SGRT release, the grid pattern in the backside hard mask layers can be seen clearly below the microchannels.

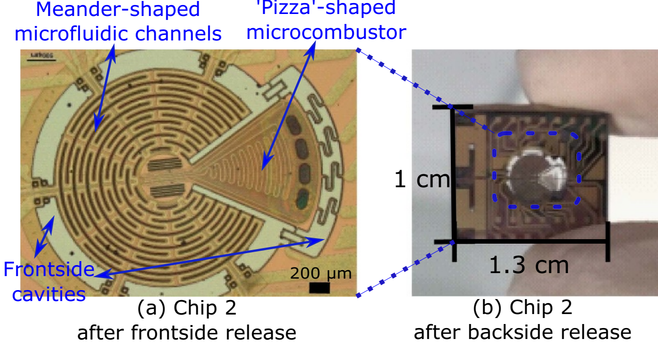

Figure 7. Microscopic top view of large areas of free-hanging microfluidic channels in chip 2 released by SGRT. (a) Meander shaped microfluidic channels are connected to a 'pizza' shaped microcombustor chamber. After the frontside release, all the channels are separated from the device layer bulk silicon by the frontside cavities. (b) After the SGRT release, a photograph shows the fully released chip 2.

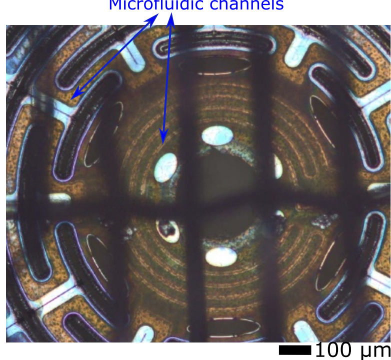

Figure 8. Microscopic bottom view of chip 3 with released microfluidic channels. No traces can be seen of remaining silicon, showing that a complete backside release was achieved by SGRT. The out-of-focus grid pattern in the hard mask layer is hanging in front of the channels. The grid beams are 60 μm wide. Each rectangular grid release window is 200 μm wide and 1000 μm long.

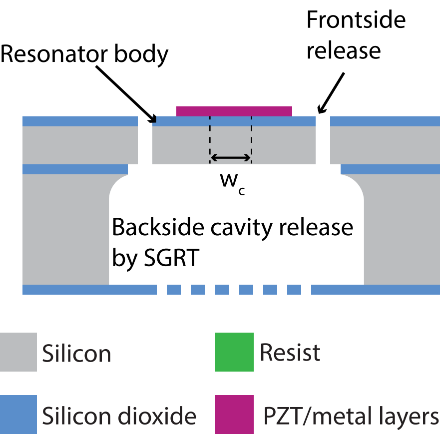

Figure 9. Schematic cross-sectional view of a thin film resonator, the backside release is obtained by SGRT. The resonator is connected with the bulk substrate by an anchor of length l_a, perpendicular to the surface of the image, and clamping width w_c.

the bottom surface of the microfluidic channels. The grid patterned backside hard mask is hanging in front of the microfluidic channels and is out of the focus. The out of the focus distance equals the handle layer thickness of the SOI wafer.

3.4. Discussion

In this application, SGRT demonstrates successful release of large areas of microfluidic channels with in-plane dimensions up to several millimeters. In addition to the release of the MEMS structure, SGRT also proves to be useful as a gentle method to separate chips from the wafer.

In this specific application, there is still two problems need to be solved. Firstly, some wafer-scale non-uniformity is generated from both the Bosch process and XeF_2 etching, meaning that the chips in the wafer center are fully released first. In practice, they were picked up from the wafer using tweezers and leave the rest of the chips to be further released. Secondly, the thin film Ta layer located on top of the microfluidic channels, as shown in figures 5(c), (d), are also etched by XeF_2 during the topside release, meaning the protective SiN_x layer did not protect it properly. A protection layer such as photoresist can be employed during the release etch to resolve this problem, as it is done in the application in section 4.

4. Application: SGRT release of thin film resonators

4.1. Introduction

Two key design parameters for thin film resonators are the clamping width and the length of the connection between the thin film and the bulk of the substrate commonly referred to as the anchor. The clamping width, that is the width of the connection between the resonator and the bulk of the chip, is ideally made as narrow as possible within the considered technology. The length of this connection is easily over-etched during the release which results in a spread in device characteristics as a result of an increased loss in the anchor [20]. The resonator can be tuned by using different lateral dimensions of the thin film, consequently different surface areas need to be released from the bulk silicon. It is demonstrated that SGRT allows for the fabrication of resonators with different dimensions while minimizing the over-etch of the anchor length. Figure 9 shows a cross-section of a typical device schematic of a thin film resonator that needs to be released from the bulk silicon.

4.2. Fabrication process

The thin film resonators are fabricated on a SOI wafer with a 3 μm thick device layer, a 500 nm thick BOX layer and 380 μm thick handle layer. The resonators are formed in the device layer according to the fabrication process as shown in figure 10. Prior to the release all frontside processing is performed. First a 300 nm thick layer of silicon dioxide is grown by means of wet thermal oxidation. This will be used as a hard mask for the front-and-backside release. Secondly the metal and piezoelectric layers are deposited, using sputtering and pulsed laser deposition, and patterned, using ion beam etching and wet chemical etching, respectively, as shown in figure 10(a). The lateral dimensions of the resonator are defined by means of a trench with an aspect ratio equal to one. This frontside release trench is etched by DRIE and the BOX layer is used as etch stop, see figure 10(b). Finally, the frontside is protected with a thick layer of photoresist of approximately 10 μm as shown in figure 10(c).

On the backside, the grid pattern for the release windows are pattered in the hard mask with RIE. The width of the silicon grid equals $t = 24$ μm and the dimensions of the rectangular release windows are $l = 170$ μm and $w = 150$ μm. To divide the wafer in dies a separation trench with a width of 10 μm surrounding the edge of the chip area is also patterned in the backside hard mask during the RIE step, not shown in the cross-section. The release windows are etched with DRIE into the silicon to a depth of $h = 360$ μm leaving $z = 20$ μm of silicon for mechanical support as shown in figure 10(d).

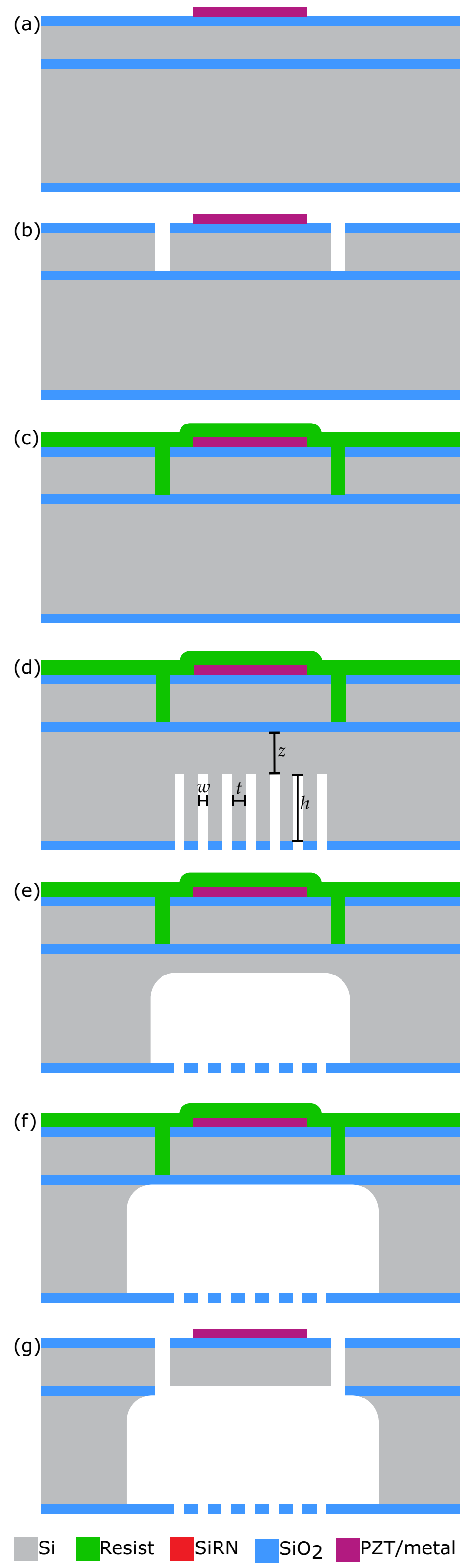

Figure 10. Cross-sectional view of the SGRT release process in a SOI wafer to obtain a single free-hanging thin film resonator.

Simultaneously, the separation trenches are etched to a depth of 260 μm. At this point the wafer can be divided in dies by mechanically breaking along the backside separation trenches.

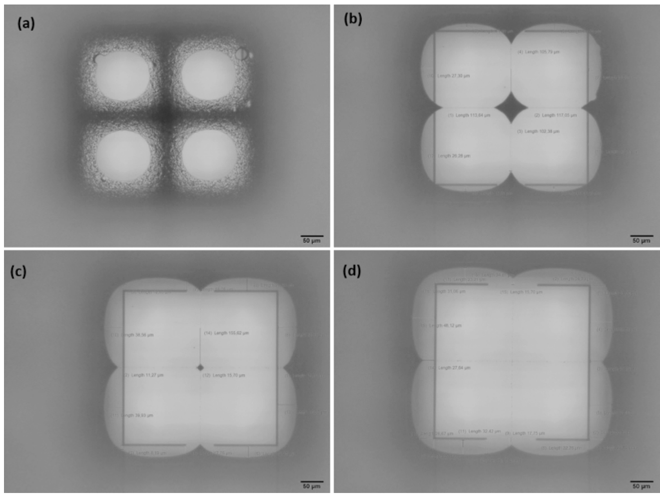

Figure 11. Backside microscopy view of the etched silicon beams for different XeF_2 etch cycles (a) 40 cycles, (b) 50 cycles, (c) 55 cycles and (d) 60 cycles.

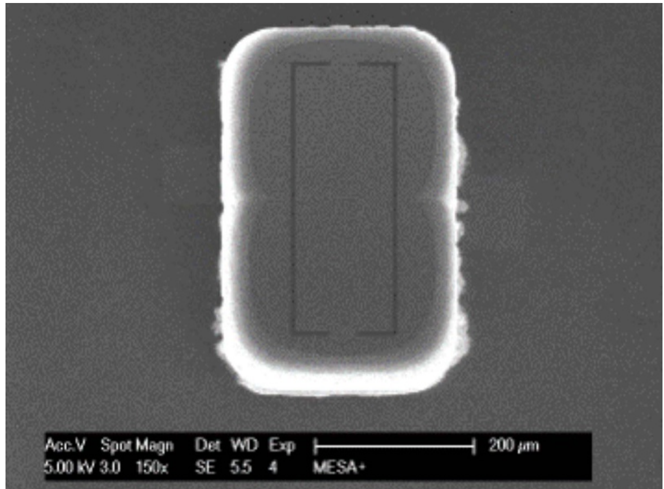

Figure 12. Backside SEM view showing the release cavity of a fully released thin film resonator based on a 1 × 2 grid.

The remaining silicon is isotropically etched with XeF_2 using the BOX layer as etch stop as shown in figure 10(f). The XeF_2 etch is performed in pulsed mode as shown in the recipe in table 1, in which each etching cycle is set to 30 s.

The remaining hard mask and photoresist at the backside is peeled of by means of adhesive tape. Finally the resonators are completely released by RIE of the BOX layer from the backside and stripping the protection photoresist on the frontside with O_2 plasma as shown in figure 10(g).

4.3. Results

A microscopic bottom view of the release process of a two by two cavity grid layout, at different number of XeF_2 etch cycles, is shown in figure 11. After 40 cycles, figure 11(a), the silicon beams between the cavities remain clearly visible. Increasing the number of etch cycles up to 50 and 55 cycles, figures 11(b) and (c) respectively, the silicon beams are completely etched

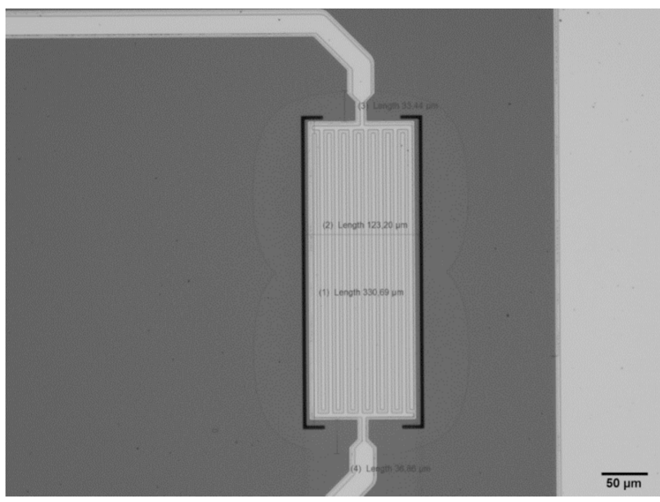

Figure 13. Frontside microscope view showing the metallization and electric connections.

and only a small silicon pillar remains on the BOX layer at the center of the cavity. For the remaining number of cycles, figure 11(d), the length of the beam connection to the bulk can be monitored allowing for good control of the etch while making sure that the resonator body is completely released from the bulk silicon.

A scanning electron microscope (SEM) image of the backside of a fully released structure is shown in figure 12. For the same structure an optical microscope photograph of the frontside view is shown in figure 13. In this figure the backside release is surrounding the resonator body as an 8-shaped cavity.

4.4. Discussions

In this application SGRT is used to successfully release thin film resonators of different size from the bulk of a SOI wafer. In addition to the release of the resonators this method proves also to be useful as a well controlled process. This makes it possible to keep the over-etch of the connection between the thin film and the bulk to a minimum. Ideally, this would be independent of the release process, in the proposed method this can be obtained by using SGRT in combination with deep trenches as etch stops [21].

In the demonstrated application the division of the wafer in chips is performed by breaking the wafer along the separation trenches on the backside. Instead of mechanically breaking the wafer, SGRT can be used as a delicate division method as shown in the first application. The division in individual chips has the advantage to overcome the wafer-scale non-uniform etch rate of XeF_2. This is preferred if the mask design consists of large differences in release area which need to be precisely controlled while ensuring a complete release of the chip.

5. Conclusions

SGRT is proposed as a versatile release solution for MEMS structures. It is especially useful to uniformly release MEMS structures with different in-plane dimensions. SGRT combines two dry etching techniques by first defining uniform sacrificial grid structures by DRIE and then removing this grid by isotropic vapor phase XeF_2 etching. Two demonstrator applications are used to verify the SGRT concept. In the first application, SGRT demonstrates successful release results for large areas of microfluidic channels of several millimeters. In the second application, fragile thin film resonators were safely released by SGRT. In addition to the release of the MEMS structure, SGRT also proves to be useful as a gentle method to separate chips from the wafer. An important advantage of SGRT is that it allows the sacrificial silicon structures to provide mechanical support. This gives freedom in wafer process flow design and guarantees to safely process large areas of free-standing fragile structures such as membranes, microfluidic channels, thin films, cantilevers.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgment

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