Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V $\Delta\Sigma$-Modulators

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***Abstract*— Subthreshold amplifiers suffer from the limited voltage headroom which leaves little space for conventional analog techniques to enhance performance and efficiency. This paper presents an evolution process of implementing conventional structures with inverters, allowing ultralow-voltage operation with increased flexibility in adopting traditional circuit techniques. Based on the proposed inverter-based elementary structure and CMFB, both the Miller-compensated (MC) operational transconductance amplifier (OTA) and the feedforward-compensated (FFC) OTA achieve significantly improved performance as compared to previous works. The proposed amplifier techniques are verified in $\Delta\Sigma$ modulator (DSM) design, with MC-OTA for a DT-DSM and FFC-OTA for a CT-DSM, both fabricated in a 0.13-μm CMOS. The 0.3-V DT-DSM achieves 74.1-dB SNDR, 83.4-dB SFDR and 20-kHz bandwidth with 79.3-μW power, resulting in a Schreier figure of merit (FoM) of 158 dB. The 0.3-V CT-DSM achieves 68.5-dB SNDR, 82.6-dB SFDR, and 50-kHz bandwidth with 26.3-μW power, leading to a Schreier FoM of 161 dB. Both DSMs exhibit highly competitive performance among sub-0.5-V designs, validating the proposed subthreshold amplifier techniques.**

***Index Terms*— Amplifiers, delta–sigma modulators, feedforward, frequency compensation, inverter-based, OTA, subthreshold, ultralow voltage.**

I. Introduction

ENERGY-CONSTRAINT applications demand lower and scalable supply voltages due to the power benefits of digital circuits under near- and sub-threshold supply voltages. The ultralow voltage design is also driven by technology scaling as well as leakage and reliability considerations [1]. While analog circuits with weak-inversion transistors benefit from high g_m/I_D due to the exponential characteristics of the V_{GS} versus I_D curve in weak inversion, the shrunk voltage headroom, and signal swing limit signal-to-noise ratio (SNR) fundamentally, and the linearity of transconductance becomes worse [2]. In addition, the decreased intrinsic gain of downscaled planar transistors makes it difficult to build high gain analog blocks [3]. It is thus very challenging to design high-linearity and high-precision analog circuits under near- and sub-threshold supply voltages, where operational transconductance amplifiers (OTAs) are fundamental. Though several approaches have been proposed to replace OTAs in particular analog systems by, e.g., time-domain circuits [4], dynamic amplifiers [5], ring amplifiers [6], zero-crossing-based circuits [7], OTAs remain indispensable due to their linear operation in closed-loop systems.

The previous studies on low-voltage amplifier designs have converged into several fundamental topologies. Differential-pair (DP) OTA is a simple and straightforward architecture [8]–[11]; however, the tail transistor and class-A output limit the output swing and slew rate of a DP OTA. Body-input OTA is capable of working under subthreshold supply voltages due to the relaxed biasing requirements [1], [12]–[14], while the low g_{mb}/I_D results in low power efficiency as compared to gate-input OTAs. Single inverter with class-AB operation is actually a neat and efficient gain stage under low supply voltages. Inverter-based OTAs with 0.2–0.5-V supply voltages were demonstrated in data converters, filters, voltage regulators, etc [15]–[20]. On the other hand, to bias an inverter for linear amplification is not trivial. It has been shown that switched-capacitor based bias is effective for an inverter-based OTA with supply voltages down to 0.2 V [20]; however, subthreshold switching is often problematic and the discrete-time nature limits its applications. Replica bias was proposed in a 0.16-V inverter-based OTA incorporating body input [21]; however, only open-loop application was demonstrated due to the sophisticated considerations on the implementation of frequency compensations. Moreover, the gain of a single inverter is limited to 20–30 dB in modern CMOS technologies [20]. Therefore, the design of high-gain and power-efficient subthreshold OTAs with competitive performance is still a topic requiring extensive research.

This paper studies low-voltage amplifiers systematically, with focus on subthreshold OTAs for general analog systems where closed-loop applications in both discrete-time (DT) and continuous-time (CT) domain are required. An inverter-based single-stage amplifier topology is proposed based on the complementary implementation of a conventional gain stage. Two-stage OTAs with Miller compensation and feedforward compensation are studied, achieving significantly improved figures of merit (FoM). To validate the proposed OTAs, two 0.3-V subthreshold $\Delta\Sigma$-modulators (DSMs)

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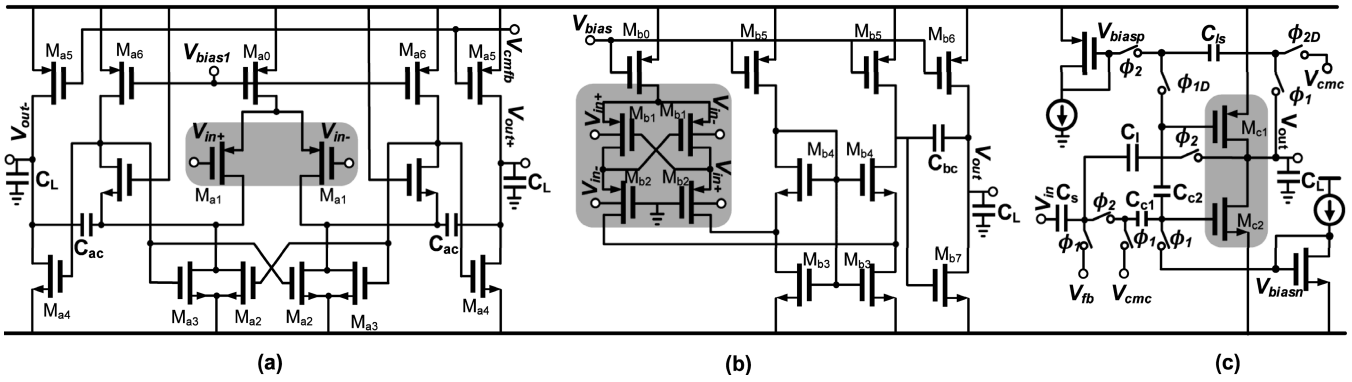

Fig. 1. Sub-0.5-V OTAs with (a) differential pair input, (b) body input, and (c) switched-capacitor-biased inverter.

TABLE I
FIRST-ORDER EXPRESSIONS OF OTA PERFORMANCE FOR FIG. 1

	DP OTA [Fig. 1(a)]	Body-Input OTA [Fig. 1(b)]	Inverter [Fig. 1(c)]
Mode	CT	CT	DT
Stage	Two	Two	One
Gain	$\frac{g_{ma1}g_{ma4}}{[g_{dsa3}+g_{dsa5}+g_{dsa6}+(g_{ma5}-g_{ma3})][g_{dsa4}+g_{dsa5}]}$	$\frac{g_{mb}g_{mb7}}{[\frac{g_{dsb1}+g_{dsb3}}{(ng_{mb4}+g_{dsb4})g_{dsb4}}+g_{dsb5}](g_{dsb6}+g_{dsb7})}$	$\frac{g_{mc1}+g_{mc2}}{g_{dsc1}+g_{dsc2}}$
GBW	g_{ma1} / C_{ac}	g_{mb} / C_{bc}	$(g_{mc1}+g_{mc2})$ / C_L
Slew Rate	I_{ma0} / $2C_{ac}$	$(I_{mb6}$-$I_{mb0})$ / C_L	I_{mc2} / C_L
Input-referred Thermal Noise	$\frac{8kT\gamma}{g_{ma1}}(1+\frac{g_{ma3}+g_{ma5}+g_{ma6}}{g_{ma1}})$	$\frac{8kT\gamma}{g_{mb}}(1+\frac{g_{mb3}+g_{mb5}}{g_{mb}})$	$\frac{8kT\gamma}{g_{mc1}+g_{mc2}}$
ICMR	[0,V_{DD}-V_{DSAT} –V_{GSa1}]	[0,V_{DD}]	[0,V_{DD}]
Output Swing	V_{DD}-2V_{DSAT}	V_{DD}-2V_{DSAT}	V_{DD}-2V_{DSAT}
Supply Limitation	3V_{DSAT}	3V_{DSAT}	2V_{DSAT}

with the same topology are demonstrated, with the Miller-compensated (MC) OTA for the DT-DSM and the feedforward-compensated (FFC) OTA for the CT-DSM, respectively. Both prototypes exhibit competitive performance among state-of-the-art sub-0.5-V designs. The CT-DSM with the FFC OTA achieves a Schreier FOM of 161.3 dB under 0.3-V supply.

Section II discusses several representative implementations of subthreshold amplifiers. Section III presents the proposed subthreshold amplifier techniques with two OTAs employing different frequency compensation schemes, which are later exploited in the DT and CT DSMs discussed in Section IV. Section V shows the measurement results and comparisons. This paper is concluded in Section VI.

II. OVERVIEW OF SUBTHRESHOLD AMPLIFIER TOPOLOGIES

Fig. 1 depicts the schematics of three representative subthreshold amplifiers with DP input [10], body input [22], and switched-capacitor biased inverter [16]. Table I summarizes the derived performance expressions of them, where the calculation is limited to the first order based on the transistor models in weak inversion [2].

The input transconductance in Fig. 1(a) can be written as

$$g_{\mathrm{ma1}}=\frac{I_{\mathrm{op}}}{2nU_T}e^{\frac{V_{\mathrm{CM}}-V_{\mathrm{TP1}}+V_{\mathrm{DS0}}}{nU_T}}\left(1-e^{\frac{V_{\mathrm{DS1}}}{U_T}}\right)\left(e^{\frac{V_{\mathrm{in}}}{2nU_T}}+e^{-\frac{V_{\mathrm{in}}}{2nU_T}}\right), \tag{1}$$

where I_{op} is the current of the PMOS tail transistor M_{a0}, n is the slope factor of the input transistors in weak inversion, $U_{\mathrm{T}}=\mathrm{kT}/q$ is the thermodynamic voltage (26 mV at 300 K). V_{CM} and V_{in} are the dc and small signal voltages at the input node. V_{DS0} and V_{DS1} are the drain to source voltages of M_{a0} and M_{a1}, respectively.

Due to the limited voltage headroom, a single DP is often unable to achieve sufficient gain. A cross-coupled pair generating negative conductance are exploited for gain enhancement, as shown in Fig. 1(a). Cross-coupling is among the few gain-enhancement options for low-voltage amplifiers [10], [23]–[26]; however, the negative conductance may

TABLE II
SIMULATED PERFORMANCE OF OTAS WITH 6-μA CURRENT BUDGET AND 2-pF LOAD UNDER 0.3-V SUPPLY

	Stage	Gain (dB)	GBW (MHz)	SR (V/μs)	Phase Margin (°)	Output Swing (V)	Input Thermal Noise @ 100kHz (nV$\sqrt{\text{Hz}}$)	FoM_S^* (MHz·pF/mW)	FoM_L^{**} (V/μs·pF/mW)
DP OTA [Fig. 1(a)]	Two	53.6	1.22	0.329	50.5	0.1	66	1,355	365
Body-Input OTA [Fig. 1(b)]	Two	59.3	0.43	0.098	46.6	0.1	92	477	108
Single Inverter	One	30.5	11.8	5.2	90.3	0.1	22	13,111	5,777
Proposed MC-OTA	**Two**	**46.2**	**2.45**	**2.4**	**52**	**0.1**	**38**	**2,720**	**2,666**
Proposed FFC-OTA	**Two**	**49.8**	**9.1**	**3.8**	**76**	**0.1**	**35**	**10,111**	**4,666**

*FoM_S =GBW·C_L/Power **FoM_L=SR·C_L/Power

cause stability issues and is inevitably sensitive to process–voltage–temperature variations, especially for transistors in weak inversion. A second gain stage was utilized to improve the dc gain of the amplifier, requiring frequency compensation to ensure the stability in closed-loop applications.

Body-input amplifiers have relaxed requirement on the supply voltage and input common-mode range (ICMR). However, the body transconductance is smaller and less efficient as compared to the gate transconductance. A positive feedback source degeneration was proposed to enhance the body transconductance, as shown in Fig. 1(b), where the effective input transconductance g_{mb} can be wrote as [22]

$$g_{mb} = \frac{n+1}{n-1} g_{mbb1}. \tag{2}$$

Considerably improved body transconductance is observed in [22]. However, the effect of the transconductance enhancement relies highly on the technology parameters.

Fig. 1(c) shows a switched-capacitor biased inverter OTA, where $\phi_1(\phi_{1D})$ and $\phi_2(\phi_{2D})$ are turned on for the biasing mode and amplification mode, respectively [16]. The effective input transconductance is contributed by both PMOS and NMOS transistors

$$g_{mc} = g_{mc1} + g_{mc2}. \tag{3}$$

In the amplification mode, high-power efficiency, large ICMR, and low noise are permitted due to the large transconductance and class-AB operation, as shown in Table I. Limitations of this architecture are mainly on the DT operation and decreased intrinsic gain in advanced nanometer technologies.

Under 0.3-V supply voltage, the above OTAs are optimized with the same current budget of 6 μA, capacitive load of 2 pF in the same 0.13-μm CMOS technology. The performance metrics are listed in Table II. It is shown that high gain is achieved in the DP OTA and body-input OTA where additional gain stages are employed. Suffering from the low g_{mb}, the driving capability and noise performance of the body-input OTA are relatively limited. The best GBW, SR, and noise performance are obtained by the single inverter due to its neat and highly efficient architecture. Both the small-signal based $\text{FoM}_\text{S} = \text{GBW} \cdot C_\text{L}/\text{Power}$ and the large-signal based $\text{FoM}_\text{L} = \text{SR} \cdot C_\text{L}/\text{Power}$ [27] indicate that a single inverter is the most power-efficient subthreshold amplifier structure. Though it can be used as a benchmark reference, the relatively lower gain limits its application in high-linearity feedback systems.

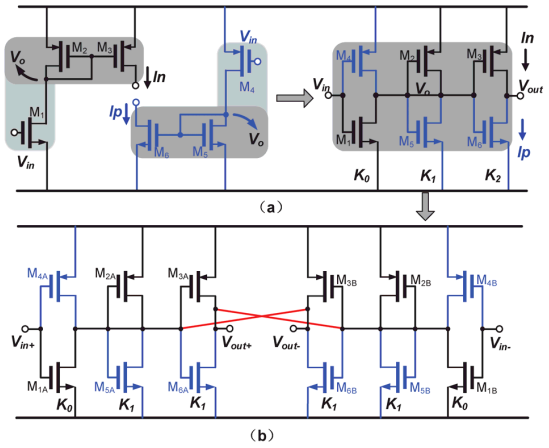

Fig. 2. Evolution process of the proposed CT-biased subthreshold amplifier from (a) single-ended to (b) cross-coupled pseudo-differential structure.

III. PROPOSED SUBTHRESHOLD AMPLIFIERS

From the above analysis, inverter-based architecture has significant advantages for subthreshold amplifiers when the bias and gain restraints are relaxed. Using multiple stages can improve dc gain effectively, which is, however, not practical with a switched-capacitor-based DT bias. Therefore, a robust CT-biased amplifier topology is fundamental.

A. CT-Biased Elementary Amplifier

Fig. 2 shows the three-step evolution process of the proposed elementary amplifier. A diode-loaded common-source stage is adopted as the starting point, as depicted in the left part of Fig. 2(a). Without a dedicated tail transistor, the diode-connected transistor (M_2/M_5) works as an internal regulator with a feedback control mechanism to self-bias the input stage [6]. This is a well-proven and widely used structure in standard-voltage analog design.

By combining the complementary parts (black and blue), an inverter-implemented structure is observed, as depicted in the right part of Fig. 2(a). The input inverter (M_1–M_4) behaves the same as the PMOS or NMOS input with transconductance increased to ($g_{m1} + g_{m4}$), implying enhanced performance and power efficiency. The diode-loaded inverter (M_2–M_5)

stabilizes the output voltage of first inverter in CT mode. Nevertheless, the output inverter (M_3–M_6) is now running without a bias control, which is sensitive to the PVT variations as well as mismatch and offset of earlier stages.

Fig. 2(b) shows the final topology of the proposed pseudo-differential amplifier. With the cross-coupled connection (red line), the diode inverter is reused to bias the output inverter of the counter side. Meanwhile, the differential operation of the OTA is enhanced by the cross-coupled bias control mechanism [28].

It is worth mentioning that a negative conductance is also introduced by the cross-coupled connection, which can be employed for gain enhancement, as was used in Fig. 1(a) and several other low-voltage designs. In this paper, however, the negative conductance is eliminated considering the stability and PVT robustness under ultralow supply voltages. The ratio of the two inverters is kept the same ($K_1 = K_2$) to cancel the negative conductance, as shown in Fig. 2(b). In addition, long channel length (0.7 μm) is used here due to the concerns on the flicker noise and mismatch.

Since the topology is fully inverter based, the proposed OTA owns the same output range and supply limitation as a single inverter. The performance expressions are derived as follows:

$$A_{\mathrm{DC}} = \frac{(g_{m1}+g_{m4})}{\sum_{\mathrm{n}=1}^{6} g_{dsn} + (g_{m2}+g_{m5}) - (g_{m3}+g_{m6})} \approx \frac{(g_{m1}+g_{m4})}{\sum_{\mathrm{n}=1}^{6} g_{dsn}} \tag{4}$$

$$\mathrm{GBW} = (g_{m1}+g_{m4})/C_{\mathrm{L}} \tag{5}$$

$$\mathrm{SR} \approx \frac{K_0}{K_0+2K_1}\frac{I}{C_{\mathrm{L}}} \tag{6}$$

$$\overline{V_{\mathrm{n,input}}^2} = \frac{8kT\gamma}{g_{m1}+g_{m4}}\left(1+\frac{2K_1}{K_0}\right). \tag{7}$$

It is shown that without any enhancement, the dc gain of the proposed elementary amplifier is slightly lower than a single inverter. The additional inverters contribute noise as well as parallel load impedance. On the other hand, the self-biased CT operation opens the possibility of incorporating sophisticated analog techniques to enhance the amplifier under ultralow supply voltages and for CT operations.

B. Two-Stage Amplifiers With Frequency Compensation

For closed-loop feedback systems, the linearity is determined fundamentally by the gain of amplifiers. With the proposed CT-biased elementary amplifier, cascading of multiple stages becomes practical for higher dc gain while preserving the advantage of inverter-based amplifiers. On the other hand, frequency compensation has to be employed to ensure the stability in closed-loop applications. For inverter-based amplifiers, Miller compensation and feedforward compensation were demonstrated in multistage designs [29].

Fig. 3(a) shows a MC two-stage OTA, where the proposed elementary amplifier of Fig. 2 is used for each stage with a Miller capacitor C_m for frequency compensation. The simplified small-signal model is depicted in Fig. 3(b). The Miller capacitor split the poles of the two-stage amplifier.

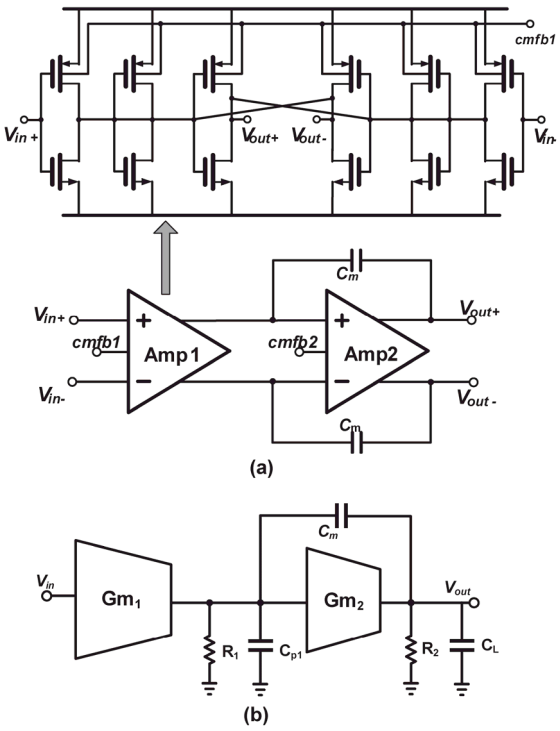

Fig. 3. (a) Schematic of the proposed two-stage subthreshold amplifier with Miller compensation and (b) simplified small-signal model.

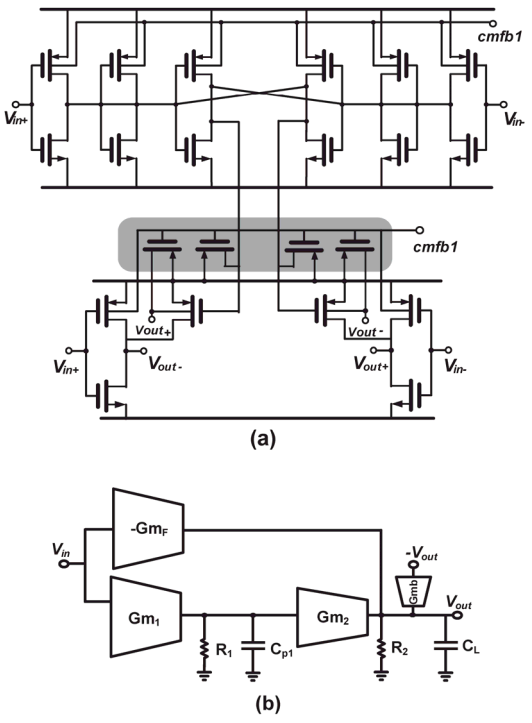

Fig. 4. (a) Schematic of the proposed two-stage subthreshold amplifier with feedforward compensation and (b) simplified small-signal model.

The frequency response is derived as

$$A(s) \approx \frac{Gm_1Gm_2R_1R_2(1-sC_m/Gm_2)}{1+Gm_2R_2R_1C_ms+s^2R_1R_2(C_mC_{p1}+C_mC_L+C_LC_{p1})} \tag{8}$$

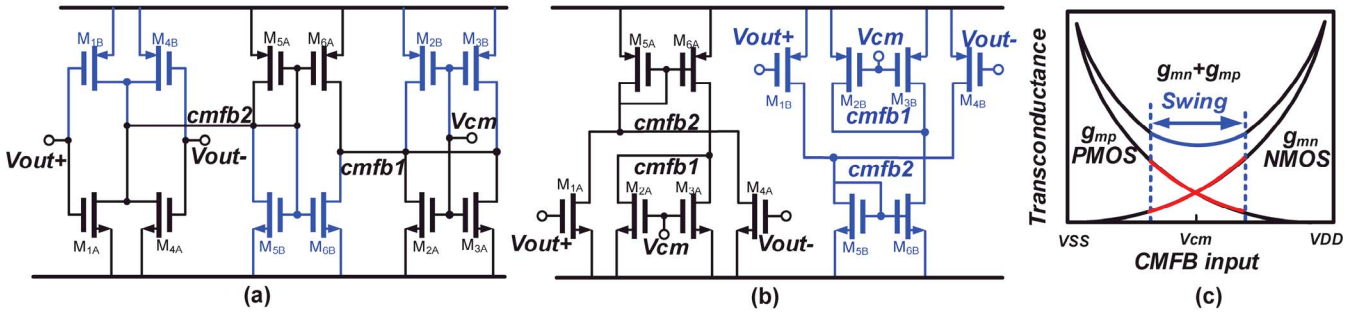

Fig. 5. Schematics of (a) proposed inverter-based CMFB circuit, (b) pseudo-differential DDA, and (c) input transconductance of the CM amplifier versus its input voltage (output of the main amplifier).

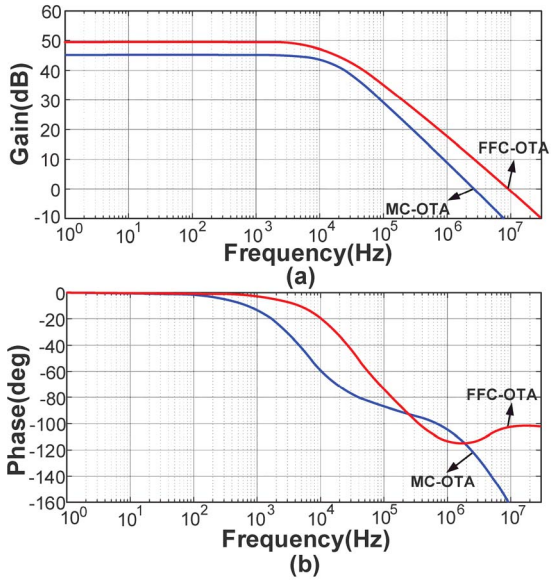

Fig. 6. Simulated frequency response of the proposed two-stage OTAs with (a) Miller compensation and (b) feedforward compensation. Both OTAs are optimized with 6-μA current budget and 2-pF load under 0.3-V supply. CMFB circuits are included.

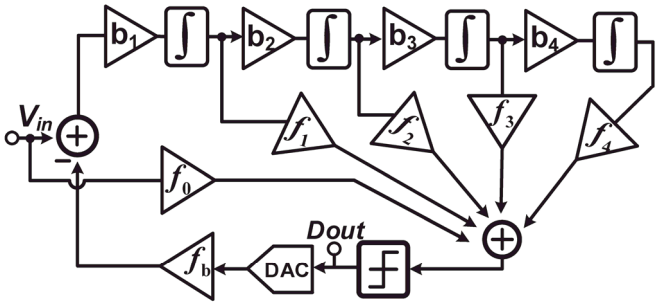

Fig. 7. System architecture of the single-bit 4th-order CIFF DSM.

where the poles can be simplified as [30]

$$p_1 \approx \frac{1}{Gm_2 R_1 R_2 C_m} p_2 \approx \frac{Gm_2}{C_L}. \tag{9}$$

As a standard Miller compensation, driving C_m consumes extra current and affects the power efficiency.

Feedforward compensation is an alternative option based on pole-zero cancellation [31], [32], where higher GBW and power efficiency can be expected. Fig. 4 shows the proposed two-stage amplifier with feedforward compensation and its

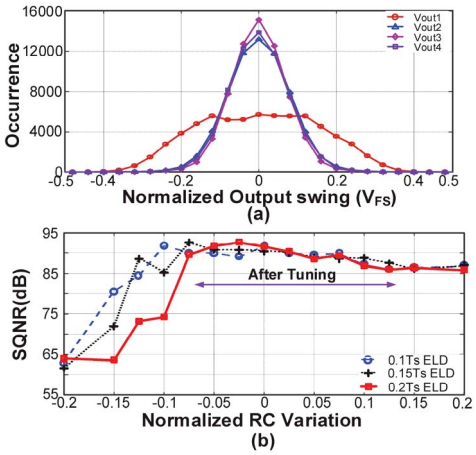

Fig. 8. (a) Normalized output swing of each stage. (b) SQNR of CT-DSM with different ELD and *RC* variations.

small-signal model. The first stage utilizes the elementary amplifier in Fig. 2(b) for noise and robustness considerations. The feedforward path is implemented with a single inverter, owing to the high transconductance requirement as well as design complexity. The second stage uses a single PMOS with cross-coupled gain enhancement through the body terminals. Note that the negative conductance created here does not cause stability concern because of the small gm_b. The frequency response is derived as

$$A(s) \approx \frac{Gm_1 Gm_2 R_1 R_2 + Gm_F R_2 + Gm_F R_1 R_2 C_{p1} s}{(1 + R_1 C_{p1} s)(1 - GmbR_2 + R_2 C_L s)}, \tag{10}$$

where

$$p_1 = \frac{1 - GmbR_2}{R_2 C_L} \quad p_2 = \frac{1}{R_1 C_{p1}} \quad z = -\frac{Gm_1 Gm_2}{Gm_F C_{p1}} + \frac{1}{R_1 C_{p1}}. \tag{11}$$

The transconductance of the feedforward stage, Gm_F, has to be sufficiently large to make the second-pole and zero close to each other. Despite the advantages in power efficiency, it is worth mentioning that the presence of the pole-zero pair may potentially complicate the settling behavior in switched-capacitor systems.

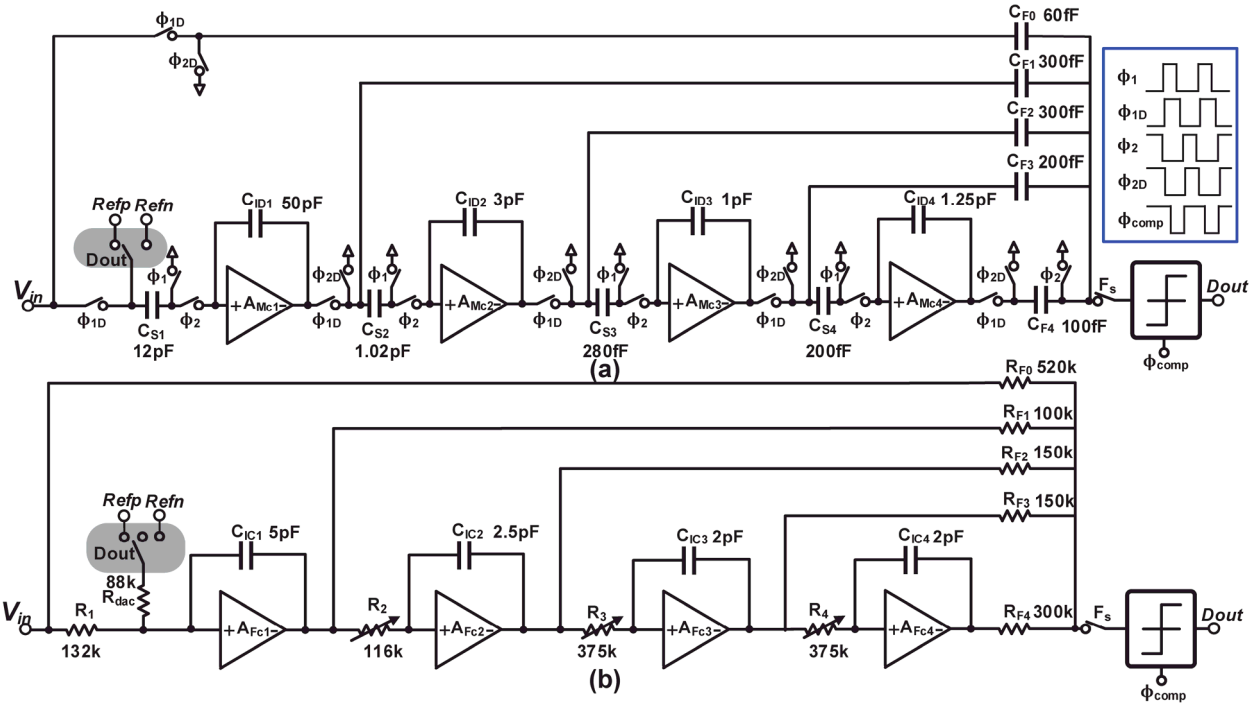

Fig. 9. Circuit implementations of the (a) DT and (b) CT DSMs.

C. Inverter-Based Common-Mode Feedback

The common-mode feedback (CMFB) has to be CT as well. For the proposed amplifier, the body of PMOS transistors are utilized for CMFB control, avoiding the requirement of triple-well technology. Fig. 5(a) shows the topology of the proposed CT amplifier for CMFB. The inverter-based implementation is obtained from a similar procedure as discussed in Section III-A. A differential-difference amplifier (DDA) is used as the original architecture [33], as depicted in Fig. 5(b). The diode inverter and the mirror load (M_5–M_6) bias the inverter-based CM amplifier for robust operations, which is similar to that in Fig. 2. Comparing with NMOS/PMOS-only DDAs of Fig. 5(b), where the input transconductance is highly dependent on the output of the main amplifier, the complementary input of the inverter-based CM amplifier offers higher and relatively stable transconductance, accommodating a wide range of output from the main amplifier, as shown in Fig. 5(c). The large output swing of the inverter-based CMFB implies a strong control of the body terminals of the PMOS feedback transistors in both amplifiers. In addition, the PMOSs in the shadowed part of Fig. 4 are utilized to increase the controllability of common mode voltages in the FF-OTA.

D. Amplifier Performance Benchmarking

For a fair comparison with state-of-the-art amplifier designs, the proposed two amplifiers are optimized with 6-μA current budget and 2-pF load under 0.3 V, which is the same condition as used in Section II. Fig. 6 shows the simulated frequency response of the MC OTA and the FFC-OTA, with a detailed list of parameters added to Table II.

It is shown that the proposed amplifiers achieve significantly improved GBW, SR, noise, and power efficiency compared to previous CT OTAs. The FFC-OTA outperforms the MC-OTA due to the capacitor-free compensation. In fact, the proposed fully inverter-based topology with feedforward compensation has improved the FoM_S and FoM_L to a level close to a single inverter, which sets the benchmark in low-voltage amplifiers.

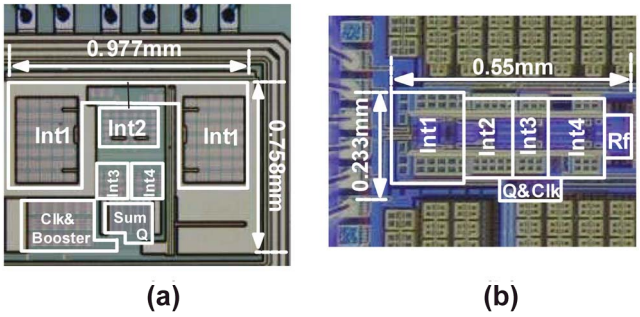

Fig. 10. Die microphotographs of the fabricated (a) DT and (b) CT DSMs.

IV. $\Delta\Sigma$ Modulators Implemented With the Proposed Subthreshold OTAs

To validate the proposed subthreshold OTAs in closed-loop analog systems, two 0.3-V $\Delta\Sigma$-modulators are implemented, where OTAs affect the system performance fundamentally. The target dynamic range (DR) is set >70 dB under 0.3 V, requiring OTAs with sufficient gain, swing, and noise performance.

A. Modulator Architecture

For linear operation under low supply voltages, it is important to reduce the swing requirement of each stage. Therefore, CIFF topology with input feedforward is employed, as shown in Fig. 7. Single-bit quantizer and DAC are utilized since they

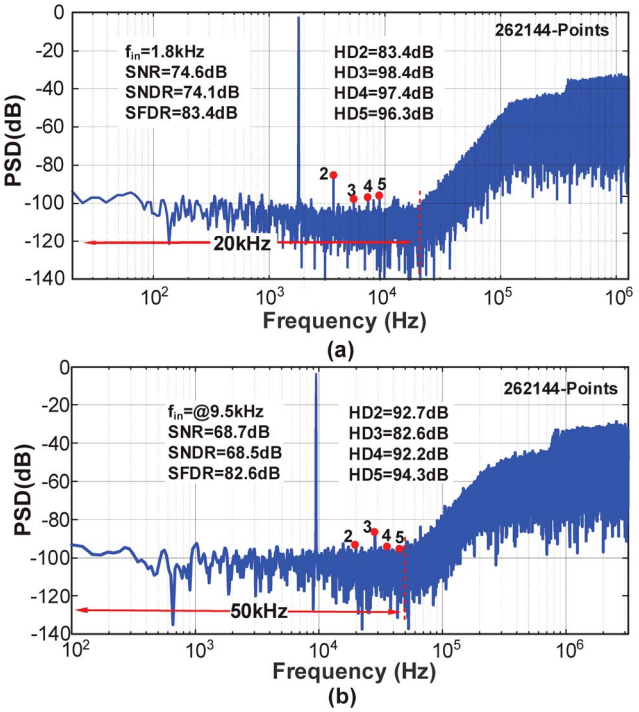

Fig. 11. Measured output spectrum of the (a) DT and (b) CT DSMs.

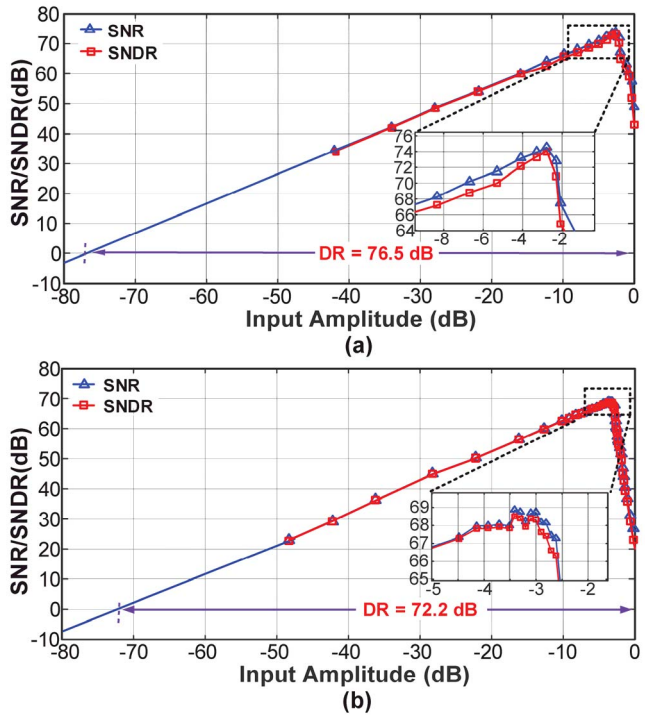

Fig. 12. SNR and SNDR versus input amplitude for the (a) DT and (b) CT DSMs.

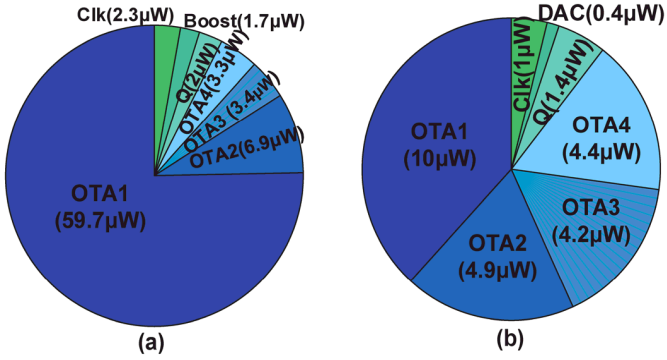

Fig. 13. Power breakdown of the (a) DT and (b) CT DSMs.

are naturally linear, so that the performance of the DSM is mainly determined by the OTAs. The signal path f_0 forward the input component before the quantizer, which improves SNDR [18]. The fourth-order CIFF modulator with OSR of 64 achieves >88-dB SQNR. Fig. 8(a) shows the optimized output swings, which are limited to ± 0.4 $V_{\rm FS}$ so as to relax the slew rate and swing requirement of integrators. The simulated out-of-band gain (OBG) is 1.42, ensuring the stability of the system.

The CIFF architecture is implemented in both DT and CT. Comparing with a low-voltage DT-DSM, a low-voltage CT-DSM suffers from the excess loop delay (ELD), resulting in potential instability. Normally, an additional local feedback DAC branch can be employed to compensate the ELD [34]. However, a large signal swing may be introduced at the output of the last integrator, degrading the linearity performance. For low-voltage DSMs, the ELD is relatively small as compared to the whole sampling period. Thus, a fast return-to-open (RTO) DAC, which is similar to the return-to-zero (RTZ) DAC, is adopted here to tolerate the small ELD [35]. Behavioral simulation shows the CT-DSM is able to achieve >85-dB SQNR with OBG of 1.35, and the system is quite stable under $0.2T_{\rm s}$ ELD, as shown in Fig. 8(b). In addition, the variation of RC time-constant is limited to [−5%, 12.5%] with a 3-b resistor tuning, which ensures a robust performance of the CT-DSM.

B. Circuit Implementation

Fig. 9 shows the circuit implementations of the DT and CT DSMs. The feedforward paths are realized by summing capacitors and resistors in DT and CT DSMs, respectively. Coefficients f_0–f_4 are determined by the ratio of $C_{\rm F0}$–$C_{\rm F4}$ or $R_{\rm F0}$–$R_{\rm F4}$.

The DT-DSM exploits the proposed MC-OTAs because of their symmetric SR and fast-settling behavior. Loaded by large integration and sampling capacitors ($C_{\rm ID1}$ = 50 p, Cs_1 = 12 p) due to the noise consideration, the first MC-OTA in the DT DSM achieves 7.8-MHz GBW, facilitating non-overlapping clocks ($\phi_1, \phi_{1\rm D}, \phi_2, \phi_{2\rm D}$) at 2.56 MHz for the DT-DSM in Fig. 9(a).

Targeting on an improved signal bandwidth, the CT-DSM employs the proposed FFC-OTAs for higher GBW and power efficiency. The noise of the CT-DSM is dominated by the input and feedback resistors of the first integrator, allowing a smaller loading capacitor $C_{\rm IC1} = 5$p. The first FFC-OTA in the CT DSM achieves 14.2-MHz GBW, facilitating a sampling frequency of 6.4 MHz. Therefore, the 0.3-V CT-DSM achieves 50-kHz bandwidth comparing with the 20-kHz bandwidth achieved by the DT-DSM.

The two DSMs utilize the same 1-bit comparator topology as used in [17] with their parameters optimized individually.

TABLE III
SUMMARY OF MEASURED PERFORMANCE AND COMPARISON WITH PREVIOUS SUB-0.5-V DSMS

Specification	This Work		JSSC 2015 [10]	JSSC 2012 [16]	JSSC 2012 [18]	JSSC 2007 [35]	ESSCIRC 2007 [36]	ESSCIRC 2016 [37]
Architecture	**DT**	**CT**	DT	DT	DS-DT	CT	VCO	VCO
Technology (nm)	**130**		130	130	130	180	90	65
Supply Voltage (V)	**0.3**		0.4	0.25	0.5	0.5	0.2	0.3
Bandwidth (kHz)	**20**	**50**	20	10	20	25	20	10
Sampling Rate (MS/s)	**2.56**	**6.4**	3.2	1.4	2.5	3.2	12	1.28
OSR	**64**	**64**	80	70	62.5	64	300	64
SNR(dB)	**74.6**	**68.7**	77.7	64	82.4	76	68.9	-
SNDR (dB)	**74.1**	**68.5**	76.1	61	81.7	74	60.3	56.1
SFDR (dB)	**83.4**	**82.6**	-	70	96	-	-	66.2
DR (dB)	**76.5**	**72.2**	82	-	85	-	-	-
Power (μW)	**79.3**	**26.3**	63	7.5	35.2	300	7.5	0.51
Area (mm^2)	**0.74**	**0.014**	0.33	0.34	0.57	0.6	0.014	0.015
$FoMs^*$ (dB)	**158**	**161.3**	161.1	152.2	169.7	153.2	154.5	159

*$FoMs$=SNDR+10log10(BW/P)

The switch boosting circuits are implemented for the DT-DSM to ensure sufficient on/off performance of the switches for both integrators and feedback DAC [16], so that the nonlinearities caused by switches are significantly minimized. For the CT-DSM, switch resistance is not a concern due to the CT operation and the large feedback resistance [35]. Therefore, the OTAs affect the performance of the two DSMs primarily, comparing with other circuit building blocks.

V. EXPERIMENTAL RESULTS AND DISCUSSION

The DT and CT DSMs exploiting the proposed OTAs have been fabricated in a 0.13-μm CMOS process. Fig. 10 shows the die photos of the fabricated chips. The DT-DSM occupies an active area of 0.74 mm^2, while the CT-DSM is much smaller with an active area of 0.128 mm^2.

The measurement was carried out comparatively under the same 0.3-V supply. Fig. 11 shows the measured output spectrum, where the DT-DSM achieves 74.1-dB SNDR while the CT-DSM achieves 68.5-dB SNDR. Both DSMs exhibit $>$82-dB SFDR, validating the significantly improved linearity of the proposed subthreshold amplifiers. Fig. 12 shows the measured SNR and SNDR with respect to the input amplitude for the DT and CT DSMs, respectively. Thanks to the low-noise and large output swing of proposed amplifiers, 76.5-dB DR is observed for the DT-DSM and 72.2-dB DR is observed for the CT-DSM under 0.3-V supply.

With an OSR of 64, the DT-DSM samples at 2.56 MHz with a signal bandwidth of 20 kHz, consuming 79.3 μW from 0.3 V. CT-DSM achieves higher bandwidth of 50 kHz with a 6.4-MHz sampling frequency, consuming only 26.3 μW from 0.3 V. Fig. 13 shows the power breakdown of the DT and CT DSMs. The first MC-OTA consumes $\sim$75% current of the whole DT-DSM to drive large capacitance due to the stringent requirement of kT/C noise and relatively larger GBW requirement as compared to CT systems.

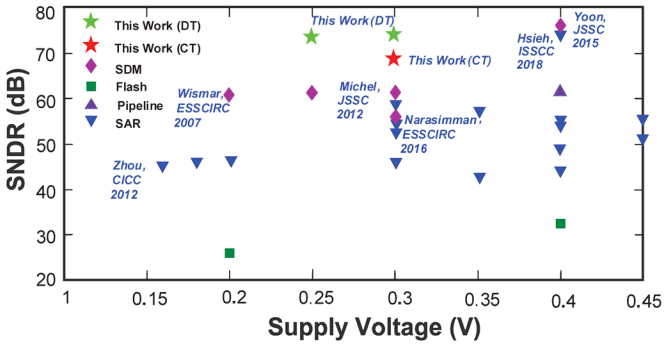

Fig. 14. Comparison with state-of-the-art sub-0.5-V ADCs.

Table III summarizes the measured performance of the DT and CT DSMs with a comparison with state-of-the-art sub-0.5-V DSMs. At a relatively lower supply of 0.3 V, both DSMs exhibit competitive performance metrics, where higher SNDR or FoMs can only be seen at DSMs with higher supply voltages. It is shown that the highest bandwidth of sub-0.5-V DSMs is achieved by the CT-DSM with the proposed FFC-OTA.

Fig. 14 plots the measured SNDR of sub-0.5-V ADCs reported to date, including both Nyquist and oversampled converters. The two DSMs are both highly competitive considering the position of SNDR together with its supply voltage. The demonstrated DSMs indicate that the proposed technique offers an interesting as well as competitive approach to subthreshold amplifier design.

VI. Conclusion

Subthreshold amplifier design has been discussed in this paper. Besides the limited signal swing, the restricted voltage headroom has prevented subthreshold amplifiers from adopting sophisticated analog techniques. An evolution procedure was proposed to convert the conventional structure to inverter-based implementations. An elementary differential amplifier was generated which is CT self-biased, allowing multistage cascading with frequency compensations. With the inverter-based CT CMFB generated from the same process, two subthreshold OTAs with significantly improved performance were designed and validated in DT and CT DSM design. Fabricated in a 0.13-μm CMOS and measured under a single 0.3-V supply, both DSMs outperform among state-of-the-art sub-0.5-V designs. It was shown the proposed subthreshold amplifier techniques provide a competitive approach to analog designs under ultralow supply voltages.

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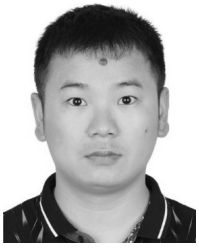

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