Analog Test Interface for IEEE 1687 Employing Split SAR Architecture to Support Embedded Instrument Dependability Applications

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***Abstract*—Embedded instruments have become ubiquitous in modern day System-on-Chips for test and monitoring purposes. IEEE 1687 or IJTAG addresses the standardization of access and operation of these embedded instruments. Recently, there has been a lot of interest in employing embedded instruments for dependability purposes. Many of these embedded instruments are required to monitor physical quantities which are analog in nature. A cost-effective architecture to integrate these analog instruments into the IEEE 1687 infrastructure is a bottleneck and has not yet been standardized. This paper presents a time and area efficient architecture to interface analog embedded instruments onto the IEEE 1687 network especially for dependability applications. The architecture mitigates the drawbacks associated with utilizing an analog test bus and enables periodic sampling with minimal hardware overhead. The simulations to illustrate the concept have been conducted with TSMC 40nm CMOS technology.**

***Index Terms*—IEEE 1687, Analog Test Bus, Monitoring, Embedded Instrument.**

I. Introduction

Modern day SoCs include several embedded instruments (EI) for various purposes such as test, debug and monitoring. The IEEE 1687 standard [1] has been developed specifically for EI access and control. The application of EIs for monitoring the health of safety-critical Cyber-Physical Systems [2] and take preventive action has become popular especially with the decreasing reliability of nanometer CMOS technologies. The integration of digital EIs has been well-defined and has served the digital community [3]. In addition to digital, analog EIs such as temperature, voltage, current monitors etc. are also essential for life-time monitoring.

The IEEE 1687.2 working group [4] has been established to extend the benefits of IEEE 1687 to the mixed-signal community. Various methods of extending IEEE 1687 for analog test [5] have been covered by the working group, some of which could be applied to monitoring. Usage of an Analog Test Bus (ATB) for monitoring analog signals has challenges such as large settling times, kick-back effects due to the switching between voltages, degradation of signal integrity etc. A concurrent sampling with local digitization technique [6] has been introduced as an alternative to ATB for measuring DC voltages. The architecture depends on a linear ramp from a digital-to-analog converter (DAC) and the time taken for access of the digital output suffers if multiple nodes with wide range of resolutions are concurrently sampled. Hence, the technique is inefficient when applied for continuous monitoring. In addition, IEEE 1687 standard was not designed to incorporate continuous sampling for monitoring purposes.

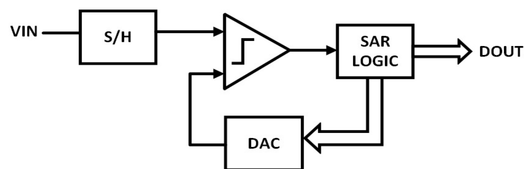

Fig. 1. Conventional SAR architecture.

A technique for fast streaming access to analog-to-digital converters (ADCs) and DACs with the "istream" PDL command has been proposed in [7]. This is under the assumption of reusing functional ADC/DAC to monitor/force analog test bus voltages. However, reusing ADC/DAC on the signal path for non-functional applications could create overheads such as routing complexity, signal integrity etc. In addition one is not able to access the instrument during device operation. Employing a dedicated ADC with time multiplexing is another alternative. However, in a typical scenario where monitors are distributed in different parts of the chip, this approach has the same overheads of an ATB such as lengthy routing of sensitive signals, kickback noise etc.

To address the above issues, this paper proposes an access-time and area-efficient architecture for integrating analog EIs employed for life-time monitoring into the IEEE 1687 framework. The key idea is employment of a "split SAR" conversion architecture for digitization. The proposed architecture mitigates the disadvantages of read-out of analog signals via an ATB and features a fully digital interface. All the analog EI signals are local to the EI and the lengthy routing is only required for digital EI signals which have a better noise immunity. The architecture includes dynamic re-configurable features and can be deployed for monitoring with periodic sampling.

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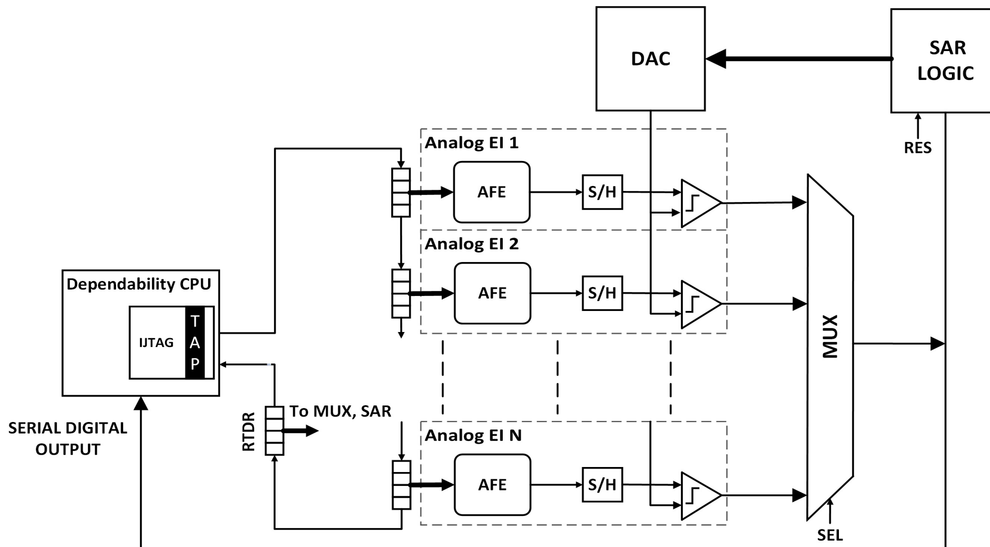

Fig. 2. The proposed split SAR architecture.

II. Proposed Architecture

Out of various ADC architectures, the Successive Approximation Register (SAR) ADC has increasingly been deployed due to its versatility for a wide range of performances in addition to the architecture being able to take advantage of technology scaling [8]. Therefore, the SAR ADC conversion technique was chosen as the base architecture to accommodate a wide range of performance requirements of various analog EIs. The advantage of technology scaling enables the architecture to be relevant with advancing technology nodes. Fig. 1 shows the conventional SAR architecture which has circuit blocks such as sample and hold (S/H), comparator, DAC and SAR Logic. In our proposed design, the circuit blocks in the conventional SAR architecture are split into two: the circuit blocks integrated into the EI and the circuits which are shared by all the EIs. Fig. 2 illustrates the proposed split SAR architecture employed in an SoC with several analog dependability EIs interfaced to the IEEE 1687 network. The dedicated dependability processor controls the operation of various EIs in addition to the execution of various dependability procedures. Each analog EI consists of a S/H circuit and a comparator in addition to the analog front-end (AFE) which generates the monitoring signals. It is provided by the EI IP provider to the system integrator. The analog EI signals are local to the EI and thus the signal integrity is improved. The SAR logic and DAC are shared by all the EIs. The DAC, which typically occupies the largest area in a SAR architecture, is shared by all the EIs and hence the area of the proposed architecture is minimized.

Some of the instruments such as a transient-current monitor would require continuous periodic sampling at high speeds. In addition, the sampling speed requirements would also vary widely for various EIs and could be much different from the IEEE 1687 clock. However, the standard was not designed with periodic sampling in consideration. The proposed architecture incorporates the feature of continuous sampling by separation of the EI outputs from the IEEE 1687 network with a minimum additional overhead of one additional wire. This is achieved by utilizing the inherent property of the SAR architecture wherein the single-bit serial comparator outputs are equivalent or complementary to the parallel digital output at the end of conversion depending on the polarity of the comparator. Hence the architecture does not require any additional parallel-to-serial-conversion circuitry. The EI to be monitored is selected via a MUX. When the particular EI along with the resolution bits are selected, one has a serial stream of data N_{EI}+2 bits in length for each sampling period; N_{EI} is the resolution of the EI and the additional 2 bits are the zero bit outputs during the sampling phase and end-of-conversion (EOC) phase. This architecture could complement the "istream" PDL command proposed in [7] with a sampling period which is not limited by the IEEE 1687 clock.

III. Design considerations and implementation

A. Analog EI IP

The analog EI IP includes the AFE which provides the monitoring signal in addition to the S/H and the comparator. The analog output signal to be measured is connected to the comparator via a S/H circuit in case of periodic sampling outputs and is directly connected to the comparator in case of measurement of DC node voltages. The design of the AFE for EIs such as a temperature and transient-current monitor has been presented in [9]. Due to the fact that EIs are not functional blocks, their designs should be optimized for the performance demanded by the dependability application with minimal area overhead. The resolution would vary for each EI depending on the factors such as sensitivity of the sensed parameter to aging and the dynamic range of the parameter. The sampling speed is dependent on the maximum rate of change of the sensed parameter. Both these specifications have

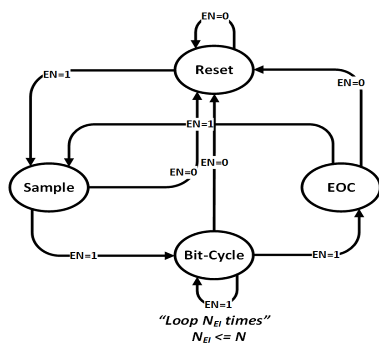

Fig. 3. State machine for a re-configurable SAR.

an effect on the S/H circuit and the comparator designs. For the resolution specification, the design considerations for an EI block are the kT/C noise and comparator input noise and offset. These noise sources are designed to be around the same magnitude as quantization noise. Double-tail latch comparator topology [10] was adopted for the implementation. For an 8-bit resolution, full-scale voltage of 0.8V and a maximum temperature of 125°C, the sampling capacitor should be greater than 7fF. The sampling-speed specification is determined by the time constant of the sampling switch and capacitor. Although a bootstrapped switch circuit [11] has been used in several works, more simple switch topologies such as an NMOS, PMOS transistor or transmission gate could suffice depending on the signal range and sampling speed thereby optimizing the design. For a clock frequency of 50kHz and an acquisition time of 10 µs, minimum sized transmission gates with low threshold transistors available in the technology were used.

B. The SAR logic and DAC

Due to the varying resolution requirements of the EIs, the data-conversion process for a fixed maximum resolution would be inefficient in terms of read-out time and power. Hence, the SAR logic block is designed to have a configurable resolution. Fig. 3 shows the state-machine of the SAR logic. The analog input is sampled into the S/H capacitor during the sampling state. During the bit-cycling state, the SAR logic approximates the input value to its digital equivalent in N_{EI} clock cycles where N_{EI} is the desired resolution of the EI to be read. The EOC state is reached when the conversion is completed and the digital output is ready. The re-configurable resolution is achieved by additional configuration bits in the test data register (TDR) for resolution and by modifying the state-machine to terminate the bit-cycle loop when the bit-cycle number matches the N_{EI} read from the TDR. The DAC being a shared resource, is designed for a maximum resolution N. In this particular paper, an 8-bit DAC is employed with binary-weighted switched capacitors. Higher resolutions are required if the architecture has to be extended for testing EIs. The SAR logic block is fully digital and is implemented using HDL in this work; it would occupy only a minimal area in nanometer CMOS technologies if synthesized.

C. The IEEE 1687 interface

As illustrated in Fig. 2 each analog EI has its own TDR. The advantage of the proposed architecture is that barring the serial digital output, the IEEE 1687 interface is the same as that of digital EIs. The TDRs are daisy-chained for illustration purposes. The TDRs consist of the configuration and calibration bits of the EIs. The setting of these bits is a one-time process in the case monitoring is required. The bits which need to be reconfigured during the monitoring phase are part of a shared TDR, referred to as reconfiguration TDR or RTDR as shown in Fig. 2. The reconfiguration TDR enables fast switching between the EIs to be read as well as setting the resolution required for the digital output. This TDR consists of select bits for selecting which EI is to be monitored and the resolution bits for the particular selected EI. The select bits in the TDR go to the MUX block, whereas the resolution bits go to the SAR logic block. The SAR logic block is set to the reset phase during the update operation of the RTDR. In addition to EI select and resolution bits, clock-selection bits for the EIs are envisioned for the architecture.

IV. Simulation Results

The proposed architecture has been designed with Cadence Virtuoso using TSMC 40nm technology libraries. The analog blocks such as S/H circuit, comparator and DAC have been designed at the technology pCell level whereas for the digital blocks such as SAR logic, HDLs were used and a mixed-signal simulation was conducted using Cadence AMS Designer simulator. Fig. 4 shows the operation of the proposed architecture. For case-study purposes, the number of analog EIs have been limited to two: namely a transient current monitor (EI 1) and a temperature monitor (EI 2). The design of the two EIs has been presented previously in [9].

The select bit *SEL* and resolution selector bits *RES* are read from the RTDR by the MUX and SAR-logic block respectively. *VREF* is the reference voltage for the DAC which is 0.8V and corresponds to the full-scale voltage expected for the EIs. In the first part of the simulation, the *SEL* bit is 0 and EI 1 is selected for data acquisition. The resolution bits *RES* correspond to 8-bit resolution which is the maximum possible resolution for the implemented design. During the falling edge of the SAMPLE signal, the EI output is sampled onto the sampling capacitor. Subsequently, the DAC output *DAC_OUT* converges to the analog output at the end of bit-cycling phase which runs for 8 (*RES*) clock (*CLK*) cycles. The *EOC* signal goes high at end of the conversion. In the second part of the simulation, an update operation occurs on the RTDR to select EI 2 which is a temperature EI with a desired resolution set to 5 bits. When the update operation takes place in the RTDR, the SAR logic block is set into reset phase by the *SAR_EN* signal for 2 clock cycles; thereafter the data acquisition starts for EI 2. Similar conversion steps such as sampling, bit-cycling and EOC also occur for EI 2. Hence, the architecture enables fast switching between various EIs with minimum latency.

DOUT is the digital output at the SAR register corresponding to the sampled EI analog output which is ready for reading

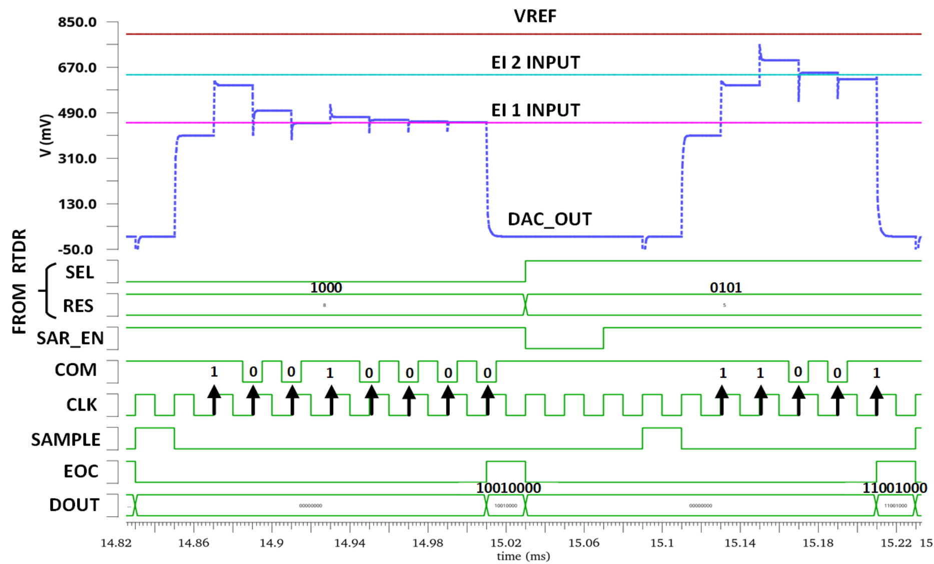

Fig. 4. Simulation results illustrating operation of the architecture.

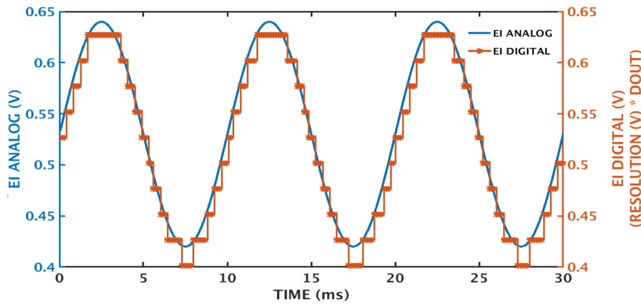

Fig. 5. Temperature EI analog output, digital output plot vs. time.

when the *EOC* signal goes high. As discussed in section II, the single-bit serial output from the comparator *COM* is used for the digital output. As shown in the figure, the serial output from the comparator matches the SAR register output for both EIs. Fig. 5 shows the digital output response from the architecture for an analog output from the temperature EI corresponding to three temperature cycles from 25°C to 125°C at a frequency of 100 Hz. The clock frequency is 50kHz and the sampling frequency is $50kHz/(RES+2)$ which is 7.14 kHz. The digital output for verification of the design is computed by multiplying the resolution in voltage by the magnitude of the digital output. The output has been digitized to the set resolution of 5 bits with a latency of one sampling interval.

V. Conclusions

In this paper, we have presented a novel cost and access-time efficient analog test interface for IEEE 1687 to support dependability applications using a split-SAR architecture. Simulation results have been presented which illustrate the operation of the architecture with a case-study of two analog EIs. Although the architecture has been developed mainly for dependability embedded instruments, the architecture can be extended to include generic analog embedded test and monitoring instruments and have a widespread use.

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