2D Materials

PAPER

Graphene-based electromechanical thermal switches

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Abstract

Thermal management is an important challenge in modern electronics, avionics, automotive, and energy storage systems. While passive thermal solutions (like heat sinks or heat spreaders) are often used, actively modulating heat flow (e.g. via thermal switches or diodes) would offer additional degrees of control over the management of thermal transients and system reliability. Here we report the first thermal switch based on flexible, collapsible graphene membranes with low operating voltage (∼2 V) and thermal switching ratio up to ∼1.3. We also employ active-mode scanning thermal microscopy to measure the device behavior and switching in real time. A compact analytical thermal model is developed for the general case of a thermal switch based on a double-clamped suspended membrane, highlighting the thermal and electrical design challenges. System-level modeling demonstrates the thermal trade-offs between modulating temperature swing and average temperature as a function of switching ratio. These graphene-based thermal switches present new opportunities for active control of fast (even nanosecond) thermal transients in densely integrated systems.

1. Introduction

Advances in modern technology have been accompanied by a surge in energy consumption and a growing need to control energy dissipation of electronics, from mobile devices to data centers [1]. Controlling energy lost as waste heat is not only desirable for increasing the energy efficiency of electronics but also critical for improving device reliability and lifetime [2]. Modern thermal management methods for electronics often include macroscale heat exchangers, such as heat sinks, heat pipes, or phase change approaches [3, 4]. These examples can be understood as *passive* thermal components, similar to thermal resistors and thermal capacitors. However, when compared to analogous electrical devices, thermal management is limited by a lack of *active* thermal devices, such as thermal transistors, switches, or diodes [5], that would be capable of manipulating heat flow in a controlled manner, similar to the routing of electricity.

A fundamental difference between active electrical components and (the relative lack of) active thermal components is that electrons obey Fermi–Dirac statistics, meaning their Fermi level can be manipulated by a gating voltage. However, heat in electronic materials is typically carried by lattice vibrations (phonons) which obey Bose–Einstein statistics, and cannot be 'gated.' Instead, phonons could be manipulated by differences in temperature, density of states, mass density [6] or by geometrical and mechanical methods such as spatial confinement and physical switching.

Among active thermal devices, thermal switches could offer the ability to regulate temperature transients and reduce thermal fatigue over concentrated

regions. A thermal switch relies on non-thermal parameters such as electric field, electrochemical potential, or pressure, to alter the device thermal conductance [5]. Several technologies have been reported for thermal switching, including liquid metal actuation [7, 8], ion intercalation between layered materials [9], externally biased phase change materials [10], and micro-electro-mechanical systems (MEMS) [11–14]. However, these devices have typically low thermal switching ratios or slow operation, which limits their potential use.

In this work, we demonstrate the first active thermal switches based on reversible, collapsible graphene membranes. These novel devices operate at low voltage (∼1–4 V with most close to ∼2 V) and could be reduced to nanoscale dimensions, operating at lower power and higher frequency. In comparison, similar thermal switches have been made with electrostatically collapsible metal membranes [11–14], however their utility is limited by high operating voltages, from 12 V to 126 V, in part due to the thickness of the metal membranes used. In contrast, graphene is an electrically and thermally conductive two-dimensional (2D) layer of carbon atoms that is ∼3.35 Å 'thick,' with the highest intrinsic tensile strength, stiffness, and in-plane thermal conductivity (2000–4000 W m^{-1} K^{-1} when suspended) of any material, comparable only to that of carbon nanotubes and diamond [15, 16]. Graphene has already been demonstrated as a promising material in nanoscale electro-mechanical switches (NEMS) [17–19], yet despite its high thermal conductivity, it has not been previously explored as a thermally conductive switching membrane.

2. Experimental work

Figure 1(a) shows an illustrated schematic of the graphene thermal switch device. Graphene microribbons are suspended over thermally and electrically insulating pillars between top (metal) and bottom (silicon) electrodes. In this 'off' state, the device demonstrates limited heat flow in the cross-plane direction. The switch is turned 'on' by applying a voltage V_A between the top (Cr/Au) and bottom (Si) electrodes to electrostatically deflect the graphene until it contacts the underlying silicon electrode. In the 'on' state, the deflected graphene membranes become channels for additional cross-plane heat flow. When the electrical bias is removed, the elastic restoring force of graphene causes the membrane to suspend, returning the device to the off state.

2.1. Device fabrication

Our devices were fabricated using high-quality monolayer graphene grown by chemical vapor deposition (CVD) [20–22]. We sequentially transferred two layers (2L) of CVD graphene (each ∼3.35 Å thick) onto 540 nm thick thermally grown SiO_2 on highly doped (n-type, 1–5 mΩ cm) Si substrates (supplementary section 1 (available online at stacks.iop.org/2DM/8/035055/mmedia)). The active regions of the graphene devices were defined using optical photolithography, a copper hard mask, and O_2 plasma etching leaving graphene channels free of photoresist residue. Top electrodes consisting of a 3 nm Cr sticking layer and 40 nm Au were deposited by electron beam evaporation which clamped the graphene to the substrate. This served both as an etch mask for the SiO_2 and as a top electrode for the final device. Approximately 500 or 540 nm of unmasked SiO_2 was removed with 20:1 buffered oxide etch (supplementary section 2), releasing the graphene membranes, which were then dried using a critical point dryer. The resulting graphene structures were thus suspended over SiO_2 pillars without collapse. An additional type of device was fabricated in which 3 nm thick Cr lines in varying geometries were deposited over the graphene, as will be shown below.

For electrical characterization, the underlying oxide was fully removed so that the graphene could electrically contact the underlying highly doped silicon, which served as a bottom electrode. For devices characterized thermally, the remaining 40 nm of SiO_2 were left to electrically insulate the scanning thermal microscopy (SThM) probe and circuit from the *in situ* electrical measurement setup (supplementary section 2). The graphene devices range in length from 12 to 24 μm, and their suspension was verified using tilted scanning electron microscopy (SEM), as shown in figure 1(b). Suspension and collapse of the electrically actuated membrane was also observed under an optical microscope during switching.

2.2. Thermal measurements

The design and dimensions of our graphene-based devices present a unique thermal metrology challenge. Due to structures that are <5 μm in lateral dimension, the spatial resolution of common optical characterization techniques such as infrared microscopy or time domain thermoreflectance is insufficient. Confocal Raman thermometry has sub-micron spatial resolution [23], however it cannot be applied to the metal regions at our device contacts, which is necessary to thermally characterize the heat flow in both the off (suspended) and on (collapsed) states. We therefore use SThM, with ∼100 nm spatial resolution, to evaluate heat flow in such NEMS devices for the first time.

SThM is an atomic force microscope technique that uses a V-shaped tip whose electrical resistance is a function of temperature. This probe tip can act simultaneously as a heater for our measured device, and as a temperature-dependent variable resistor within a Wheatstone bridge circuit [24–27]. When the device is switched, the increase of cross-plane heat flow

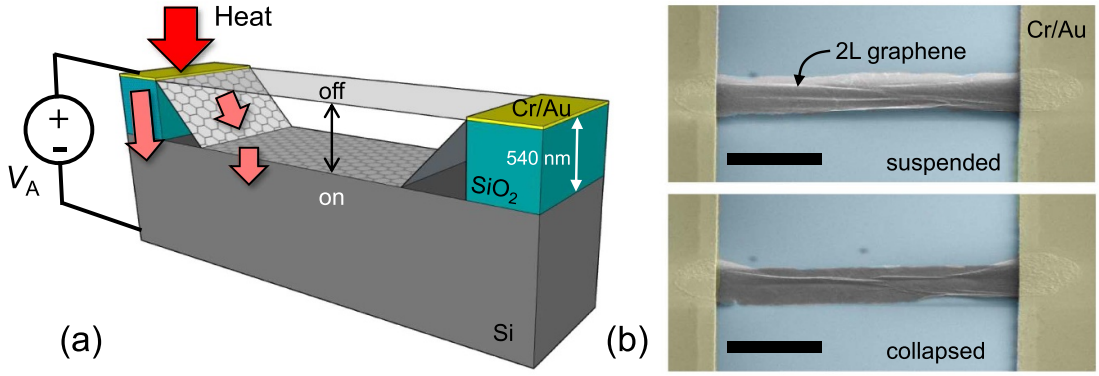

Figure 1. (a) Schematic of the electrostatic thermal switch based on a graphene membrane. The arrows indicate parallel heat flow paths, through the supporting pillar and through the graphene membrane, when this is collapsed. (Also see parallel thermal resistors in figure 2(b)). (b) Tilted, colorized SEM images of the fabricated device in the off state when the graphene is suspended and the on state when the graphene membrane is collapsed. Scale bar is 5 μm.

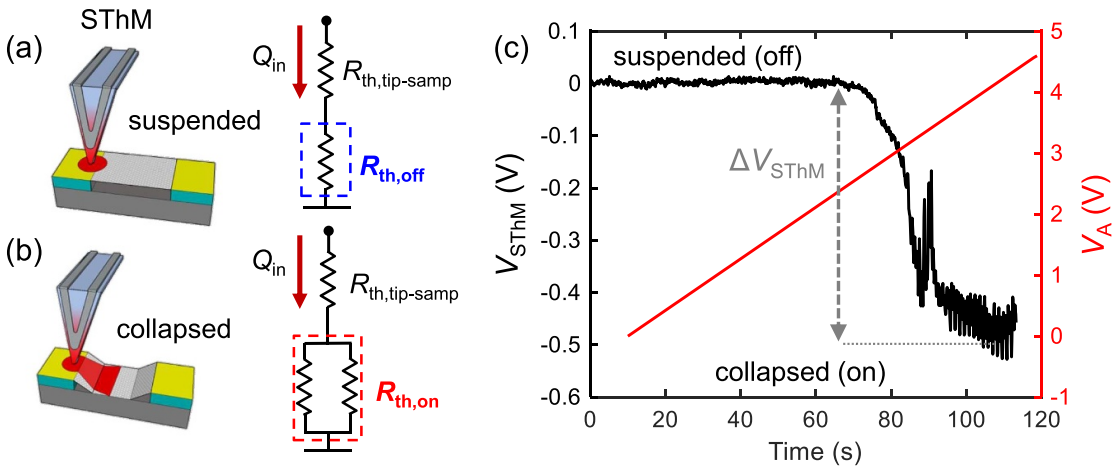

Figure 2. (a) Schematic and thermal resistance circuit of SThM measurement setup, as the graphene is suspended in the off state. (b) Schematic and thermal resistance circuit of SThM thermal measurement setup, as the graphene is collapsed in the on state. The red region illustrates the heat flow path from the SThM tip, through the graphene, into the substrate. (c) Measured voltage change in SThM circuit vs time and applied actuation voltage vs time. SThM voltage change is observed as a result of change in thermal conductance when the device is switched from off to on state. The anomaly at time ~90 s likely corresponds to the SThM tip temporarily losing contact with the metal. We note this device became stuck in the 'on' state after holding V_A for 10 s of seconds.

through the collapsed graphene causes a corresponding temperature decrease and electrical resistance change of the SThM probe tip, which is reflected in the change of SThM circuit voltage, ΔV_{SThM}. (Additional details of SThM are provided in supplementary section 3).

As shown in the schematic of figure 2(a), we place the SThM probe tip in contact with our top electrode at a fixed location near the graphene-metal edge. We employ active-mode SThM whereby the tip is electrically heated at a constant power, and we wait for the tip to reach thermal steady state. When we ramp the voltage up to 5 V between the top and bottom electrodes of our thermal switch, the graphene membrane collapses as depicted in figure 2(b), inducing a measurable voltage change of the SThM tip, as shown in figure 2(c). This represents clear evidence of the dynamically changing heat flow path from the SThM tip, through the graphene membrane, and into the substrate. Figures 2(a) and (b) display a schematic of the thermal circuit in the off (suspended membrane) and on states (collapsed membrane). Because we are measuring *differences* in tip voltage, ΔV_{SThM}, these measurements automatically eliminate extrinsic thermal effects (such as thermal convection, thermal radiation, and thermal contact resistance) between the off and on device states. We note the lateral resolution of the SThM is ~100 nm and its voltage uncertainty ranges from 3.3 mV to 28.8 mV in the off and on states in figure 2(c), respectively. (Additional details in supplementary section 3).

3. Results and discussion

From the SThM voltage changes between the off and on states of the graphene membrane device, we

calculate the resultant thermal switching ratios as follows:

$$\Delta T = Q_{\text{in}}\mathcal{R}_{\text{th}} = \frac{1}{\alpha}\left(\frac{R_{\text{probe}}}{R_0} - 1\right) \quad (1)$$

where ΔT is the temperature rise of the SThM tip above ambient, Q_{in} is the electrical power heating the SThM tip, $\mathcal{R}_{\text{th}}$ is the thermal resistance between SThM tip and thermal ground (figure 2(c)), R_0 is the electrical resistance of the SThM probe at room temperature, and α is the temperature coefficient of resistance of the Pd tip [28]. Then, the off/on thermal switching ratio ($\mathcal{R}_{\text{ratio}}$) of the device is

$$\mathcal{R}_{\text{ratio}} = \frac{\mathcal{R}_{\text{th,off}}}{\mathcal{R}_{\text{th,on}}} = \frac{\Delta T_{\text{off}}}{\Delta T_{\text{on}}} = \frac{\frac{R_{\text{probe, off}}}{R_0} - 1}{\frac{R_{\text{probe, on}}}{R_0} - 1} \quad (2)$$

where R_{probe} is the measured electrical resistance of the SThM tip.

We measured 27 devices made with 2L graphene and found their mean thermal switching ratio was 1.08 $\pm$ 0.02. This did not appear to scale with the length of the suspended membrane, suggesting that strain-related changes to the graphene thermal conductivity [29] are negligible here, ostensibly due to wrinkling apparent in our suspended devices (see, e.g. figure 1(b)).

We placed the SThM probe tip within 1 μm accuracy at the edge of our top electrode immediately adjacent to the graphene switching membrane. We carried out finite element simulations to determine the effect of SThM probe placement and collapse length of the switching membrane on the thermal measurement (supplementary section 3). Our models considered the cases of the tip placement immediately at the center of the 5 μm wide top electrode (2.5 μm away from the graphene), and near the edge of the graphene–electrode junction (200 nm away from the graphene, corresponding to the diameter of the SThM tip). Given that during measurements the SThM tip was placed within 1 μm of the graphene–electrode junction, it is estimated from the finite element model (supplementary section 3) that the error from tip placement in measuring the thermal switching ratio is <0.02.

3.1. Compact analytical model

To gain physical insight for optimizing the thermal switch design, we developed a compact analytical model of the thermal switching ratio. The thermal switching ratio is defined as the ratio of the off-state thermal resistance to the on-state thermal resistance, given by:

$$\mathcal{R}_{\text{ratio}} = \frac{\mathcal{R}_{\text{th,off}}}{\mathcal{R}_{\text{th,on}}} \approx 1 + \frac{t_{\text{stack}}}{k_{\text{stack}} \cdot L_{\text{contact}}} \times \left(\frac{\mathcal{R}_{\text{th,boundary}}}{L_{\text{collapse}}} + \frac{L_{\text{total}} - L_{\text{collapse}}}{k_{\text{membrane}} t_{\text{membrane}}}\right)^{-1} \quad (3)$$

where t_{stack} is the height of the insulating pillar and k_{stack} its thermal conductivity, while t_{membrane} and k_{membrane} refer to the thickness and thermal conductivity of the switching membrane, respectively, illustrated in figure 3(a). L_{contact} is the length of the metal contact clamping down the switching membrane and L_{total} is the total length of the free-standing membrane in the off state. L_{collapse} is the length of the collapsed region after the device is switched on, and is a function of the applied voltage based on an electrostatic model (supplementary section 4). The thermal boundary resistance of the collapsed graphene with SiO_2 is $\mathcal{R}_{\text{th,boundary}} \approx 2 \times 10^{-8}$ m^2 K W^{-1} [6, 30].

We used our thermal model in conjunction with a modified electrostatic model developed by Bao *et al* [31] (supplementary section 4) to simulate the expected thermal switching ratios as a function of applied voltage. Figure 3(b) shows the abrupt change in thermal switching ratio at the mechanical pull-in condition. We note that while the measured thermal switching ratio is comparable to the results of the compact model, the measured switching voltage is significantly lower than the predicted values. This observed low voltage switching is most likely due to a graphene membrane which was not initially taut, whereas the model is based on a taut membrane with no initial deflection. For example, during the polymer-assisted transfer process wrinkles are introduced to the graphene on a flat substrate. Upon suspension and release, the wrinkles unfold under the strain of the now doubly clamped suspended graphene membrane [32].

We derived our device design principle based on the compact model, with consideration for electrical and thermal parameters. From an electromechanical perspective, we designed the suspended structure to have low height-to-length aspect ratio, and a thin (sub-nanometer) switching membrane in order to minimize the actuation voltage. We fabricated membranes ranging from 12 to 24 μm in length (L_{total}), with an average actuation voltage of 2.2 V; these are all much lower than ~40 V in [31], which used ~3 μm long graphene membranes. However we observed no trend of the actuation voltage vs membrane length (see supplementary figure S6), ostensibly due to variations in wrinkling right after fabrication, as noted in figure 1(b). On the other hand, from a thermal perspective, our model shows that it is critical to minimize off-state thermal leakage, either through materials selection or by increasing the height of the device support pillars, and a thicker switching membrane to maximize on-state thermal conductance.

Our compact model predicts that while a device with a membrane consisting of multiple (~10) layers of graphene has an improved thermal switching ratio, it is also predicted to have a significantly increased switching voltage compared to a device with only two graphene layers. To increase the switching membrane

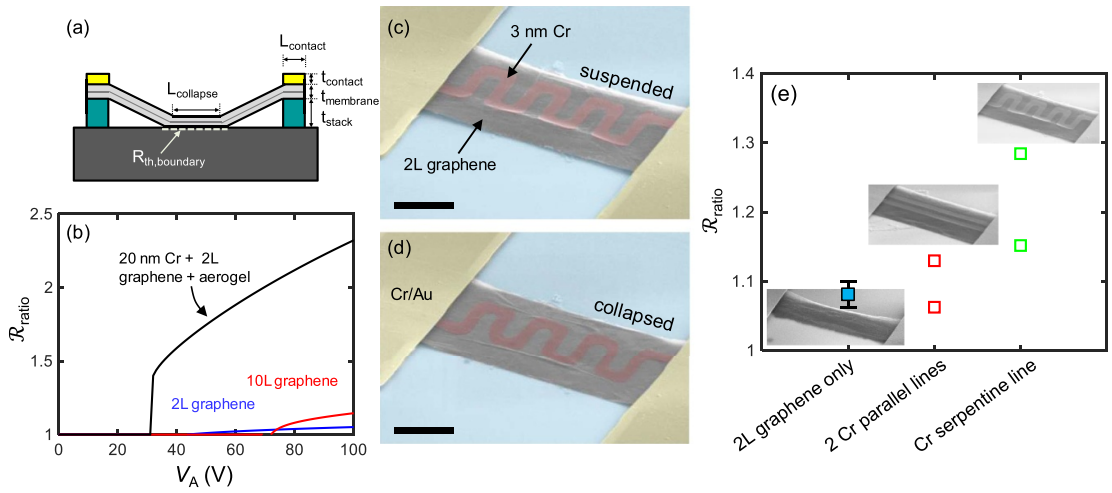

Figure 3. (a) Cross-section schematic of the device showing parameters of the compact model. (b) Calculated change in thermal conductance vs applied voltage based on the compact analytical model, for three different scenarios: two layers (2L) of graphene, ten layers (10L), and 2L with 20 nm thick Cr serpentine and low thermal conductivity aerogel under the metal contacts instead of SiO_2. (c, d) Tilted SEM images of suspended graphene devices patterned with additional serpentine Cr lines in the off (suspended) and on (collapsed) states. Scale bar is 5 μm. (e) Summary of measured thermal switching ratios across all our devices. For devices with only 2L graphene, the average $\mathcal{R}_{ratio}$ of 27 devices is shown, with error bars indicating standard deviation.

thickness and thermal conductance in a facile manner, we deposited additional lines of 3 nm thick chromium (Cr) over the graphene in various geometries (supplementary section 5). We made devices with two parallel line Cr beams over the graphene, and were able to measure an improved thermal switching ratio up to 1.13, as shown in figure 3(e).

We also patterned serpentine Cr structures over the graphene as shown in figures 3(c) and (d), which increased the coverage of metal on graphene while remaining flexible enough to not significantly increase the switching voltage of the device. These devices reached thermal switching ratio up to 1.28 (see figure 3(e)) with an average actuation voltage of $V_A \approx 3.5$ V. The graphene integration in such a NEMS structure is critical, because the taut underlying graphene allows the flexible serpentine metal to remain suspended. Figure 3(e) summarizes the measured off/on ratio for all graphene-based thermal switches measured in this work and supplementary figure S6 summarizes all switching voltages. Based on our thermal model described above, several improvements can yet be made to optimize the thermal performance of such a graphene switch. For example, if SiO_2 is replaced with low thermal conductivity dielectrics such as porous silica or alumina aerogels with thermal conductivity of $\sim$0.1 W m^{-1} K^{-1}, and serpentine metal lines of 20 nm thick chromium are patterned over 50% of the graphene, a thermal switching ratio $\mathcal{R}_{ratio} > 2$ could be achieved according to our calculations, as shown in figure 3(b).

3.2. System level simulations

There are several temperature-dependent failure mechanisms in microelectronics, including packaging thermomechanical failure, metal diffusion, and leakage currents which exponentially increase with temperature [2]. One promising application of thermal switches is thermal regulation, as discussed in [5]. When deployed as a thermal regulator, a thermal switch is able to reduce the temperature fluctuation of a microelectronic component or system undergoing time-varying heat loads, thus reducing its thermal fatigue [5]. This section analyzes the thermal system and periodic operating condition shown in figure 4(a) to provide insight into the impacts of the thermal switching ratio on temperature regulation. The system consists of a periodic heat source Q, which represents the heating of a CPU or power inverter, with period P and duty-cycle D, where $0 < D < 1$. This heating source has a temperature T_d and a thermal capacitance C_d. The thermal switch with thermal resistance, $\mathcal{R}_{th}$, is placed between the heat source and a heat sink with constant temperature, T_s. To achieve thermal regulation, the thermal switch is operated as shown in figure 4(b), such that it is 'on' during the heat load, $\mathcal{R}_{th} = \mathcal{R}_{th,on}$, and 'off' in between heat loads, $\mathcal{R}_{th} = \mathcal{R}_{th,off}$. Thus, the thermal switch is capable of reducing the amplitude of the temperature oscillations, $T_{amp} = T_{max} - T_{min}$, when compared to the case where the thermal switch is always on. However, this reduction in amplitude comes at the cost of increasing the average temperature of the system, $T_{ave} = 0.5\,(T_{max} + T_{min})$. Thus, the goal is to design a thermal switch that minimizes T_{amp} without significantly increasing T_{ave}.

To determine the effects of the thermal switch ratio, $\mathcal{R}_{ratio}$, on T_{amp} and T_{ave}, the differential equation for the device temperature is given by

$$C_d \frac{dT_d}{dt} = Q - \frac{1}{R_{th}}(T_d - T_s). \quad (4)$$

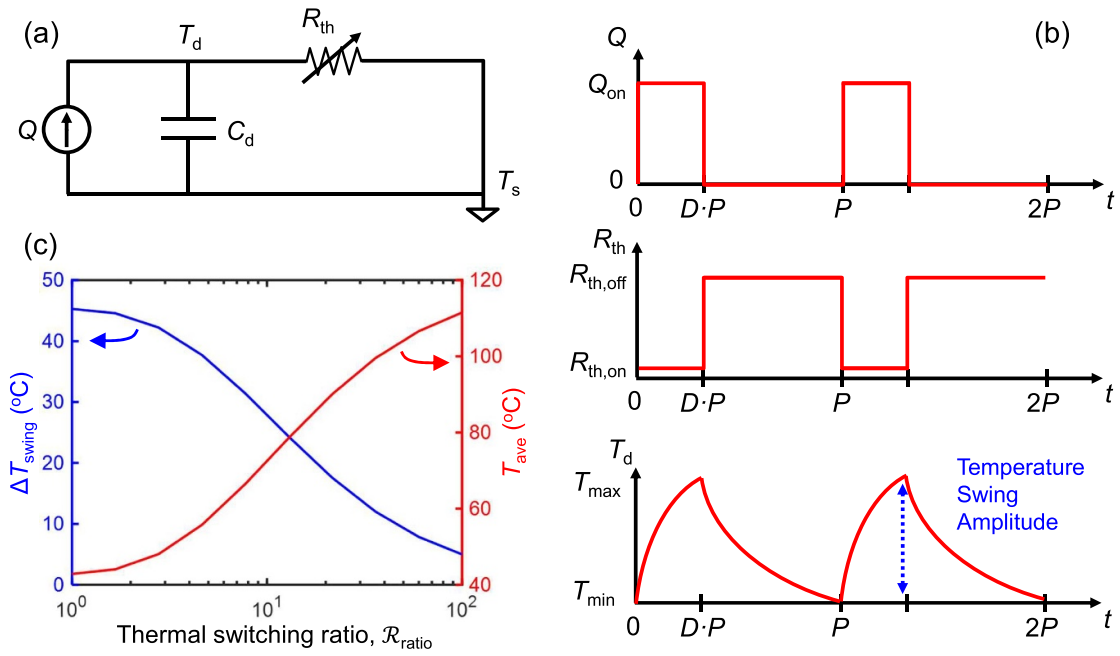

Figure 4. System-level impact of thermal switch. (a) Thermal circuit of thermal switch with heat load. (b) Schematic plot demonstrating proposed switching with a variable heat load and resultant temperature swing. (c) Plot of temperature swing amplitude and average temperature as a function of thermal switching ratio for a 1 × 1 cm system with 100 W heat operating at kHz frequency.

Analyzing each of the two modes of operation it is possible to derive the following analytical relationships for T_{amp} and T_{ave}:

$$T_{amp} = \mathcal{R}_{th,on} Q_{on} \frac{\left(1 - e^{-\theta\varphi}\right)\left(1 - e^{-\theta}\right)}{1 - e^{-\theta(1+\varphi)}} \quad (5)$$

$$T_{ave} = T_s + \frac{1}{2}\mathcal{R}_{th,on} Q_{on} \frac{\left(1 + e^{-\theta\varphi}\right)\left(1 - e^{-\theta}\right)}{1 - e^{-\theta(1+\varphi)}} \quad (6)$$

where $\theta = DP/(C_d \mathcal{R}_{th,on})$ and $\phi = (1/\mathcal{R}_{ratio}) * (1/D - 1)$. While these relationships are applicable to any thermal switch design and operation, it is valuable to consider a particular case to observe the benefit of the thermal switch. For a 1 × 1 cm area representative of the periodically heated system, the parameters can be approximated as $Q_{on} = 100$ W, $P = 10^{-3}$ s, $D = 0.1$, $C_d = 1.7 \times 10^{-4}$ J K^{-1}, and $T_s = 20$ °C. Assuming the thermal switch is designed to achieve on-state resistivity $\mathcal{R}'_{th,on} = 10^{-4}$ m^2 K W^{-1} (per area), figure 4(c) shows the effect of $\mathcal{R}_{ratio}$ on T_{amp} and T_{ave}.

The results of this model demonstrate there is an optimal switching ratio where the temperature swing amplitude can be reduced at the cost of increasing the average temperature. Figure 4(c) illustrates that with no thermal switching ($\mathcal{R}_{ratio} = 1$) thermal spikes in the form of temperature swing amplitude may exceed 40 °C. As $\mathcal{R}_{ratio}$ increases, the temperature swing decreases while the average temperature increases. However if $\mathcal{R}_{ratio}$ is too high, the average temperature of the system can increase to the point of inducing failure (e.g. interconnect failure in microelectronics [2]). Under the above state conditions, in this model we find that $\mathcal{R}_{ratio} > 10$ would not be optimal from a thermal budget perspective. The parameters also highlight the significance of geometry, materials, and switching speed on the system-level impact of thermal switches (supplementary section 6). The equivalent thermal resistance of the thermal switch is ideally low in the on- and high in the off-state for a better switching ratio. However, if either state has high thermal resistance, the average temperature of the system will rise. Moreover, at higher switching speeds the thermal switch becomes limited by its thermal time constant and the thermal switching ratio has less impact on the temperature swing amplitude. Both of these results highlight the need for high thermal conductivity materials with low thermal boundary resistance interfaces in the design and implementation of thermal switches.

3.3. Reversible cycling

Reversible cycling of the thermal switch was verified by electrical measurements and thermal testing by SThM. Voltage pulses of 1.5 V amplitude and 30 s width were applied to the device and the cross-plane current through the graphene to the Si substrate was measured, as shown in figure 5(a). (The cross-plane electrical measurement was enabled by extending the liquid etch to remove all underlying SiO_2, allowing the graphene to contact the underlying Si.) A gradual decrease of on-state current is attributed to electrostatic attraction of ambient particles and possible damage of the graphene at the edge contacts. However, we can verify the graphene is fully suspended in

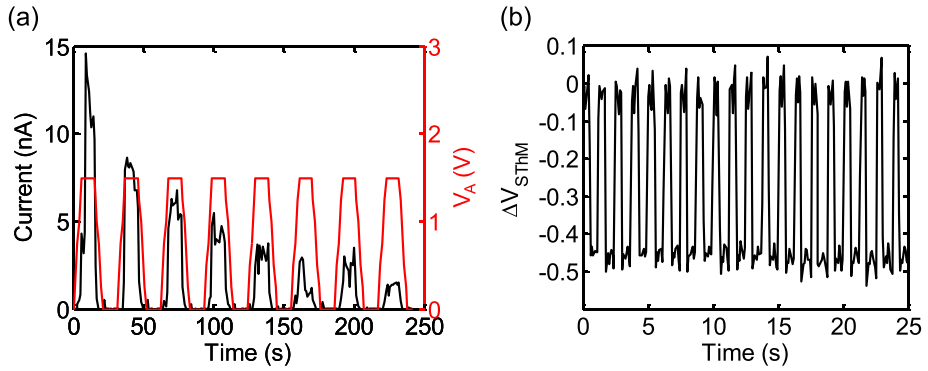

Figure 5. Repeatability of electrical and thermal switching. (a) Measured current between top electrode and Si substrate when the graphene membrane is actuated by a train of voltage pulses. (b) Measured SThM voltage as a function of time as the graphene membrane is repeatedly collapsed and released (suspended). The bottom (low) ΔV_{SThM} values correspond to the collapsed state of the graphene switch.

the off-state, as the off-state current reaches the noise floor of the measurement (∼pA).

To directly measure thermal resistance switching, we used the SThM probe tip to mechanically collapse and suspend the graphene membrane, by pushing on the graphene near the electrode edge. Figure 5(b) displays this measurement, clearly demonstrating repeatable thermal cycling, where the changes in ΔV_{SThM} correspond to changes in the heat flow path between the SThM tip and the Si substrate. These measurements show a switching frequency of 0.8 Hz, which is limited by the scanning rate of the SThM tip. However, previous studies have shown NEMS resonators made with suspended graphene can reach the MHz range [33], suggesting that such thermal switches may be among the fastest achievable. Speed of switching may not be limited by mechanical resonance alone; we must also consider the thermal time constant of the device, or how quickly the device can heat and cool. The thermal time constant is given by $\tau \approx \rho c_p V \mathcal{R}$ where $\mathcal{R}$ is the thermal resistance, c_p the material specific heat, ρ the material density, and V the volume of the body. Dollerman *et al* [34] have measured 25–250 ns as the thermal time constant for 2–5 μm wide suspended graphene membranes. The thermal time constant will further increase when factoring in the additional thermal boundary resistance of graphene as it makes contact with the underlying substrate.

One common concern with MEMS reliability is the issue of stiction, or irreversible collapse of the membrane [17]. Variables that may mitigate the effects of stiction for our device include the surface roughness of the underlying substrate and the number of graphene layers, both of which impact the adhesion energy between graphene and the bottom surface. This occurs because the bending modulus of graphene increases with number of layers, which in turn impacts its ability to conform to a nano-textured surface [35, 36]. A circular switch structure could minimize graphene tearing and reduce graphene-substrate contact area for a more mechanically reliable switch [37]. However, these methods of reducing stiction are likely to be accompanied by a trade-off in thermal switching ratio, as diminished graphene adhesion is expected to increase thermal contact resistance, and a circular switch geometry would introduce additional thermal leakage paths.

4. Conclusions

In conclusion, we designed and fabricated the first graphene-based NEMS thermal switch and demonstrated multiple, reversible electrical and thermal switching at low electrostatic actuation voltages (∼2 V). We have also realized the first practical demonstration of thermal metrology for a NEMS device using active mode SThM. A compact analytical model shows the thermal performance of our device can be improved by adding flexible metal structures stacked on atomically thin membranes. This is experimentally demonstrated using graphene switches patterned with overlying serpentine Cr lines, which reach close to ∼1.3 thermal switching ratio. Additional modeling demonstrates the effect of active thermal switching on a system under varying heat load, and illustrates the trade-off between reducing temperature swing and average temperature as a function of thermal switching ratio. The results of this work demonstrate the feasibility of implementing high thermal conductivity materials in nanoscale thermal switches, and are essential for the future design and implementation of active thermal management for densely integrated systems.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgments

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