A Single-Trim Frequency Reference Achieving ± 120 ppm Accuracy from -50 to 170 °C

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***Abstract*—A single-trim, highly accurate Colpitts-based frequency reference is presented. Our analysis shows that the Colpitts-topology outperforms the cross-coupled LC-topology in terms of temperature stability. Measurements on prototypes in a 0.13 μm high voltage CMOS SOI process were carried out from -50 to 170 °C. Based on sample-specific single room temperature trim and batch calibration, our frequency reference achieves an accuracy of ± 120 ppm for 16 samples from a single wafer utilized for extracting the batch-calibration polynomial, and ± 300 ppm for 48 samples across 3 wafers from the same batch. This is a 4x improvement over related single-trim state-of-the-art solutions. Frequency drift due to ageing, tested after a 6-day 175 °C storage, is below 100 ppm. The oscillator core dissipates 3.5 mW from a 2.5 V supply and has 220 ppm/V supply-sensitivity without supply regulation.**

***Index Terms*—Frequency reference, batch calibration, Colpitts oscillator, single-trim, temperature stability, trimming.**

I. Introduction

ACCURATE frequency references are crucial in many electronic systems to be compliant to wired and radio communication standards and timing specifications. Accurate fully-integrated on-chip frequency references are highly desirable to replace bulky, expensive external frequency references like quartz crystal oscillators (XO).

The required accuracy of a frequency reference is application-dependent. Wireline applications, like 1G Ethernet, require frequency accuracies up to ± 100 ppm [1], while wireless applications require even stricter accuracy levels. These accuracy levels must be achieved over a wide range of operating conditions, including process-voltage-temperature (PVT) variations, ageing, and mechanical stress.

Trimming may be used to achieve the required absolute frequency accuracy level. However, the challenge is to guarantee sufficient performance while simultaneously achieving high yield and low production/test costs. For example, multi-temperature trimming after packaging is expensive and significantly adds to the production costs. For low-cost applications, single temperature trimming at wafer level is highly desirable. Bulky and relatively expensive quartz crystal oscillators are the de-facto standard solution in the industry. These oscillators have ppm-level accuracy and minimal temperature dependency. The drawback of quartz crystals is the low-level of integration and the need for a hermetically sealed package. A higher level of integration is achieved by MEMS oscillators, where a mechanical resonator is implemented in hermetic cavities in/on a CMOS die [2]–[4]. These frequency references are becoming increasingly popular. However, on-chip hermetic cavities are not compatible with the standard CMOS processing flow and hence require extra processing steps that add costs. Bulk acoustic wave (BAW) resonator based oscillators that utilize a dual-Bragg acoustic resonator (DBAR) do not need hermetic cavities and are feasible with inexpensive non-hermetic plastic packages [5]. Stacked on top of a CMOS die containing the active circuitry these oscillators achieve sufficient accuracy for wireless applications [5].

In an attempt to eliminate mechanical resonators and move to single die, fully integrated solutions, several on-chip frequency references have been published [1], [6]–[19]. The Colpitts LC-oscillator in [10] obtains the highest reported frequency accuracy with ± 1.7 ppm over a 80 °C operating range, but requires trimming at 16 temperatures per sample. Using two-point temperature (2T) trimming per sample, the highest reported accuracies for an LC- [16] and RC-based [6] frequency reference are ± 50 ppm over a temperature range of 105 °C and ± 200 ppm over 130 °C respectively. To the best of our knowledge, the work in [20] reports the best single temperature (1T) trimmed frequency reference. The RC-based reference with a frequency locked-loop achieves an accuracy of ± 400 ppm over 130 °C.

We present a Colpitts-based frequency reference, parts of which were introduced in [21]. Using only 1T-trimming per sample, the measured frequency accuracy is on par with the 2T-trimming work presented in [16], but over the much wider temperature range of -50 to 170 °C. For 1T-trimming solutions, the frequency stability is improved by a factor of 4 compared to the state-of-the-art.

In addition to [21], detailed analyses of the frequency temperature coefficient of both the cross-coupled LC-oscillator and the Colpitts-oscillator are presented. This analysis shows that the latter is inherently more stable over temperature for frequencies in the low GHz range (e.g. 1-3 GHz). Also the most important aspects of achieving maximum frequency stability will be addressed. This paper is extended with multi-wafer measurements and accelerated lifetime test results to demonstrate the robustness of our approach. Lastly, device

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characterization results of the implemented inductor and capacitors are included.

The paper is organized as follows: frequency stability and different trimming approaches are discussed in Sections II and III, respectively. The oscillation frequency and its temperature dependence of the cross-coupled LC-oscillator and Colpitts-oscillator are analyzed in Section IV. Section V discusses the circuit level implementation of the presented frequency reference, and Section VI provides the measurement results. Conclusions are drawn in Section VII.

II. Stability of On-Chip Components

The implementation of the time-constant of an integrated oscillator is crucial for the stability and accuracy of frequency references. Excluding mechanical resonators and propagation-speed-dependent oscillators as in [7], the components of choice to define the oscillation frequency are typically on-chip resistors, capacitors, and inductors. All these components and their parasitics are typically process and temperature-dependent. They may also be dependent on voltage and mechanical stress and may be prone to ageing effects. These aspects will briefly be discussed in the following subsections.

A. Temperature dependency

The impedance of passive components includes a (temperature-dependent) interconnect resistance while its key parameter is also temperature-dependent. This key parameter can be e.g. capacitance, inductance or resistance of the component.

The resistance of a material depends on both the number of mobile carriers and carrier mobility in that material. For resistors implemented in a semiconductor material, this typically results in a nonlinear $R(T)$ with an additional significant voltage dependency. For resistors in the backend — which includes interconnect resistances — the temperature dependency is quite linear and well-defined [22].

The temperature dependency of backend metal-oxide-metal (MOM) capacitors results from thermal expansion and a temperature-dependent change in the oxide dielectric properties [23]. Capacitors using non-degenerate semiconductor material [24] for at least one capacitor plate show a significant nonlinear temperature and voltage dependency.

The inductance of a spiral inductor is mainly determined by its diameter (typically 100–300 μm) and the number of windings (typically 1–5). The temperature-dependency of the metal conductivity affects the skin-depth and eddy-currents, which vary the self-inductance and affect inductor temperature coefficient [10], [25], [26]. Physical dimensions of the inductor are negligible affected by e.g. thermal expansion [25], [27].

The temperature sensitivity of passives can be expressed as a Taylor series as

$$X(T) \quad = \quad X_{T_0}(1 + \mathrm{TC_X} \cdot \Delta T + \mathrm{TC_{X2}} \cdot \Delta T^2 + \ldots)$$

where $X \in \{R, L, C\}$ denotes the type of passive component, and where X_{T_0} is the component value at some reference temperature T_0 (e.g. 27 °C), $\mathrm{TC_X}$ and $\mathrm{TC_{X2}}$ are the linear and quadratic temperature coefficients which are usually expressed in ppm/°C and ppm/°C^2, respectively, and ΔT the temperature difference w.r.t. T_0. The work in [10], [23] report $\mathrm{TC_L}$ and $\mathrm{TC_C}$ at roughly 30 ppm/°C, where the exact temperature coefficients depend on the technology and structure of the devices. For a copper interconnect $\mathrm{TC_R}$ is around 4000 ppm/°C [22].

B. Process spread

The characteristics of doped semiconductor devices (such as poly-resistors, transistors, and diodes) depend, besides temperature, heavily and nonlinearly on the doping levels in and around the component. They are, therefore, highly sensitive to process spread. For backend components such as metal resistors, MOM capacitors and inductors, the spread is mainly in layer thicknesses, which translates in a (proportional) change of the component values. The proportional change ideally doesn't give residual spread after single trim.

C. Ageing

Components may change (degrade) over lifetime and thereby shift their electrical behavior. For components realized in a semiconductor material, significant degradation effects are due to dopant (de)activation, hot carrier injection, hydrogen release, etc. [28], [29]. These ageing effects may result in a drift of the transistor parameters such as threshold voltage, current factor, capacitance and more. Similarly, properties of junctions, varactors and passives in the process front end shift over time.

For components and interconnect realized in the process backend, the major degradation effect is generally electromigration, which is irrelevant for oscillators due to the relatively low current density levels. Other ageing mechanisms for backend devices are not explicitly reported in literature to the best of our knowledge. Previous LC-based frequency references report frequency drifts up to $100 - 200$ ppm over reliability tests such as highly accelerated stress test (HAST) and high-temperature operation lifetime (HTOL) [12], [16].

D. Mechanical stress

Mechanical stress on the silicon die can be induced by e.g. different thermal expansion of the silicon die and the plastic encapsulation of cost-efficient plastic packages. This causes static and random variation in frontend devices, such as CMOS transistors, BJTs and resistors [30]–[32]. Existing solutions include package-level trimming, addition of a stress-relief layer [30], [32] or using a ceramic package [30] instead of a plastic package. All these solutions add to production costs.

E. Wrap up

From the previous subsections, it follows that for a maximally stable oscillator, the impact of frontend components, such as transistors, (poly-)silicon resistors and varactors, on the oscillation frequency should be minimized. In contrast, backend components — realized in metal and oxide only — show much lower aging effects and demonstrate significantly

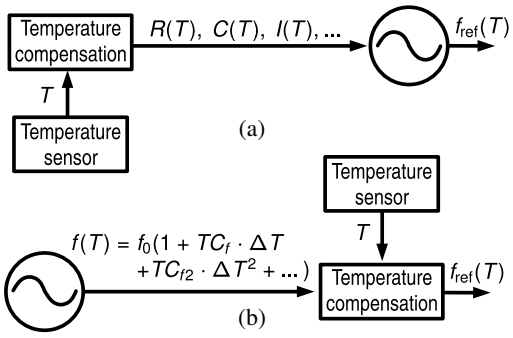


Figure 1. Frequency compensation: (a) T-dependently changing oscillator component's values (b) T-dependently post-processing the oscillator frequency.

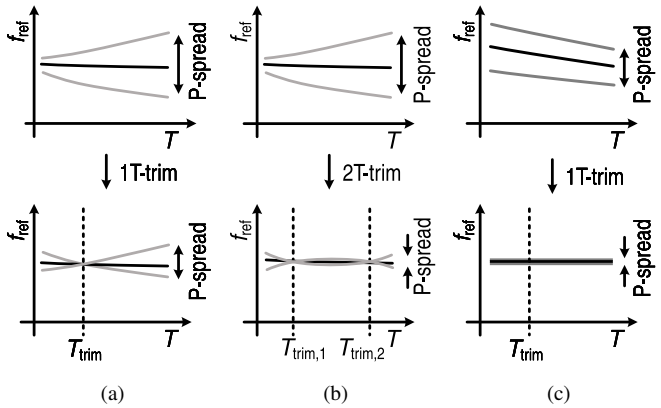


Figure 2. Pre- and post-trim behavior of f_{ref} over temperature and different process corners (P-spread) with (a) 1T-trim, (b) 2T-trim (c) 1T-trim in case of a well-behaved temperature dependency.

better defined temperature dependencies. However, a minimum amount of frontend devices is required to sustain oscillation. We restrict the remainder of this paper to LC-type oscillators where the inductor(s) and the capacitor(s) are realized in the CMOS process's backend.

III. Frequency trimming

Typical on-chip high-accuracy frequency references consist of three parts: an oscillator, a temperature compensation block, and a temperature sensor. Without temperature compensation, an actual oscillator produces a temperature-dependent oscillation frequency $f(T)$ due to the temperature dependency of the components that determine the oscillation frequency (e.g. the inductor $L(T)$ and the capacitor $C(T)$ in an LC-oscillator). Figure 1a shows temperature compensation of an oscillator by temperature-dependently electronically adapting component values in the oscillator, as done in e.g. [9], [10], [12]–[15]. Figure 1b depicts temperature compensation applied to the temperature-dependent oscillation frequency of the oscillator, as done in e.g. [8], [16], [17]. Both approaches aim to achieve a temperature-independent reference frequency f_{ref}.

In both approaches the polynomials in the temperature compensation block are preset in the design, and coefficients are adapted using production trimming. Process variation yields both a shift in the reference frequency as well a change in the $f_{\text{ref}}(T)$-slope that may be uncorrelated or (partially) correlated with the shift in f_{ref}. Only the correlated part can be compensated by an 1T-trim, as shown in Figure 2a for pre-trim and resulting 1T-trim behavior. Extending the 1T-trim to a 2T-trim allows the spread in the average gradient to be compensated; the corresponding pre- and post-trim behavior is depicted in Figure 2b.

Pre-trim spreading $f_{\text{ref}}(T)$ that is mainly a scaled version of the nominal $f_{\text{ref}}(T)$ can be compensated by a *fixed* temperature compensation polynomial and a 1T-trimmed frequency divider to obtain 1T-trim post-trim behaviour as shown in Figure 2c. In this work, we aim at high-frequency stability with 1T-trimming per sample using a fixed low order batch calibrated temperature compensation polynomial, requiring the pre-trim temperature behavior in Figure 2c.

In Figure 1b, the temperature compensation block can be implemented in several ways in the system setup. The conventional options include using a fractional divider [16] or the usage of a PLL [33]. We aim at a slightly different system that also effectively implements a fractional divider function: we employ a free-running low-power current controlled oscillator (CCO) that is regularly re-trimmed so that a long term stable, temperature-independent frequency is obtained from the CCO. The internal re-trimming uses the LC-oscillator described in this paper as an accurate frequency reference. This system combines the low-power properties of the CCO and the LC-oscillator's high-accuracy properties; which has similarities with the work in [33]. The system's accuracy is determined by that of the LC-oscillator, which is the current paper's focus. For this paper, we implemented temperature compensation as an ideal fractional divider in software.

IV. Temperature Stability of LC-Oscillators

Prior art LC-based frequency references [1], [9]–[19] report high frequency-stability ($\leq$200 ppm) over PVT and lifetime. To compensate the frequency drift over temperature many of these designs use temperature-controlled varactors [1], [9]–[11] and hence implement the approach in Figure 1a. The varactor is then part of the tank capacitance and is controlled by a temperature-dependent voltage. Other compensation techniques include the so-called 'TNULL' principle to operate the oscillator at a more temperature stable phase of the tank impedance [19], [34], or deliberately lowering the Q-factor of the tank capacitance [12] which counteracts the inherent temperature drift.

These techniques introduce extra frontend components (transistors, varactors) to the oscillator core, aiming to compensate temperature dependencies but introducing new ones at the same time. In the work in [8], [16], [17] a non-tunable oscillator core is followed by a variable fractional divider, implementing the approach depicted in Figure 1b. This maximizes the tank frequency stability (as well as quality factor). The division ratio of the dividers in [16], [17] is controlled from a temperature sensor and a look-up table

(LUT). The LUT is filled during post-processing by a sample-specific 2T-trim (at 0 and 70 °C).

Although the majority of the LC-based frequency references can achieve the required frequency accuracy of ± 100 ppm over the commercial temperature range (0 to 70 °C), none of them achieves this with a 1T-trim. The main reason for the relatively narrow temperature range is the effect of process spread on the oscillation frequency's temperature dependency. This yields a 1T-trim behavior similar to that in Figure 2a, thus requiring multi-T trims to achieve the reported accuracy levels and temperature ranges.

The majority of prior art LC-based frequency references use a cross-coupled LC-oscillator topology [1], [9], [11]–[19]. Reasons for its popularity include the reported superior phase noise performance in the $1/f^2$ region [35], its associated benefits for transmit/receive systems and ease of implementation.

However, the focus of this work is to obtain a stable frequency over PVT and lifetime, where we do not target the very tough phase noise specifications required for high data rate transmitters/receivers. It is known that various types of LC-oscillators, like Colpitts or cross-coupled LC-oscillator, have different sensitivities to, e.g. the quality factor of L and C [36]. Related to this, [10] claimed that a Colpitts oscillator's temperature dependence is less sensitive to the variation of Q_{L} than that for the cross-coupled LC-oscillator but this was not quantified. The next subsections present a comparison of the temperature sensitivity for 3 basic LC-oscillators: of an ideal LC-oscillator, the cross-coupled LC-oscillator, and the Colpitts oscillator.

A. The Ideal LC-oscillator

The oscillation frequency of an ideal lossless LC-tank is

$$f_{\mathrm{osc}} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

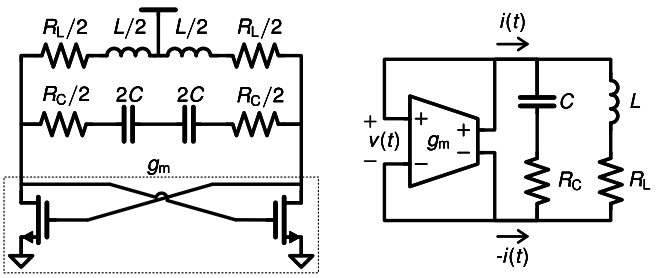
where L is the inductance and C is the capacitance of the LC-tank. Temperature-dependent $L(T)$ and $C(T)$ result in $f_{\mathrm{osc}}(T)$. The first-order temperature coefficient of f_{osc} is defined as

$$\mathrm{TC_f} \triangleq \frac{1}{f_{\mathrm{osc}}}\frac{\partial f_{\mathrm{osc}}}{\partial T} = \frac{1}{f_{\mathrm{osc}}}\left(\frac{\partial f_{\mathrm{osc}}}{\partial L}\frac{\partial L}{\partial T} + \frac{\partial f_{\mathrm{osc}}}{\partial C}\frac{\partial C}{\partial T}\right). \tag{2}$$

Assuming first-order temperature dependency for $L(T)$ and $C(T)$, then Equation (2) yields

$$\mathrm{TC_f} \approx -\frac{\mathrm{TC_L}}{2} - \frac{\mathrm{TC_C}}{2}. \tag{3}$$

This first-order approximation of $\mathrm{TC_f}$ is independent of the actual values of L and C itself, which eliminates their impact on process spread of $\mathrm{TC_f}$. The $\mathrm{TC_L}$ and $\mathrm{TC_C}$ are mainly defined by backend metal and oxide properties and hence show a very low (process) spread. Measured values for the temperature coefficients, for our specific technology and implementation and at the 1.5 GHz oscillation frequency of our oscillator, are $\mathrm{TC_L} \approx 75$ ppm/°C and $\mathrm{TC_C} \approx 15$ ppm/°C, see Section VI-A. Using these numbers, the $\mathrm{TC_f}$ of an ideal LC-tank is about -45 ppm/°C.



(a) Schematic (b) Small signal equivalent circuit

Figure 3. Schematic and small signal equivalent of a cross-coupled LC-oscillator.

B. Cross-coupled LC-Oscillator

Figure 3 shows the schematic and small-signal equivalent circuit of a typical cross-coupled LC-oscillator with a lossy inductor and a lossy capacitor, whose losses are modelled by series resistances R_{L} and R_{C} respectively. The oscillation frequency is

$$f_{\mathrm{osc}} \approx \frac{1}{2\pi\sqrt{LC}} \times \sqrt{\frac{Q_{\mathrm{L}}^2(1+Q_{\mathrm{C}}^2)}{Q_{\mathrm{C}}^2(1+Q_{\mathrm{L}}^2)}} \tag{4}$$

where inductor quality factor $Q_{\mathrm{L}} = 2\pi f_{\mathrm{osc}} L/R_L$ and capacitor quality factor $Q_{\mathrm{C}} = 1/(2\pi f_{\mathrm{osc}} R_C C)$. Then the first-order temperature coefficient of f_{osc} is

$$\begin{aligned}\mathrm{TC_f} &\triangleq \frac{1}{f_{\mathrm{osc}}}\left(\frac{\partial f_{\mathrm{osc}}}{\partial L}\frac{\partial L}{\partial T} + \frac{\partial f_{\mathrm{osc}}}{\partial C}\frac{\partial C}{\partial T} + \frac{\partial f_{\mathrm{osc}}}{\partial Q_{\mathrm{L}}}\frac{\partial Q_{\mathrm{L}}}{\partial T} + \frac{\partial f_{\mathrm{osc}}}{\partial Q_{\mathrm{C}}}\frac{\partial Q_{\mathrm{C}}}{\partial T}\right) \\ &\approx -\frac{\mathrm{TC_L}}{2} - \frac{\mathrm{TC_C}}{2} - \frac{\mathrm{TC_{R_L}}}{Q_{\mathrm{L}}^2} + \frac{\mathrm{TC_{R_C}}}{Q_{\mathrm{C}}^2}.\end{aligned} \tag{5}$$

For a copper backend to implement L and C, $\mathrm{TC_{R_L}} = \mathrm{TC_{R_C}} \approx 4000$ ppm/°C. At frequencies in the low-GHz range, $Q_{\mathrm{L}} \approx 10$ which translates into $\mathrm{TC_{R_L}}/Q_{\mathrm{L}}^2 = 40$ ppm/°C while Q_{C} is easily an order of magnitude higher than Q_{L}. Consequently, the impact of $\mathrm{TC_{R_C}}$ is negligibly small compared to that of $\mathrm{TC_{R_L}}$. A systematic approach (in the low-GHz range) to minimize the frequency error due to temperature is by optimizing Q_{L} and hence reducing the large impact of $\mathrm{TC_{R_L}}$.

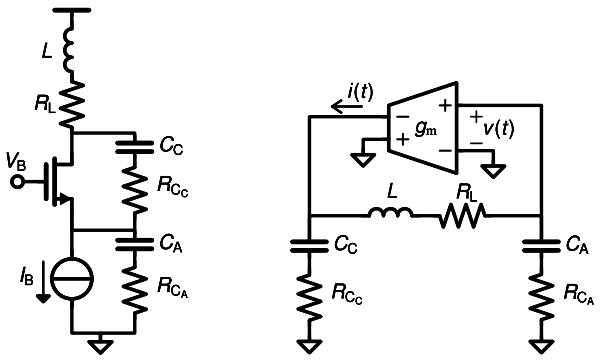
It follows that the $\mathrm{TC_f}$ of the cross-coupled LC-oscillator — excluding any effect of the transconductance amplifier — is dominated by $\mathrm{TC_L}$, $\mathrm{TC_C}$, and $\mathrm{TC_{R_L}}$. Of these, $\mathrm{TC_L}$ and $\mathrm{TC_C}$ are mainly determined by material properties and device structure. The backend process spread impacts metal-thickness and track-roughness and thereby impacts Q_{L} and Q_{C}, which yields spread in $f_{\mathrm{osc}}(T)$.

C. Colpitts LC-Oscillator

Figure 4 shows the schematic and small-signal equivalent circuit of a Colpitts oscillator; its oscillation frequency is

$$f_{\mathrm{osc}} \approx \frac{1}{2\pi\sqrt{LC_{\mathrm{S}}}} \times \sqrt{1 + \frac{1}{Q_{\mathrm{L}}}\left(\frac{1}{Q_{\mathrm{C_A}}} + \frac{1}{Q_{\mathrm{C_C}}}\right)} \tag{6}$$

where C_S is the series combination of the tank capacitors C_{A} and C_{C}. $Q_{\mathrm{C_A}}$ and $Q_{\mathrm{C_C}}$ are the quality factors of C_{A} and C_{C}, respectively. From (6) the first order frequency temperature



(a) Schematic (b) Small signal equivalent circuit

Figure 4. Schematic and small-signal equivalent circuit of a Colpitts oscillator.

Table I
COMPARISON OF TC_F BREAKDOWNS FOR DIFFERENT LC-OSCILLATORS.

	Ideal	Cross-coupled	Colpitts
$TC_{f,L}$	$-\frac{1}{2}TC_L$	$-\frac{1}{2}TC_L$	$-\frac{1}{2}TC_L$
$TC_{f,C}$	$-\frac{1}{2}TC_C$	$-\frac{1}{2}TC_C$	$-\frac{1}{2}TC_C$
TC_{f,R_L}	0	$-\frac{1}{Q_L^2}TC_R$	$\frac{1}{Q_L Q_C}TC_R$
TC_{f,R_C}	0	$\frac{1}{Q_C^2}TC_R$	$\frac{1}{Q_L Q_C}TC_R$

coefficient of the Colpitts oscillator — excluding any effect of the transconductance amplifier — is

$$TC_f \approx -\frac{TC_L}{2} - \frac{TC_C}{2} + \frac{TC_{R_L}}{Q_L Q_C} + \frac{TC_{R_C}}{Q_L Q_C} \qquad (7)$$

where for simplicity it is assumed that $C = C_A = C_C$ and $Q_C = Q_{C_A} = Q_{C_C}$. From (6) and (7), the oscillation frequency of the Colpitts oscillator becomes independent of Q_L when $Q_C \to \infty$, and its TC_f approaches that of the ideal LC-oscillator. In contrast to the cross-coupled LC-oscillator the impact of TC_{R_L} for the Colpitts oscillator can be reduced by increasing the product of Q_L and Q_C.

D. Comparison

The temperature coefficients for the ideal LC-oscillator, the cross-coupled LC-oscillator and the Colpitts oscillator are summarized in Table I. For this table, it is assumed that $TC_{R_C} = TC_{R_L} = TC_R$ for the interconnect series resistances of C and L. Table II shows the corresponding numerical values in the low GHz-range.

For all three topologies the $TC_{f,L}$ and $TC_{f,C}$ terms in total contribute roughly -45 ppm/°C to TC_f. The terms for TC_{f,R_L} and TC_{f,R_C} are different across the various topologies. Compared to the cross-coupled LC-oscillator, the TC_f of the Colpitts oscillator with $Q_C = 200$ is inherently a factor of $Q_C/(2Q_L) \approx 10$ less sensitive to the combined effects of TC_{f,R_L} and TC_{f,R_C}.

The compensation scheme depicted in Figure 1b with a per-sample 1T-trim as shown in Figure 2c requires an extremely low spread in TC_f. TC_f spread cannot, or at least only to a small degree, be corrected by a 1T-trim and hence can contribute significantly to the total frequency inaccuracy. To

Table II
NUMERICAL VALUES FOR TABLE I BASED ON $TC_L = 75$ PPM/°C, $TC_C = 15$ PPM/°C, $TC_R = 4000$ PPM/°C, $Q_L = 10$ AND $Q_C = 200$. THE LAST ROW REPORTS THE SUM PER TOPOLOGY.

	Ideal	Cross-coupled	Colpitts
$TC_{f,L}$ [ppm/°C]	-37	-37	-37
$TC_{f,C}$ [ppm/°C]	-8	-8	-8
TC_{f,R_L} [ppm/°C]	0	-40	2
TC_{f,R_C} [ppm/°C]	0	0.1	2
TC_f [ppm/°C]	-45	-85	-41

estimate the spread of TC_f for the cross-coupled LC-oscillator and Colpitts oscillator, we assume ±10% process variation on the specific metal resistance. The spread on Q_L and Q_C is then about ±10%.

For the cross-coupled LC-oscillator, therefore, spread of $TC_{f,R_L} = TC_{R_L}/Q_L^2$ and $TC_{f,R_C} = TC_{R_C}/Q_C^2$ is about ±20%, which yields a combined spread of about ±10 ppm/°C in TC_f. This amounts to a frequency error of roughly ±1000 ppm over a temperature range of 200 °C. To reach high accuracy levels (e.g. ±100 ppm) over process variations and across a large temperature range, this TC_f-spread level requires at least 2T-trimming in Figure 2b. For the Colpitts oscillator, on the other hand, metal resistance spread translates into a (combined) spread of only about ±1 ppm/°C in the total TC_f, which amounts to roughly ±100 ppm over a temperature range of 200 °C.

V. CIRCUIT IMPLEMENTATION

Based on the frequency stability and TC_f analysis in Sections II and IV, the Colpitts oscillator is chosen as core of the presented frequency reference. The LC-tank is implemented without additional frequency tuning or switching elements, e.g. analog varactors or digitally-controlled capacitors. Temperature compensation is done as explained in Section III. The choice of a Colpitts oscillator with a non-tunable LC tank enables 1T-trimming over PVT and lifetime for ±100 ppm accuracy.

Figure 5 shows the functional schematic of the presented Colpitts-based frequency reference. For this demonstrator vehicle process sensitive parts, such as the oscillator core and the temperature sensor, were integrated on-chip while the fractional divider was implemented off-chip in software for measurement flexibility reasons. Furthermore, the integrated part includes a buffer, a limiting amplifier, a divide-by-two frequency divider, and a peak-detector to implement amplitude control. For measurement flexibility, the amplitude control loop is closed off-chip by measuring V_{peak} and adjusting I_B. The externally measured output of the peak-detector V_{peak}, for amplitude control, is regulated with a resolution of about 1 mV.

The schematic of the common-gate Colpitts oscillator is shown in Figure 6. The LC-tank is formed by inductor L and series capacitance C_S of C_A and C_C. Transistor M_1 implements the sustaining transconductance g_m which is biased via

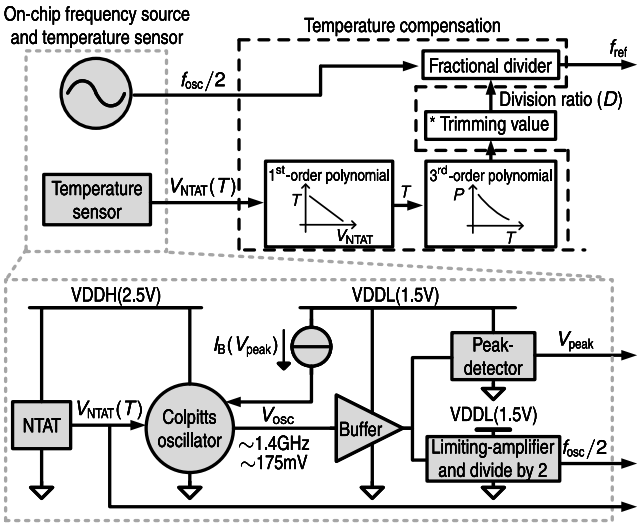


Figure 5. Functional schematic of the presented frequency reference (integrated parts in grey).

the current mirror formed by M_2 and M_3. The temperature-dependent g_m to sustain oscillation is

$$g_\mathrm{m} \approx \frac{(C_\mathrm{C}+C_\mathrm{A})\cdot(R_\mathrm{L}+R_{\mathrm{C_C}}+R_{\mathrm{C_A}})}{L} \tag{8}$$

where R_L is the series resistance of the inductor, $R_{\mathrm{C_A}}$ and $R_{\mathrm{C_C}}$ are the series resistance of C_A and C_C respectively and where all parameters on the right hand side of (8) are temperature-dependent. The correct g_m is set by an amplitude control loop.

A. Selecting C_A, C_C and voltage swings

There is a degree of freedom in selecting C_A and C_C. For a fixed value of C_S and defining $\chi = C_\mathrm{A}/C_\mathrm{C}$, $C_\mathrm{A} = C_\mathrm{S}\,(1+\chi)$, $C_\mathrm{C} = C_\mathrm{S}\left(1+\chi^{-1}\right)$. Higher values for χ result in (at a fixed voltage swing of V_osc) a lower swing at the source of M_1 and result in a reduced effect of C_A-variation on C_S:

$$\Delta C_\mathrm{S} \approx \Delta C_\mathrm{A}\cdot(1+\chi)^{-2} \tag{9}$$

Both the PVT-sensitive gate-source capacitance $C_{\mathrm{gs,M1}}$ of M_1 and the PVT-sensitive drain-source capacitance $C_{\mathrm{ds,M2}}$ of M_2 appear in parallel to C_A. Equation (9) shows that the impact of variations $\Delta C_{\mathrm{gs,M1}}$ and $\Delta C_{\mathrm{ds,M2}}$ on changes ΔC_S decrease rapidly with increasing χ. Our design choice of $\chi \approx 3.5$ is a compromise between suppressing the influence of the parasitic capacitances and their PVT spread on the effective C_S, and the required transconductance and current consumption of transistor M_1, see (8). For this $\chi = 3.5$ the second term on the right-hand side in (9) is about 1/20, which is a 5 times reduction compared to using $\chi = 1$. The required g_m is increased by a factor 1.4 compared to selecting $\chi = 1$ which yields minimum power consumption.

The amplitude of V_osc can be adjusted by the bias current I_B. A higher amplitude result in (strongly) increased harmonic content in I_D which affects the oscillation frequency [36].

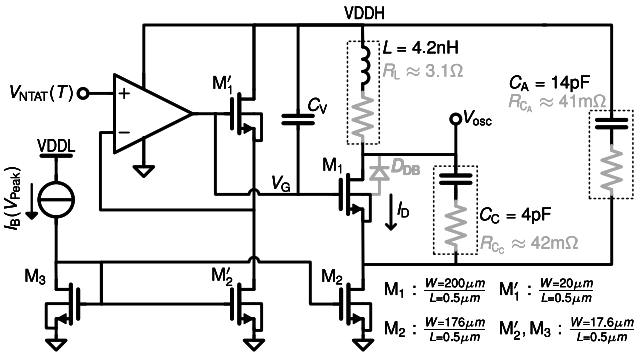


Figure 6. Circuit diagram of the presented Colpitts oscillator. The values of R_L, $R_{\mathrm{C_A}}$ and $R_{\mathrm{C_C}}$ have been extracted from the layout.

From harmonic power balance, the f_osc for the Colpitts oscillator, including harmonic content, is [36]

$$f_\mathrm{osc} \approx \frac{1}{2\pi\sqrt{LC_\mathrm{S}}}\sqrt{1+\frac{1}{Q_\mathrm{L}}\left(\frac{1}{Q_{\mathrm{C_A}}}+\frac{1}{Q_{\mathrm{C_C}}}\right)-\frac{1}{Q_\mathrm{L}^2}\sum_{n=2}^{\infty}\frac{h_n^2}{n^2-1}}$$

where $h_n = I_{\mathrm{D,n}}/I_{\mathrm{D,1}}$ is the normalized n^{th} harmonic in the drain current of M_1. The frequency shift due to the harmonic content also depends on Q_L and thus PVT-variations. The harmonic content is kept sufficiently low by keeping the amplitude of V_osc around 175 mV via the amplitude control loop that includes the peak-detector and a variable bias current I_B. The g_m required to sustain oscillations is about 14 mS (see equation (8)) at room temperature, and increases with temperature due mainly to increased R_L, $R_{\mathrm{C_A}}$ and $R_{\mathrm{C_C}}$ resistance values.

B. Compensating the junction capacitance of M_1

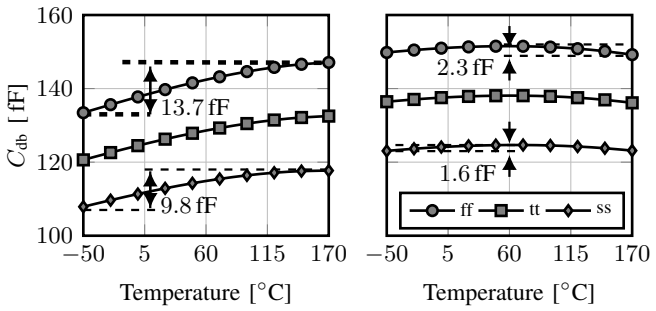
In Section V-A we addressed the parasitic capacitances that are in parallel to C_A. The parasitic capacitance C_db associated with the drain-bulk/source junction D_DB of M_1 is in parallel to C_C and significantly contributes to the frequency spread of $f_\mathrm{osc}(T)$ over PVT.

Assuming a linearly graded junction in D_DB, its junction capacitance can be written as [24]

$$C_\mathrm{db} \approx A_{D_\mathrm{DB}}\cdot\sqrt[3]{\frac{qa\epsilon_S^2}{12\,(\phi_i+V_\mathrm{DB})}}$$

where q is the elementary charge, a is the doping gradient, A_{D_DB} is the area of the junction, ϵ_S is the permittivity of silicon, ϕ_i is the built in voltage of the junction, and V_DB is the reverse voltage across the junction. To obtain a constant junction capacitance, $\phi_i + V_\mathrm{DB}$ must be constant. For a typical ϕ_i at 300 K of 0.7 V, for a linearly graded junction it can be derived that ϕ_i has a linear temperature coefficient of about -1.7 mV/K. For a constant $\phi_i + V_\mathrm{DB}$ then V_DB must ideally have a temperature coefficient of about $+1.7$ mV/K.

Biasing the gate of the transistor in Figure 4a at a fixed voltage V_G, the voltage drop across the transistor's D_DB is determined by V_G and the temperature and process corner dependent V_GS of the MOS transistor. To avoid the impact of PVT spread on C_db and to ensure a constant $\phi_i + V_\mathrm{DB}$, in our circuit implementation a supply-tracking NTAT voltage



(a) Using constant $V_G = 1V$. (b) Using compensated $V_G(T)$.

Figure 7. Simulated C_{db} without and with temperature compensation for 3 process corners.

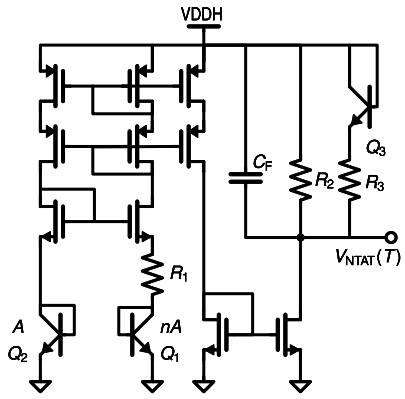


Figure 8. Schematic of the $V_{NTAT}(T)$ generating circuit. The bulk of NMOS and PMOS are connected to GND and VDDH respectively.

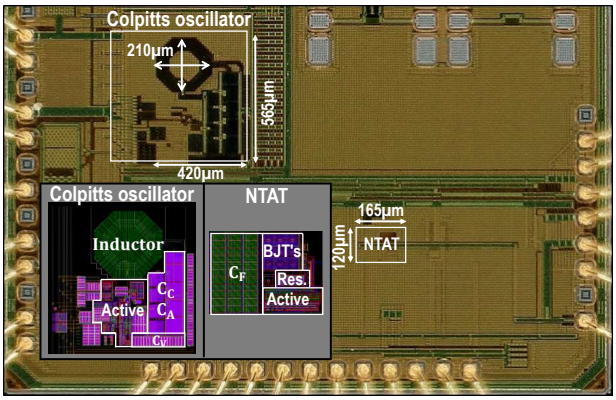


Figure 9. Die micrograph of the test chip.

V_{NTAT} is forced at the source of M_1 using the replica circuit M_1', M_2' and the opamp which is implemented by a two-stage design with Miller-compensation. The circuit that implements the supply-tracking NTAT voltage is discussed in Section V-C.

The simulated C_{db} as a function of temperature for 3 process corners in the technology we used (see Section VI) is shown in Figure 7.

Figure 7a shows C_{db} for a fixed $V_G = 1\,V$ as a function of temperature for 3 process corners. A per sample 1T-trim of f_{osc}, as depicted in Figure 1b, addresses only the shift of $C_{db}(T)$ at the trimming temperature. The spread of the (average) slope of the $C_{db}(T)$ curves results in TC_f spread and requires at least a 2T-trim.

Figure 7b shows $C_{db}(T)$ for a temperature-compensated V_G, for the same process corners. Using a 1T-trim, only the curvature difference between the curves contributes to post-trim inaccuracies in f_{osc}. As a rough estimation, the residual PVT spread in f_{osc} when using a temperature compensated V_G is 20 ppm, a factor of 6 reduction compared to when using a fixed V_G.

C. NTAT generator / temperature sensing core

The V_{NTAT} generator, shown in Figure 8, both provides the $V_{NTAT}(T)$ to the opamp in Figure 6 and doubles as core for the temperature sensor. For operation as temperature sensor, the voltage $V_{DDH} - V_{NTAT}(T)$ was digitized externally for this demonstrator and has a TC of roughly $-3.1\,mV/°C$. The circuit schematic of this circuit is similar to the work in e.g. [37]. For this circuit

$$V_{NTAT} \approx V_{DDH} - \frac{R_3}{R_2+R_3} \times \left(\frac{R_2}{R_1}\frac{kT}{q}\ln(n) + \frac{R_2}{R_3}V_{BE,Q_3} \right), \quad (10)$$

where n is the emitter area ratio of Q_1 and Q_2.

VI. Measurement Results

Figure 9 shows a micrograph of the test chip, fabricated in a $0.13\,\mu m$ high voltage CMOS SOI process and assembled in a plastic package by a transfer molding process. The Colpitts based frequency reference occupies an active area of $0.26\,mm^2$. For device characterization of the LC-tank devices, dedicated test-structures (including de-embedding) were implemented. The typical power consumption of the oscillator core and NTAT-circuit is about 3.5 mW from a 2.5 V supply, while the buffer and peak-detector consume 0.75 mW and 6 μW from a 1.5 V supply respectively.

A. Passives characterization

A 3.75 turn octagonal inductor with an outer diameter of 210 μm, a track width of 6 μm and a patterned ground-shield in polysilicon implements the LC-tank inductor. The capacitors are implemented by 3 layers of metal-oxide-metal capacitors. The devices are characterized at 25 °C, 75 °C and 100 °C and the results are shown in Figure 10. For both devices, the measured linear temperature coefficients increase with frequency and are roughly 75 ppm/°C and 15 ppm/°C for the inductor and capacitor respectively at 1.5 GHz. The TC_f of the Colpitts oscillator due to only TC_C and TC_L is hence about −45 ppm/°C.

B. Colpitts oscillator intrinsic behavior

Figure 11 shows the measured frequency of the Colpitts oscillator, where the results in black were first published in [21]. In total 48 samples, from 3 different wafers of the same batch, were measured over a temperature range from −50 to 170 °C (set by a thermo streamer). Figure 11 shows mainly a shift in the absolute frequency value (not in TC_f) between the samples; furthermore, results for the samples from

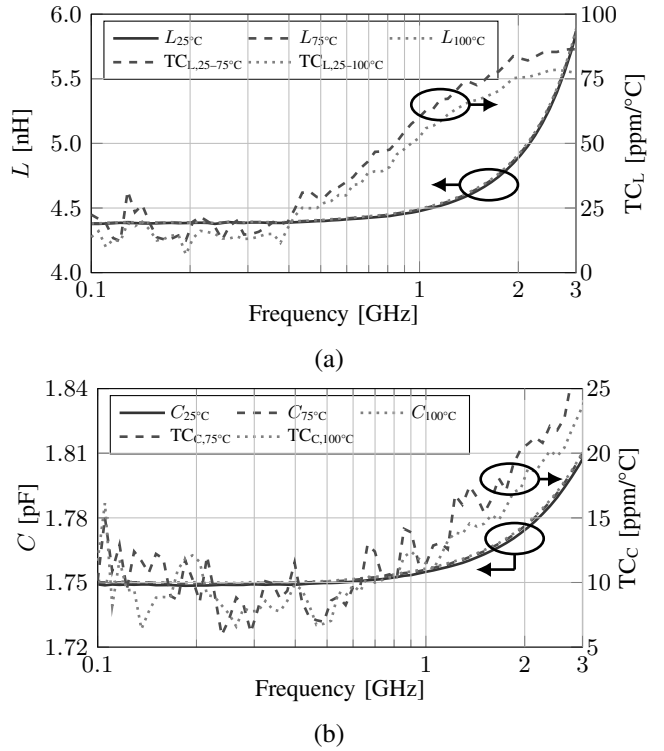


Figure 10. Measurement results of the inductor and capacitor characterization.

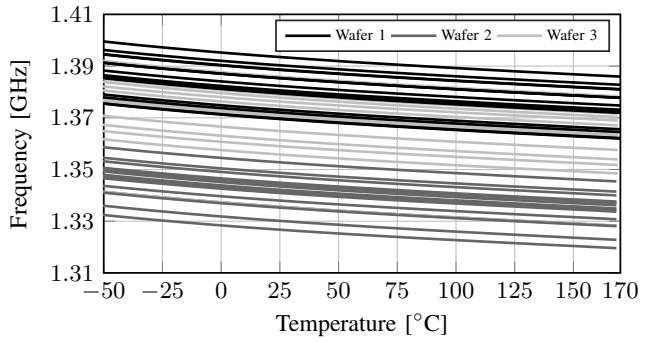


Figure 11. Measured frequency f_{osc} over temperature for 48 samples from 3 wafers.

the same wafer — indicated by curves in black, dark gray and light gray — appear to be grouped, which indicates wafer-to-wafer spread.

Figure 12 shows the frequency deviation of all these Colpitts oscillators over temperature, with f_{osc} normalized to 25 °C. The native frequency deviation over temperature stays within ± 5500 ppm which corresponds to -44.5 ppm/°C (box-method), in agreement with the frequency deviation due to the TC_C and TC_L values obtained from device characterization. Note that this measured behavior meets our initial target as depicted in Figure 2c, therefore allowing 1T-trimming to be effective against die-to-die and wafer-to-wafer variations.

The measured phase noise at the output of the divide-by-2 frequency divider is -102 dBc/Hz@100 kHz with a 1/f-corner at 15 kHz, which gives an Allan deviation floor of 0.25 ppm.

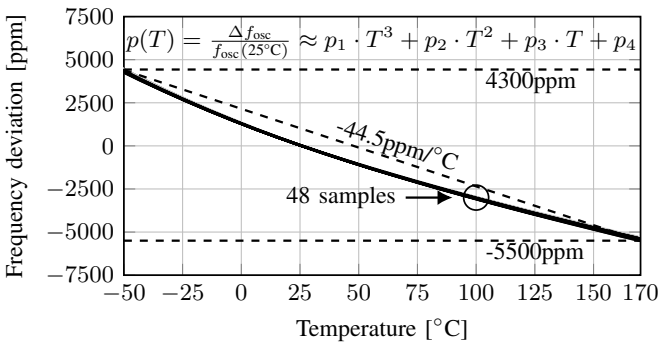


Figure 12. Measured frequency deviation of f_{osc} over temperature for 48 samples from 3 wafers of 1 batch (normalized to f_{osc} at 25 °C). The polynomial coefficients are: $p_1 \approx -2.6 \cdot 10^{-10}$ °C^{-3}, $p_2 \approx 1.3 \cdot 10^{-7}$ °C^{-2}, $p_3 \approx -5.3 \cdot 10^{-5}$ °C^{-1} and $p_4 \approx 0.0013$.

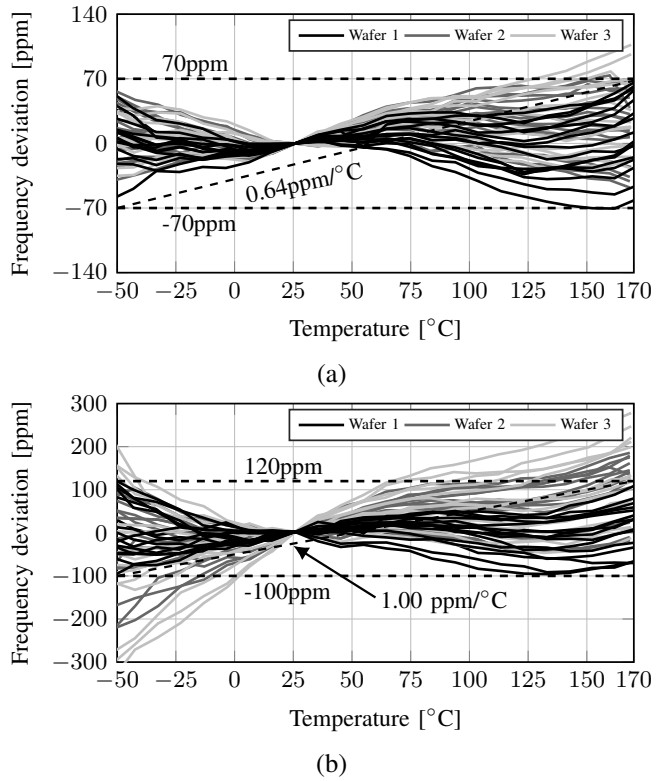


Figure 13. Measured frequency deviation over temperature of 3 wafers with third-order correction polynomial and 1T-trimming, using (a) an external PT100 temperature sensor (b) the internal temperature sensor.

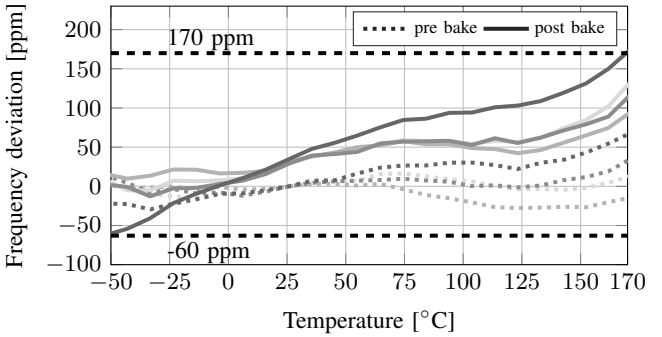


Figure 14. Measured frequency deviation before and after 6-day storage bake of 4 randomly selected samples of the first wafer.

Table III
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR WORK IN INTEGRATED FREQUENCY REFERENCES.

	This work	[10]	[9]	[16][a]	[6]	[20]	[7]
reference principle	Colpitts	Colpitts	LC Cross-coupled	LC Cross-coupled	RC	RC	Thermal Diffusivity
frequency [MHz]	1380	52	24	100	7	16	16
temp. range [°C]	-50 to 170	0 to 80	0 to 70	-20 to 85	-45 to 85	-45 to 85	-55 to 125
temp. coefficient [ppm/°C][b]	1.0	0.05	1.8	0.7	2.5	5.2	11.2
trimming temp. [°C] (# trim. points)	RT[c] (1)	0, 5, ..., 80 (16)	NA (-)	0 and 70 (2)	-35 and 75 (2)	RT[c] (1)	RT[c] (1)
supply sensitivity [ppm/V]	220	4270	≤ 8[d]	2.6[d]	1800	0.2	NA
lifetime $\Delta f/f$[ppm] (method)	±100 (6-day 175 °C bake)	NA (-)	NA (-)	±205 (HAST, HTOL, reflow)	NA (-)	NA (-)	NA (-)
number of samples	48	3	1	28	8	18	24
power [mW]	4.25[e]	14.25	49.5	14.85[f]	0.78	0.16	2.1
rms period jitter [ps]	0.5[g]	3.2	6.5	12	24	10.2	45
area [mm^2]	0.26	5 [h]	2.25 [h]	0.2	1.59	0.14	0.5
technology	130nm HV CMOS SOI [i]	350nm CMOS	250nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	160nm CMOS

[a] Some numbers from private communication as not available from [16] itself. [b] Box-method [c] Room-temperature [d] On-chip voltage regulator
[e] Fractional divider not included. For comparison, the fractional divider in [16] consumes 12.15 mW. [f] For a supply voltage of 2.7 V.
[g] Measured at the output of the divide-by-two frequency divider. [h] Entire chip [i] For this frequency reference, there is no specific benefit compared to a typical bulk CMOS process. NA = Not Available

C. Single-trim frequency reference behavior

The frequency reference, shown in Figure 5, consists of the Colpitts oscillator and temperature compensation in terms of a programmable frequency divider. For this paper, we focused on the on-chip frequency source and implemented an ideal fractional divider off-chip in software. In post-processing, the fractional divider utilizes the measured untrimmed frequency at a single temperature of Figure 11 as an input. Furthermore, the fractional divider employs a per-sample 1T room temperature trim and a fixed third-order correction polynomial $p(T)$ to determine the division ratio:

$$D(T) = \frac{f_{\text{osc}}(25\,^\circ\text{C}) \cdot (1 + p(T))}{f_{\text{ref}}}. \tag{11}$$

The polynomial $p(T)$, shown in Figure 12, is determined from wafer 1 only and serves in batch calibration for all 48 samples from the 3 wafers. In this equation f_{ref} is the target frequency of the frequency reference as defined in e.g. Figure 5.

The temperature (T in Figure 5) was determined based on the internally generated NTAT-voltage, which is externally measured alongside a PT100 temperature sensor for characterization reasons.

Figure 13a and Figure 13b show the resulting frequency deviation after single room temperature trim, using an external PT100 and the internal temperature measurement for temperature compensation, respectively. The majority of the measurements based on the PT100 stay within ±70 ppm over the temperature range, and minimal spread between the different wafers is visible. The measurement results with the internal temperature sensor on the wafer that was used for batch calibration stay within ±120 ppm over the entire temperature range. This can be attributed to a measured maximum die-to-die spread of the temperature sensor core of roughly ±2 °C which yields an additional frequency error of roughly ±90 ppm (based on Figure 12). Samples from other wafers show a total frequency deviation of ±300 ppm. The increased spread in Figure 13b compared to Figure 13a is due to the wafer-to-wafer spread of the integrated temperature sensor core (up to ±5 °C) that is used to estimate the chip temperature.

D. Single-trim behavior over lifetime

For high-accuracy frequency references, performance degradation over lifetime should be low. To demonstrate the robustness of our design, we did accelerated ageing test in the form of a 6-day storage bake at 175 °C for four randomly selected samples from one wafer. For the samples, a 1T-trim using the batch polynomial was done at 25 °C before the storage bake.

The samples were characterized before and after the storage bake. Pre- and post-bake results use the same (pre-bake) third-order compensation polynomial, the same (pre-bake) 1T-trimming settings and use the external temperature sensor. Figure 14 shows the frequency deviation before (dotted) and after the bake (solid) over a temperature range from −50 to 170 °C. The largest frequency deviation between pre- and post-bake measurement, with 100 ppm, is observed at 170 °C.

E. Benchmarking

The summary of the measured performance of the presented Colpitts based frequency reference and reported performance metrics from literature is provided in Table III; the data in the columns are organized based on the reference principle. It follows that the presented reference provides the highest 1T-trim accuracy. Of the 2T-trimmed references, the work [16] reports an accuracy level somewhat higher than our work, although only in about half our temperature range.

Furthermore, this Colpitts oscillator's supply sensitivity is roughly 20x better compared to the work in [10] thanks to the supply tracking NTAT-biasing and the replica substrate biasing for the driving transistor.

VII. Conclusions

An on-chip Colpitts oscillator is presented that meets high accuracy over a large temperature range using only a single-temperature trim. With the LC-oscillator approach, the frequency is mainly defined by the metal backend, which both yields a well-defined temperature dependence of the oscillator as well as an inherently minimum ageing. The Colpitts topology was shown to have an inherently lower dependence on the process and temperature-dependent quality factor of the LC-tank compared to that of the cross-coupled LC-oscillator. Several dependencies of the frequency accuracy over process variation, temperature variation and ageing are reduced by a non-tunable oscillator core, amplitude control, an optimized tank capacitor ratio, and NTAT biasing.

The aforementioned design choices and circuit techniques ensure a small frequency temperature coefficient. The residue is compensated off-chip by a fixed 3$^{\text{rd}}$-order correction polynomial applied for the whole batch. After a sample-specific single room-temperature trim, our proposed frequency reference system achieves an accuracy of ± 120 ppm from -50 to $170\,^{\circ}\text{C}$ for 16 samples from one wafer, using batch-calibration. Using the same polynomial coefficients from the batch-calibration, the accuracy across 3 different wafers is about ± 300 ppm. Excellent robustness against ageing is verified with a 6-day storage bake at 175°C. The oscillator, with $0.26\,\text{mm}^2$ active area, dissipates $3.5\,\text{mW}$ from a $2.5\,\text{V}$ supply in the Colpitts core, and an additional $0.75\,\text{mW}$ for the buffer and amplitude detector.

VIII. Acknowledgments

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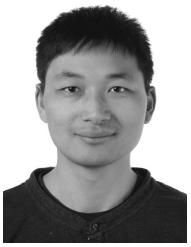

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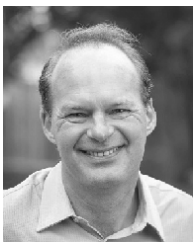

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