Low-Temperature Electrical Performance of PureB Photodiodes Revealing Al-Metallization-Related Degradation of Dark Currents

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***Abstract*— Pure boron (PureB) deposition as the anode region of Si photodiodes creates negative fixed charge at the boron/silicon interface, which is responsible for effective suppression of electron injection from the bulk, thus ensuring low saturation/dark current densities. This mechanism is shown here to remain effective when PureB diodes, fabricated at 700 °C, are operated at cryogenic temperatures down to 100 K. Although the PureB junctions were only a few nanometers deep, they displayed the same current–voltage (*I–V*) characteristics as conventional deep diffused p^+–n junction diodes in the whole temperature range and also maintained ideality factors close to $n = 1$. Al-contacting was found to reveal process-related defects in the form of anomalous high current regions giving kinks in the *I–V* characteristics, often only visible at low temperatures. They were identified as minute Al–Si Schottky junctions with an effective barrier height of ∼0.65 ± 0.05 eV. In PureB single-photon avalanche diodes (SPADs), Al–Si perimeter defects appeared but did not affect the breakdown voltage characteristics set by implicit guard rings. Low series resistance required thin B-layers that promoted tunneling. In particular, for such thin layers, avoiding Al-related degradation puts stringent requirements on wafer cleaning and window etch procedures.**

***Index Terms*— Aluminum, cryogenic measurement, interface charge, photodiode, pure boron (PureB) diodes, single-photon avalanche diode (SPAD), thin-film boron layers, ultrashallow junctions.**

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I. Introduction

OPERATION of silicon photodiodes at cryogenic temperatures is routinely exploited as a means of improving performance of detectors, such as charge-coupled devices (CCDs) [1], [2], single-photon avalanche diodes (SPADs) [3], and drift detectors [4], [5]. For SPADs, the dark count rate (DCR) is reduced, while the photon detection probability is increased, which has received much attention for potential use in high-sensitivity imagers and quantum computation [6], [7]. The latter application has also encouraged increased research into the operation of semiconductor devices at low temperatures. For example, the reliable operation of CMOS circuits at cryogenic temperatures down to 4.2 K (liquid helium) is believed to be pivotal for the development of quantum, neuromorphic, and optical computation architectures that operate exclusively at cryogenic temperatures [8], [9].

Low-temperature operation can further improve the already attractive optoelectrical properties of diodes made by depositing pure boron (PureB) as anode regions on silicon [10]. For the PureB photodiodes operated at room temperature (RT), the lowest dark currents and most robust B thin films are achieved by depositing the B-layer at 700 °C. Devices incorporating these B-layers have been commercialized as PureB detectors for low-energy electrons [11], [12] and vacuum ultraviolet/near-ultraviolet (VUV/NUV) light [10], [13]. The attraction for these applications lies in the extremely shallow junction depth and low dark currents, combined with exceptional optoelectronic stability and chemical robustness [14]–[16]. The latter is due to the strength of the B–B bonds that even for these amorphous thin films provide resistance to many chemical etchants and cleaning methods used in Si processing and detector maintenance [10], [16]. The optoelectrical stability is largely due to the B–Si bonds that form a monolayer of fixed negative charge, enough to attract a high concentration of holes to the interface. An inversion layer of holes gives a suppression of electron injection from the bulk comparable to that of conventional deep diffused p^+-n junctions [17]. This damage-free method of fabricating

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the PureB p^+-region has also been implemented as the anode region in SPADs with low DCR [18].

In other photodiode fabrication technologies, oxides, such as MoO_x and Al_2O_3, are used to introduce a negative fixed charge and create an inversion layer at the silicon/insulator interface [19]–[22]. Due to the insulating properties of oxides, the silicon/insulator interface is usually contacted via a doped Si region [20]. This is in contrast to the noninsulating B-layers that are contacted directly by metal deposition. In PureB technology, Al-metallization is often used in a very cost-efficient process module for patterning the interconnect while opening the light-entrance windows to the B-layer [23]. Since the electrical behavior of PureB diodes relies on the interface properties rather than B-doping of the bulk Si and the B-layer itself is a few nanometers thin, any weak spots or pinholes in the B-layer are known to lead to undesirable current increase when metallized [17]. The diode perimeter was particularly susceptible to such unintended interactions with Al [24], a problem that could be avoided in large diodes by using implanted guard rings (GRs) at the perimeter.

In this article, the current–voltage (I–V) characteristics of PureB photodiodes at temperatures down to 100 K are examined for a number of different photodiodes, ranging from millimeter-large devices designed for use in the linear regime to micrometer-small devices designed for operation as SPADs. The objective was to learn whether the exceptional electrical properties would be maintained at these temperatures despite the nanometer-shallow nature of the junction. The results are also supported by device simulations using the PureB diode model established in [17] and [25]. The study revealed that the Al-metallization could be the source of anomalous leakage currents that, in some cases, were only evident at low temperatures. The nature of the defects associated with this leakage was examined for large devices with conventional implanted GRs and small SPAD-design devices without GR perimeter protection.

II. Experimental Methods

A. Device Fabrication

The basic design of the three types of PureB diodes studied here is shown in Fig. 1, and an overview of the device sizes and processing variations is listed in Table I. Diodes were studied with sizes from a few micrometers to hundreds of micrometers. In the type shown in Fig. 1(a), the p^+-type region was formed solely by a B-layer deposition. In the type shown in Fig. 1(b), a p^+ GR was added around the perimeter of the PureB region. For small diodes, such GRs are mainly not appropriate, so either no GRs were applied or, in the case of SPADs, an implicit GR, as shown in Fig. 1(c), was implemented by the implantation of phosphorus (P^{++}) in the central region of the diode. This sets the breakdown voltage away from the perimeter as described in detail in [26].

The substrates used for the fabrication of all the PureB diodes except for the SPADs were n-type (100) Si wafers with resistivity 1–10-Ω·cm. For the large diodes, GRs were created by 180-keV B^+ implantation to a dose of 10^{13} cm^{-2} through a 300-nm-thick thermal oxide followed by annealing at 1000 °C for 20 min. Windows in the oxide were wet-etched to expose the Si surface that then was prepared for B-deposition using the methods described in [23]. The deposition was performed at 700 °C for times from 6 to 30 min, which on blanket wafers gave a B-layer thickness from 2.5 to 12 nm, respectively [27], [28]. Due to loading effects and varying size of surrounding oxide areas, the thickness may be as much as a nanometer higher than this in actual devices on the same wafer [29]. Since this variation in actual B-layer thickness does not affect the conclusions of this study, the thickness values that we refer to in the following will be the known blanket-deposition values.

On one of the large devices, the PD0-GR, a 20-min B-layer was deposited and then covered with LPCVD oxide. This prevented B-desorption during the following anneal at 900 °C.

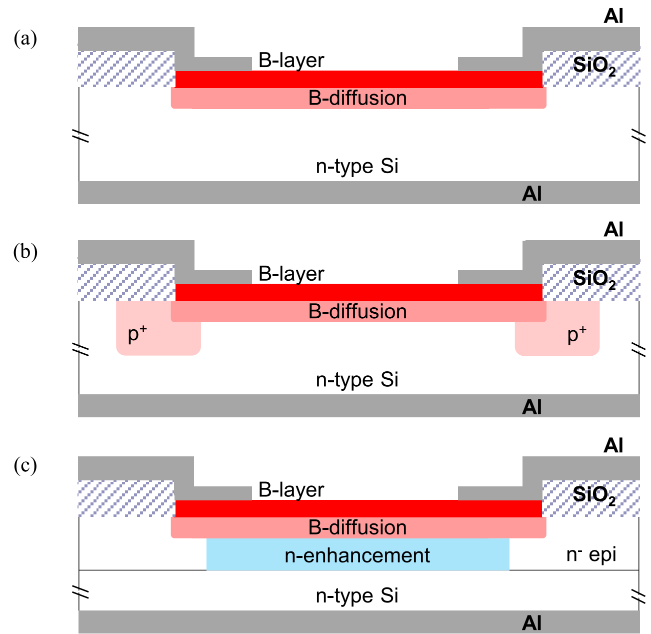

Fig. 1. Schematic cross section of the basic PureB diode designs with (a) PureB-only p^+-type region and (b) B-implanted or (c) implicit P-implanted GRs.

TABLE I
PureB Diode Processing Details and Simulated Values for Metallurgic Junction Depth and Total Doping Concentration From B-Doping of the Bulk Si

Diode type	B-layer dep. time	Post dep. anneal	GR	B-layer thickness (nm)	Anode sizes (µm^2)	Junc. depth (nm)	Total Si B-doping (cm^{-2})
PD6	6 min	-	-	2.5	4-2000	5.4	2.3×10^{12}
PD15	15 min	-	-	6	4-2000	8.5	3.7×10^{12}
PD30	30 min	-	-	12	4-2000	12	5.2×10^{12}
PD6-GR	6 min	-	B	2.5	2000-1×10^6	5.4	2.3×10^{12}
PD20-GR	20 min	-	B	8	2000-1×10^6	9.8	4.3×10^{12}
SPAD6-N	6 min	1 min @ 850 °C	P	2.5	4-2000	23.5	3.5×10^{13}
SPAD6-P	6 min	1 min @ 850 °C	P	2.5	4-2000	23.5	3.5×10^{13}
PD0-GR[(a)]	20 min	20 min @ 900 °C	B	0	2000-1×10^6	199.2	4.1×10^{14}

(a) For this diode type, the B-layer was removed after post-deposition anneal.

The oxide and B-layer were removed before metallization. All the diodes were contacted by sputtering 875-nm-thick pure Al that was patterned by resist and plasma etching down to about 100 nm. The remaining Al was removed in the light-entrance windows by dip-etching in diluted HF [23]. Al was deposited on the backside of the wafer as the cathode contact. The processing was completed by performing an alloying step in forming gas at 400 °C. This method of processing is possible because the B-layer is resistant to HF and also forms a barrier that prevents Al from reacting with the underlying Si [30].

For the small SPAD devices, the contacting of the n-region included the fabrication of buried n^+-layers, a lightly doped n-type epitaxial layer, and n^+-plugs, as described in [18]. Two different batches of SPADs were examined: one processed on p-substrate wafers and the other on n-substrates, but otherwise. the same process flow was followed. The n-enrichment implicit GR was created by implanting phosphorus to a dose of 10^{12} cm^{-2} at 40 keV plus 5×10^{12} cm^{-2} at 300 keV. The anode contact windows were plasma etched in 300-nm oxide with soft-landing on the Si before a 6-min B-deposition at 700 °C, followed by a 1-min anneal at 850 °C. Metallization with pure Al and light-entrance window opening was performed as for the large diodes.

B. Low-Temperature Measurement Setup

For measurements down to 100 K, a cryostat setup was used with liquid nitrogen as a cryogen. The liquid nitrogen was stored inside a dewar, where a cold head with integrated heaters was connected to the exchange gas tube. Liquid nitrogen was pumped to the cold head, the temperature of which was adjusted by integrated heaters joined to two thermostats controlled by a Lakeshore 331. In order to establish good thermal contact with the cold head, samples were mounted to it using a thermal paste.

Measurements in the temperature range from −50 °C to 100 °C were performed with a PM300 Suss MicroTec probe station equipped with an ATT liquid-cooled thermal chuck. In all cases, a Keithley 4200 parameter analyzer was used to measure the I–V characteristics of the devices.

III. Device Simulation Models

Simulations of the low-temperature PureB device behavior were performed based on the technology computer-aided design (TCAD) model developed in [17] and [25] with Synopsys Sentaurus Device software [31]. The bulk-Si was simulated as an n-type region with a thickness of 500 μm and a constant doping of 10^{15} cm^{-3}. The material properties of the B-layer were set to have the same parameters as Si except for bandgap varied in the range 0.5–1.3 eV [25], [32], [33] and electron affinity varied in the range 3.9–4.7 eV [25], [34], [35]. These parameters were found to be important for simulating the series resistance at low temperatures. The actual values are largely unknown and found to be of secondary importance for the suppression of electron injection. Of main importance, was the concentration of the interfacial negative fixed charge, N_I, that in the 10^{14} cm^{-2} range was found to be sufficient to explain the very low electron saturation current levels [25]. Based on experimental values found from PureB-emitter p-n-p bipolar-transistor measurements, N_I was set here to be 5×10^{14} cm^{-2}, which approximates the number of activated holes expected in a deeply diffused p^+ region with a Gummel number equivalent to that of 700 °C PureB emitters [28]. Apart from the bandgap and electron affinity, to account for the series resistance through the bulk B-layer, a tunneling mass for holes, m_h, was varied from $0.1 \times m_0$ to $1 \times m_0$ as a fitting parameter.

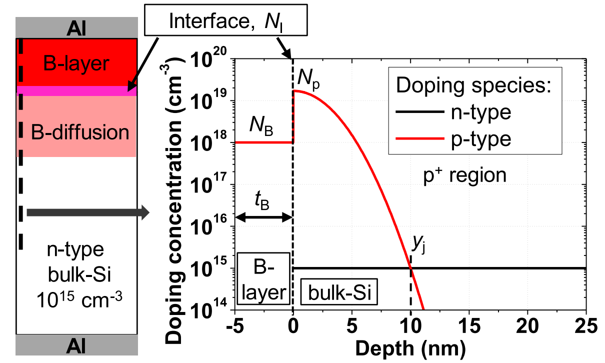

Fig. 2. Cross section of the simulated PureB diode and doping concentration profile, with $N_B = 10^{18}$ cm^{-3}, $t_B = 5$ nm, and $y_j = 10$ nm.

A schematic cross section of the simulated PureB diode is shown in Fig. 2 together with an assumed doping profile and all parameters of importance. The B-layer p-type doping, N_B, is assumed to have the highest reported value of 10^{18} cm^{-3} [36]. For B-deposition at 700 °C, in-diffusion of B into Si is expected. To match the junction depths determined by secondary-ion mass spectrometry (SIMS) measurements [28], [37], process simulations of boron diffusion were performed using Sentaurus Process [38]. Extracted junction depths at a background n-doping of 10^{15} cm^{-3}, and integral doping of the Si, are listed in Table I for each type of device. For the PD0-GR device, the integrated Si doping is as high as 4.1×10^{14} cm^{-2}. For 700 °C PureB diodes, the diffused p-region is simulated in Sentaurus Device by defining a Gaussian profile with peak concentration, N_p, at the surface of 1.7×10^{19} cm^{-3}, the solid solubility of B in Si at 700 °C [39], and a p-n junction depth, y_j, at a background n-doping of 10^{15} cm^{-3}.

The work function of the Al-metal on top of the B-layer, φ_m, is assumed to have a value of 4.1 eV [31]. The thermionic emission model [40] and Philips unified mobility model [41] were applied, and Fermi–Dirac statistics [42] were assumed for electrons and holes. The best results were achieved using the parameters for B-layer bandgap of 0.55 eV, electron affinity of 4.3 eV, and a fitting parameter $m_h = 0.3 \times m_0$.

IV. Results

A. Ideal Low-Temperature Diode Characteristics

The forward I–V characteristics of ideal large diodes are shown in Fig. 3 for measurement temperatures from 373 down to 100 K. The deeply diffused diode, PD0-GR, was measured only down to 223 K. The two PureB diodes, PB6-GR and PD20-GR, as well as the diffused diode PD0-GR, show practically the same I–V characteristics, with a significant

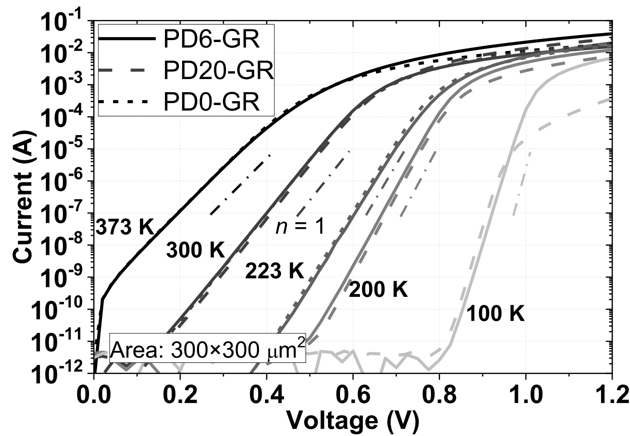

Fig. 3. Temperature-dependent I–V characteristics of PD6-GR, PD20-GR, and PD0-GR diodes. Slope for ideality factor $n = 1$ is plotted next to its respective temperature curve.

difference only appearing in the series resistance at low temperatures. At 223 K and above, the series resistance of all the diodes is approximately the same. As the temperature drops, the series resistance of the PB6-GR diode, with a 2.5-nm-thick B-layer, remains constant, while the device with the much thicker 8-nm-thick layer, PB20-GR, has decades higher series resistance at 100 K. This indicates that the B-layer resistivity increases with decreasing temperature. In the past, the B-layer resistivity was found to be high, in the range $500–10^4 \Omega \cdot$ cm at RT [43], but thin layers allow tunneling, which keeps the contact resistance low [28]. This is now also confirmed here by these low-temperature measurements. The ideality factor, n, of the two measured PureB diodes was found to be $n \sim 1$, for temperatures above 300 K, and at lower temperatures, it only increases slightly to become $n \sim 1.1$ at 100 K.

In Fig. 4, the current density simulated by the PureB TCAD model is compared to that of the measured PureB devices. A simulation of a diffused diode is also included. The simulated B-layer thicknesses were $t_B = 2.5$ nm and $t_B = 8$ nm. The junction depth of the simulated PD0-GR diffused p$^+$ region was set in the simulations to be 0.2 μm, while the peak concentration of the Gaussian doping profile at the surface was 7×10^{19} cm^{-3}, which corresponds to the diffused B junction profile obtained from process simulations. This diode simulation shows the same temperature dependence as the simulated PureB junctions, in agreement with the experimental results. In the ideal current range, not affected by the series resistance, the simulations and measurements overlap for the temperatures of 300 and 200 K, while for 100 K, the simulated currents are slightly lower than the measured values. The temperature dependence of the mobility and lifetime used in the simulations could be different from the actual experimental values, and tuning of the temperature-dependent fitting parameters could provide better agreement between simulations and measurements at low temperatures.

For the device with $t_B = 2.5$ nm, the simulations also confirm that the holes tunnel through the B-layer to the Al contact, ensuring an almost constant series resistance independent of the temperature. The experimentally observed increasingly higher resistivity of the PB20-GR diode is also reproduced.

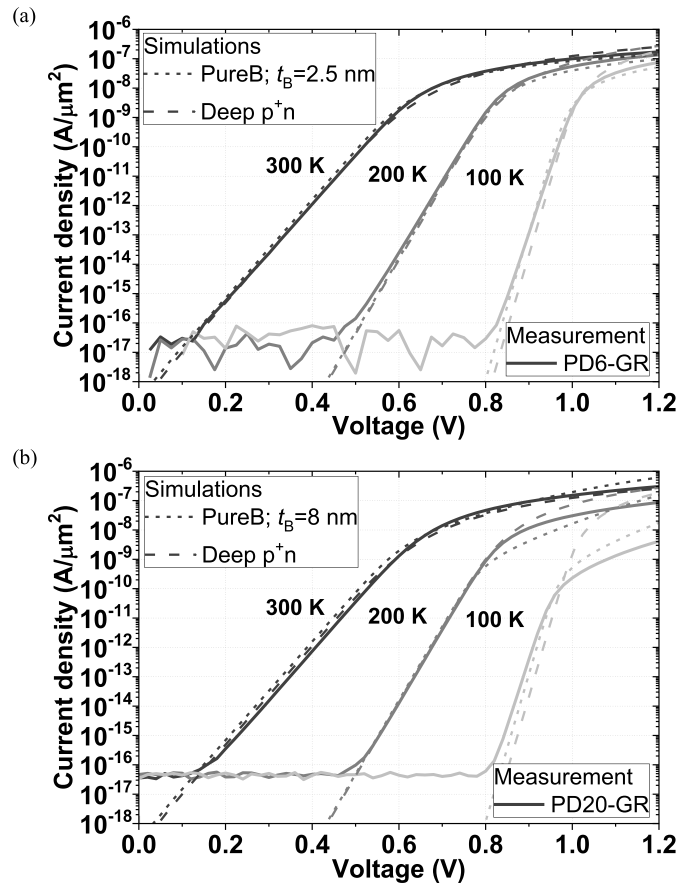

Fig. 4. Comparison of the simulated and measured current densities for temperatures of 100, 200, and 300 K for (a) PB6-GR diode compared to a simulated PureB diode with $t_B = 2.5$ nm and (b) PB20-GR diode compared to a simulated PureB diode with $t_B = 8$ nm. Simulations of a conventional deeply diffused p$^+$-n junction diode are also shown for reference.

It is expected that the holes move through the B-layer by variable-range-hopping conduction, which is common for such amorphous materials [44], [45]. However, variable-range-hopping conduction could not be modeled properly by the applied simulation software, and a rough approximation was made by assuming a single tunneling mass.

For the small PureB diodes, without GR, PB6, PB15, and PB30, ideal diode characteristics with $n \sim 1$ were also regularly measured down to the cryostatic temperatures. This was also the case for the SPAD6-P diodes.

B. Al-Induced Leakage in Large PureB Diodes

Fig. 5 shows an example of a PD6-GR device with 13% diode area covered with Al. This diode displays nonideal currents, with a kink in $I–V$ characteristics which is more prominent at lower temperatures. The kink separates a high from a low current region, each with $n \sim 1$. All PD6-GR devices with smaller Al coverage of 7% exhibit ideal behavior, as shown in Fig. 5 where a comparison is also made to a PD0-GR device. With respect to this undesirable behavior, the yield of the diodes very clearly reflects the role of the Al-coverage and the thickness of the B-layer [17]. For the PB20-GR diodes, the yield was almost 100%, independent of Al-coverage [17].

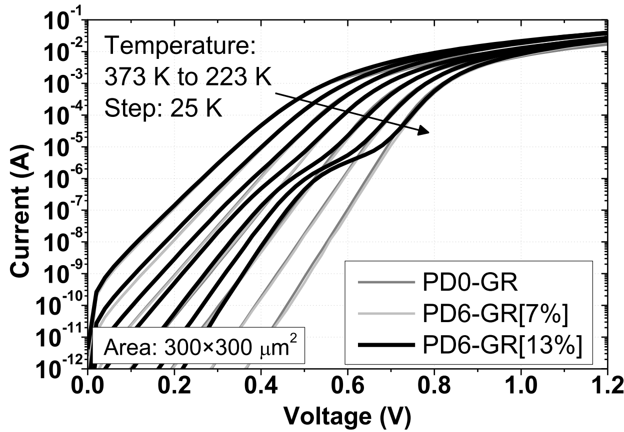

Fig. 5. Temperature-dependent I–V characteristics of PD0-GR and PD6-GR diodes with 7% and 13% diode area covered with Al.

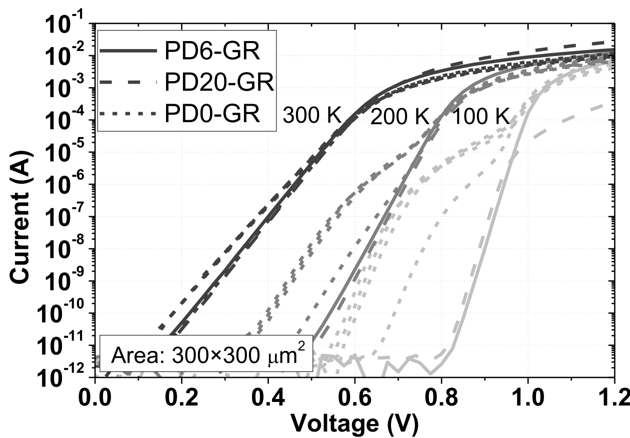

Fig. 6. Temperature-dependent I–V characteristics of a PD6-GR, a PD20-GR, and four PD0-GR diodes.

For the diffused diodes PD0-GR, the majority of RT characteristics had $n > 1$ and clear kinks were frequently observed, as shown in Fig. 6. Characteristics of PD6-GR and PD20-GR diodes that did not display kinked behavior are shown for comparison. The measurements at lower temperatures revealed that any nonideality at RT was in fact associated with kinked behavior that became more and more predominant as the temperature decreased. Unlike the PureB devices, a p^+-Si region forming the anode of PD0-GR devices was not protected from alloying with Al and spiking was to be expected. The pits that then form are known to readily become as deep as 1 μm, piercing the diffused p-region and forming a Schottky junction with locally high current.

C. Al-Induced Leakage in Small PureB Diodes

Although SPAD6-N and SPAD6-P diodes were processed with the same B thickness and post-B-deposition anneal, the SPAD6-N devices displayed current levels that were decades higher than those of the SPAD6-P, as shown in Fig. 7. The origin of this discrepancy was examined in [24], and it was found that the perimeter of the defected SPAD6-N devices was not sufficiently protected by the B-layer upon metallization although there were no signs of actual spiking of Al into Si. High leakage currents at RT were also frequently observed for PD6 devices, while the saturation currents of PD15 and

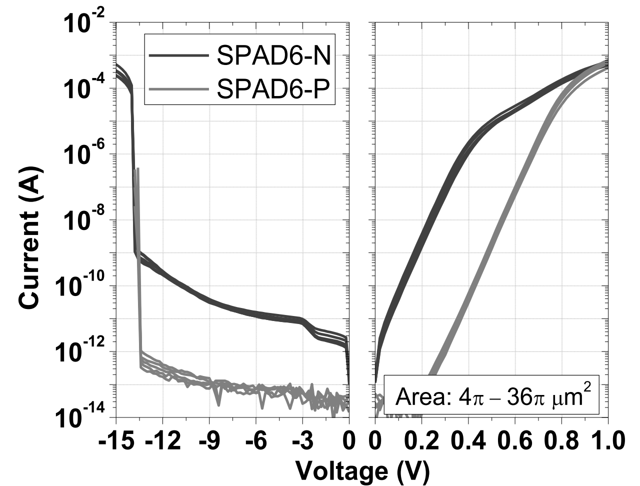

Fig. 7. Reverse (left) and forward (right) I–V characteristics of five SPAD6-N and SPAD6-P diodes measured at 25 °C.

PD30 devices were always the same as for the implanted p^+n-junction diode. This again underlines that thickening the B-layer is a way to obtain complete B-coverage.

For the operation as SPADs, it was important that the breakdown characteristics display an abrupt transition from the low to high current region [18]. This transition is shown in Fig. 7 for both SPAD6-N and SPAD6-P diodes. Despite the almost three decades higher dark currents of the SPAD6-N devices, an abrupt breakdown occurs at the same voltage, 13.5–13.8 V, in both cases. This demonstrates the effectiveness of using an implicit GR configuration to set the breakdown away from the more defect-prone perimeter region [26].

V. Discussion

All the devices examined here that displayed nonideal I–V characteristics at RT, whether as slight increases of n or as clear kinks, were revealed to have prominent kinks when measured at 100 K. In addition, a few devices that appeared to be ideal at RT nevertheless displayed kinked behavior at this low temperature. To further characterize the anomalous high current region that clearly had a different temperature dependence than the ideal region, Richardson plots of $\ln(I_D/T^2)$ as a function of $1/T$ for each measured diode were made from the I–V characteristics to extract the activation energy E_a [42], [46]. Here, I_D is the current of a diode at a bias voltage V_D for a temperature T. If the current is dominated by diffusion, E_a corresponds to the semiconductor bandgap E_g. For thermionic dominated current, E_a corresponds to the effective barrier height ϕ_B of the metal–semiconductor junction [42], [46].

The results are compiled in the histogram shown in Fig. 8. The low current and high current regions represent two distinctly different activation energies being distributed closely around 1.12 eV for the low and 0.65 eV for the high saturation current regions. The different temperature dependence of diffusion- and thermionic-dominated currents means that at temperatures above 348 K, the thermionic-dominated current is no longer discernable, so it was mainly determined at temperatures below 300 K. The extracted barrier heights range

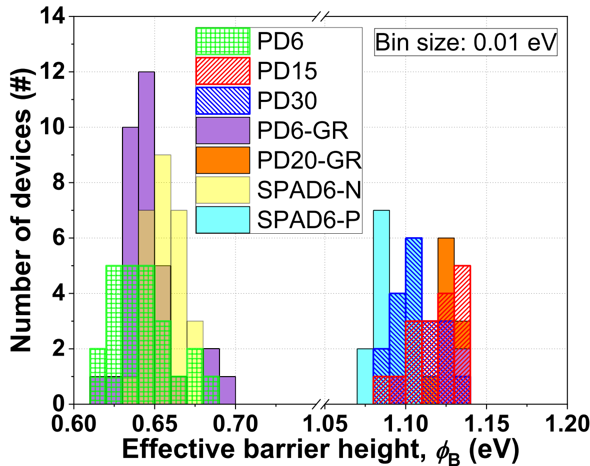

Fig. 8. Histogram of extracted effective barrier heights for many of the PureB diodes described in Table I.

from about 0.6 to 0.7 eV, values that are typically found for Al-n-Si junctions, depending on the exact processing conditions [47]–[49]. When leakage currents were not observable at any temperature, the activation energy originating from diffusion-dominated conduction in Si, 1.12 eV, was found.

Although kinks were frequently observed for the PB6-GR diodes, from the dependence on Al-coverage, the actual number of defects was very low, estimated to be no more than about 10^5 cm^{-2}, and very likely related to particle contamination of the Si surface before B-deposition. In view of the values of the anomalous currents, decades below that of even a few micrometer large Al–Si Schottky diodes, the size of the defects is expected to be less than a micrometer. Even for the SPAD6-N diodes with considerable perimeter leakage, device imaging, using methods such as atomic force microscopy (AFM) and scanning/transmission electron microscopy (SEM/TEM), did not reveal pitting of Si [24]. In the past, studies of B-layers as a material barrier to the Al-metallization did show several pits (inverted pyramids) per 100 μm^2 with cavity sizes mainly smaller than a micrometer if the B-layer was very thin, in that case only 1.8 nm as measured by TEM analysis [30].

Although pits could not be visually identified in the present devices, the concentration of the extracted barrier heights around 0.65 eV strongly suggests that Al is in fact touching Si. In [17], the simulation results led to the conclusion that if the B-layer was locally thinned to values below about 1 nm, current increases would also be seen due to the metal work function causing a lowering of the barrier to electrons otherwise created by the interfacial hole layer. Such a transition region between Al–Si Schottky and Si p^+-n-type junction behavior could not be identified in the present measurements.

The PureB temperature-dependent diode characteristics make clear that the electron injection is efficiently suppressed down to cryogenic temperature just as found for the diffused p^+-n diodes. This supports the earlier observations that the concentration of holes at the Si surface of the PureB devices must be comparable to the doping concentration of diffused p^+-n junctions, even though the holes are locked into an nanometer-narrow space at the interface. However, since the Gummel number of the p^+- and n-regions of the latter devices is such that the hole current is 10–100 times higher than the electron current, depending on the doping of the n-substrate, an exact comparison of the actual electron currents in the two types of diodes cannot be made from these diode measurements. This would require separate measurement of the electron and hole currents as made possible by, for example, vertical bipolar transistors [28].

The use of pure Al as interconnect metal is no longer common in the Si technology due to the undesirable strong reactions with the Si. Nowadays, Al saturated with about 1% Si is used to prevent spiking during the alloying step, but for strongly downscaled devices, barriers between Al and Si are commonly applied, for example, by using a refractory compound such as TiN. Experiments with PureB photodiodes were performed where an additional nanometer-thin TiN layer on top of the B-layer was used to replace the Al grid. Typically, such a grid was patterned to have a 2% coverage of the light-entrance window, with the purpose of lowering the series resistance [11], [23]. TiN has much lower sheet resistance than the bulk B-layer, but, as a disadvantage, the TiN layer formed an extra dead layer for light/electron detection and could not be locally removed by wet-etching. A few experiments were also devoted to the physical vapor deposition of a 10-nm-thick ZrN layer as a barrier between the Al and the B-layer, in the hope that the particle-contamination-related defects would be less likely to result in the appearance of kinks in the I–V characteristics. This, however, did not appear to be the case, probably because the defected structuring was also transferred to the ZrN layer. Nevertheless, ZrN did have the advantage that it was readily etched in diluted HF and could therefore be removed from the light-entrance windows together with Al. The overall impression was that these extra protection/barrier layers increased processing complexity without any notable improvement in the device performance or yield. However, firm conclusions would have to be made on the basis of more statistically sound measurement results.

VI. Conclusion

The temperature-dependent I–V characteristics of 700 °C PureB Si diodes, measured down to cryogenic temperatures, were found to be practically identical to that of diffused Si p^+-n junctions with about the same apparent Gummel number of the p^+-region, corresponding to an integral doping $\sim 5 \times 10^{14}$ cm^{-2}. This indicates that the B–Si interface bonds responsible for the high concentration hole inversion layer in PureB diodes do not lose their efficiency at such low temperatures, i.e., there is no significant current degradation due to freeze-out of the interfacial acceptor states. The PureB diode model incorporating fixed negative interfacial charge instead of B-doping of the bulk Si correctly predicted results down to 100 K, thus giving additional affirmation that the developed model includes the dominant PureB transport properties and associated TCAD simulations are of broad practical value.

Despite the nanometer-shallow nature of the PureB junction, most of the examined devices display near ideal behavior, with ideality factors only increasing from 1 to about 1.1 when the temperature was decreased from 300 to 100 K. Some of the

large photodiodes with a targeted B-layer thickness of 2.5 nm did exhibit nonideal currents in the form of high currents levels that appeared at forward voltages below about 0.5 V, also with $n \approx 1$. In many cases, such current kinks only became evident at low temperatures. The temperature behavior of these high current regions corresponded to that of Al–Si Schottky junctions with $E_a \sim 0.65 \pm 0.05$ eV, while diodes with low current levels consistently displayed $E_g = 1.1 \pm 0.05$ eV. It is plausible that particle contamination of the Si surface before B-deposition was responsible for weak spots in the B-layer that allowed Al to make local contact with Si.

The perimeter of the PureB diodes was critical with respect to avoiding the formation of Al–Si Schottky junctions, which in large diodes was prevented by implementing p^+-implanted GRs around the perimeter. In SPAD devices, implicit GRs leave the perimeter in that respect unprotected. Some of the inspected SPAD devices did display high Schottky-like perimeter currents, but the breakdown voltage was nevertheless abrupt and set entirely by the implicit GR.

The most straightforward way to avoid the risk of Al–Si Schottky formation is to increase the B-layer thickness. This, however, becomes a tradeoff electrically with respect to the series resistance and optically with respect to the dead layer thickness. In particular, at cryogenic temperatures, B tunneling layers are needed to maintain low vertical resistance through the layers since the already high bulk B resistance becomes decades higher when going from RT to 100 K. Therefore, for thin B-layer coverage of large diodes, the cleaning procedure before B-deposition must receive critical attention. For small devices such as SPADs for imagers, the open etching of the anode windows for B-deposition becomes an additional critical step.

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