IoT Receiver Techniques

On Filtering, Power Consumption and Phase Noise

Bart J. Thijssen

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On Filtering, Power Consumption and Phase Noise

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Abstract

The wireless receiver has a significant impact on the connectivity performance and battery lifetime of Internet-of-Things (IoT) devices. High selectivity becomes increasingly important with an increasing number of devices that compete in the congested 2.4GHz industrial, scientific and medical (ISM) band. In addition, low power consumption is very important for IoT receivers as the burden of changing batteries increases proportionally with the number of the devices. Complementary metal-oxide-semiconductor (CMOS) technology allows for highly integrated IoT devices with small form factor, low digital processing power consumption and low costs. This dissertation presents circuit innovations for a CMOS wireless IoT receiver.

Chapter 2 introduces the concept of analog finite impulse-response (FIR) filtering as a low-power, highly-selective and highly flexible channel filter for IoT receivers. An extensive literature overview shows that analog FIR filters have been thoroughly researched for other applications, but these filters have a high power consumption of >1mW.

Analog FIR filtering is proposed in Chapter 3 to realize low power channel selection filters for IoT receivers. High selectivity is achieved using an architecture based on only a single — time-varying — transconductance and integration capacitor. The transconductance is implemented as a digital-to-analog converter (DAC) and is programmable by an on-chip memory. The analog FIR operating principle is shown step-by-step, including its complete transfer function with aliasing. The filter bandwidth and transfer function are highly programmable through the transconductance coefficients and clock frequency. Moreover, the transconductance programmability allows an almost ideal filter response to be realized by careful analysis and compensation of the parasitic circuit impairments. The filter, manufactured in 22nm fully-depleted silicon-on-insulator (FD-SOI), has an active area of 0.09mm^2. Its bandwidth can be accurately tuned from 0.06 to 3.4MHz. The filter consumes 92µW from a 700mV supply. This low power consumption is combined with a high selectivity: $f_{-60\text{dB}}/f_{-3\text{dB}}$=3.8. The filter has 31.5dB gain and 12nV/$\sqrt{\text{Hz}}$ input-referred noise

Parts from this abstract are published in the papers that are the basis of this dissertation. These papers are listed in the List of Publications on page 123 and cited in the corresponding chapters.

for a 0.43MHz bandwidth. The output-referred third-order intercept point (OIP3) is 28dBm, independent of the frequency offset. The output-referred 1dB-compression point is 3.7dBm, and the in-band gain compresses by 1dB for an –3.7dBm out-of-band input signal, while still providing >60dB of filtering.

In Chapter 4, a 2.4GHz zero-IF receiver front-end is proposed that reduces power consumption by 2× compared to state-of-the-art and improves selectivity by >20dB without compromising on other receiver metrics. To achieve this performance, the entire receive chain is optimized. The low-noise transconductance amplifier is optimized to combine low noise figure (NF) with low power consumption. State-of-the-art sub-30nm CMOS processes have almost equal strength complementary transistors, which result in altered design trade-offs. A Windmill 25%-duty cycle frequency divider architecture is proposed that uses only a single NOR-gate buffer per phase to minimize power consumption and phase noise. The proposed divider requires half the power consumption and has 2dB or more reduced phase noise when benchmarked against state-of-the-art designs in simulation. An analog FIR filter is implemented to provide very high receiver selectivity with ultra low power consumption. The receiver front-end is fabricated in a 22nm FD-SOI technology and has an active area of 0.5mm^2. It consumes 370µW from a 700mV supply voltage. This low power consumption is combined with 5.5dB NF. The receiver has –7.5dBm input-referred third-order intercept point (IIP3) and 1dB gain compression for a –22dBm blocker — both at maximum gain of 61dB. From three channels offset onward the adjacent-channel rejection is ≥63dB for BLE, BT5.0 and IEEE802.15.4.

A feedforward phase noise cancellation technique to reduce phase noise of the output clock signal of a phase-locked loop (PLL) is presented in Chapter 5. It uses a sub-sampling phase detector (SSPD) to measure the phase noise and a variable time delay for cancellation. Both phase noise and spurs are reduced. Analytical expressions have been derived that characterize the performance of this technique and show its fundamental limitations. A sub-sampling phase-locked loop (SSPLL) with the cancellation technique as a built-in feature is described. The feedforward technique has no stability requirements in contrast to conventional PLL improvements. The phase noise reduction bandwidth is increased to almost a third of the reference frequency — 3× the maximal bandwidth for 3$^{\text{rd}}$ order type-II PLLs. The proposed analytical model shows a phase noise reduction of 9dB at a frequency offset of $f_{ref}/10$. The total rms jitter is improved by 7.2dB. The analytical results are verified by simulations.

To summarize, this dissertation proposes system and CMOS circuit architectures that allow to improve the performance of an IoT receiver while reducing its power consumption. The analog FIR filter allows for a >20dB increased selectivity. Furthermore, the analog FIR techniques proposed in this dissertation have many other potential applications. The proposed Windmill divider architecture halves the power consumption while reducing the phase noise. The feedforward phase noise cancella-

tion architecture reduces the PLL rms jitter by 7.2dB without significantly increasing its power consumption.

Samenvatting

De draadloze ontvanger heeft een aanzienlijke impact op de connectiviteit en de batterijlevensduur van een apparaat voor het Internet-der-Dingen (Internet-of-Things (IoT)). Hoge selectiviteit wordt alleen maar belangrijker, omdat er steeds meer apparaten concurreren in de al overvolle 2.4GHz industriële, wetenschappelijke en medische (ISM) frequentieband. Naast hoge selectiviteit is een laag energieverbruik zeer belangrijk voor IoT-ontvangers — de last van het vervangen van de batterijen stijgt evenredig met het aantal apparaten. Complementaire metaal-oxide-halfgeleider (CMOS) technologie maakt IoT apparaten mogelijk met een hoge vorm van integratie, een kleine vormfactor, lage kosten en een laag energieverbruik van de digitale signaalverwerking. Dit proefschrift presenteert circuit innovaties voor een CMOS draadloze IoT ontvanger.

Hoofdstuk 2 introduceert analoge eindige-impulsresponsie (FIR) filters als een zeer selectief, zeer flexibel en tevens laag vermogen oplossing voor kanaalfilters in IoT-ontvangers. Een uitgebreid literatuuronderzoek toont aan dat analoge FIR filters uitvoerig zijn onderzocht. Deze gepubliceerde analoge FIR filters hebben echter een hoog energieverbruik van >1mW.

Analoge FIR filters worden geïntroduceerd in Hoofdstuk 3 om kanaalfilters met een laag energieverbruik te realiseren voor IoT-ontvangers. Hoge selectiviteit is bereikt door middel van een architectuur met slechts één enkele — tijdafhankelijke — transconductantie en integratie condensator. De transconductantie is geïmplementeerd als een digitaal-naar-analoog omzetter en is programmeerbaar door middel van een geheugen op de chip. Het analoge FIR werkingsprincipe is stap-voor-stap uitgelegd, inclusief de volledige overdracht en vouwvervorming (aliasing). De bandbreedte en overdracht van het filter zijn programmeerbaar via de transconductantiecoëfficiënten en klokfrequentie. Een bijna ideale filteroverdracht kan worden gerealiseerd, door de filter coëfficiënten zo te programmeren dat het effect van de parasitaire uitgangsweerstand van de transistor wordt gecompenseerd. Het filter, geproduceerd in 22nm fully-

Onderdelen van deze samenvatting zijn een vertaling van de gepubliceerde artikelen die de basis vormen van dit proefschrift. Deze artikelen zijn opgesomd in de List of Publications op pagina 123 en geciteerd in de bijbehorende hoofdstukken.

depleted silicon-on-insulator (FD-SOI), heeft een actieve oppervlakte van 0.09mm^2. De filter bandbreedte kan nauwkeurig worden ingesteld tussen 0.06 en 3.4MHz. Het filter verbruikt 92µW van een 700mV voeding. Dit lage energieverbruik wordt gecombineerd met een hoge selectiviteit: $f_{-60\text{dB}}/f_{-3\text{dB}}$=3.8. Het filter heeft 31.5dB versterking en 12nV/$\sqrt{\text{Hz}}$ ruis gerefereerd naar de ingang bij een 0.43MHz bandbreedte. Het uitgangsgerefereerde derde-orde snijpunt (OIP3) is 28dBm, onafhankelijk van de frequentieafstand. De 1dB-compressie is 3.7dBm gerefereerd naar de uitgang. De versterking in de signaalband comprimeert met 1dB bij een 3.7dBm ingangssignaal buiten de filterband, terwijl het signaal buiten de band nog steeds >60dB wordt verzwakt.

In Hoofdstuk 4 wordt een 2.4GHz ontvanger frontend geïntroduceerd met 2× lager energieverbruik en verbeterde selectiviteit van >20dB ten opzichte van de meest recente publicaties zonder concessies te doen aan andere ontvangerseigenschappen. De volledige ontvangstketen is geoptimaliseerd om te komen tot deze prestaties. De lage ruis transconductantie versterker (LNTA) is geoptimaliseerd om een laag ruisgetal (NF) te combineren met een laag energieverbruik. Moderne sub-30nm CMOS processen hebben even sterke transistoren, wat resulteert in nieuwe ontwerpcompromissen. Een Windmolen 25%-arbeidscyclus frequentiedeler architectuur wordt gepresenteerd met maar één NOF-poort buffer per uitgangsfase om het energieverbruik en de faseruis te minimaliseren. De frequentiedeler heeft een gehalveerd energieverbruik en heeft ≥2dB minder faseruis in vergelijking — door middel van simulatie — met de meest recente publicaties. Een analoog FIR filter voorziet de ontvanger van een zeer hoge selectiviteit zonder het energieverbruik (significant) te verhogen. Het ontvanger frontend is geproduceerd in een 22nm FD-SOI technologie en heeft een actieve oppervlakte van 0.5mm^2. De ontvanger verbruikt 370µW van een 700mV voeding in combinatie met een 5.5dB NF. Het ingangsgerefereerde derde-orde snijpunt (IIP3) is –7.5dBm en er is 1dB versterkingscompressie bij een –22dBm verstoorder — beide voor de maximale versterking van 61dB. Vanaf 3 kanalen afstand is de naburig kanaalonderdrukking (ACR) ≥63dB voor de radiostandaarden BLE, BT5.0 en IEEE802.15.4.

Hoofdstuk 5 presenteert een vooruitgekoppelde faseruis annuleringstechniek om de faseruis te verminderen van het uitgangskloksignaal van een fase gekoppelde lus (PLL). Een sub-bemonstering (sub-sampling) fasedetector wordt gebruikt om de faseruis te meten en een varieerbare vertragingsbuffer voor annulering. Zowel de faseruis als andere onzuivere signalen worden gereduceerd. Analytische expressies zijn afgeleid om de prestatie van deze techniek te bepalen alsook de fundamentele limieten. Een sub-sampling PLL (SSPLL) met een ingebouwde faseruis annulering is beschreven. De vooruitgekoppelde techniek introduceert geen stabiliteitsproblemen in tegenstelling tot conventionele PLL technieken. De faseruisreductiebandbreedte is toegenomen tot bijna een derde van de referentiefrequentie — 3× de maximale bandbreedte van 3de orde type-II PLLs. Het analytische model toont een faseruisreductie van 9dB

voor een frequentieafstand van $f_{ref}/10$. De totale rms jitter is verbeterd met 7.2dB. De analytische resultaten zijn geverifieerd door middel van simulaties.

Dit proefschrift presenteert systeem en CMOS-schakeling architecturen die de prestaties van een IoT-ontvanger verbeteren voor een verminderd energieverbruik. Het analoog FIR filter zorgt voor een sterk verbeterde selectiviteit (>20dB). De analoge FIR technieken uit dit proefschrift zijn niet gelimiteerd tot zuinige ontvangers, maar kunnen worden gebruikt in vele toepassingen. De Windmolen frequentiedeler architectuur halveert het energieverbruik in combinatie met een gereduceerde faseruis. De faseruisannuleringsarchitectuur vermindert PLL rms jitter met 7.2dB zonder het energieverbruik significant te verhogen.

Dankwoord

It has been an interesting journey studying at and working for the Integrated Circuit Design (ICD) group. It all started in 2012 — the second year of my advanced technology (AT) bachelor — with Elbasfun and now comes to an end with this dissertation. The main thing I have learned from all of you is the ICD design approach: Finding simple solutions for the most difficult problems. We do this by fully understanding the challenges, including every important detail. I fully agree with and really enjoy this design philosophy.

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There's a way to do it better —
find it.

Thomas A. Edison

1

Introduction

Wireless connectivity is one of the cornerstones that enable modern society. It allows people to keep in touch with their family and friends across the world. The possibility to access entertainment, but also knowledge and know-how anytime and anywhere. Businesses to operate globally.

Nowadays, there is a trend to connect more and more devices to the internet in the so-called Internet-of-Things (IoT), sometimes referred to as Internet-of-Everything (IoE). The connected devices allow for monitoring and optimization of all kinds of systems, e.g.:

- Health care, e.g., by monitoring heart beat and by making electrocardiograms (ECGs) using smartwatches;
- Entertainment, e.g., by wireless earbuds;
- Productivity, e.g.;
    - in the office, smart pens, wireless mice and keyboards that connect to multiple computers;
    - in industry, smart tools in factories that automatically provide the correct torque to different bolts;
    - in agriculture, connected tractors that drive automatically between crops;
- Safety, e.g., wireless connected smoke detectors;

- Home automation, e.g., smart thermostats that heat your house when you drive home; retractable awnings that open when its sunny and close during a storm by a wireless connected sun detector and wind detector, respectively.

Basically, the list of potential applications is endless.

Wireless connectivity is at the heart of the IoT trend. It is *the* essential building block in making devices smart: Connecting devices to a smartphone, the cloud or both. IoT devices often have a small form factor in the order of centimeters. Furthermore, many IoT devices are battery powered to remove the costs of installing cables, increase convenience and reduce the form factor.

The IoT scope is to connect *literally everything*. As a result, the wireless environment will become increasingly congested. Therefore, high selectivity and good linearity become increasingly important to allow proper operation of wireless links — also for low power IoT devices. On the other hand, low costs are desired to enable the large increase of connected devices.

Both form factor and costs drive the trend to maximum integration — minimal off-chip components. Complementary metal-oxide-semiconductor (CMOS) technology enables these highly integrated devices as it allows for implementation of wireless connectivity, digital processing and sensor/actuator interfaces on a single chip. Considering the rapidly increasing number of IoT devices, the burden and costs of changing batteries increases proportionally. It is therefore paramount to minimize the energy consumption to increase lifetime.

The IoT devices are often not connected to the internet themselves, because a Wi-Fi or mobile connection entails to much power consumption. It would require a too large battery. Most often they are connected to a bridge device — that is connected to the internet — using a low power wireless standard such as Bluetooth Low Energy (BLE) [1] or IEEE802.15.4, e.g. music streaming to wireless earbuds via a smartphone using BLE.

The contradictory requirements necessitate innovations on the wireless connectivity. The main research subject of this dissertation is to improve the selectivity of a CMOS 2.4GHz IoT receiver while reducing its power consumption. This chapter introduces the context of this dissertation. High performance receivers, with high selectivity, have been published, but have off-chip components and/or high power consumption. Therefore, the chapter starts with providing a more general perspective on the energy consumption constraint and the related battery capacity. Maximum integration of the receiver is accomplished by having *no* off-chip components for matching or filtering. The next section describes the requirements on the other performance metrics of a wireless IoT receiver — in the context of the given power consumption — followed by a summary of the motivation and goal of this work. The last section provides the outline of this dissertation.

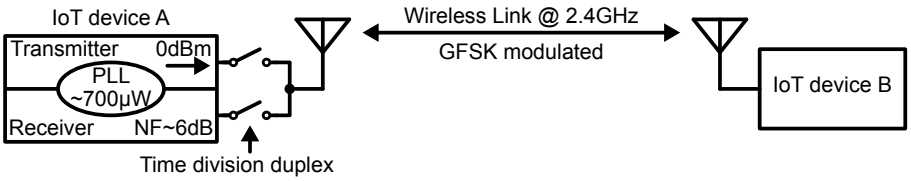


Figure 1.1: A BLE wireless link.

1.1 Wireless Connectivity Energy Consumption

As most IoT devices are battery powered, low energy consumption is perhaps the most important metric for IoT devices. The wireless communication is often the dominant contributor to the power consumption [2]. Therefore, the communication is heavily duty-cycled to increase battery lifetime. Although duty-cycled, the wireless communication is still a major contributor to the IoT device's energy consumption.

First, the power consumption in a wireless 2.4GHz IoT link is described to provide more context. Afterwards, a closer look on battery capacity is taken to reveal important insights in battery lifetime followed by a summary.

1.1.1 Power Consumption Wireless Link

Fig. 1.1 shows a typical wireless link for BLE. Wireless radio communication requires both transmission and reception. These functionalities are provided by the transmitter and receiver, respectively. Both functionalities are implemented together in a transceiver. From an electronics perspective these functionalities can generally be divided into separate architectures. Both transmitter and receiver require a phase-locked loop (PLL) clock for up-conversion and down-conversion, respectively. IoT standards most often use time-division duplexing, which allows a separate configuration of the matching network for transmission and reception and thereby a single antenna. Using multiple antennas or a circulator is too expensive.

Most IoT communication standards employ constant envelope modulation techniques based on phase or frequency modulation. This allows for highly non-linear power amplifiers on the transmit side, which are much more efficient than linear power amplifiers; as required for non-constant envelope modulation schemes. E.g. BLE employs Gaussian frequency-shift-keying (GFSK) [1].

A couple of specifications can already be estimated from the power consumption of the PLL. A state-of-the-art very low power all-digital phase-locked loop (ADPLL) for BLE consumes roughly 700µW [3]. This is constrained by the limited Q-factor and inductance value of on-chip inductors. The voltage-controlled oscillator (VCO) voltage swing — which is part of a PLL — is directly related to its minimal power

consumption to maintain oscillation [2]. A ring oscillator can be designed with a lower power consumption. However, it is not an option as it requires roughly 1000× more power consumption for the same phase noise compared to an *LC*-oscillator. The theoretical figure-of-merit (FoM)[1] of a ring oscillator is –165dBc/Hz [4], while a state-of-the-art *LC*-oscillator has a FoM of –195dBc/Hz [5]. If an *LC*-oscillator with a power consumption 10× below its practical limitation is desired, a ring oscillator alternative would require 100× more power than the *LC*-oscillator minimum. The 700µW PLL power consumption provides a lower limit on the power consumption for transmission and reception.

The transmitted power is often around 0dBm [1], so the total transmission power consumption is at least 1.7mW. Reducing the transmitted power further does not reduce the power consumption a lot, since the total power consumption is limited to ∼700µW.

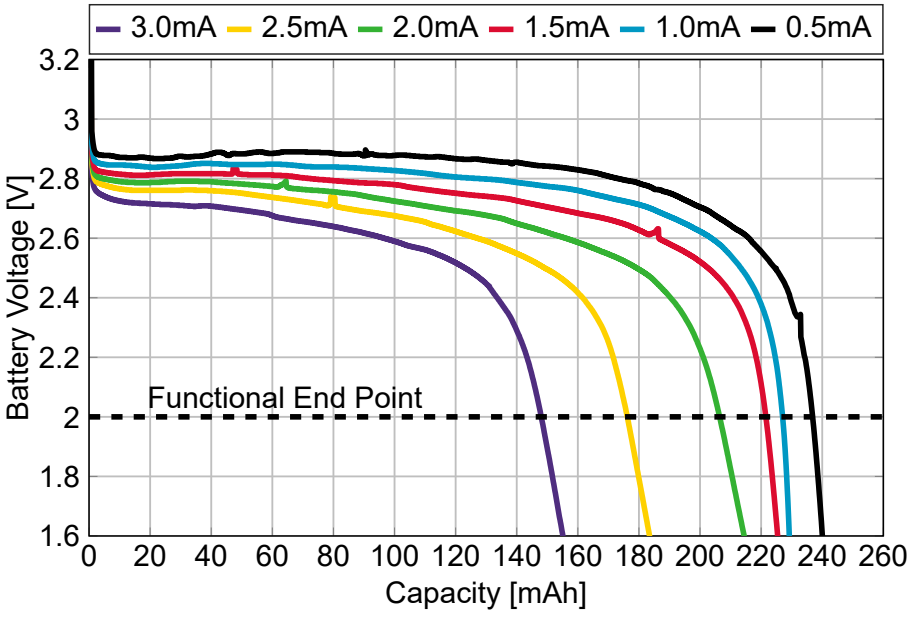
From the receiver perspective, it cannot be justified to compromise on the receiver front-end performance to reduce its power consumption far below the 700 µW limit. Practically, the noise figure (NF) should be sub-6dB as this NF can be obtained in designs of around 1mW [6–9]. Furthermore, considering the link budget, it can be concluded that comprising on the NF is not desired. E.g. a 9dB NF transceiver with 3dBm transmit power would provide the same link budget, but would increase the transmission power consumption by at least 1mW, which is roughly equal to the entire power consumption of sub-6dB NF receiver front-end.

1.1.2 Battery Lifetime

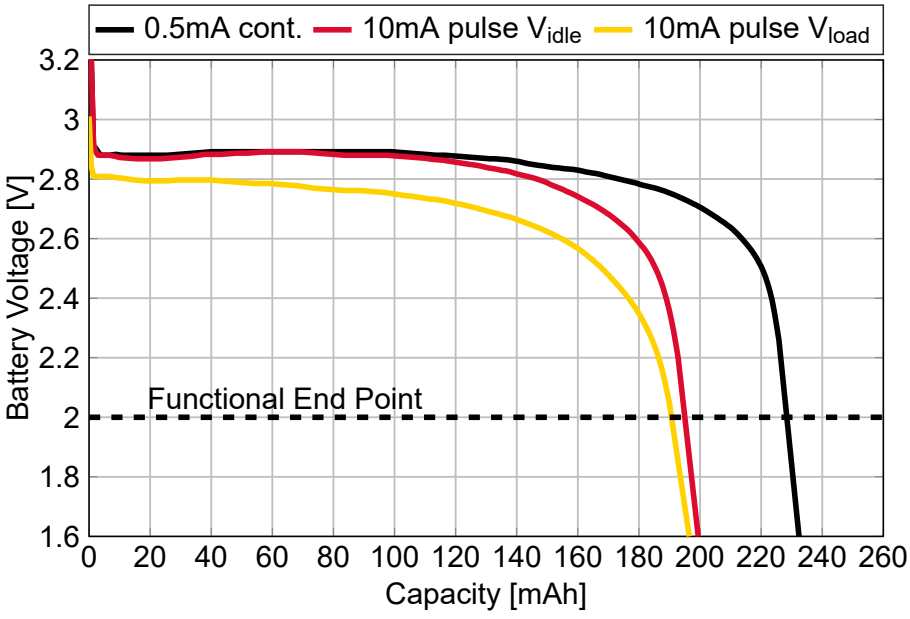
Fig. 1.2 shows the capacity of the commonly used CR2032 coin cell battery [10]. The battery capacity is limited by the functional end point of the IoT device — the minimum voltage at which the device can operate. Fig. 1.2a shows the CR2032 capacity for different load currents. By reducing the current from 3mA to 0.5mA, the battery capacity increases by about 60%. The lifetime is increased more than 9.5× instead of the 6× prediction based on current consumption alone.

Since the wireless communication is most often duty-cycled, the current that the battery has to provide is pulsed. The current consumption during communication is much larger than otherwise. Fig. 1.2b compares the battery capacity of a 0.5mA continuous load with a pulsed load. The pulsed load consists of a continuous 0.1mA current plus a 10mA, 1ms current pulse every 25ms to maintain the same average load current of 0.5mA [10]. Both the battery voltage when idle (V_{idle}) and during a pulse (V_{load}) are shown. The pulsed current battery capacity is reduced by roughly 20%.

[1] FoM $= \mathcal{L}(\Delta f) - 20\log(f_{osc}/\Delta f) + 10\log(P/1\text{mW})$, where $\mathcal{L}(\Delta f)$ is the phase noise in dBc/Hz at frequency offset Δf, f_{osc} the oscillator frequency and P the power consumption in mW.



(a)



(b)

Figure 1.2: CR2032 coin cell battery voltage during discharging. (a) Continuous current [10]. (b) Continuous and pulsed current compared; 1ms on, 24ms off [10].

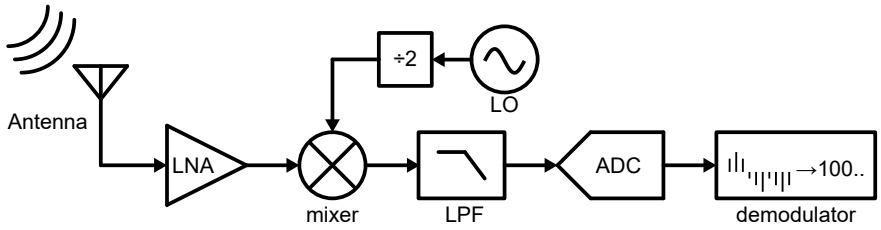


Figure 1.3: A typical wireless receiver architecture.

1.1.3 Summary

The scope of this work is the receiver including PLL. The receiver is important in terms of power consumption and wireless performance of IoT devices. Furthermore, it is clear that also the PLL is very important in terms of the total power consumption and provides a design constraint.

To increase battery life, low power consumption is important from multiple viewpoints. Low power consumption reduces the energy drawn per second and therefore the lifetime given a battery capacity. A larger current consumption reduces the battery capacity. Furthermore, when duty-cycling is employed to increase the lifetime, a high peak current reduces the battery capacity and thereby the lifetime.

1.2 Wireless Receiver for IoT

Fig. 1.3 shows a typical wireless receiver architecture, either with zero intermediate frequency (IF) or low-IF. A radio signal is detected by an antenna. This received signal is amplified by a low-noise amplifier (LNA). Afterwards the amplified signal is downconverted to baseband by means of a mixer. The mixer employs multiphase clocks that are provided by a frequency divider. The frequency divider has as input a clock signal that comes from a local oscillator (LO) — the PLL. Channel selection filtering is done in baseband by means of a low-pass filter (LPF). The filtered signal is fed to an analog-to-digital converter (ADC) to allow demodulation in the digital domain. The performance metrics are discussed in the context of a 2.4GHz IoT receiver.

Other architectures were proposed to reduce power consumption, e.g., sliding-IF [11–15], phase domain [6–8, 16–18], a combination [19] or in-phase/quadrature-phase (I/Q) generation in the radio frequency (RF) signal path [20]. However, these proposals do not obtain lower power consumption than the more conventional zero-IF [9, 21, 22] or low-IF [23–36] architectures.

Power consumption is important, but other receiver metrics should also be ade-

quate. The noise performance of a receiver is characterized by its NF or sensitivity. A state-of-the-art NF is roughly sub-6dB, resulting in a sensitivity of around –94dBm or lower [6–9, 11–15, 21, 22, 25, 26, 28–33, 36] — depending on the demodulation technique.

Other receiver metrics like filtering and linearity are also important to characterize its performance. Unfortunately, these are not always provided in publications, which makes fair comparison difficult. State-of-art adjacent-channel rejection (ACR) is roughly 40dB at 3MHz offset for BLE [7, 8, 14, 22, 33, 35, 36]. The best published linearity in terms of input-referred third-order intercept point (IIP3) is around –6dBm at maximum gain [23, 24]. However, this receiver has an 8.5dB NF and two supply voltages.

1.3 Motivation and Goal

High selectivity will become increasingly important in the already congested 2.4GHz ISM-band. However, this should not come at the cost of other receiver metrics and, preferably, at minimal power consumption to improve battery lifetime. Furthermore, re-configurability of the receiver is increasingly important, because modern IoT receivers should cope with an increasing number of standards, that include more and more flexibility. To summarize, the goal of this work is to invent circuit techniques to obtain a receiver front-end that has:

- Improved selectivity, significantly above 40dB ACR;
- Sub-6dB NF;
- >–10dBm IIP3;
- Minimal off-chip components, i.e. no off-chip matching or filtering;
- Reduced power consumption, significantly below 1mW;
- Flexibility/Programmability.

As the receiver selectivity increases, a low phase noise LO source becomes more important. Therefore, also techniques to reduce the LO phase noise for the same power consumption are researched.

1.4 Dissertation Outline

The dissertation is organized as follows. Chapter 2 gives is an overview of analog finite impulse-response (FIR) filters, discussing the concept and transfer function. This is

followed by a literature overview that presents analog FIR filtering from a historical, implementation and application perspective. The prior art is discussed with respect to the IoT receiver application of this work. Furthermore, analog FIR circuits that are implemented in other domains are reviewed.

Chapter 3 presents a low power analog FIR filter architecture that is designed as a channel selection filter for an IoT receiver. The full transfer function is analytically derived — including all aliases. The filter architecture performance is determined by measurements on a prototype in 22nm fully-depleted silicon-on-insulator (FD-SOI) technology.

Chapter 4 presents a 2.4GHz highly selective IoT receiver front-end implemented in 22nm FD-SOI. This design incorporates the analog FIR filter of Chapter 3 as baseband channel selection filter. It combines the best selectivity and lowest power consumption to date, with good NF and linearity compared to state-of-the-art IoT receivers. The low power consumption is obtained by a zero-IF architecture with circuit optimizations across the entire receive chain, including a novel frequency divider architecture.

The improved ACR of the receiver front-end in Chapter 4 requires low LO phase noise. A phase noise cancellation PLL architecture that can accomplish this is described in Chapter 5. A theoretical analysis of the technique is provided. This architecture can be used to reduce the PLL phase noise without (significant) increase of its power consumption.

Chapter 6 presents the final conclusions of this dissertation, including the original contributions to the field and recommendations.

The published papers of this work are the foundation of this dissertation. These papers are listed in the List of Publications on page 123 and cited in the corresponding chapters. The author is aware that Chapters 3 to 5 partially overlap with other chapters. However, the author preferred minimal modification of the — already — reviewed and accepted papers.

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I have not failed. I've just found
10,000 ways that won't work.

Thomas A. Edison

2

Analog FIR Filtering

Highly selective receivers require channel selection filters with steep roll-off and strong attenuation. FIR filters have these properties and can be part of a low power receiver architecture when implemented in the analog domain.

This chapter provides an overview of analog FIR filters. First, the basics of analog FIR filtering is explained. This section was previously co-published in IEEE Solid-State Circuits Letters [1] and at the European Solid-State Circuit Conference [2]. In the next section, the analog FIR transfer function properties are analyzed in detail. Section 2.3 describes the previously published work from a historical, implementation and application perspective. Furthermore, the prior art is discussed in the context of the IoT receiver application. Analog filters with a finite impulse-response that are not implemented on-chip are outlined in Section 2.4. The chapter finalizes with a summary.

2.1 Basic Concept

Fig. 2.1 illustrates the working principle of analog FIR filters by comparing it to its digital equivalent. A 6-tap digital FIR filter is shown in Fig. 2.1a. The input signal $x[n]$ is passed through a delay line with delays z^{-1}. The delayed samples of $x[n]$ are multiplied by an appropriate weight w_a and summed providing the output $y[n]$. The weights w_a represent the impulse response of the FIR filter. $y[n]$ can be downsampled resulting in output signal $y^*[k]$ without introducing significant aliases in-band, when

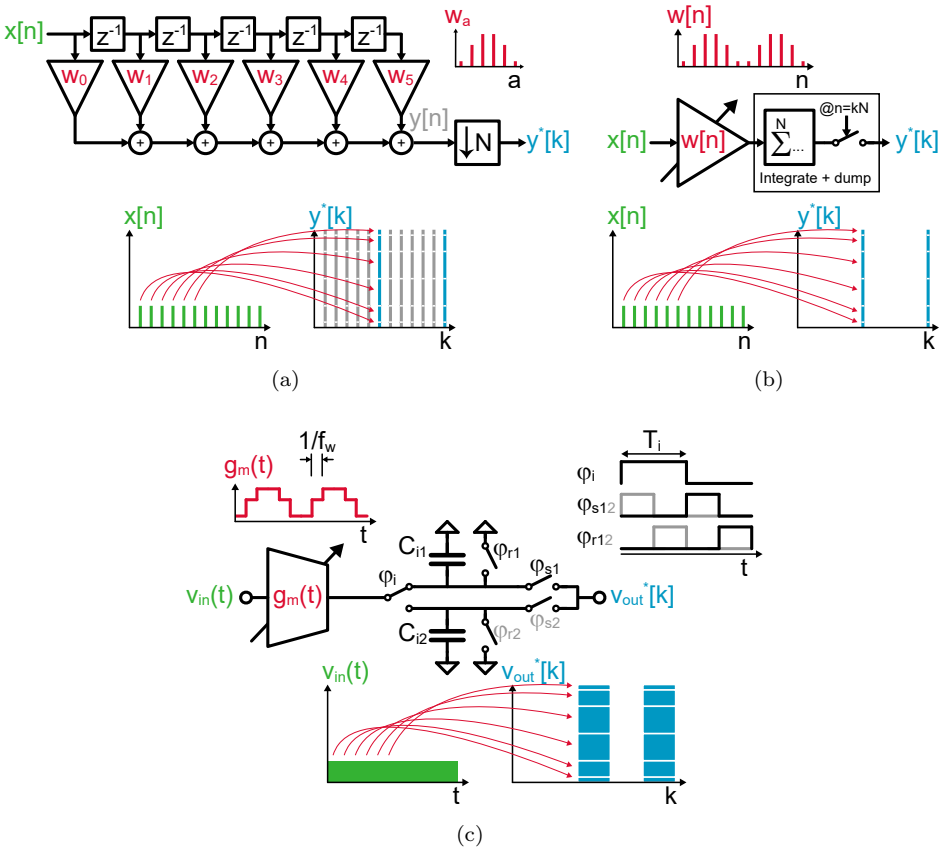


Figure 2.1: Comparison of different implementations of 6-tap digital and analog FIR filters. Input signals $x[n]$ and $v_{in}(t)$ are assumed constant for simplicity. (a) Digital FIR with downsampling. (b) Digital FIR with accumulator. (c) Hardware efficient analog FIR.

the FIR filter rejection is sufficient. The corresponding timing diagram shows that an output sample of $y^*[k]$ consists of the weighted sum of different time instances of $x[n]$. The straightforward analog implementation is to store the input on multiple capacitors and sum the capacitor voltages while applying the appropriate weighting [3, 4]. However, this becomes very hardware intensive when moving towards a high number of FIR taps.

Fig. 2.1b shows an alternative approach to implement the same filter. Instead of storing the previous input samples, $x[n]$ is multiplied by *time-varying* weighting coefficient $w[n]$ and accumulated in the integrate+dump block. The output signal

$y^*[k]$ is constructed in the same way as in Fig. 2.1a and therefore the implementation of Fig. 2.1b has the same filter response.

The proposed analog FIR filter is shown in Fig. 2.1c. It performs a similar operation as its digital analogy (Fig. 2.1b). The input signal $v_{in}(t)$ is converted to current via transconductance $g_m(t)$. The transconductance $g_m(t)$ varies in time at rate f_w according to the FIR weighting coefficients w_a. The transconductor output current is integrated (summed) on integration capacitor C_{i1} during ϕ_i. The output voltage sample $v^*_{out}[k]$ is sampled during ϕ_s and reset in during ϕ_r. Meanwhile, the input signal is integrated on the other capacitor C_{i2}; providing time for readout and reset. The output samples are thus determined by a weighted summation of previous input "samples" — similarly as in Fig. 2.1a and Fig. 2.1b. However, the windowed integration at f_w introduces an extra sinc pre-filter.

The analog FIR transfer function neglecting aliasing is[1] [5]

$$H(f) \approx \underbrace{\frac{\overline{g}_m T_i}{C_i}}_{\text{gain}} \underbrace{\operatorname{sinc}\left(\frac{f}{f_w}\right) e^{j\pi \frac{f}{f_w}}}_{\text{windowed } \int} \underbrace{\sum_{a=0}^{N-1} w_a z^{-a}\Big|_{z=e^{j2\pi \frac{f}{f_w}}}}_{\text{FIR}} \tag{2.1}$$

where $\overline{g}_m$ is the average transconductance, w_a the weighting coefficients normalized to $\sum w_a = 1$ and N the number of FIR coefficients. The transfer consists of three parts: gain, sinc windowed integration and the FIR filter. Note that the filter characteristic is determined by the weighting coefficients — only the gain is dependent on $\overline{g}_m/C_i$. The analog FIR input signal is time-continuous and the output signal time-discrete, so in addition to filtering also aliasing occurs. The output sample rate f_s is significantly lower than the time-continuous input. Fortunately, the very strong filtering characteristic of the analog FIR provides sufficient pre-filtering by itself.

The filter bandwidth is inversely proportional — for a given set of FIR coefficients w_a — to the filter delay $1/f_w$ and integration time $T_i = N/f_w$. By doubling T_i, the filter bandwidth is halved. Fig. 2.1c describes a *single path* analog FIR design, which filter characteristic is limited by the fixed relationship between sample rate and bandwidth: $f_s = 1/T_i$. This constraint is broken by interleaving multiple paths. For m paths, this results in an output sample rate

$$f_s = \frac{m}{T_i} \quad m = 1, 2, 3... \tag{2.2}$$

2.2 Transfer Function Analysis

FIR filter theory can be used to design the analog FIR filter's coefficients. This section starts from the transfer function characteristics based on (2.1) and ends by including

[1] In this dissertation, sinc refers to the normalized function: $\operatorname{sinc}(x) = \frac{\sin \pi x}{\pi x}$

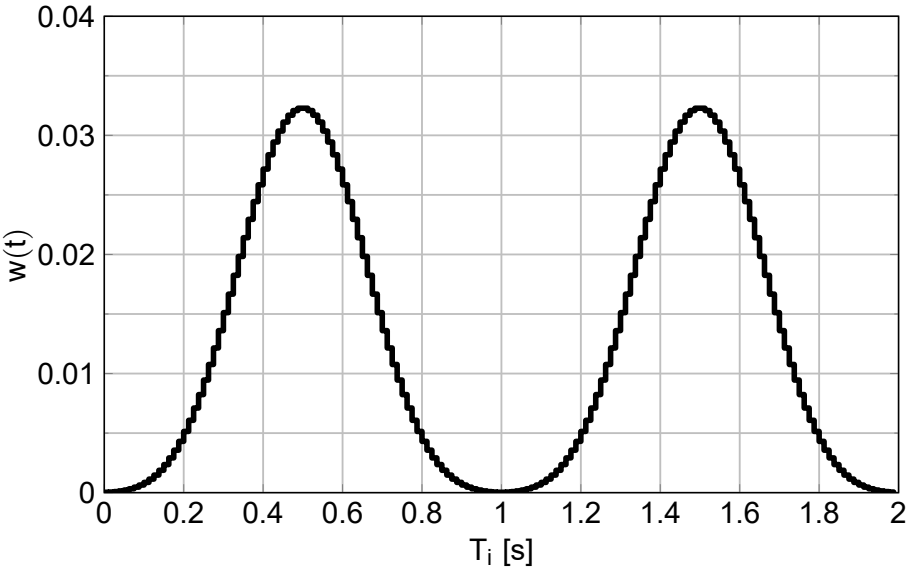


Figure 2.2: Normalized filter coefficients as function of T_i.

the aliasing due to the output sample rate to provide the complete aliasing picture. A more elaborate analytical derivation is provided in Section 3.2 on page 43, including a frequency domain example starting from several input signals.

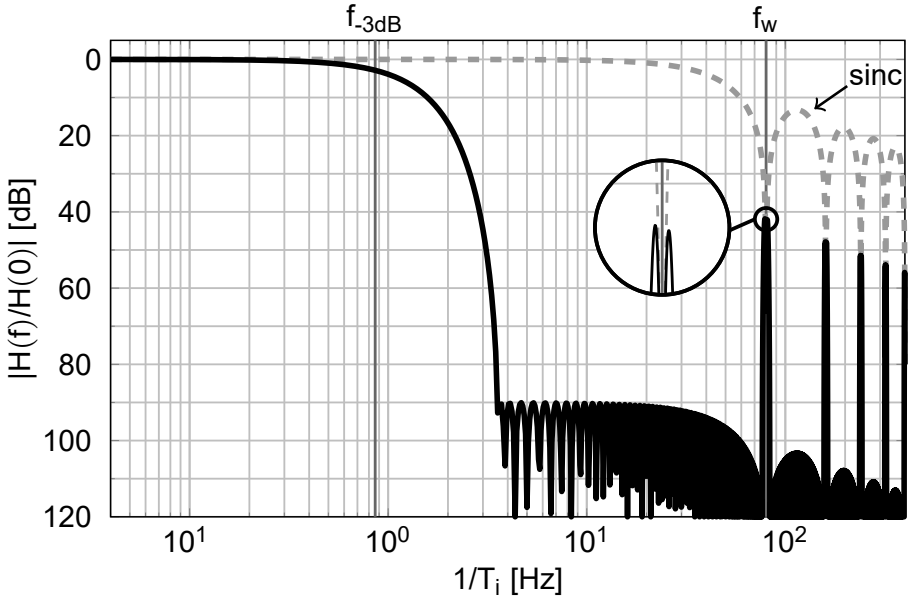
The coefficients of a Chebyshev window with –90dB stopband depth are shown in Fig. 2.2. The time variant filter code $w(t)$ is periodic — one set of coefficients are provided each integration cycle. The coefficients are normalized to $\overline{w(t)} = 1/N$ as in (2.1). The number of coefficients is

$$N = f_w T_i \tag{2.3}$$

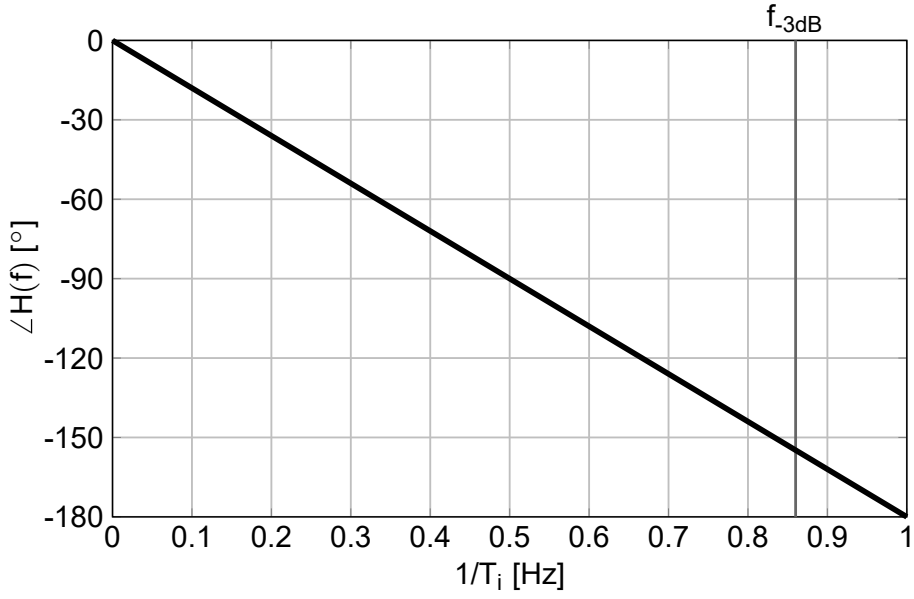
in this example 80. The code is provided with a zero-order hold to the input, which results in the sinc filtering in (2.1).

Fig. 2.3 shows the corresponding analog FIR filter response as function of the integration frequency $(1/T_i)$. The filter –3dB-bandwidth $f_{-3\text{dB}}$ is approximately $0.86/T_i$. The gain shows a very steep roll-off (Fig. 2.3a). The stopband starts at $4.1 f_{BW}$ and has –90dB attenuation as designed. Filter aliases are located at multiples of f_w and are filtered by the inherent sinc filter as expected. The FIR filter transfer is independent of the number of filter coefficients, only the filter aliases are. The phase response is shown in Fig. 2.3b. It has a linear phase response, because the filter coefficients are symmetric.

The number of time-interleaved paths determines the output sample rate and thereby the aliasing at the output.



(a)



(b)

Figure 2.3: Analog FIR filter transfer as function of the integration frequency. (a) Normalized gain. (b) Phase.

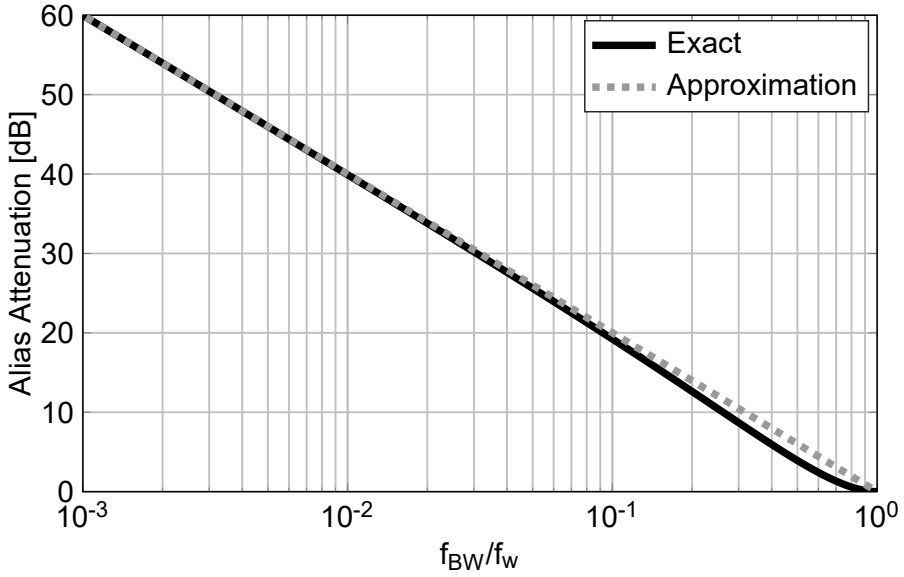


Figure 2.4: Attenuation of the first analog FIR filter alias as function of the normalized filter bandwidth.

2.2.1 Filter Alias Attenuation

Fig. 2.3a already indicates that the filter alias attenuation depends on the filter bandwidth f_{BW}: A more narrowband filter will result in a smaller alias as it is more strongly suppressed by the sinc notches. The filter aliases occur on both sides of a notch, but the alias left of the notch is the largest. The sinc gain at the first alias is

$$\begin{aligned} |H_{\text{sinc}}(f_w - f_{BW})| &= \left| \text{sinc}\left(\frac{f_w - f_{BW}}{f_w} \right) \right| \\ &\approx f_{BW}/f_w \end{aligned} \tag{2.4}$$

assuming $f_{BW} \ll f_w$. (2.4) provides the filter alias gain for a brick-wall pass-band. The filter alias attenuation is shown in Fig. 2.4 as function of bandwidth ratio, the alias attenuation is approximately 3dB more if the –3dB filter bandwidth is used. The alias at the left-hand side of the notches can be removed by using the quadrature signal path in a radio receiver. The approximation of (2.4) also holds for the right-hand side alias as long as $f_{BW} \ll f_w$.

2.2.2 Time-Interleaving and Output Sample Rate

The number of time-interleaved filter paths determines the output sample rate f_s proportionally according to (2.2). f_s eventually determines the output Nyquist rate

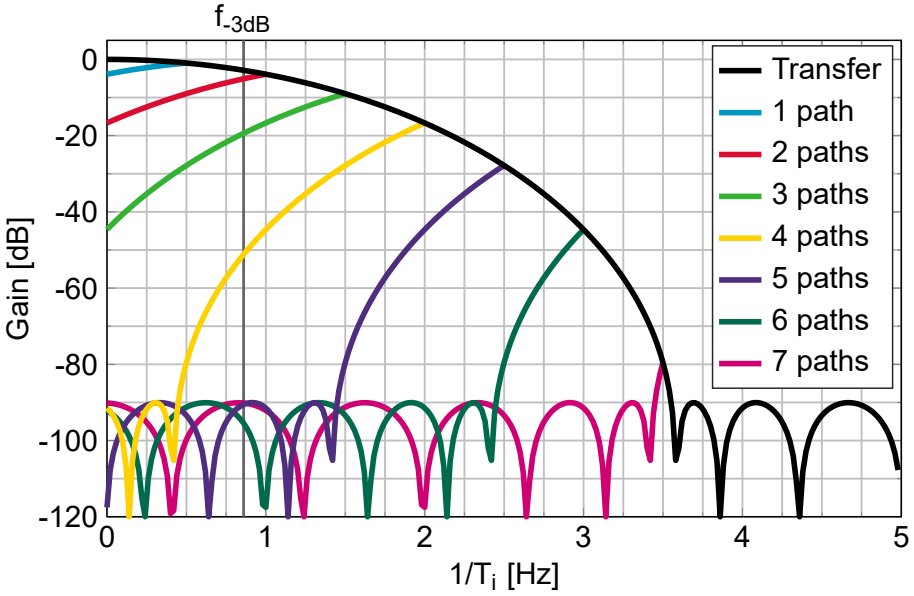


Figure 2.5: Analog FIR filter aliasing of the second Nyquist zone into the first Nyquist zone for different number of time-interleaved paths.

and hence the aliasing at the output. Fig. 2.5 shows the filter transfer as function of the integration time, including the alias of the second Nyquist zone folded into the first Nyquist zone for different number of time-interleaved paths. The first Nyquist zone ends at $f_s/2$. An analog FIR filter with only a single path has $f_s/2 = 0.5/T_i$, almost half of the filter f_{-3dB} frequency. Therefore, close-in frequency components are hardly attenuated. The result is significant aliasing of unwanted close-in components, including noise. The strength of the close-in aliases falling into the first Nyquist zone reduces for increasing number paths. Starting from 5 time-interleaved paths, the in-band aliasing ($< f_{-3dB}$) is constrained to the stopband depth –90dB and does not reduce further. Beyond 7 paths the whole first Nyquist zone has only aliases of –90dB attenuation. The required number of paths depends on the application, but the maximum number of "useful" paths is somewhere between 4 to 7, also depending the filter coefficient design. It is clearly not desirable to have $f_w = f_s$ — in other words, 80 paths in this example — for minimal hardware and power consumption.

2.3 Analog FIR Filters Prior Art

There are many analog FIR and related circuits published. Analog FIR techniques are sometimes also referred to as *transversal* filtering (before the year 2000) or *Filtering-*

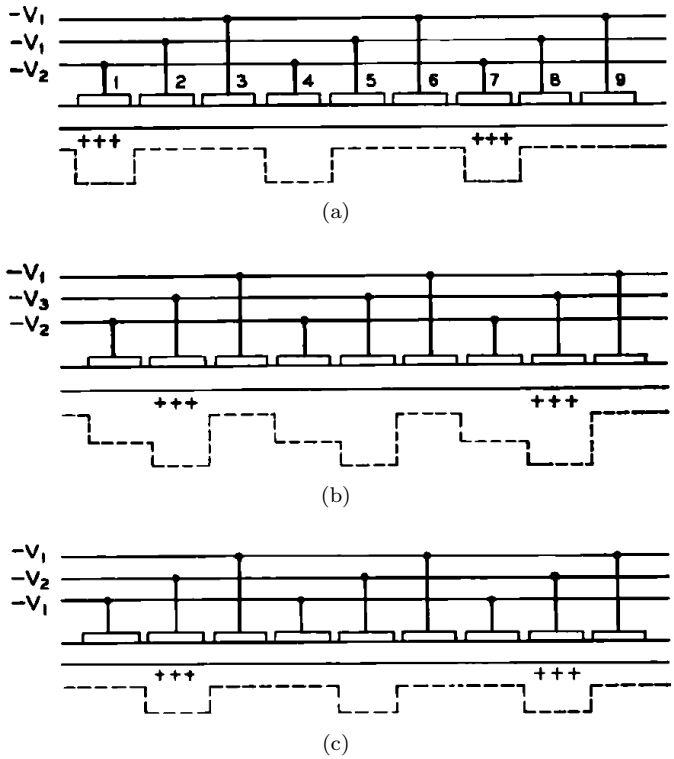


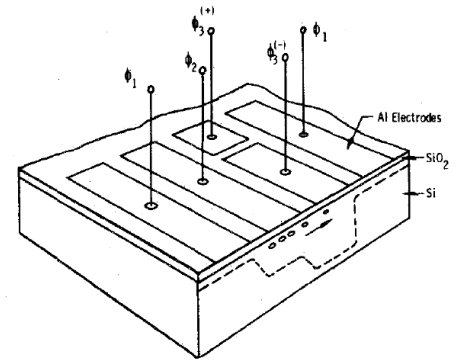
Figure 2.6: CCD delay line operation [6]. (a) Initial storage state. (b) Charge transfer to the next well. (c) Storage after shifting the charge one well.

by-Aliasing (recently by the University of California, Los Angeles).

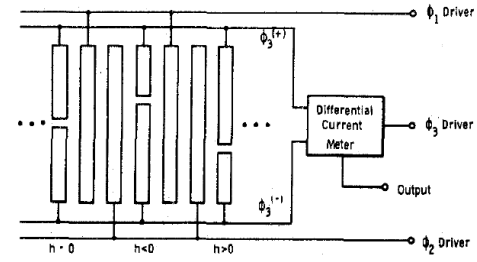
First, the analog FIR prior art is described from a historical perspective. Second, the different implementation techniques are discussed. Third, the analog FIR prior art is reviewed in terms of their application. Finally, the prior art is discussed in the context of an IoT receiver.

2.3.1 History

Research on integrated analog FIR filters started since the development of charge transfer devices in the late 1960s, early 1970s [7, 8]. Various techniques of charge transfer devices were developed, including bucket-brigade devices (BBDs) [9–11], charge coupled devices (CCDs) [6], surface charge transistors (SCTs) [12], peristaltic charge coupled devices (PCCDs) [13], bulk channel charge coupled devices (BCCDs) [14, 15] and charge injection devices (CIDs) [16, 17]. The filter implementations follow the structure of Fig. 2.1a: A delay-line in which a discrete-time input signal (charge) is



(a)



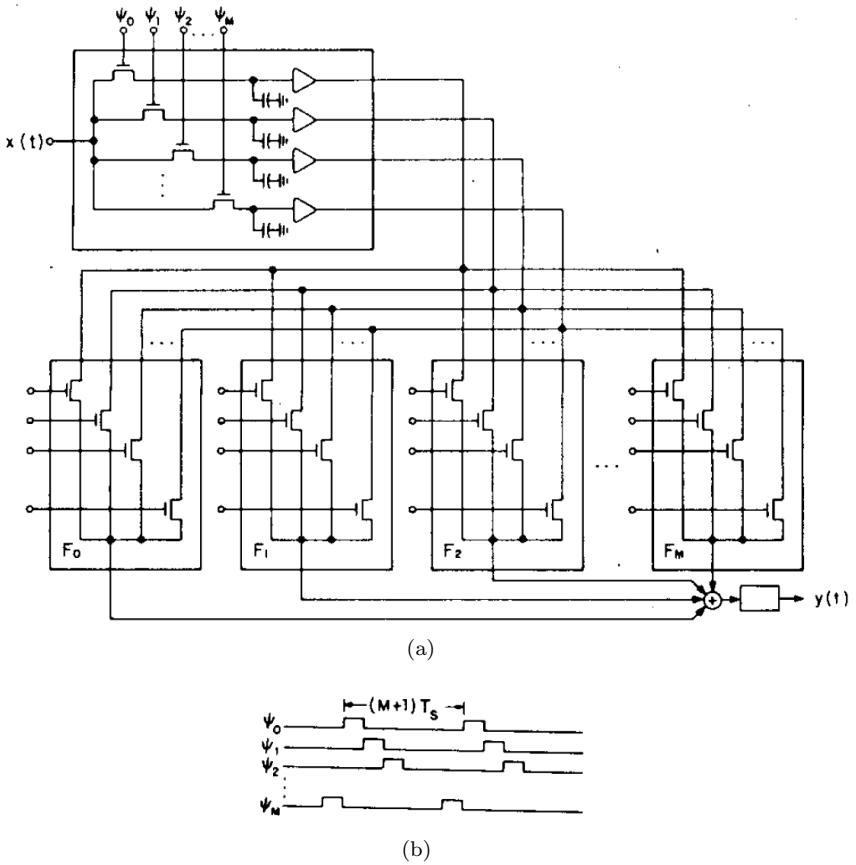
(b)

Figure 2.7: CCD based analog FIR filter [20]. (a) 3d impression. (b) Schematic.

transferred from one memory element (capacitor) to another [7, 8, 18–38].

The operating principle of these charge transfer analog FIR filters is explained on the basis of the CCD, because this one was the most popular. The CCD delay line operating principle is shown in Fig. 2.6 [6]. Below every electrode a potential well is placed where charge can be trapped. Every electrode above a well is connected through a metal line. The timing contains two phases: storage and transfer. Fig. 2.6a is in the storage phase. The storage wells are 1, 4, 7, and so on where charge is stored in wells 1 and 7, well 4 is empty. Fig. 2.6b shows the transfer phase. The voltages to the electrodes are applied such that $-V_3 < -V_2 < -V_1$ and the charge transfers to the subsequent well. In Fig. 2.6c, the delay line is back in the storage phase. Except, the charge has moved one potential well. The third electrode, here 3, 6, 9 and so on blocks the charge from transferring backwards — ensuring unilateral operation.

This delay line structure allows to implement an analog FIR filter. Fig. 2.7 shows an implementation employing the CCD delay line [20]. The differential current when transferring the charge to the electrodes connected to ϕ_3 is measured and summed to provide the filter weights and summation. The weights (h in Fig. 2.7b) are determined by the position where the electrode is split. The delayed inputs are weighted



(a)

(b)

Figure 2.8: Analog FIR filter with rotating inputs and coefficients [39]. (a) Implementation. (b) Timing waveforms.

and summed to create an output sample. The input and output run at the same rate. The first proposals used only signed weights (–1 or +1) for minimal complexity [18]. Shortly after more complicated weights were introduced to provide steeper filtering [7, 19, 20, 26, 27], but all these implementations still have fixed weights and thereby a fixed filter shape. The analog FIR circuits are inherently programmable by changing the sampling clock frequency proportionally. More flexibility is obtained by programmable coefficients to allow for a flexible transfer function shape [8, 21, 23, 24, 28–38].

CMOS technology became popular in the 1980s and thereby switch-capacitor implementations of analog FIR filters. Several approaches still used the direct implementation architecture (Fig. 2.1a) [40–51] — where the delay line is implemented using switch-capacitor amplifiers [52] — similar to the charge transfer device analog FIR

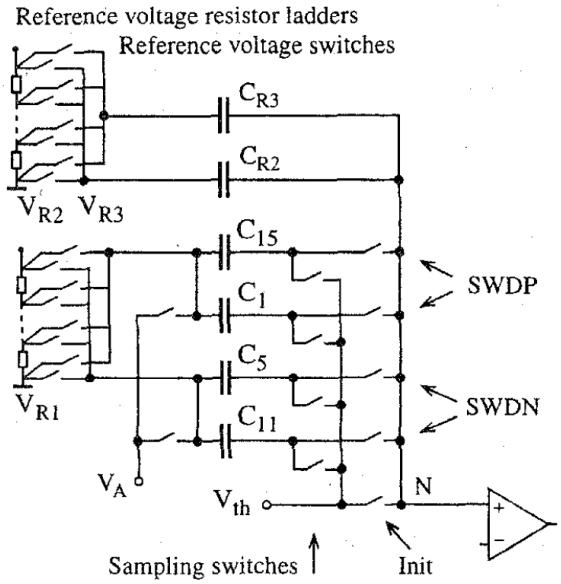


Figure 2.9: Analog FIR filter with sub-sampled output as pre-filter of a SAR ADC [68].

architectures. An alternative circuit implementation removes the need to transfer the stored inputs [39, 44, 53–67] as shown in Fig. 2.8. Instead of transferring previous inputs from one storage element to another, the input is rotated among different storage capacitors. Also the coefficients rotate among the capacitors to create the desired filter response. The stored charge is not passed on. It is undisturbed, which removes the imperfect transfer issues of the direct implementation approach.

The next important step in analog FIR filter development is time-varying coefficients and sub-sampling at the output [3–5, 68–110] as — to the author's knowledge — first proposed by *Eklund et al.* in 1996 [68]. The filter is implemented as prefilter and IF downconverter of a successive-approximation register (SAR) ADC. Downconversion is accomplished by multiplying the filter coefficients with a triangle wave sequence of $1, 0, -1, 0$. Subsequent samples of the input are sampled on C_1, C_{11}, C_{15} and C_5. The capacitor ratios create the filtering coefficients. Only four capacitors are required for the eight coefficient filter, because half of the coefficients are multiplied by a zero coefficient of the triangle wave. The ADC conversion is done separately for the positive and negative coefficients. The digital values are afterwards subtracted, which is equivalent to correlated double sampling to cancel comparator offset and $1/f$-noise. However, it results in a constraint on the filter coefficients. The positive and negative coefficients have to add up equal to remove the DC input. The architec-

ture with inherent sub-sampled output makes use one of the most common purposes of a filter: Allow sampling at a low(er) sample rate without significant aliasing.

The introduction of charge domain sampling [84, 111–113] in 1995 by *Carley et al.* [111] allows for a continuous-time input to the analog FIR filter. The charge domain analog FIR filter does not sample the input signal before providing the coefficients, but uses a continuous-time input signal as in Fig. 2.1c [3, 5, 65, 66, 69–73, 77–79, 85–88, 90, 92, 93, 96–98]. This has an advantage of filtering the filter aliases by the inherent windowed integration sinc filter, instead of having unattenuated aliases when employing voltage sampling. However, it can result in sinc "distortion" [3, 93, 98] if the filter bandwidth is large compared to the coefficient update rate.

2.3.2 Implementation Techniques

A typical analog FIR circuit has a continuous-time voltage domain input and discrete-time voltage domain output. To obtain an analog FIR filter four functions are required:

1. Coefficient multiplication;
2. Voltage-to-current (V→I) conversion, or alternatively voltage-to-charge (V→Q) conversion;
3. Integration or summation;
4. Sampling.

In CMOS processes, integration is typically implemented by a current or charge onto a capacitor. The V→I or V→Q conversion is directly related, since the input is typically voltage-domain and a current or charge is required for integration.

The coefficient multiplication can be implemented in various ways, resulting in different configurations of the analog FIR filters as shown in Fig. 2.10. Most analog FIR publications use charge based signal processing with coefficients based on capacitor ratios, which places the filter after either voltage-mode (Fig. 2.10a) [38, 40–42, 44, 45, 47, 49–51, 53–56, 67, 68, 74, 76, 82, 89, 94, 95, 107–109, 114–118] or current-mode sampling (Fig. 2.10b) [3, 79, 81, 85, 86, 86, 88, 90–93, 96–98, 119] of the input signal. The weights can also be applied prior to sampling as illustrated in Fig. 2.10c. The V→I conversion can e.g. be implemented as a time-varying transconductor [4, 57, 61, 62, 110]. An alternative is to use resistors (conductors) to implement the coefficients in the V→I conversion process [69, 100–106, 110, 120]. Prior to the V→I conversion, the weights can be applied in the voltage domain by voltage amplification or attenuation [70, 72, 73] as shown in Fig. 2.10d. Fig. 2.10e shows the implementation where the weights are implemented in the current domain after the V→I conversion [5, 43, 58–60, 63–66, 71, 77, 78].

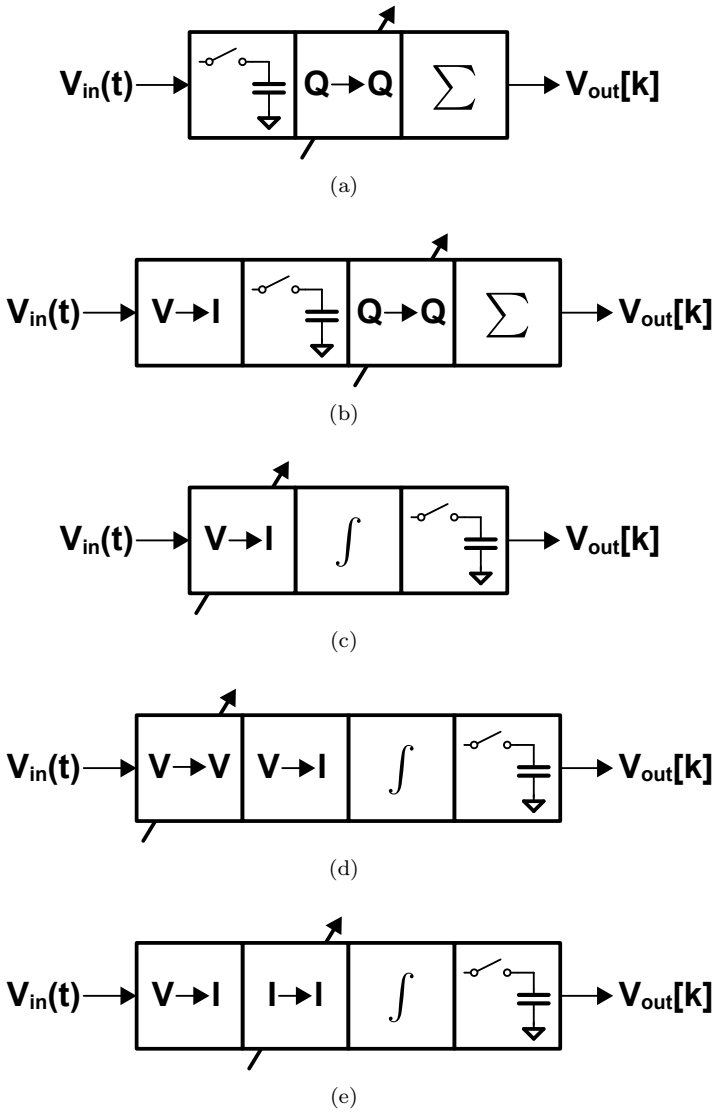


Figure 2.10: Different analog FIR filter configurations.

2.3.3 Applications

An analog FIR circuit is basically a signal processor that can implement any arbitrary finite impulse-response. Fig. 2.11 provides an analog FIR circuit overview categorized by the applications.

Analog FIR filters are most often applied as LPF [3–5, 22, 27, 31, 34–37, 39, 42, 43, 51, 53, 54, 58, 63, 64, 67, 70–77, 79–83, 85–97, 100, 114–116, 119, 121, 122] as

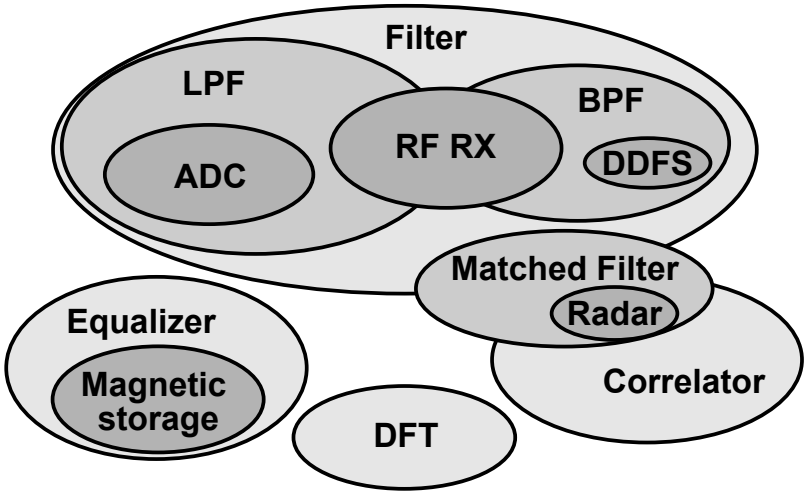


Figure 2.11: Analog FIR circuit applications.

they can provide (programmable) filters with steep roll-off and linear phase. The bandwidth is tunable by the FIR coefficient update rate. Bandpass filters (BPFs) can be implemented by multiplying the LPF FIR coefficients by the center frequency sine wave [5, 22, 34, 35, 41, 49, 50, 53, 55, 58, 65, 68, 69, 77, 78, 80, 100–106, 110].

Analog FIR filters are very suitable to implement anti-aliasing filtering of a subsequent (SAR) ADC to reduce the required sample rate and dynamic range of the ADC and thereby its power consumption [4, 5, 51, 67, 68, 75–77, 79–82, 91, 94, 95, 108, 109, 115, 116, 119, 121, 123]. Analog FIR anti-alias filters can also be used to remove digital-to-analog converter (DAC) replicas e.g. for in direct-digital frequency systhesis (DDFS) systems [49, 50].

In RF receivers (RXs) analog FIR filters were first introduced as (higher order) sinc filters, which provide not much filtering [74, 79, 80, 116, 119, 121]. The selectivity demand is increasing with the increasing number of wireless devices. Instead of higher order sinc filters, FIR coefficient design can be used to increase the selectivity of the analog FIR filters in RF receivers [51, 67, 75, 76, 81, 83, 91, 94, 95, 101, 102, 102–106, 110, 115, 122, 124].

In addition to filters, the analog FIR circuits are used as general purpose sampled analog signal processing. The first analog FIR circuits were applied as binary matched filters to pseudo-random noise signals [7, 18, 19, 29]. The analog FIR matched filters also have a potential application in radar receivers [125]. An alternative is to employ the analog FIR circuits implemented as analog-analog or analog-digital cross-correlators [21, 23, 24, 28, 30, 33, 38]. It is an alternative to digital signal processing units and was also advocated as such in the first decade of analog FIR research.

Analog FIR techniques can also be implemented as equalizers [45–48, 57, 59–62, 117]. In the 1990s, the analog FIR equalizer was a popular research topic for the read-out circuits of magnetic storage devices [45, 46, 48, 57–62].

The analog FIR circuits can be paralleled to implement a discrete Fourier transform (DFT), because each discrete Fourier coefficient is the sum of weighted delayed inputs [21, 25, 26, 40, 107, 118].

2.3.4 Discussion

Almost all prior art analog FIR filters have a high power consumption of >1mW and most of them much more, which is higher than the desired power consumption of the entire IoT receiver. To reduce power consumption, first of all, sub-sampling is important. The inherent anti-alias filtering of the analog FIR filter allows for a low sample rate at the output — in the order of twice the filter bandwidth — when the filter roll-off is steep.

A very steep filter roll-off can be obtained by properly designing the filter coefficients and having a sufficiently long integration time, which is not used by most prior art. The Filtering-by-Aliasing publications [99–106, 110] do have steep filtering. The FIR weights are applied at the input resistor of a mixer first receiver. Therefore the required update rate of the FIR coefficients is very high — much larger than the frequency of the RF wanted signal. The result is very high power consumption (>60mW) at 500MHz RF input frequency — much lower than the 2.4GHz ISM band [101, 102, 105, 106, 110].

The only <1mW work is by *Harpe* in 2018. The analog FIR anti-aliasing filter in the SAR ADC consumes only 15.2µW [108, 109]. However, the filter has limited stopband attenuation of 42dB and has no suppression of the sinc aliases.

2.4 Analogous Filters

Analog finite impulse-responses are not only used in on-chip circuits, but are also employed in other application areas. Two examples are shortly discussed in this section: (spatial) filtering in phased-array antennas and surface acoustic wave (SAW) filters.

2.4.1 Phase-Array Antennas

A phased-array antenna with 6 radiating elements is shown in Fig. 2.12. At the far-field wavefront, the waves coming from different elements experience a different delay.

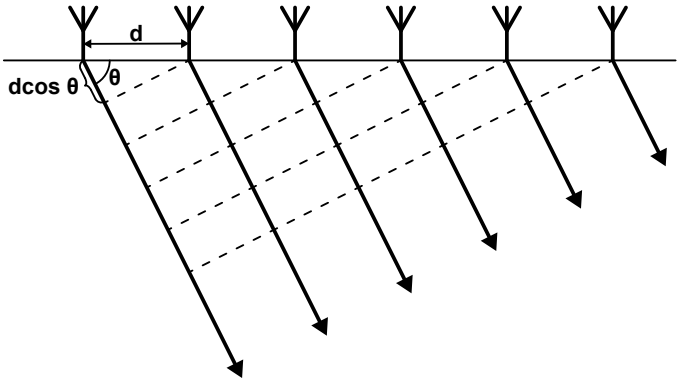


Figure 2.12: Linear phased-array antenna consisting of 6 radiating elements.

The delay between the waves of two neighboring antennas is [126]

$$\Delta t = \frac{d \cos \theta}{c} \tag{2.5}$$

where c is the speed-of-light in air. FIR frequency filtering can be achieved by applying a different weight to each antenna element, e.g. at the amplifier before the antenna.

The result is an FIR filter frequency response in the far-field for a given angle θ. The other way around, a single frequency will experience different delay per element in different directions. Therefore, the signal strength is different in different directions depending on the element weights (amplitude and phase). This results in spatial filtering, which is the main application of phased array antennas. It is very similar to the FIR frequency filtering, except that the spatial characteristics show up in the factor $\cos \theta$.

2.4.2 Surface Acoustic Wave Filters

A basic SAW filter schematic is shown in Fig. 2.13a [127, 128]. An input signal is connected to an interdigital transducer (IDT) that acts as the input — converting the electrical signal to an acoustic signal by means of piezoelectric material. The signal is transferred as a surface acoustic wave to the output IDT where the signal is converted back to the electrical domain. Absorbers are often used to suppress spurious SAW transmissions, because the IDTs are bidirectional [127, 128].

The operating principle of the filtering is as follows. The electrical signal arrives approximately instantaneous at all the fingers of the input IDT. The effective surface acoustic wave is the sum of the individual waves traveling from the fingers that all have a different distance to the wavefront. The acoustic wave velocity is much smaller than the electro-magnectic velocity. Therefore, the individual waves experience a different

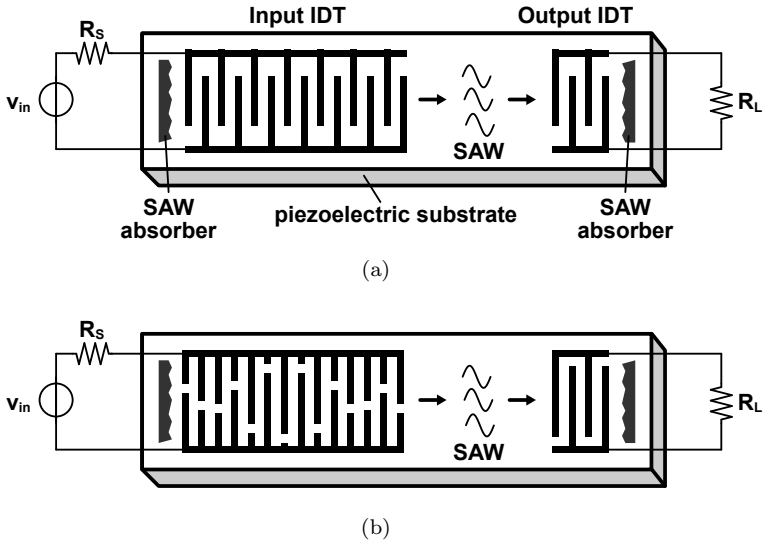


Figure 2.13: SAW filter. (a) Basic schematic. (b) Filter with one apodized IDT.

delay — similar to an end-fire ($\theta = 0°$) array antenna. In Fig. 2.13a all fingers are the same length, which results in sinc filtering — FIR filtering with all equal weights — around the center frequency

$$f_0 = v/\lambda_0 \tag{2.6}$$

where v is the SAW velocity and λ_0 the IDT finger spacing. By changing the finger size of one IDT, the strength of the corresponding individual waves is changed and therefore the transfer function's coefficients as shown Fig. 2.13. This apodizing of an IDT was first proposed by *Hartemann and Dieulesaint* in 1969 [129]. A sinc IDT finger profile will result in a "brick-wall" filter in the frequency domain as for an FIR filter with sinc coefficients.

2.5 Summary

Analog FIR filters employ the advantages of (digital) FIR filters in the analog domain. They have inherently stable steep filtering with linear phase response, for symmetric coefficients, and are programmable. However, analog FIR filters are not common practice in (IoT) receivers, because of their high power consumption or designs with only limited filtering. SAW filters, that exhibit a finite impulse-response, are employed in almost all smartphone and cellphone RF front-end modules units used today for the purpose of steep filtering a particular frequency band. Analog FIR filters could

provide highly selective receiver front-ends for IoT applications as long as their power consumption is low.

Analog FIR circuits have many potential applications: e.g. as (channel) filter in RF receivers, anti-aliasing filters of ADCs, matched filters for radar, correlator or to perform discrete Fourier transforms. Circuit implementation improvements designed for the targeted IoT receiver application in this dissertation can be reused in other analog FIR applications.

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Success is the ability to go from one failure to another without loss of enthusiasm.

Winston Churchill

3

Analog-FIR Highly-Selective Low-Power Channel Filter

The contents of the chapter are published in IEEE Journal of Solid-State Circuits [1] except for Section 3.5.1 which was published in IEEE Solid-State Circuit Letters [2]. In addition, Section 3.4.6 is included. The patent application related to this work is allowed [3].

3.1 Introduction

Low power highly selective channel filters become increasingly important. The trend to connect everyone and everything creates a need for highly selective wireless receivers, since the radio environment becomes increasingly crowded. Additionally, when targeting IoT applications minimal power consumption is desired to increase battery life.

A typical zero-IF receiver is shown in Fig. 3.1. It consists of a LNA, mixer, local oscillator, LPF and ADC. In this chapter, we target a highly-selective integrated LPF with minimal power consumption, which is implemented employing an analog FIR (AFIR) architecture.

The author is aware that the content of this chapter partially overlaps with Chapters 1 and 2. However, the author preferred minimal modification of the already reviewed and accepted papers.

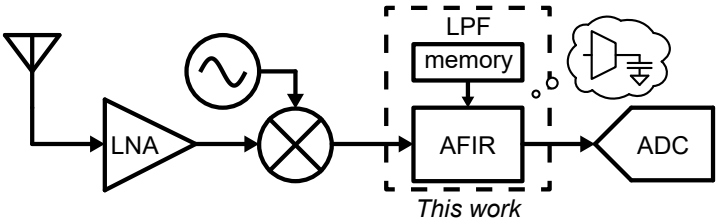


Figure 3.1: This work in a receiver.

Conventionally, these LPFs have g_m-C [4, 5] or opamp R-C [6] implementations. Both require multiple transconductors to create higher order filters. These transconductors introduce noise which limits the signal-to-noise ratio (SNR) for a given power consumption and filter characteristic. Alternatives are the time-discrete analog infinite-impulse response (IIR) filters of [7–9], but they do not achieve a sharp filter transition.

Analog FIR filters [10–14], some of which referred to as Filtering-by-Aliasing [15–17], have a very sharp filter transition and good out-of-band (OOB) rejection. The most straightforward analog FIR filter implementation stores samples of the input signal, provides a weighting coefficient for every time step and delivers an output sample at the input sampling rate [11, 13]. This requires a lot of storage capacitors for a high filter order. The analog FIR filter can be implemented more efficiently by realizing that the output sample rate does not need to equal the input sample rate [10, 14–18]. As the filter removes the unwanted signal components (outside the filter bandwidth), the filtered signal can be downsampled without corrupting it by aliasing.

Previous analog FIR implementations use a high FIR update rate [15–17], cascaded FIR stages [12] or a power hungry transconductor [18] and have therefore high power consumption. [14] shows a low power implementation, but has limited OOB rejection and an unattenuated filter alias.

This chapter is an extension on [2] where we proposed a low power analog FIR filter implementation as a channel selection filter. It contains a single inverter based g_m-C integrator for maximal SNR per power [19]. The transconductor is implemented as a digital-to-analog converter: g_mDAC. In the nominal operation mode, the filter bandwidth is 0.43MHz, which roughly resembles the I/Q baseband bandwidth of a 1Mbps IoT-standard, e.g. BLE. The filter programmability allows for a tunable bandwidth from 0.06 to 3.4MHz. The power consumption is only 92µW, because of a low FIR update rate, power efficient transconductor and partially thermometer design. The filter's power consumption is an acceptable fraction of the total power consumption of state-of-the-art IoT receivers [20–23].

In this chapter, a detailed derivation of the analog FIR transfer function — including all aliases — is provided. The proposed circuit is analyzed in detail; showing its

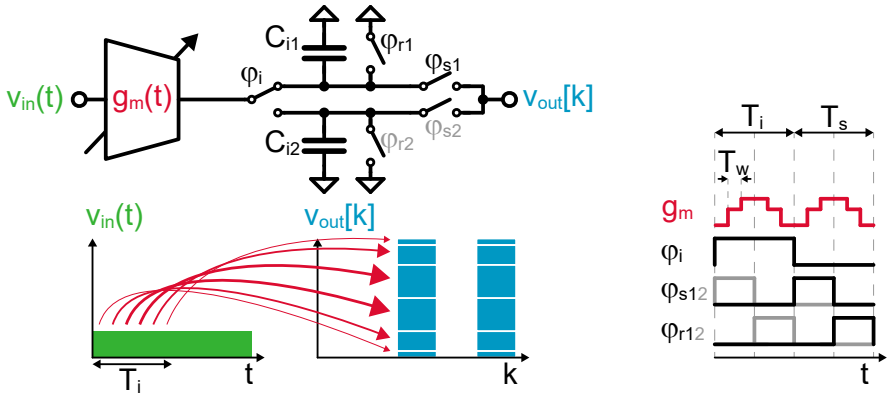


Figure 3.2: Analog FIR filter with 6 filter coefficients.

parasitic impairments, but also providing solutions to mitigate these. Furthermore, additional measurements of the transfer function and distortion give a more complete picture of the filter's performance.

The structure of the chapter is as follows. In Section 3.2, the analog FIR filtering approach is analyzed in detail. Section 3.3 discusses the low power analog FIR implementation. A comprehensive analysis of the device impairments due to mismatch and parasitics is described in Section 3.4. Section 3.5 discusses the measurement results and the conclusions are provided in Section 3.6.

3.2 Analog FIR Filtering

In this section, the analog FIR filter theory is discussed. First, the architecture is introduced, followed by a detailed analysis of its transfer function and a simple mathematical model, a frequency domain example and a summary of how to tune the filter bandwidth.

3.2.1 Architecture

Fig. 3.2 shows a 6-tap analog FIR filter architecture. In Section 2.1 [2], a step-by-step explanation is provided starting from a conventional digital FIR filter to the analog FIR filter of Fig. 3.2. Here, the working principle is just briefly summarized. For simplicity, the input signal is assumed constant. The input signal $v_{in}(t)$ is converted to current by a transconductance $g_m(t)$, which varies in time and provides the FIR weights at rate $f_w = 1/T_w$. Different time instances of $v_{in}(t)$ are weighted differently as in a textbook FIR filter [24]. Starting on an empty capacitor C_{i1}, the weighted current is summed on C_{i1} during integration phase ϕ_i for integration time T_i. The output is sampled during ϕ_s creating an FIR filtered output voltage $v_{out}[k]$ sample.

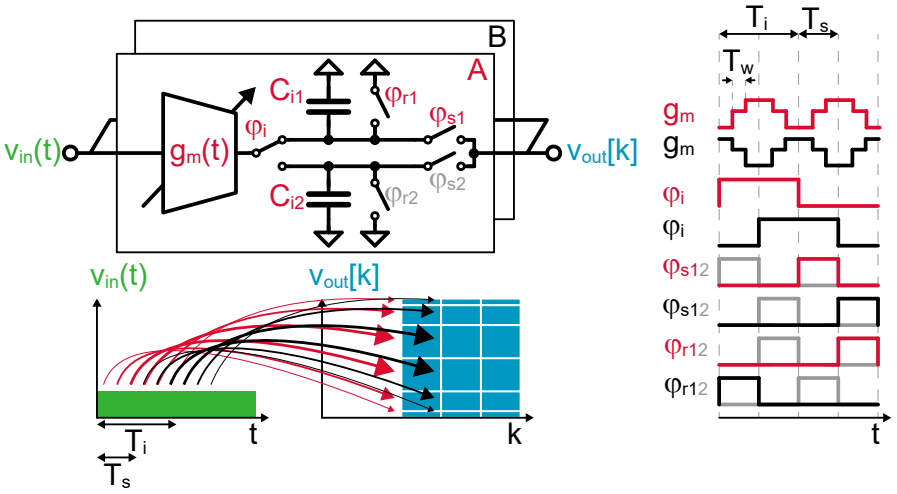


Figure 3.3: Two-path time-interleaved analog FIR filter with 6 filter coefficients ($m = 2$).

Afterwards, the voltage on C_{i1} is reset during ϕ_r. Two integration capacitors are used to allow for simultaneous integration of the input and read-out at the output. Fig. 3.2 illustrates the concept using a 6-tap analog FIR architecture, where the 6 coefficients are processed in one integration cycle.

3.2.2 Time-Interleaving

In Fig. 3.2, the output sample rate $f_s = 1/T_s = 1/T_i$ and is thus limited to the integration time. This constraint is broken by time-interleaving multiple paths: the output sample rate can be increased for the same filter shape and bandwidth. For m paths, this results in an output sample rate

$$f_s = \frac{m}{T_i}, \quad m = 1, 2, 3, ... \tag{3.1}$$

Fig. 3.3 shows a two-path ($m = 2$) 6-tap time-interleaved analog FIR filter. The output sample rate is doubled for the same filter transfer function (and FIR coefficients).

3.2.3 Filter Transfer Function

The filter transfer function is determined using the time-domain representation of Fig. 3.3. As illustrated by the different blocks in $v_{out}[k]$, an output voltage sample consists of N charge contributions. N is the number of filter taps and related to the integration time and weights update time according to $N = T_i/T_w$. The individual

charge contributions $q[n]$ become available at

$$t = nT_w, \quad n = ..., -1, 0, 1, ... \tag{3.2}$$

The output charge is

$$q[n] = \overline{g_m} w[n] \int_{(n-1)T_w}^{nT_w} v_{in}(t) \mathrm{d}t \tag{3.3}$$

where $w[n] = g_m(nT_w)/\overline{g_m}$ is the time-dependent FIR coefficient and $\overline{g_m}$ the average transconductance. The output voltage samples are available at

$$t = kT_s = k\frac{NT_w}{m}, \quad k = ..., -1, 0, 1, ... \tag{3.4}$$

The output voltage samples consist of the sum of N charge contributions during a single integration period

$$v_{out}[k] = \frac{1}{C_i} \sum_{a=0}^{N-1} q[kN - a] \tag{3.5}$$

The input is thus integrated over time T_w, sampled at nT_w, weighted by an FIR coefficient, summed and sampled at kT_s. The reset is implicitly present in (3.5); output number k contains only charge contributions of one integration cycle.

Since, f_w and f_s have an integer relationship and $f_w \geq f_s$, the two sampling actions can be seen as a single sampling action at the lower rate f_s — the first "sampling" by the weighting coefficients does not place the signal in a different position in the f_s Nyquist zones. The output spectrum $S_{out}(f)$ is derived from the input spectrum $S_{in}(f)$ by taking the Fourier Transform of (3.3) and (3.5)

$$S_{out}(f) = \sum_{k=-\infty}^{\infty} H(f - kf_s) S_{in}(f - kf_s) \tag{3.6}$$

where the harmonic transfer function $H(f)$ is

$$H(f) = \underbrace{\frac{\overline{g_m} T_i}{C_i}}_{\text{gain}} \underbrace{\operatorname{sinc}\left(\frac{f}{f_w}\right) e^{-j\pi \frac{f}{f_w}}}_{\text{windowed } \int} \underbrace{\sum_{a=0}^{N-1} w_a z^{-a}\Big|_{z=e^{j2\pi \frac{f}{f_w}}}}_{\text{FIR}} \tag{3.7}$$

where

$$w_a = w[N - a], \quad a = 0, 1, ..., N - 1 \tag{3.8}$$

are the FIR weighting coefficients, normalized to $\sum w_a = \sum^N w[n] = 1$. (3.7) was derived in [18] as the ideal FIR transfer function with windowed integration prefiltering. Note, that the time varying code $w[n]$ resembles the time-inverse FIR impulse-response w_a [15, 16].

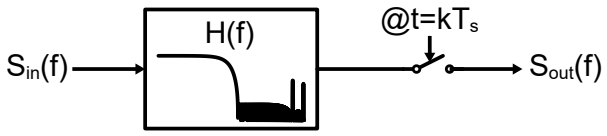


Figure 3.4: Analog FIR filter model.

Three components can be distinguished in (3.7): gain, sinc windowed integration and the FIR filter. The FIR filter provides very selective filtering with a sharp filter transition and can be designed to have linear phase. The windowed integration acts as a prefilter, attenuating the FIR filter aliases at integer multiples of f_w. The gain is determined by $\overline{g_m}/C_i$, which is PVT sensitive. The normalized analog FIR filter transfer function is only dependent on g_m-ratios and clock frequencies, which is PVT independent (apart from mismatch).

The analog FIR filter characteristics can be modeled as shown in Fig. 3.4. The input spectrum is filtered by $H(f)$ and sampled afterwards at $t = kT_s$.

3.2.4 Frequency Domain Example

In this section, we give an example to provide more intuition of the analog FIR filtering function. Fig. 3.5 shows the step-by-step analog FIR filtering operation as indicated by the arrows. Consider an input spectrum $S_{in}(f)$ consisting of four equal power signals: a wanted signal A and three unwanted signals B, C and D. The harmonic transfer function $H(f)$ shows the final gain of the input signals. All inputs have a non-zero bandwidth to ensure that they are not completely canceled by a spectral null. The analog FIR filters as follows:

1. The signal is sinc filtered. Mainly C is attenuated.
2. The signal is sampled at f_w resulting in aliasing of C and D. Hereafter, we only consider the signal in the first Nyquist zone: [0 $f_w/2$]. C and D are grayed out at their original positions.
3. The signal is FIR filtered; attenuating B and D considerably.
4. The signal is sampled at f_s resulting in aliasing of B and D to [0 $f_s/2$].

In $S_{out}(f)$, all signals are in the frequency band [0 $f_s/2$] and fall (almost) on top of each other. However, the previous filtering reduces the signal-to-interference ratio sufficiently not to corrupt the wanted signal A. C is filtered by the windowed integration sinc, but is filtered less than B and D. Additional prefiltering is needed, but a first-order low-pass prefilter can significantly reduce this alias if f_w is sufficiently

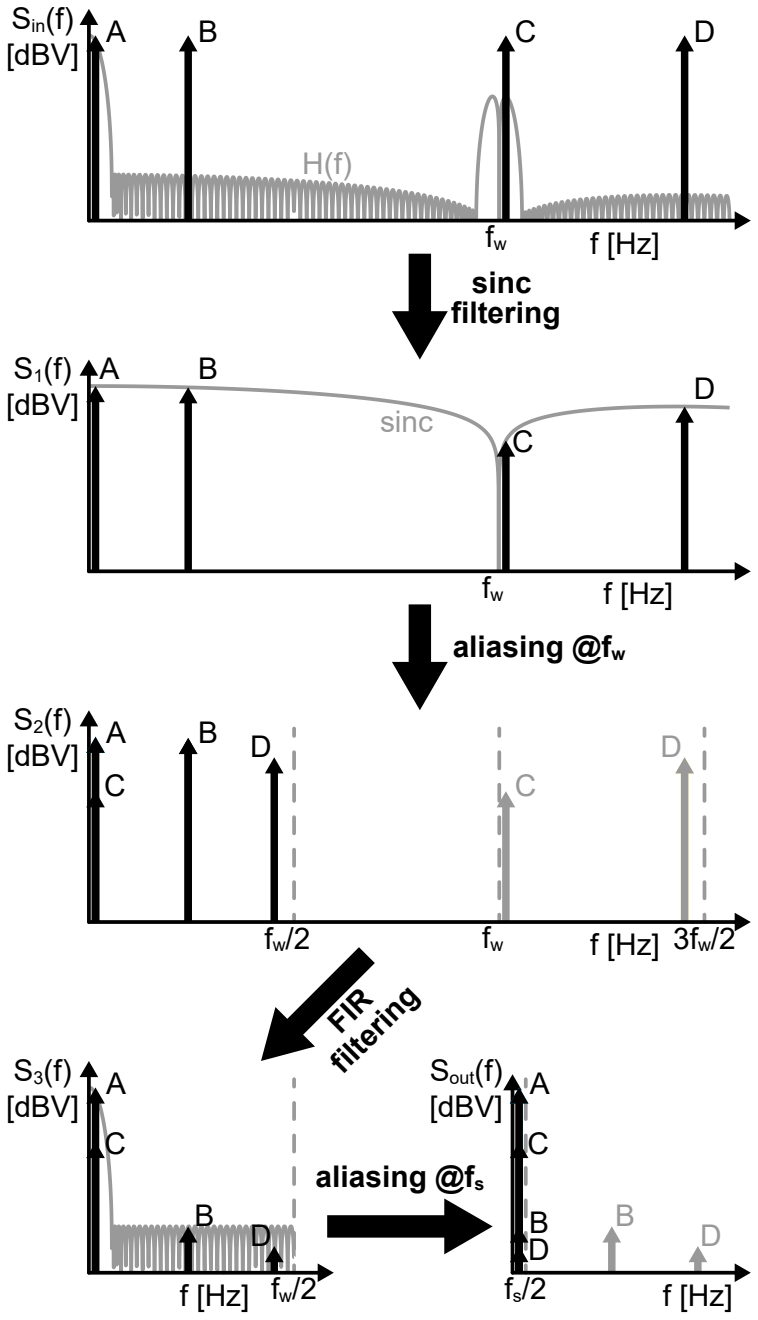


Figure 3.5: Analog FIR filter frequency response example. The filter has four equal power input signals: A, B, C and D.

higher than f_s. The same output spectrum can directly be obtained by applying the model of Fig. 3.4, where the intermediate sampling at f_w is neglected.

3.2.5 Designing the Filter Bandwidth

The filter bandwidth and roll-off is determined by the shape of its coefficients and T_i. The filter coefficients can be designed using standard digital FIR filter theory. The number of time-interleaved paths is then determined by the desired f_s. The filter aliases are at integer multiples of f_w. Increasing f_w, increases the number of coefficients for the same FIR filter.

The filter bandwidth can be tuned by changing $1/T_i$ proportionally. E.g. the bandwidth is doubled by halving T_i, the other parameters can change in two ways:

1. Double f_w, constant N. The frequency offset of the filter aliases, relative to the filter bandwidth, remains constant and thereby the sinc suppression of the aliases.

2. Constant f_w, half N. The frequency offset of the filter aliases, relative to the filter bandwidth, reduces and thereby the sinc suppression of the aliases.

Most often, it is desirable to keep the sample-rate to bandwidth ratio constant, so that the close-in aliasing at f_s is not changed.

3.3 Circuit Implementation

Fig. 3.6 shows the proposed circuit implementation. Two time-interleaved paths (A and B) are implemented to double the output sample rate (1MHz) for a 2µs integration time. The nominal filter bandwidth is 0.43MHz. The variable transconductance is implemented as a pseudo-differential 10bit transconductance digital-to-analog converter (g_mDAC). The 10bit g_m tunability is determined from the mismatch analysis including the number of bits (Section 3.4.3). The analog FIR g_mDAC code and control logic is reclocked by a differential clock at 64MHz. The maximum integration time of 2µs for a 64MHz g_mDAC update rate requires 128 filter coefficients (FIR taps) — which are provided by an on-chip memory for each time-interleaved path. The sample and reset phases partially overlap to ensure that the parasitic capacitances of the PCB and measurement probe are also reset.

The implemented integration capacitor is 20pF. In this prototype, the capacitor value can be increased 4× by differentially implemented capacitors (not shown) to (partially) compensate for gain variation when changing the bandwidth. The integration capacitors could be reused as a sampling capacitor of a SAR ADC, removing the need of an intermediate buffer. The circuit implementation is described block-by-block below.

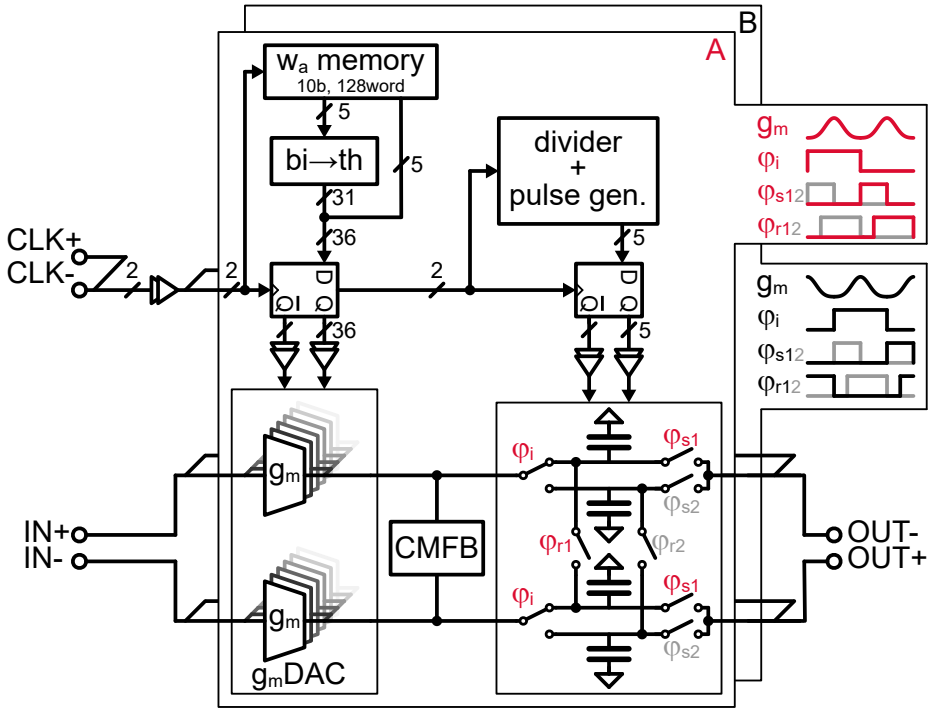
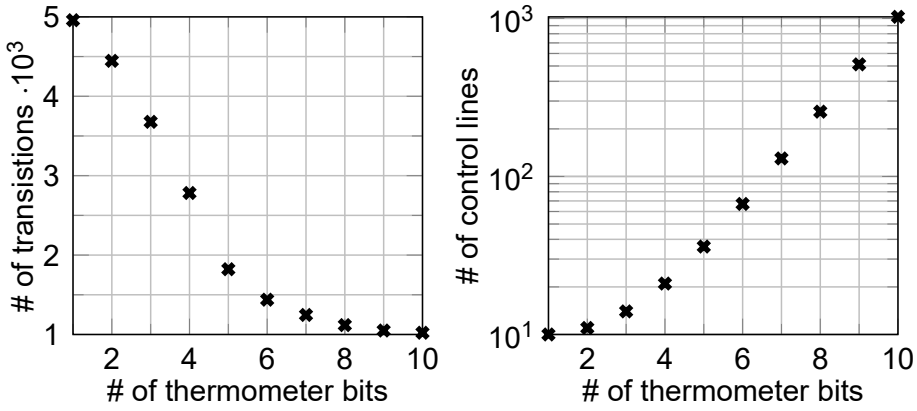


Figure 3.6: Analog FIR circuit implementation.

3.3.1 Digital Control and Memory

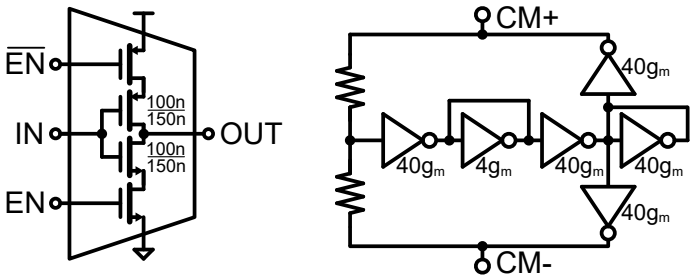
The g_m-code and integration capacitor control signals are reclocked in D-flipflops by a pseudo-differential clock at 64MHz. The digital power consumption is significantly reduced due to this relatively low update rate compared to previous analog FIR designs [11, 12, 17, 18]. However, the filter has aliases around integer multiples of this 64MHz as illustrated in Fig. 3.5. By careful design, we choose to allow these aliases, as they are severely suppressed by the sinc notches. Furthermore, a simple first-order prefilter can sufficiently attenuate these aliases for the 0.43MHz bandwidth.

When observing a single integration phase, the g_m-value monotonically increases to the g_mDAC maximum and afterwards it monotonically decreases to the minimum value — the g_mDAC is effectively only turned on/off once during a single integration phase. Therefore, the power consumption of the buffers driving the g_mDAC enable switches can be significantly reduced by implementing the g_mDAC (partially) thermometer coded. Fig. 3.7a shows the number of code transitions versus the number of MSB thermometer bits for a 10bit g_mDAC; a fully binary coded DAC contains 1 thermometer bit. A 5bit thermometer coded g_mDAC reduces the number of transitions — and thus the buffer power consumption — by 2.7× compared to a fully binary design.



(a) (b)

Figure 3.7: Partially thermometer implementation of a 10bit DAC. (a) Number of transitions per output sample. (b) Number of control lines.



(a) (b)

Figure 3.8: Circuit implementations. (a) Unit g_m-cell. (b) Common-mode feedback.

Furthermore, Fig. 3.7b shows that the complexity of a 5bit thermometer design is manageable.

Each g_mDAC is controlled by a 10bit 128word memory, making the filter code highly reconfigurable.

3.3.2 g_mDAC

The g_mDAC is split: 5bit thermometer and 5bit binary weighted as determined from the digital control power consumption and g_m-cell mismatch analysis (Section 3.4.3). It is constructed from unary g_m-cells of 1.3µS, which are implemented as shown in Fig. 3.8a. The g_m-cell is turned on/off by the enable signal EN. The g_m-cells have

a push-pull architecture to double the supply current efficiency. In addition, the g_mDAC current consumption is proportional to the FIR code — resulting in higher SNR per power consumption than for the current steering design of [18]. The inverter transconductor architecture is very suitable for modern CMOS processes with a low supply voltage.

3.3.3 Common-Mode Feedback

The common-mode feedback (CMFB) circuit is shown in Fig. 3.8b. The g_mDAC output common-mode is set to the voltage of a self-biased inverter, roughly $V_{DD}/2$. The switching of the g_mDAC results in common-mode charge injection to the output, which is suppressed by the CMFB. The dominant pole of the CMFB loop is placed at CM+ and CM-, because the parasitic output capacitance of the g_mDAC is ill-defined. Therefore C_i is implemented single-ended, although a differential implementation would save area. The CMFB circuit has three non-dominant poles. Two non-dominant poles are at $f_t/2$ and $f_t/10$, which can be very high in a state-of-the-art CMOS process[1]. The third is determined by the CM sensing resistors and the inverter parasitic input capacitance. High common-mode sensing resistors are chosen, for which the CMFB-loop is stable across PVT in extracted simulations, to minimize charge loss during integration. The power penalty is small: only 20% of the total g_mDAC power consumption. The noise of the center transconductors is common-mode and has no effect on the differential output signal. The noise contribution of the last transconductors is small; since g_m is only 40 unit g_m's, 10 times smaller than the average g_mDAC code of roughly 400.

3.3.4 Practical Considerations

In this work, the analog FIR filter is designed with a BLE IoT receiver in mind, although the analog FIR concept is not limited to this application. In this section, we show that the proposed implementation fits within a BLE receiver design.

The noise factor of the receiver in Fig. 3.1 is

$$F = 1 + \Delta F_{\text{LNA}} + \Delta F_{\text{Mixer}} + \frac{\overline{v_{in,n}}^2}{A_v^2 kTR_{ant}} < 4 \tag{3.9}$$

where ΔF is the respective noise factor contribution, $\overline{v_{in,n}}$ the input-referred noise voltage of the analog FIR filter, A_v the voltage gain from the antenna to the analog FIR filter input and R_{ant} the antenna impedance, typically 50Ω. The noise figure of the state-of-the-art BLE receivers is sub-6dB ($F < 4$) [20–23].

[1] In this chapter, f_t is defined as the unity-gain frequency of an inverter with a self-biased inverter load.

An estimate of the filter's input-referred noise voltage is

$$\begin{aligned}\overline{v_{in,n}}^2 &\approx \frac{\overline{i_n}^2|_{\mathrm{g_m DAC}} + \overline{i_n}^2|_{\mathrm{g_m CMFB}}}{\overline{g_m}^2|_{\mathrm{g_m DAC}}} \cdot 2 \cdot \frac{1}{m} \\ &\approx \frac{4kT\gamma \cdot (400+40) g_m}{(400 g_m)^2}\end{aligned} \tag{3.10}$$

where k is the Boltzmann constant, T the absolute temperature, γ the noise excess coefficient and $\overline{i_n}$ the respective average single-ended output noise current from the $\mathrm{g_m}$DAC and CMFB. When assuming $\gamma \approx 2$, the analog FIR filter noise factor contribution is about 0.34 for 30dB LNA+mixer gain and 1.3µS g_m-cells, which is reasonable for $F < 4$.

The analog FIR filter gain can be estimated from (3.7) as 34dB for 20pF integration capacitors. The 34dB gain is well below the intrinsic gain ($g_m r_o = 162$ in simulation) of the $\mathrm{g_m}$DAC. Therefore, the $\mathrm{g_m}$DAC output impedance has limited effect on the filter's transfer function.

3.4 Circuit Analysis and Solutions

The circuit implementation has several practical impairments compared to the theoretical model of Section 3.2. This section analyzes these impairments and provides practical solutions.

3.4.1 Output Impedance

A limited output impedance of the $\mathrm{g_m}$DAC results in charge loss during the integration phase. This effect is illustrated in Fig. 3.9. During integration, previously integrated charge leaks away through parasitic resistance $r_o(t)$. Hence, the effective charge q_a (FIR coefficient) is smaller than the programmed charge q_{g_m} of the $\mathrm{g_m}$DAC; more so, for earlier applied coefficients. Although, the effect on the filter transfer function is limited in this design, because the DC gain is lower than the $\mathrm{g_m}$DAC intrinsic gain, it is still desirable to compensate for it. The net charge contributions with and without a limited output impedance are shown in Fig. 3.9b. The effective FIR code is skewed. The charge contribution q_a to the total charge at the end of integration is

$$q_a = w_a \overline{g_m} r_{o,a} \overline{v_{in}} C_i \left(1 - e^{\frac{-T_w}{r_{o,a} C_i}}\right) \prod_{b=0}^{a} e^{\frac{-T_w}{r_{o,b} C_i}} \tag{3.11}$$

where w_a is the coefficient number ($a = 0, 1, .., N-1$) of the $\mathrm{g_m}$DAC and $\overline{v_{in}}$ the average input voltage during T_w. The corresponding output resistance $r_{o,a}$ is

$$r_{o,a} = R_{fixed} \parallel \frac{\mu}{w_a \overline{g_m}} \tag{3.12}$$

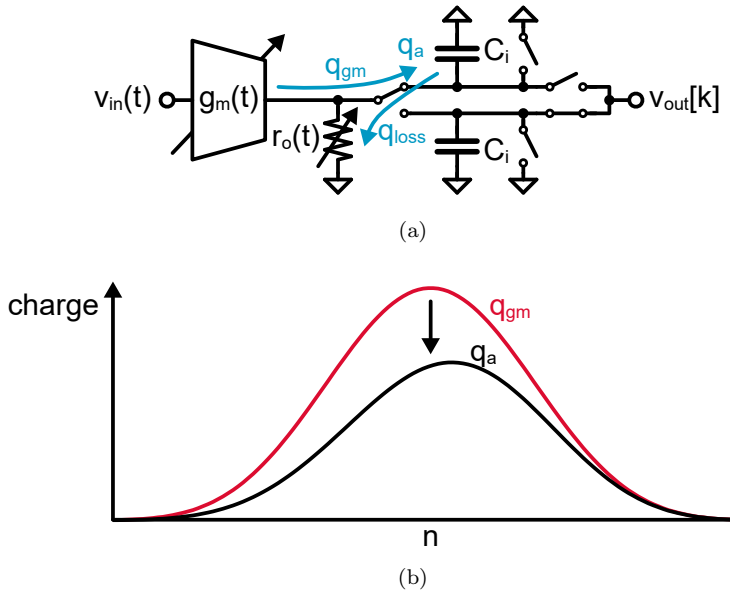


Figure 3.9: Effect of limited output impedance. (a) Schematic. (b) Ideal charge q_{g_m} and actual integrated charge q_a at the end of T_i.

where μ is the transconductor intrinsic voltage gain and $\|$ denotes the parallel configuration of the impedances. It contains a fixed component R_{fixed}, from the CMFB sensing resistors, and the g_mDAC output impedance which varies in accordance with the transconductance value. When high CMFB resistor values are chosen, the fixed term can be neglected.

Fortunately, the filter shape is determined by the relative size of the coefficients. Therefore, a precorrected code can be determined, that takes into account the charge loss and can be applied to the analog FIR memory to closely match the effective charge profile with the ideal profile.

The algorithm to calculate the precorrected code $\vec{c}$, with coefficients c_a, is shown in Fig. 3.10. First, the ideal weights are scaled by α. This scaling factor ensures that $\vec{c}$ matches the g_mDAC full-scale (normalized to 1), to minimize the quantization error. Therefore, α starts from $1/\max(w_a)$. Starting from $a = 0$ (the last code in time, first of the impulse-response), code c_a is precorrected for all future charge loss. In addition, the instantaneous charge loss during its own integration period has to be corrected. The required coefficient can be derived as

$$c_a = -\frac{\mu C_i}{g_m^\dagger T_w} \ln\left(1 - \alpha w_a \frac{g_m^\dagger T_w}{\mu C_i} \underbrace{\prod_{b=0}^{a} e^{\frac{T_w}{r_{o,b} C_i}}}_{\text{future loss}}\right) \tag{3.13}$$

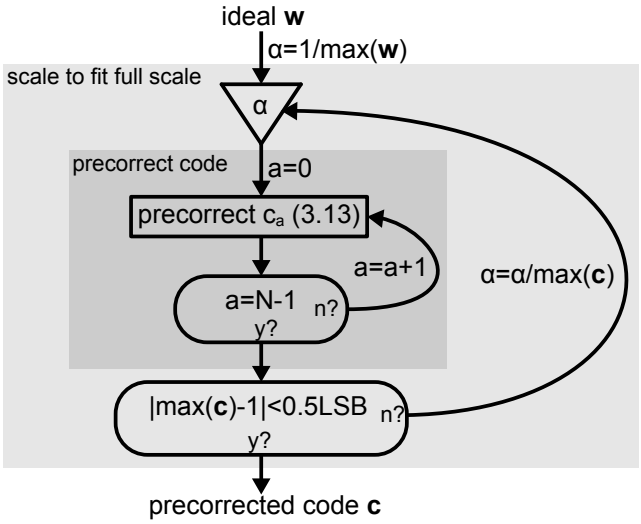


Figure 3.10: Algorithm to calculate r_o-precorrected code.

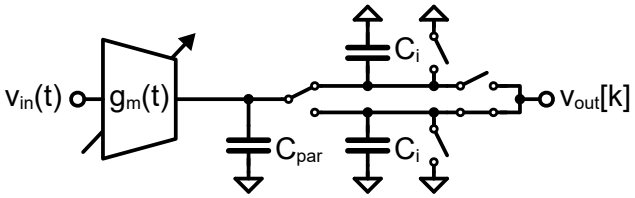


Figure 3.11: Parasitic capacitance at g_m output.

where $g_m^{\dagger}$ is the maximum transconductance. The future loss is corrected by the product of exponentials and the rest compensates for the loss during its own integration period, neglecting R_{fixed} only for its own period. c_a is calculated for all N coefficients. Afterwards, $\vec{c}$ is compared to the g_mDAC full scale and α is varied until the precorrected code exactly fits within. The correction can even be applied to a purely resistive transconductor with $\mu = 1$. A similar code precorrection approach, for a purely resistive transconductor with source resistance, is provided in [16].

3.4.2 Parasitic Capacitance

The filter transfer function can be affected by the g_mDAC parasitic output capacitance C_{par} as shown in Fig. 3.11. The charge of subsequent output samples are shared though C_{par}, because this charge is not reset. This results in an additional IIR

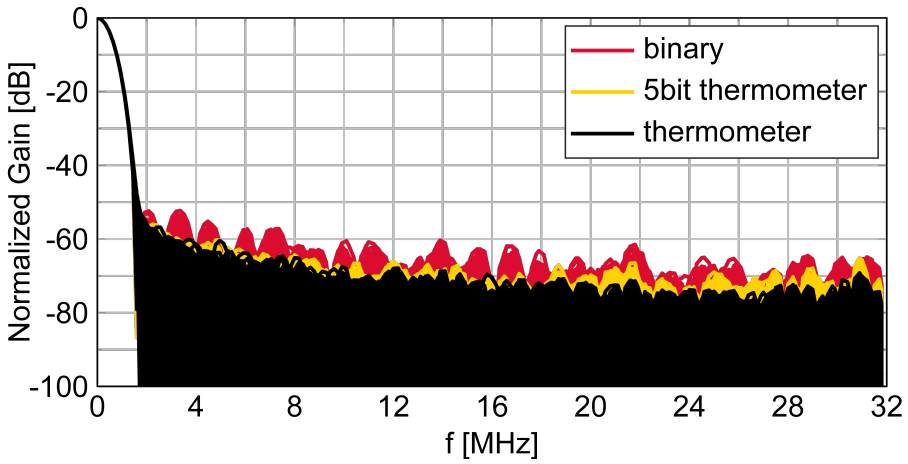


Figure 3.12: Transfer function of 500 g_mDAC mismatch realizations for different g_m-code control.

filtering according to

$$H_{C_{par}}(f) = \frac{1}{1 - \frac{C_{par}}{C_{par}+C_i} z^{-1}} \Bigg|_{z=e^{j2\pi f T_i}} \tag{3.14}$$

The extra filtering is at the output of the model in Fig. 3.4. If significant, this effect can be easily mitigated by resetting the parasitic capacitance during the first T_w integration period, at the loss of only a single filter coefficient.

3.4.3 g_m-cell Mismatch

The filter stopband attenuation is limited by the g_m-cell mismatch of the g_mDAC. Given the simulated mismatch of a single unary g_m-cell ($\sigma_{g_m}/g_m = 10.7\%$), the transfer function is determined for numerous g_mDAC mismatch realizations; neglecting sinc filtering and aliasing. The aggregation of these transfer functions provides an estimate of the worst-case filter transfer function, which is shown in Fig. 3.12 for 500 realizations and different g_mDAC control. The filter bandwidth and roll-off is unaffected by the mismatch — only the stopband floor level is impacted. The binary controlled transfer functions show spurious responses, which are reduced by >8dB in the (5bit) thermometer controlled g_mDAC realizations.

The mismatch realizations of Fig. 3.12 allow for a more detailed analysis of the implications on the filter transfer function. Fig. 3.13 shows the cumulative distribution of the g_mDACs that have a certain f_{-60dB}; for frequencies $f \geq f_{-60dB}$ the attenuation is ≥60dB. The binary coded g_mDACs have unwanted filter spurs as can

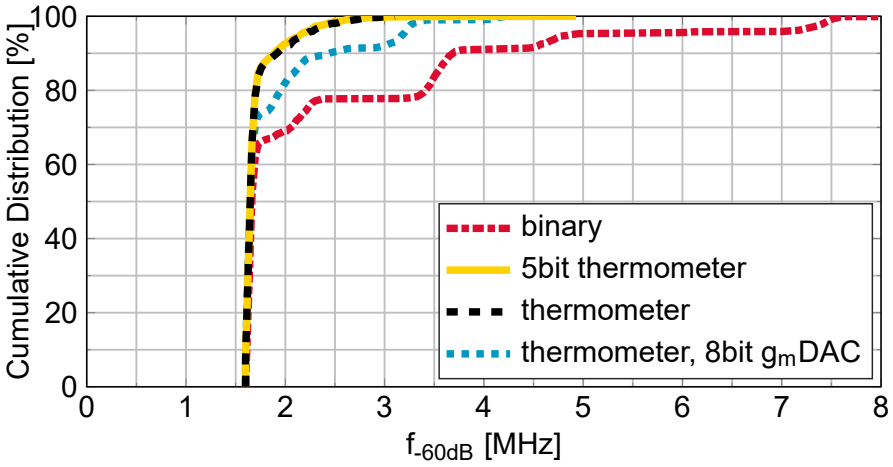


Figure 3.13: Cumulative distribution of the 10bit g_mDACs versus $f_{-60\text{dB}}$.

be recognized from the steps in Fig. 3.13. The performance is significantly improved when implemented as a thermometer-coded g_mDAC. 5bit thermometer coding has similar performance as a fully thermometer coded g_mDAC, but adds significantly less complexity. The stopband attenuation can further be improved by mismatch calibration as done in [15, 16].

Fig. 3.13 also shows the cumulative distribution for an 8bit fully thermometer coded g_mDAC with the same MSB g_m size. The performance is clearly reduced compared to a 10bit design. 9bit and 10bit designs have similar filter suppression, including mismatch. A 10bit design is chosen to ensure that the filter performance is not limited by the number of bits.

3.4.4 g_mDAC Transient Behavior

The dynamic switching of the g_m-cells in the g_mDAC has an effect on the analog FIR filter's performance in terms of circuit and system level. The transient switching behavior has three contributing error sources; charge injection to the input (driving stage) of the filter, settling behavior of the g_m-value and charge injection to the output. All three effects are common-mode, since the g_m for the pseudo-differential paths is identical. The injected charge does not, to first order, disturb the differential wanted signal.

The charge injection to the input, or kickback, is of little concern in the receiver application. The simulated peak-to-peak and rms common-mode voltage variations are <1mV and <0.1mV, respectively; when assuming a parallel output impedance of

about 24kΩ and 2pF of the previous stage[2].

The settling behavior of a switching g_m-cell changes its effective g_m-value. This effect can be compensated by taking into account the error in g_m-value in a transition and compensating for this in the code. Simulations showed that for the proposed design, this was not required.

The effect of charge injection to the output is alleviated by the time-continuous common-mode feedback circuit and by placing the integration capacitors to ground — providing a low-impedance for the high frequency common-mode switching signals — as verified by simulations.

Partially thermometer coding of the g_mDAC reduces all three effects by reducing the number of transitions as discussed in Section 3.3.1.

3.4.5 Time-Interleaving Gain Mismatch

The output sample rate is increased by time-interleaving two paths for the same filter shape, which allows for a flexible analog FIR design. g_mDAC mismatch in the two paths, results in a gain mismatch — effectively multiplying the input signal with a square wave with frequency $0.5f_s$. The result is spurs at

$$f_{spur} = f_{in} \pm n \cdot 0.5f_s, \quad n = 1, 2, 3, .. \tag{3.15}$$

For in-band signals this creates unwanted distortion components. In an IoT receiver, this is of minor concern. Typically, only low SNR (10-20dB) is required for demodulation, yet strong suppression of (much larger) interferers is desired — which is realized by the strong filter suppression of >60dB.

3.4.6 Timing Errors

The filter code accuracy is affected by the timing of the reclocking D-flipflops. A timing error results in different weighting coefficient time T_w and therefore an error in the FIR coefficient w_a. The simulated timing mismatch σ_{T_w} is 20ps. Due to the 5bit binary design the largest code transition controlled at a clock edge is 32LSBs. For this design T_w is 16ns, resulting in a σ_{w_a} due to timing of about 0.04LSB. Indicating that the implemented filter performance is not constrained by timing errors.

3.5 Measurement Results

The analog FIR filter was designed and fabricated in a 22nm FD-SOI process. The chip operates at a 700mV supply voltage and has an active area of 0.09mm^2. Fig. 3.14

[2] 12kΩ is the input impedance of the self-biased g_m-cells that provide the input bias.

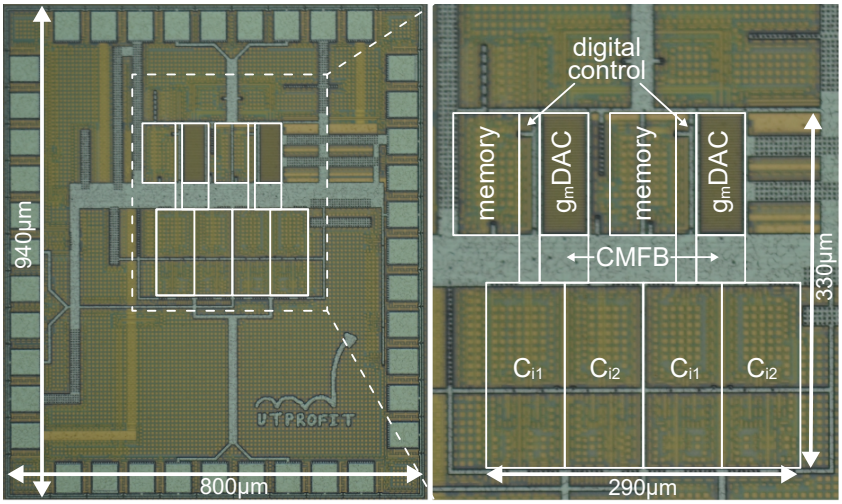


Figure 3.14: Chip photo indicating filter blocks.

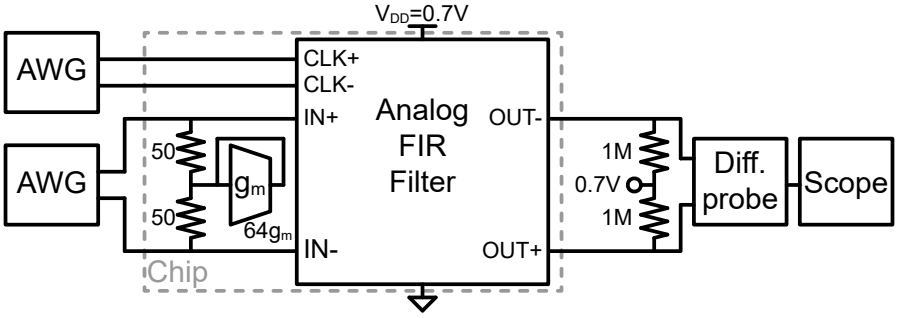


Figure 3.15: Analog FIR measurement setup.

shows the chip micrograph, indicating its major blocks. The FIR code is a Chebyshev window with r_o-precorrection, where r_o is estimated from simulation.

3.5.1 Measurement Setup

Fig. 3.15 shows the measurement setup. The input voltage and the 64MHz clock are provided by arbitrary waveform generators (AWGs) with a differential output. The input common-mode voltage is set by on-chip self-biased g_m-cells. A differential 50Ω input match is provided to allow characterization of the analog FIR up to RF frequencies. The output samples are only available half of the time, because ϕ_s and ϕ_r partially overlap. In this way, the capacitances of the measurement probe and PCB are also reset to avoid an extra undesired IIR filtering by averaging subsequent output

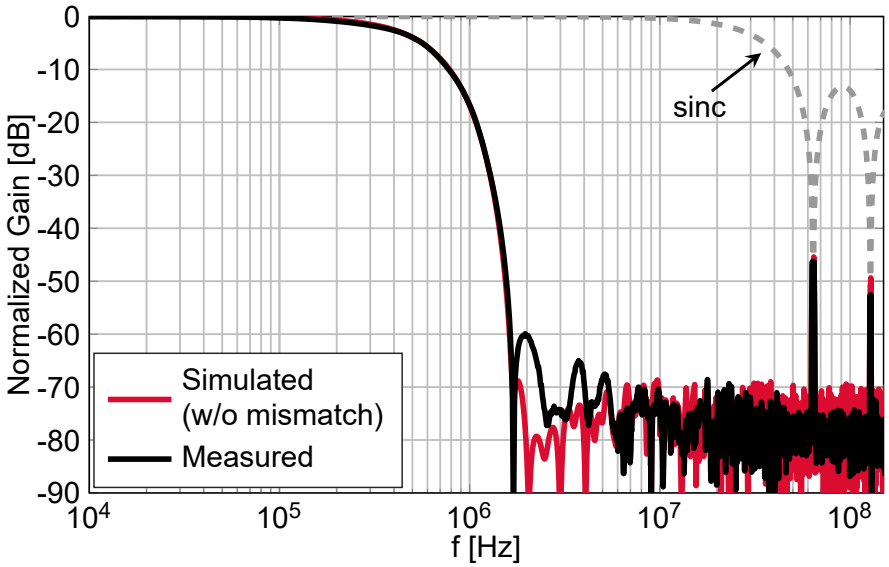


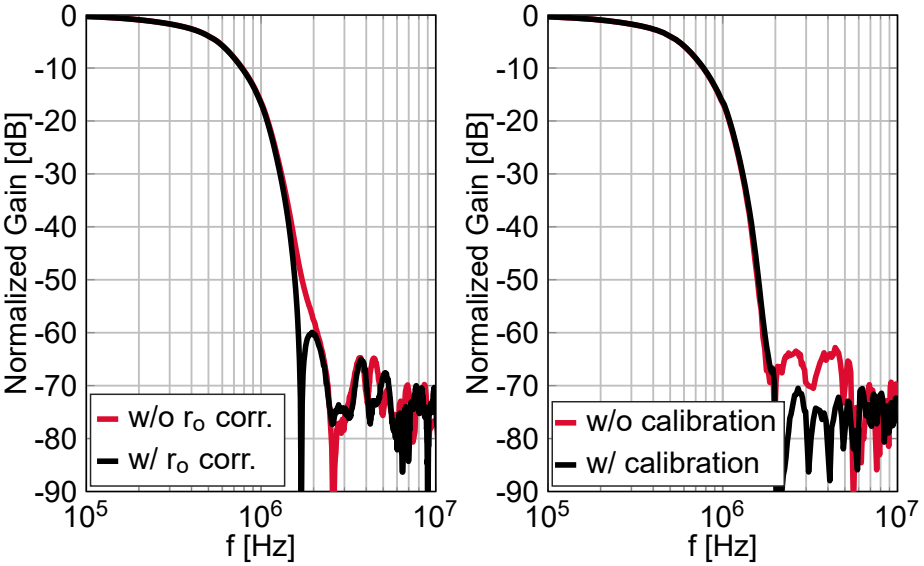
Figure 3.16: Measured normalized transfer function at a bandwidth of 0.43MHz (without calibration).

samples. The charge sharing between the integration capacitors and the measurement probe (and PCB) capacitors results in a gain reduction, which is de-embedded. The gain reduction was estimated as 3.1dB from the capacitances of extracted simulations and the Teledyne LeCroy AP033 datasheet. The output bias network compensates for the resistive common-mode loss of the probe. The bandwidth is set at 0.43MHz, unless specified otherwise.

3.5.2 Transfer Function

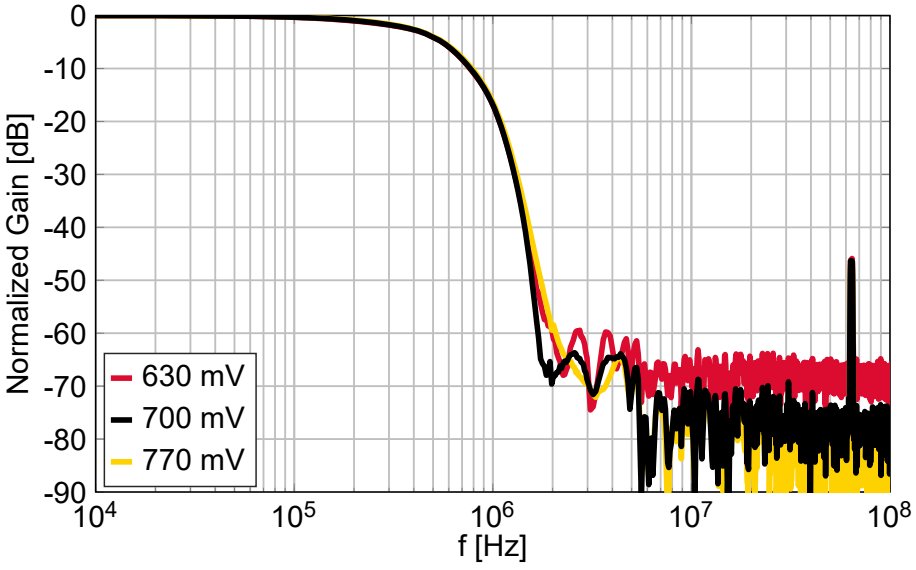
The filter has a DC gain of 31.5dB. Fig. 3.16 shows the simulated and measured normalized filter transfer function without g_m-cell mismatch calibration. The measured transfer function is very close to the simulation result including the very steep transition: the ratio between the 60 and 3dB attenuation frequencies is only 3.8. The stopband attenuation is limited to about 60dB at 2MHz which can be expected from the mismatch analysis of Section 3.4.3. The filter aliases at 64 and 128MHz are suppressed by >45dB — as expected from the windowed integration sinc filter (3.7).

The effect of r_o-precorrection is shown in the measurement of Fig. 3.17a. The transfer function error is mainly in the transition band. Here, the input varies slowly in comparison to the integration time, requiring "long-term" accuracy of the coefficients. High offset frequencies are locally canceled during integration and are thus affected



(a)

(b)



(c)

Figure 3.17: Measured filter transfer function for 0.43MHz bandwidth. (a) r_o-precorrection (b) g_m-cell mismatch calibration. (c) Different supply voltages.

less by the skewed effective impulse-response. r_o-precorrection clearly improves the filter transition.

The parasitic output capacitance of the g_mDAC was minimized in the design. The measured in-band attenuation is only 0.3dB compared to the ideal transfer function (3.7), which is not a significant error in the targeted application.

Fig. 3.17b shows the measured transfer function with and without mismatch calibration of the g_m coefficients after characterizing the g_mDAC. g_m-cell mismatch has little effect on the transfer function roll-off. The stopband depth is improved by 8dB, indicating that the stopband suppression is indeed limited by the g_mDAC mismatch.

Fig. 3.17c shows the filter transfer function for different supply voltages; 700mV ± 10%. The filter bandwidth is independent of the supply voltage as expected from (3.7). The transfer functions have only small deviations in the transition and stopband — especially, considering the gain variation of –9dB (630mV) and +7dB (770mV). All supplies use the same r_o-compensation code, which explains the reduced roll-off for the non-nominal cases. The stop-band attenuation is limited for the 630mV case by the error caused by g_m-cell transitions, while the relative mismatch improves for a larger overdrive voltage. Process and temperature variations will have similar effect on the filter transfer function. In a practical application, it could be desirable to have some coarse trimming settings to reduce gain and supply current variations.

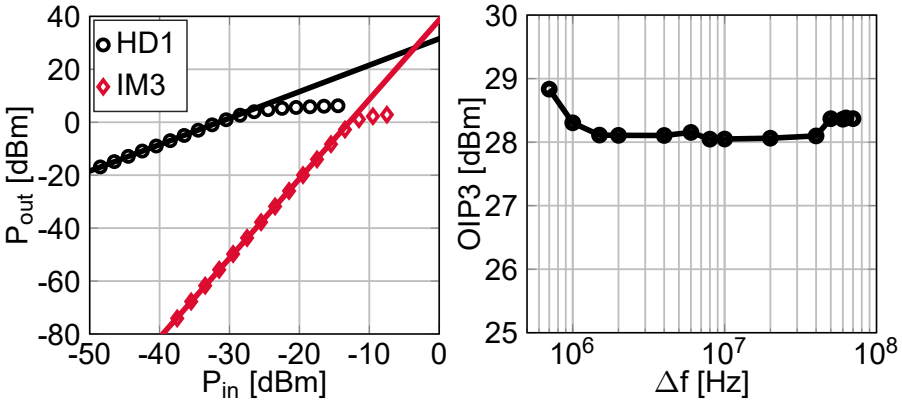
3.5.3 Noise and Distortion

In this section, the analog FIR filter is characterized for several performance metrics. The measured input-referred noise (IRN) is $12\text{nV}/\sqrt{\text{Hz}}$; averaged across 0.01-0.43MHz.

The in-band compression is characterized by the in-band gain shown in Fig. 3.18a. The output-referred 1dB compression point ($\text{OP}_{1\text{dB}}$) is 3.7dBm, which corresponds to almost 1V_{pp} — 70% of the 1.4V differential voltage range.

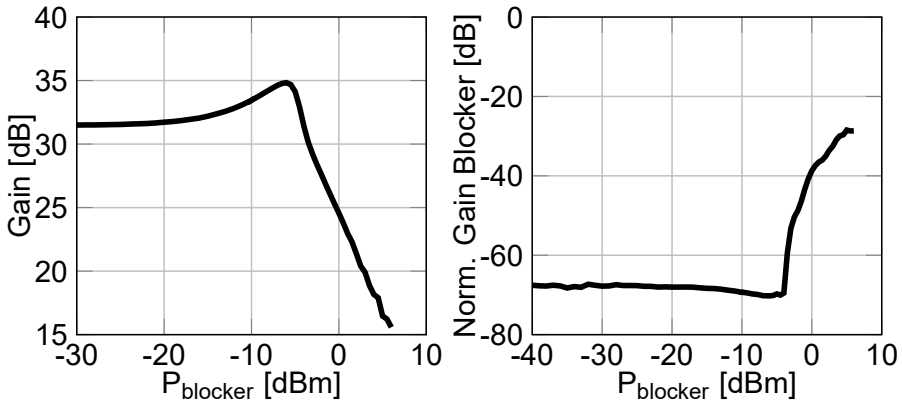
The small signal nonlinearity is characterized by the output-referred third-order intercept point (OIP3). The third-order modulation (IM3) is measured by placing two tones at Δf and $2\Delta f$. In Fig. 3.18a, the IM3 is shown for 5.01 and 9.98MHz signals. The IM3-tone is at 40kHz, which does not coincide with the aliases of the two input tones. Fig. 3.18b shows the OIP3 for various frequency offsets Δf. The measured OIP3 is 28dBm and constant for different offset frequencies, which implies that the 3^{rd}-order nonlinearity is dominated by the transconductance rather than the output resistance.

Large OOB signals can degrade the filter performance. 60dB of filtering is only useful when this dynamic range can also be handled for large blockers. Fig. 3.19a shows the measured in-band gain for a blocker at 5.14MHz, where the blocker input power is swept. The $\text{B}_{1\text{dB}}$ is –3.6dBm; the blocker input power for which the in-



(a) (b)

Figure 3.18: Measured linearity. (a) In-band gain and out-of-band OIP3. (b) OIP3.



(a) (b)

Figure 3.19: Measured filter characteristics for a blocker at 5.14MHz. (a) In-band gain. (b) Normalized gain blocker.

band gain is 1dB compressed. Fig. 3.19a shows a gain increase just before the B_{1dB}. The class-AB biasing of the g_mDAC increases the gain when a large (OOB) signal is applied.

Fig. 3.19b shows the gain of an OOB blocker at 5.14MHz versus its input power; where the gain is normalized to the DC gain. The blocker remains attenuated by almost 70dB up to an input power of -4dBm, after that the filtering sharply degrades. The input range for OOB blockers is about 400mV_{pp} differentially, concluding from

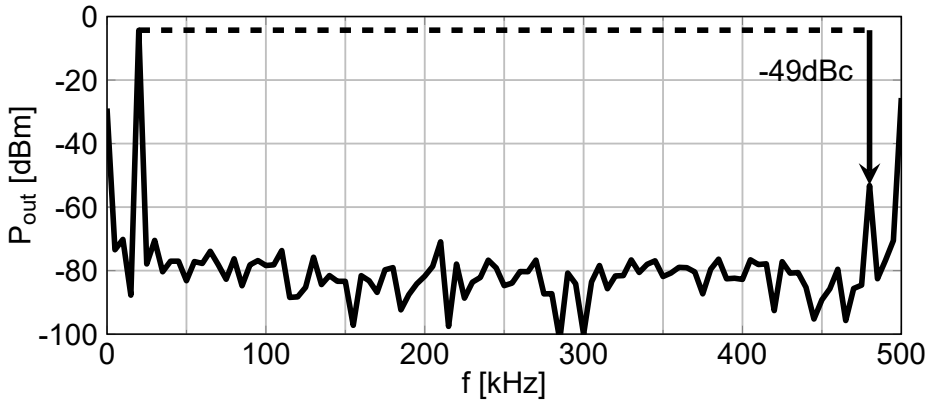


Figure 3.20: Measured output spectrum for a 20kHz input frequency.

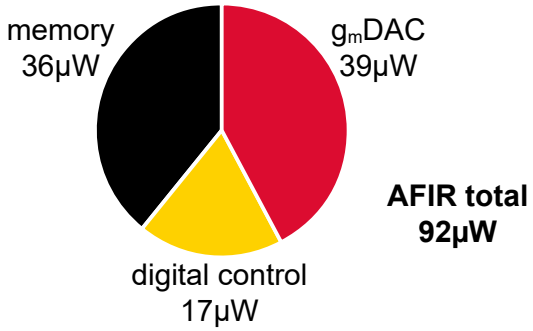


Figure 3.21: Power consumption breakdown.

the in-band gain and large signal filtering in Fig. 3.19.

Time-interleaving two paths doubles the output sample rate. However, a spur is expected due to the gain mismatch of the paths (Section 3.4.5), which is a consequence of the g_m-cell mismatch. The output spectrum for a 20kHz input signal is shown in Fig. 3.20. The time-interleaving spur at -49dBc is in accordance with the simulated g_mDAC mismatch of about 0.33%. Calibration of the g_mDAC coefficients can reduce this spur. Underestimation, of the CMFB inverter mismatch manifests itself as a DC offset and a tone at 500kHz of about 30mV_{pp} differentially, which can be removed by calibration.

3.5.4 Power Consumption

Fig. 3.21 shows the power consumption breakdown. The total power consumption is 92µW. The power consumption of the digital and analog (g_mDACs, including CMFB)

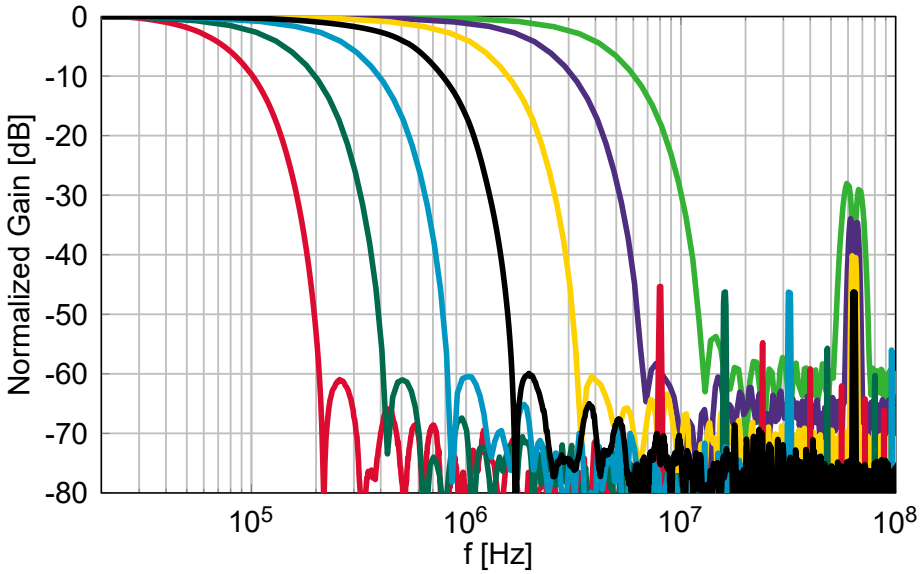


Figure 3.22: Measured filter transfer function for different bandwidth settings.

blocks is about equal. The memory is not specially designed for this application, allowing of further power reduction.

3.5.5 Flexibility

The filter is highly reconfigurable. In this section, the flexibility is demonstrated without (significantly) increasing the power consumption. Fig. 3.22 shows the filter transfer function for bandwidths from 0.06 to 3.4MHz.

The bandwidth is reduced by decreasing the g_mDAC update rate and g_mDAC output sample rate proportionally. This is accomplished by reducing the input clock frequency (Section 3.2.5, option 1). The filter aliases are at lower frequencies, because the g_mDAC update frequency is reduced.

The bandwidth is increased by reducing the number of coefficients, while maintaining the same clock frequency (Section 3.2.5, option 2). The filter alias remains at 64MHz; the number of filter coefficients are reduced. The filter alias is attenuated less, because it has a larger bandwidth for the same sinc windowed-integration filter. The power consumption is only increased by 10% for a filter bandwidth of 3.4MHz.

3.5.6 Comparison

The proposed filter performance summary and a comparison to state-of-the-art power-efficient filters is shown in Table 3.1. This work achieves the lowest power consumption

Table 3.1: Performance Summary and Comparison.

	This work	[9] VLSI'17	[12] JSSC'13	[7] JSSC'14	[6] JSSC'09	[4] JSSC'10	[5] CICC'17	[8] TCAS-I'18
Topology	128-tap AFIR	Passive IIR	Cascaded AFIR	g_m-C IIR	Opamp RC	g_m-C	g_m-C	g_m-C IIR
Supply voltage [V]	0.7	1.2	1.2	1.2	0.55	2.5	1.3	1.8
Power cons. [mW]	0.092	0.15	8.4	1.98	3.5	1.26	0.65	4.3
f_{-3dB} [MHz]	0.06-3.4[a]	0.54	5-26	0.4-30	11.3	2.8	20	0.49-13.3
f_{-60dB}/f_{-3dB}	3.8	10[b]	1.5[c]	7.8[c]	-	5.9[b]	4.8[c]	7.5[c]
Gain [dB]	31.5	0[c]	41	9.3	0	15	0	17.6
IRN [nV/$\sqrt{\text{Hz}}$]	12	23.3	12	4.57	33	23	15.3	6.54
OP_{1dB}[e][dBm]	3.7	-	-	10	-0.5	-	6.3	12.93
OOB OIP3[f][dBm]	28	55.1	13[d]	21	13	50.6	28.8[d]	32.63
B_{1dB} [dBm]	-3.7	-	-	-	-	-	-	-
Technology	22 nm FDSOI	130 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	90 nm CMOS	180 nm CMOS	180 nm CMOS
Active Area [mm^2]	0.09	0.06	0.52	0.42	0.43	0.5	0.12	2.9

[a] Other specifications are measured at 0.43MHz; [b] Extrapolated from figure; [c] Estimated from figure; [d] In-band;
[e] $OP_{1dB} = P_{1dB}$ + Gain - 1; [f] OIP3 = IIP3 + Gain;

in combination with a very sharp transition band. [12] has a sharper filter transition, but at >90× more power consumption. The filter IRN is low and the linearity is competitive. The active chip area is relatively small.

When comparing the classical opamp R-C and g_m-C filters with the recent digitally controlled analog FIR and IIR filters, the FIR and IIR analog filters show very strong potential in modern CMOS processes. Digital control is attractive as it only consumes dynamic power, while its power consumption scales down with technology and low supply voltages. The proposed analog FIR approach allows for a very steep filter with a single transconductor to maximize the SNR for a given power consumption. The programmability of the proposed analog FIR implementation, not only allows for a flexible filter shape and bandwidth, but it can also be deployed to reduce the effect of circuit impairments e.g. the limited output impedance of a transconductor.

3.6 Conclusions

An analog FIR filter architecture is proposed, to serve as a channel selection filter for low power receivers. It employs a hardware efficient implementation that requires only two 10bit pseudo-differential transconductor DACs (g_mDACs) and four integration capacitors to obtain a 128-tap FIR filter.

The bandwidth is accurately tunable from 0.06 to 3.4MHz. Very sharp filtering is obtained, the stopband attenuation at small frequency offsets — 3.8× the -3dB bandwidth — is 60dB, without g_m-cell mismatch calibration. A low power consumption (92µW) is achieved by: the single transconductor (g_mDAC) design with a low update-rate and 5bit thermometer coding. The filter shows constant in-band gain and filtering for blockers with an input power of up to -4dBm.

The analog FIR filter low power consumption and high selectivity enable future IoT receivers in an increasingly crowded wireless environment. Furthermore, the programmability supports software defined IoT receivers.

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Simplicity is the ultimate
sophistication.

Leonardo da Vinci

4

Highly-Selective IoT Receiver Front-End with Power Optimization

The contents of this chapter are published in the IEEE Journal of Solid-State Circuits [1]. Fig. 4.12 is published at the IEEE International Solid-State Circuits Conference [2]. In addition, Section 4.7 is included. The analog FIR filter and receiver front-end are patented in [3].

4.1 Introduction

Low power receivers with very high selectivity are a prerequisite for the next generation IoT applications. It is expected that the number of wireless devices will increase rapidly. Battery life-time becomes increasingly important because the burden of charging or changing batteries directly increases with the number of devices. An increasing number of devices compete in the already crowded low-GHz spectrum, thereby increasing the receiver's interference rejection requirements; especially, in the popular 2.4GHz industrial, scientific and medical (ISM)-band.

The author is aware that the content of this chapter partially overlaps with Chapters 1 to 3. However, the author preferred minimal modification of the already reviewed and accepted papers.

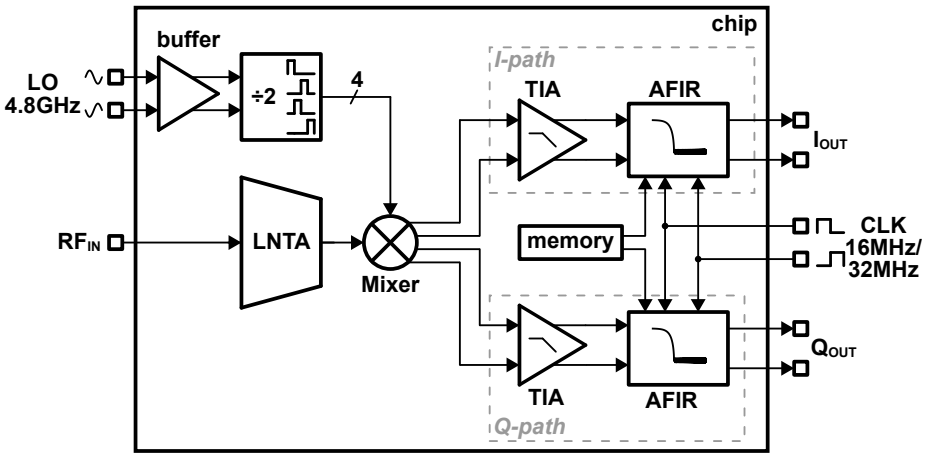


Figure 4.1: Proposed receiver front-end architecture.

Reduced power consumption and improved selectivity should be achieved without compromising on NF. A good NF for state-of-the-art IoT receivers is 5-6dB [4–9]. In IoT receivers all blocks tend to contribute to the total power consumption [4–13]. Therefore, a fully optimized (system) design is required to obtain minimal power consumption.

This chapter is an extension on [2], where we proposed an IoT receiver front-end that combines reduced power consumption with improved selectivity and without compromising on NF or linearity. Power optimization is applied across the entire receive chain: the low-noise transconductance amplifier (LNTA), frequency divider with mixer and baseband filter. The baseband filter is implemented as analog FIR filter to improve selectivity without increasing the power consumption. The receiver front-end is designed for BLE, BT5.0 and IEEE802.15.4 and contains on-chip impedance matching. In this chapter, we provide an extensive analysis of the optimizations in the LNTA, frequency divider and baseband filtering architectures. Furthermore, the measurement results are extended, including additional linearity measurements and discussion on the obtained performance.

The structure of the chapter is as follows. First, the receiver front-end overview is provided in Section 4.2. Followed by a detailed description of the optimizations in the LNTA (Section 4.3) and frequency divider (Section 4.4), including a comparison to other divider approaches. The baseband filter architecture, including an analog FIR filter is described in Section 4.5. Section 4.6 discusses the measurement results and the conclusions are provided in Section 4.8.

4.2 Circuit Implementation

Fig. 4.1 shows the proposed receiver front-end with zero-IF architecture [2]. A single-ended RF input is converted to current by an LNTA. This current is passed through a four-phase passive mixer to create differential I/Q baseband signals. The current is converted to voltage and low-pass filtered by a transimpedance amplifier (TIA). The channel selection is performed by an analog FIR (AFIR) filter, clocked at 16MHz and 32MHz for a 1Mbps and 2Mbps data-rate, respectively. The four-phase clock signals are provided by the divide-by-two frequency divider. For this prototype, the 16MHz/32MHz and 4.8GHz LO clocks are provided externally, but multiphase clock generation and clock distribution is on-chip.

4.3 Low-Noise Transconductance Amplifier

An inductive degenerated LNTA combines a low NF with low power consumption [14]. However, for very low power consumption the design trade-offs change. In the 2.4GHz IoT receiver application targeted in this work, our design goal is minimum power consumption at a reasonable NF.

4.3.1 Ideal Inductors

Fig. 4.2a shows the inductive degenerated topology. The input impedance is

$$Z_{in} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{4.1}$$

where g_m is the transistor's transconductance. Matching is accomplished at the resonance frequency

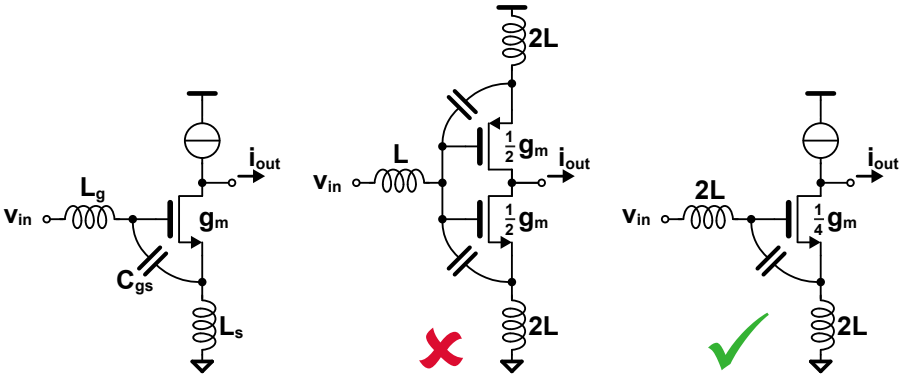
$$w_c^2 = \frac{1}{(L_s + L_g)C_{gs}} \tag{4.2}$$

for which $\mathrm{Im}(Z_{in}) = 0$ and

$$Z_{in} = \frac{g_m}{C_{gs}} L_s = Z_0 = 50\Omega \tag{4.3}$$

where Z_0 is the source (antenna) impedance, here 50Ω. The noise performance of the LNTA can be described by its noise factor: the SNR degradation from input to output. Including only the thermal noise of the transistor transconductance, the noise factor is [14, 15]

$$F = 1 + \gamma Z_0 \frac{\omega_c^2 C_{gs}^2}{g_m} \tag{4.4}$$



(a) (b) (c)

Figure 4.2: Inductive degenerated LNTA design. (a) Architecture. (b) Push-pull implementation. (c) $2L$ implementation.

where γ is the transistor's noise excess factor. The noise factor can be rewritten using (4.2) and the matching condition (4.3) as

$$F = 1 + \gamma \frac{1}{1+\alpha} \tag{4.5}$$

with $L_g = \alpha L_s$. The corresponding required transconductance is

$$g_m = \frac{1}{F-1} \cdot \frac{\gamma Z_0}{w_c^2 L_{tot}^2} \tag{4.6}$$

where $L_{tot} = L_s + L_g$. (4.5) provides a possibly somewhat non-intuitive result: F is independent on g_m. It is solely determined by the inductor ratio α for a given γ, assuming impedance matching and ideal inductors. According to (4.6), the minimal g_m is obtained for a maximum F and maximum L_{tot}. The maximum allowed F is often specified. The maximum inductor value is generally constrained by its self-resonance frequency or chip area requirements. In IoT applications, it is not desirable to have a very high inductor ratio α — often applied in ultra-low NF-designs to obtain minimal NF — but high L_{tot} should be pursued to minimize g_m and hence lower power consumption. The L_g and L_s values are in the same order of magnitude, given the maximum inductor value constraint.

Fig. 4.2 shows a thought experiment regarding the LNTA design; assuming $\alpha = 1$ provides a sufficiently low NF and for simplicity the current source is ideal. Starting from $L_g = L_s = L$ one could propose a push-pull design (Fig. 4.2b), since it provides double the g_m for the same bias current [16]. At first sight, this seems favorable only half the bias current is required. However, two $2L$-sized inductors are required to

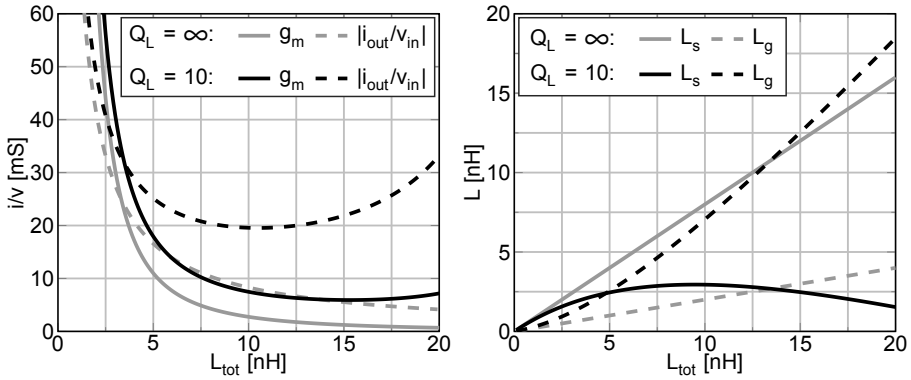


Figure 4.3: LNTA parameters of Fig. 4.2a for different Q_L with $F = 1.8$. (a) Required transconductance and transconductance gain. (b) Inductance.

provide an effective $L_s = L$. When a maximum inductance value of $2L$ is available, the circuit of Fig. 4.2c can also be implemented. This configuration requires only $\frac{1}{4}g_m$ — in other words, half the bias current of the push-pull architecture — because $g_m \propto 1/L_{tot}^2$. It also requires a smaller area than Fig. 4.2b. This is a non-intuitive result and would mean that the push-pull architectures of [2, 16–18] are unfavorable.

4.3.2 Including Q_L

Detailed analysis shows that the circuits in Fig. 4.2 are oversimplified. Integrated inductors are far from ideal and have a typical quality factor Q_L of 10 in the GHz frequency range. Including the limited Q_L, the noise factor becomes

$$F = 1 + \frac{r_g}{Z_0} + \frac{r_s}{Z_0} + \gamma\frac{1}{1+\alpha}\left(\frac{Z_0 + r_g + r_s}{Z_0}\right)^2 \tag{4.7}$$

where r_g and r_s are the resistance of L_g and L_s, respectively. Not only the two resistive noise terms are added, but also the i_{out}/v_{in} and $i_{out}/i_{n,g_m}$ transfers change and thereby the γ term, which was neglected in [14]. The γ term increases for higher r_g and r_s (lower Q_L). The Q_L limitation affects the circuit matching only little, but it has a significant effect on the noise factor and thus the required g_m. Using (4.7), the required g_m is

$$g_m = \frac{1}{F - \left(1 + \frac{\omega_c L_{tot}}{Q_L Z_0}\right)} \cdot \frac{\gamma Z_0}{\omega_c^2 L_{tot}^2}\left(1 + \frac{\omega_c L_{tot}}{Q_L Z_0}\right)^2 \tag{4.8}$$

which simplifies to (4.6) for no inductor losses ($Q_L \to \infty$).

Fig. 4.3 shows the required g_m and inductances for $Q_L = \infty$ and $Q_L = 10$ as function of L_{tot}, assuming a desired noise factor of 1.8 and $\gamma \approx 1$. The required g_m is higher for $Q_L = 10$ as expected. Some interesting observations can be made: For $L_{tot} \geq 10$nH, the required g_m is roughly constant; higher inductance hardly reduces the required g_m. Even when neglecting that high valued on-chip inductors typically have lower Q_L. The result is that chip area can be saved. Furthermore, the required L_s does not increase above 2.9nH (Fig. 4.3b). g_m is no longer proportional to $1/L_s^2$. The push-pull configuration is favorable when the maximum attainable inductor value is $\geq 2L_s$ (here $\geq$5.8nH).

Fig. 4.3a also shows the LNTA transconductance "gain" $|i_{out}/v_{in}|$. A higher $|i_{out}/v_{in}|$ will result in smaller noise contribution of subsequent stages. At minimum g_m, $|i_{out}/v_{in}|$ is also at its minimum. However, it cannot be changed much by changing L_{tot}. By decreasing L_{tot}, $|i_{out}/v_{in}|$ increases, but the required g_m increases more rapidly and thus the LNTA current consumption; when taking into account that $|i_{out}/v_{in}|$ is squared regarding the noise contribution for subsequent stages. $|i_{out}/v_{in}|$ increases slightly for high inductor values, but the Q_L and self resonance frequency will decrease significantly for very large inductors ($L >$ 8nH).

The above analysis provides insight in the design complexity of the inductive degenerated LNTA. It concludes that L_g and L_s should be in the same order of magnitude and a push-pull architecture can become favorable when including $Q_L = 10$ in the analysis. The LNTA transconductance gain cannot be increased much to reduce the noise contribution of subsequent stages, because this would result in a large increase in power consumption or impractically large inductors.

4.3.3 Brute-Force Search Model

Including the limited Q_L is insufficient to fully optimize the LNTA design. This requires the more complex circuit of Fig. 4.4 to model the LNTA's small-signal behavior. Parasitic capacitors are included: C_{pcb} the PCB parasitic, C_{ESD} the ESD diodes' capacitance including pad parasitics, and C_g the parasitic to ground at the gate. L_b is the bondwire inductance, which has an estimated Q-factor of 35. L_s is modeled with $Q_L = 10$. L_g is not connected to ground and requires the more extensive Π-model. The L_g Π-models are derived from the S-parameters at 2.44GHz, which is sufficient to optimize for our target application. A design space for L_s, C_{gs}, g_m is estimated from the results of the simplified analysis. About 20 different L_g designs were characterized using Momentum simulations. All resistors and the g_m have an associated noise source.

Based on this design space, brute-force search is applied to find the minimal required g_m for the NF and S_{11} <–15dB in the 2.4GHz ISM-band requirements — optimizing the design. A push-pull architecture is selected, because the required L_s

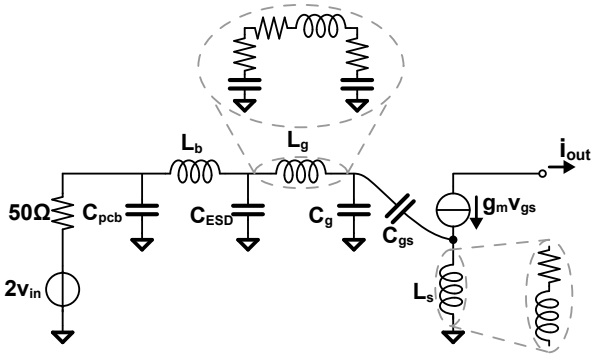


Figure 4.4: Small-signal model for brute-force optimization of the LNTA.

is sufficiently low at 3.6nH. L_g is 4.3nH, the inductors are approximately equal as expected to minimize g_m.

In addition to minimum g_m for a given NF, the linearity requirement has to be satisfied. The main non-linearity sources are the transistor transconductance and output impedance. The output impedance non-linearity contribution depends on mixer/TIA design. Typically, the TIA input impedance is limiting in-band while OOB the mixer switch on-resistance. The transconductance non-linearity can be changed by the biasing conditions. A larger overdrive voltage improves the linearity at the cost of transconductance efficiency g_m/I_{DC} and hence power consumption. An alternative measure would be to increase L_s (the transconductance feedback), but the desired L_s is already high.

4.3.4 LNTA and Mixer Topology

Fig. 4.5 shows the proposed LNTA including the passive mixer switches. In this design, both FETs are nominally biased at roughly half supply to allow for maximum voltage swing and to minimize large signal clipping given the supply headroom. The OOB IIP3 is slightly limited by drain voltage swing induced non-linearity in the LNTA due to the large mixer switch resistance values, which have been optimized to save power. The OOB IIP3 could be improved by 4dB, according to simulation, by reducing the mixer switch resistance. The simulated output impedance magnitude of the LNTA is 3.3kΩ. The linearity is state-of-the-art for a BLE receiver (IIP3>–10dBm) combined with a low mixer load to the frequency divider. Constant g_m-biasing is employed to maintain the LNTA NF, matching and IIP3 specifications across PVT variations.

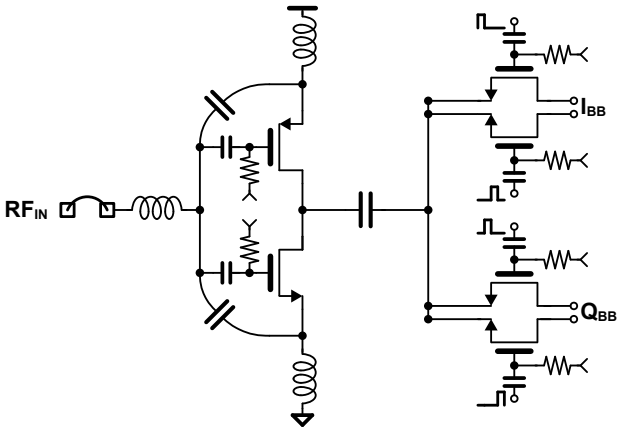


Figure 4.5: Proposed LNTA including mixer.

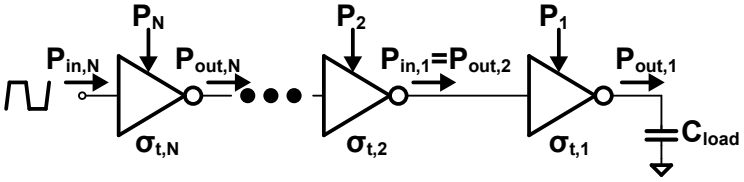


Figure 4.6: Power consumption of multiple buffers driving a capacitive load.

4.4 Frequency Divider

A significant part of the power consumption is consumed by the frequency divider and mixer clock buffers in an IoT receiver, e.g. one third in [8]. The proposed receiver front-end employs 25% duty-cycle clocks to downconvert the single-ended LNTA output RF current to differential I/Q baseband currents. In this section, a minimum logic gate design strategy to minimize power consumption is explained, followed by a novel "Windmill" frequency divider architecture to achieve very low power consumption [2]. Finally, the Windmill divider performance is evaluated by a comparison to multiple prior art designs.

4.4.1 Minimum Logic Gate Design Strategy

Fig. 4.6 shows a chain of multiple (inverter) buffers; P_n is the power provided by the supply and $P_{in,n} = P_{out,n+1}$ is the power required to drive stage n. The fundamental required power to drive the (mixer) load is

$$P_{load} = f_m C_{load} V_{DD}^2 = P_{out,1} \tag{4.9}$$

where f_m is the mixer clock frequency and V_{DD} the supply voltage. All other power is "lost" — in the output parasitics of the buffer, as crowbar current or in driving the buffer. Therefore, the power dissipation of a single buffer stage is

$$P_{diss,n} = P_n - P_{out,n} + P_{in,n} \tag{4.10}$$

and the total dissipated power of an N stage buffer is

$$P_{diss} = \sum_{n=1}^{N} P_n - P_{out,1} + P_{in,N} = \sum_{n=1}^{N} P_{diss,n} \tag{4.11}$$

The total random time deviation σ_t, either by phase noise and/or mismatch, is the sum of the variances

$$\sigma_t^2 = \sum_{n=1}^{N} \sigma_{t,n}^2 \tag{4.12}$$

assuming that the individual random timing deviations are uncorrelated. (4.11) and (4.12) show that minimum P_{diss} and σ_t^2 is obtained when the most efficient buffers — in terms of minimum P_{diss} and σ_t^2 — are used with a minimal number of stages. Therefore, a minimum number of efficient gates — e.g. CMOS logic gates — is a strong starting point to optimize the frequency divider.

4.4.2 Windmill Frequency Divider

Fig. 4.7 illustrates the design procedure of the 25% duty-cycle frequency divider starting from the minimum — *single* — gate design strategy. Typically, differential 50% duty-cycle LO signals are available at $2f_m$ or $4f_m$ to generate the mixer clocks [8–12, 19, 20]. At minimum one selective gate is required to create the 25% duty-cycle mixer phases. Here, we start with $2f_m$ clocks. This results in less power consumption in the buffers that create the square wave LO from the sinusoidal VCO signals.

The available signals of the design are the input signals $LO+$ and $LO-$, 50% duty-cycle at $2f_m$, and the output signals Q_x ($x = 1..4$), 25% duty-cycle at f_m, as shown in Fig. 4.7 (top left). The second illustration shows the single gate implementation using a NOR-gate. A NOR-gate is chosen, because it provides selectivity on high pulses as required. NOR-gates are very efficient in modern CMOS technologies where NFETs and PFETs are approximately equal strength. $LO-$ is inverted through the NOR-gate to create Q_1. Every other $LO-$ low should be passed to Q_1 which requires a memory element to count the $LO-$ lows. The memory element is implemented as shown in Fig. 4.7 (bottom left) by a NOR SR-latch. Signals Q_2 and Q_4 create an enable signal E_1, which is low for every other $LO-$ low. This structure is repeated in the last illustration for every output, to create the "Windmill" divider — indicating

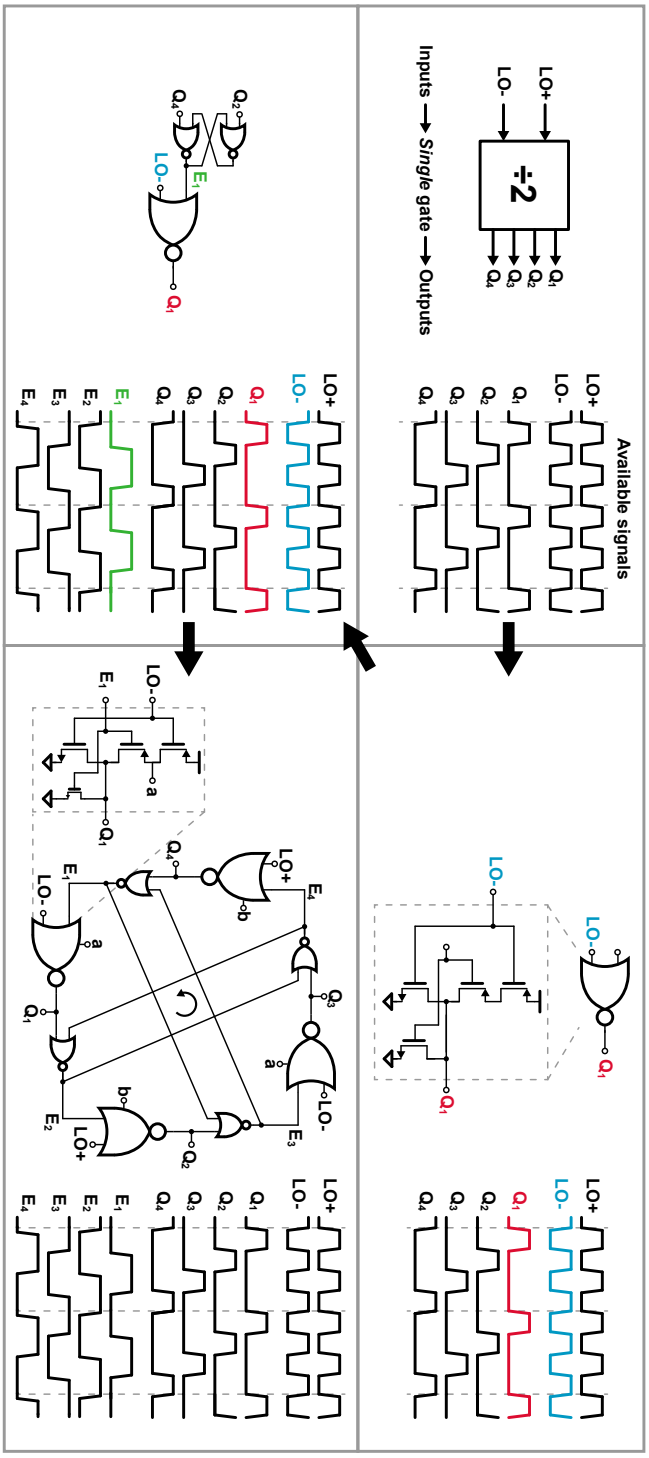


Figure 4.7: Step-by-step design of the 25% duty-cycle "Windmill" frequency divider.

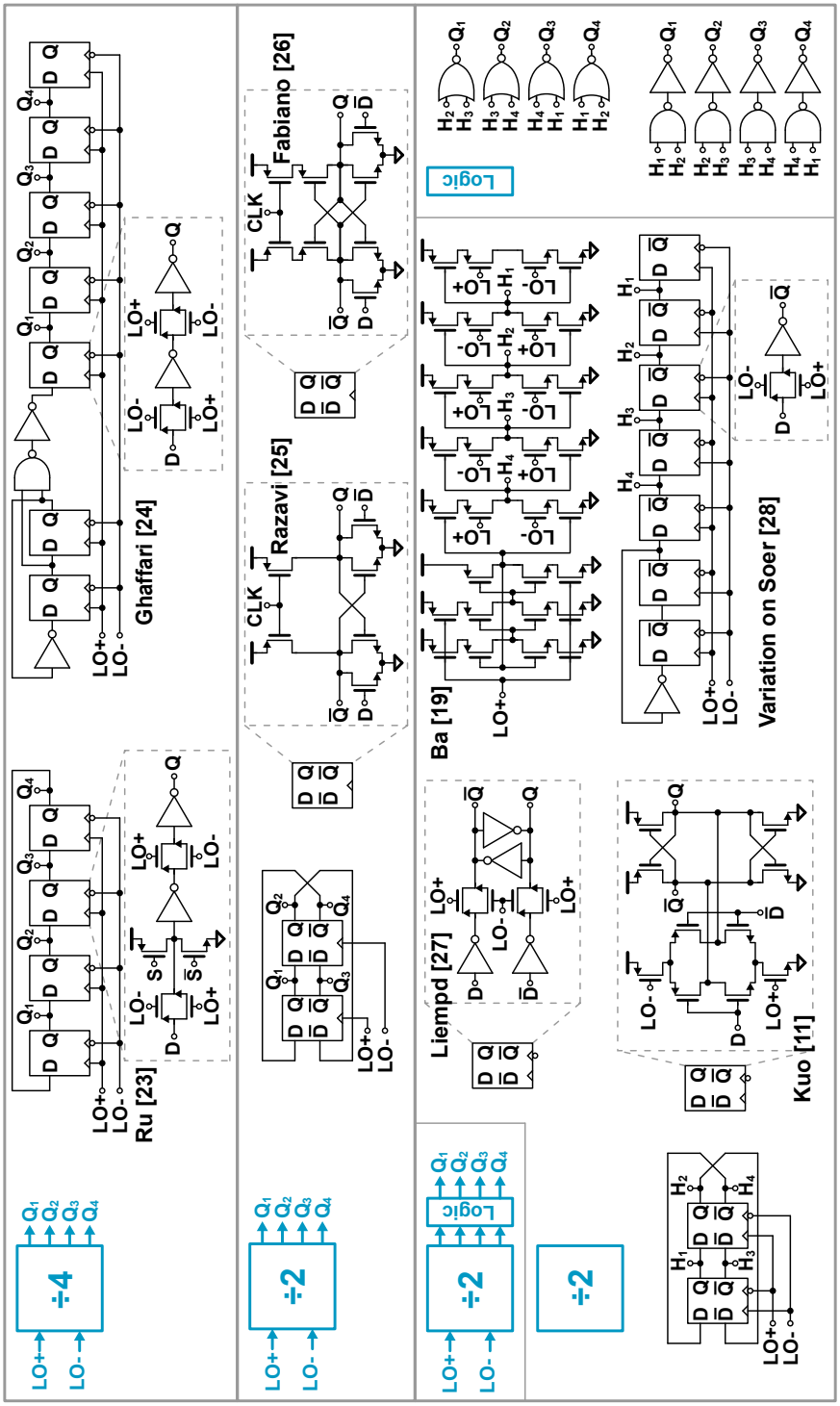


Figure 4.8: Prior art divider architectures to create 25% duty-cycle clocks.

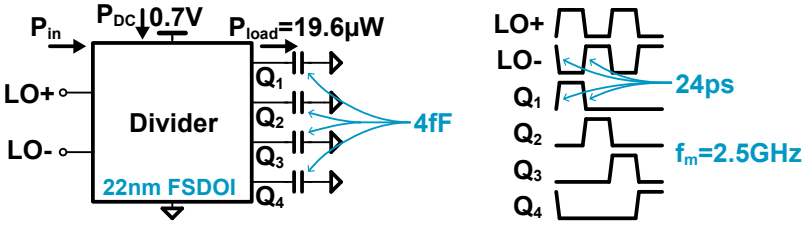


Figure 4.9: Assumptions (highlighted) for simulation based 25% duty-cycle divider comparison. The LO signals are shown for the divide-by-2 case.

the rotating nature of the gate enable signals E_x and outputs Q_x. The latches toggle the $LO-$, $LO+$ to Q_1/Q_3, Q_2/Q_4, respectively.

Only the large transistors in the large NOR gates contribute to the output edges and have to be scaled to the drive mixer load. All other transistors can be minimal size as long as the divider meets the speed requirement. Furthermore, only those large transistors contribute to the phase noise and mismatch. In this way, very low power consumption is achieved while also realizing good phase noise and mismatch as only a single gate propagation delay contributes to timing uncertainty. The top PFET of the opposite large NOR gates is shared, via nodes a and b, to reduce the uncorrelated phase noise contributions that degrade the receiver's NF [21, 22]. In addition, since the PFET is shared, a single PFET is used to create two rising edges; reducing the power consumption of the preceding buffers. The phase relation of the outputs is independent on the start-up condition as verified by the I/Q mismatch simulations.

4.4.3 Divider Comparison

In this section, we provide a comparison between published divider architectures that create 25% duty-cycle clock signals. Three approaches can be distinguished as illustrated in Fig. 4.8:

- Direct divide-by-4; divide a differential LO at $4f_m$ by four to create 25% duty-cycle clock signals; [23, 24].
- Direct divide-by-2; divide a differential LO at $2f_m$ by two to create 25% duty-cycle clock signals; the Windmill divider (Fig. 4.7) and [25, 26].
- Divide-by-2 with logic; divide a differential LO at $2f_m$ by two to create 50% duty-cycle clock signals at f_m and use subsequent logic to create 25% duty-cycle outputs; [11, 19, 27] and a variation on [28] without the extra intermediate inverters to reduce its power consumption.

The dividers, all designed in 22nm FDSOI, are compared by simulation with the assumptions as summarized in Fig. 4.9. C_{load} is 4fF for each Q_x-output — equal

to the mixer switch that is optimized by using 3× the minimal finger gate pitch to reduce its parasitic capacitance and contact resistance by increasing the number of source and drain contacts. The output frequency is 2.5GHz, which means an input frequency of 10GHz and 5GHz for the divide-by-4 and divide-by-2 cases, respectively. The required power to drive the mixer load is 19.6µW for a 700mV supply. The LO rise- (5%→95%) and fall-times (95%→5%) are 24ps. The transistors are sized such that the outputs Q_x have equal rise- and fall-times as the inputs: 24±0.3ps. All designs are optimized in terms of scaling, e.g. in [24] the first divider is minimal size as these transistors do not contribute to the phase noise or mismatch. The dividers of [19, 24, 28] contain a dummy device to avoid I/Q-offsets.

The schematic simulation results are summarized in Table 4.1, where the best performance per specification is highlighted by bold text. The dividers are compared on power dissipation (P_{diss}) as defined in (4.10), phase noise in the white and 1/f regions and I/Q-mismatch (σ_{IQ}). I/Q mismatch is of little concern in the proposed zero-IF architecture, but is included for a complete comparison of the dividers. The divider DC power consumption (P_{DC}) is also included for completeness.

The power dissipation of the Windmill divider is 42% reduced or more compared to the other architectures. The Windmill divider has the lowest phase noise by 2dB or more in the white noise region. The 1/f-noise is less dominant, because the noise corner is at a low offset frequency of about 2MHz. Only [26] has a slightly better I/Q-mismatch than the Windmill divider at a significantly higher power dissipation. For [11], the two different logic architectures are compared. The NOR-based design has lower phase noise and I/Q-mismatch at a similar power dissipation. The NOR-gate benefits from the equal NFET-PFET strength in modern CMOS processes.

Some remarks: [23] requires start-up circuitry, controlled by S and $\overline{S}$, which can introduce possible start-up issues. [25, 26] have clock overlap, because the rising edge of Q_{x+1} triggers the falling edge of Q_x. [19] has an additional static 1.2% I/Q-offset, because the rising edge of H_4 is relatively slow. During H_4's rising edge, the input of the tri-state inverter is not at ground, because of charge injection of the previous stage while the input node is floating. Furthermore, [19] has a significantly asymmetric load to the driver of the divider.

All in all, the Windmill divider consumes almost half the power and has 2dB less phase noise. The Windmill divider is the only design with only a single gate involved in creating both rising and falling output edges and has outstanding performance. Moreover, it does not have any of the (potential) issues mentioned above. These results are not IoT application specific — all designs can be scaled for more drive power or to reduce phase noise and/or I/Q-mismatch.

Table 4.1: Simulated Performance Comparison of 25% Duty-Cycle Clock Dividers in 22nm FD-SOI.

	Windmill	Ru [23]	Ghaffari [24]	Razavi [25]	Fabiano [26]	Kuo [11]		Liempd [27]	Ba [19]	Soer [28] inspired
Division factor	2	4	4	2	2	2		2	2	2
50% → 25% duty-cycle	-	-	-	-	-	AND	NOR	AND	AND	AND
P_{DC} [µW]	**36.1**	41.7	53.1	187.0	57.4	62.9	63.9	59.7	59.7	57.9
P_{diss} [µW]	**27.3**	47.1	70.0	172.5	51.1	53.5	54.5	48.7	57.1	49.2
Phase Noise, white [dBc] (@100MHz)	**-159.0**	-157.0	-157.0	-155.3	-154.5	-154.9	-156.7	-155.4	-154.6	-154.9
Phase Noise, 1/f region [dBc] (@10kHz)	**-135.0**	-132.8	-132.9	-132.5	-134.5	-130.4	-132.2	-130.9	-130.0	-129.9
σ_{IQ} [%]	0.60	0.82	0.84	0.71	**0.55**	1.0	0.75	1.0	1.1	1.1

The assumptions for this comparison are shown in Fig. 4.9.

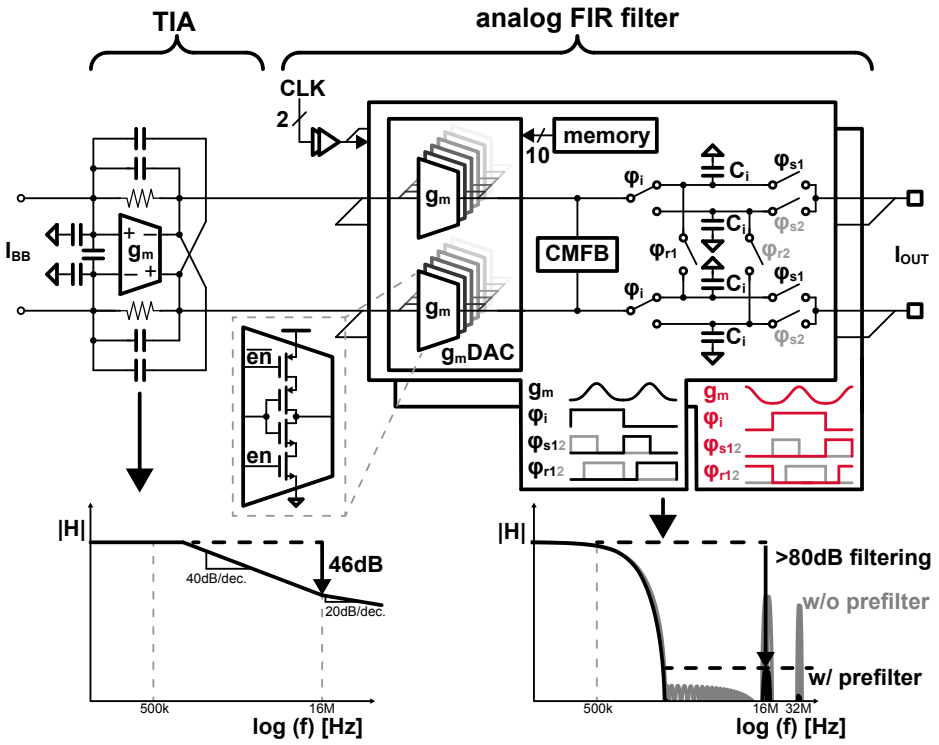


Figure 4.10: Baseband filter consisting of TIA and analog FIR filter.

4.5 Baseband Analog FIR Filter

High selectivity is achieved by the baseband analog FIR filter as shown in Fig. 4.10. It contains two time-interleaved paths to double the sample-rate for the same filter bandwidth [29, 30]. The transconductor is implemented as a 10bit pseudo-differential g_mDAC. A detailed explanation of the analog FIR filtering operation is described in Chapters 2 and 3. Low power consumption is obtained by push-pull transconductors, 5bit thermometer coding of the g_mDAC and a low update rate of the g_mDAC. The push-pull transconductors have low input referred noise for a given supply current. 5bit thermometer coding of the g_mDAC reduces the number of transitions in the g_mDAC, because the filter code turns fully on/off only once per integration cycle, much slower than the g_mDAC update frequency. Furthermore, the partially thermometer coding of the g_mDAC reduces the effect of transconductor mismatch on the filter stopband — in this design limited to –60dB [30].

The g_mDAC update-rate is 16MHz instead of 64MHz [29, 30] to further reduce the power consumption [2]. This comes at the cost of a closer filter alias and proportion-

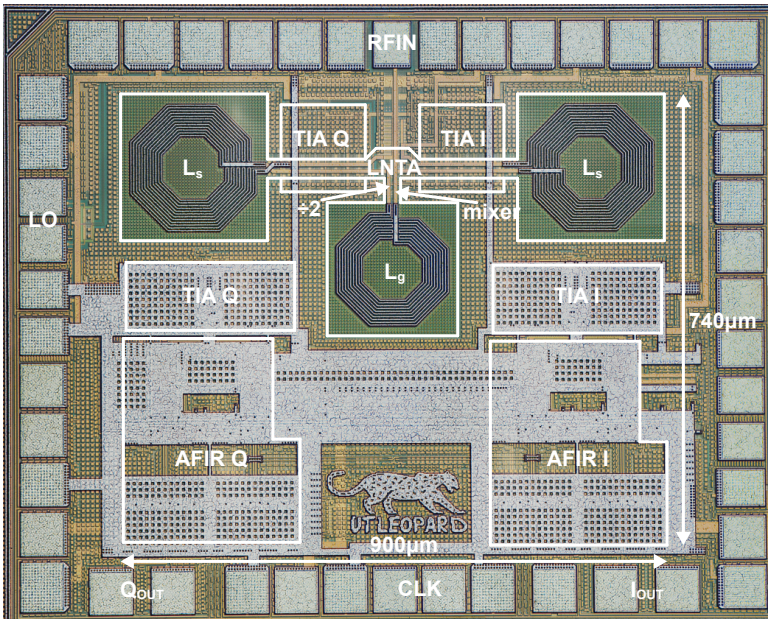


Figure 4.11: Die micrograph indicating the major blocks.

ally reduced attenuation of the filter alias. The inherent sinc windowed integration provides now only 34dB of attenuation of this alias. The TIA is employed to provide a prefilter that mitigates the remaining alias. The TIA provides 2^{nd}-order filtering by feedforward capacitors for about one decade [31]. In this way, 46dB of filtering is achieved at the alias frequency. Resulting in 80dB of total attenuation of the analog FIR alias. The exact cut-off frequency of the TIA is relatively relaxed, because it only has to provide prefiltering of the alias. Furthermore, the filtering characteristic is determined by the g_mDAC-code and clock signals — making the baseband filtering PVT insensitive [30]. Back-biasing is employed to compensate for the differential DC-offset in the TIAs. In this way, the DC-offset can be compensated without a significant increase in power consumption or noise — in contrast to current injection. The differential DC-offset of the g_mDACs is very small, well below 1mV referred at the output.

4.6 Experimental Results

The receiver front-end was designed and fabricated in a 22nm FD-SOI process and wire-bonded in a 40×40 pin QFN package. The die has an active area of 0.5mm^2 and the supply voltage is 700mV. Fig. 4.11 shows the die micrograph.

The measurement setup is shown in Fig. 4.12. The package is placed in a ZIF

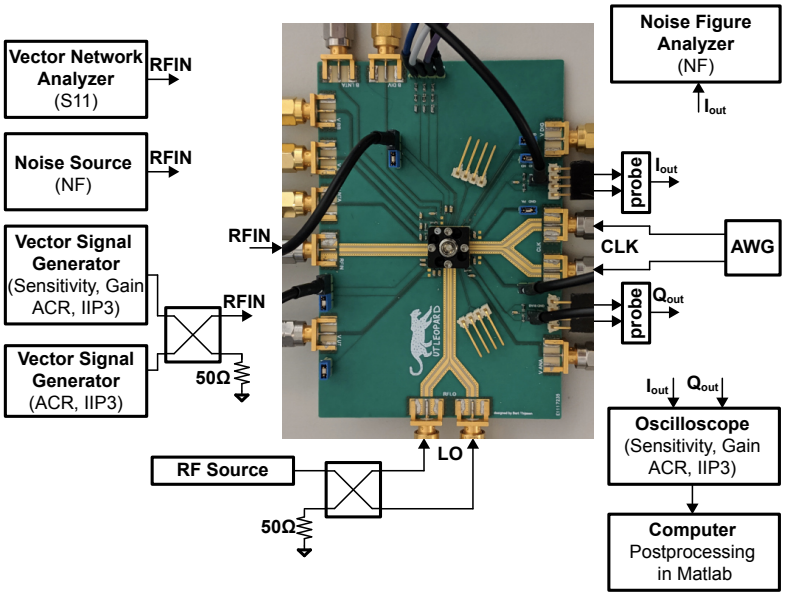


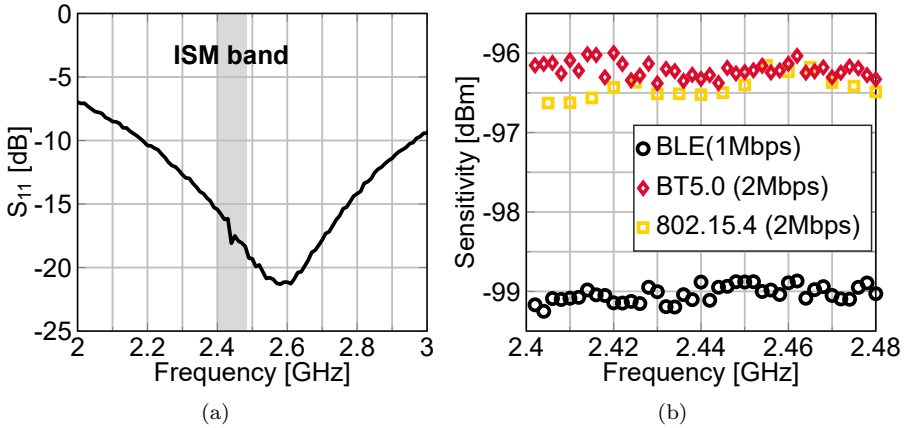
Figure 4.12: Measurement setup.

socket (Ironwood SG-MLF). Impedance matching is realized on chip — no external matching components are used. The capacitor output voltage is measured using an active probe (Teledyne LeCroy AP033) and the charge sharing loss is de-embedded as in Chapter 3 [30]. The measurements are performed in BLE (1Mbps) mode unless stated otherwise.

4.6.1 Matching and Sensitivity

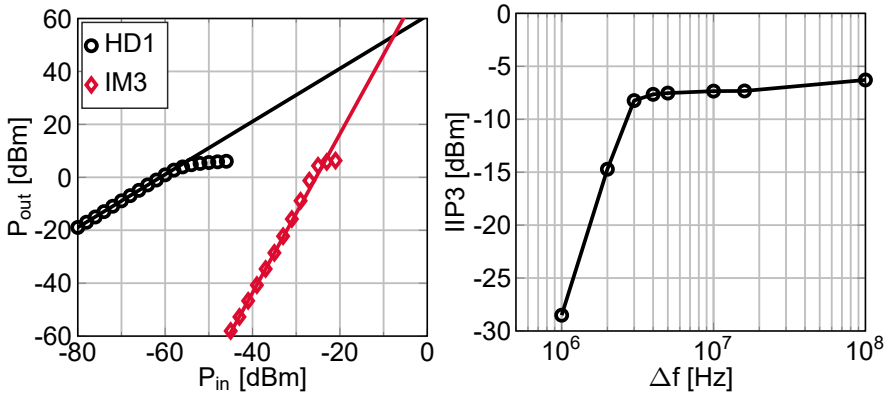
The measured S_{11} is shown in Fig. 4.13a. Good matching (S_{11} <–10dB) is achieved between 2.2 and 2.9GHz. The receiver's S_{11} is below –15dB in the ISM-band which is used in the targeted applications.

The measured noise figure is 5.5dB. The measured sensitivity for <0.1% bit-error-rate (BER) is shown in Fig. 4.13b for each channel. The transmitted signal is a PRBS-9 sequence. The received signal is demodulated using Matlab CPM demodulator (BLE, BT5.0) and MSK demodulator (802.15.4). For BLE, the Matlab CPM demodulator requires roughly 8dB SNR to achieve 0.1% BER, which is about 2dB less than a coherent receiver with threshold detection. The sensitivity is flat across the measured band. The 802.15.4 standard is characterized at 2Mbps HS-OQPSK raw data rate without despreading as in [6, 7].



(a) (b)

Figure 4.13: Measured receiver front-end performance. (a) S_{11}. (b) Sensitivity.



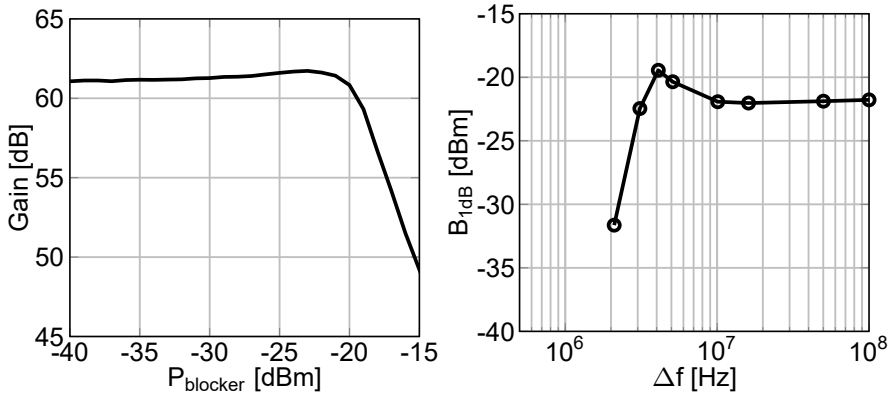
(a) (b)

Figure 4.14: Measured linearity. (a) In-band gain and out-of-band IM3 (for Δf = 4.01MHz and $2\Delta f$ = 7.98MHz input tones). (b) IIP3 versus frequency offset.

4.6.2 Linearity

The large signal in-band linearity is characterized by the compression point. The in-band gain is shown in Fig. 4.14a. The maximum gain is 61dB, roughly 30dB in both the front-end up to the TIA and analog FIR filter. The OP_{1dB} is 5.0dBm, corresponding to a $1.1V_{pp}$ differential output voltage.

The small-signal nonlinearity is characterized by the IM3 product as shown in Fig. 4.14. The IIP3 is –7.5dBm for a 4.01MHz offset at maximum gain of 61dB. The IIP3 is approximately flat from a 3MHz offset frequency. Simulation shows that this



(a) (b)

Figure 4.15: Measured receiver front-end performance in presence of a blocker. (a) Gain for a blocker at 4.1MHz offset. (b) B_{1dB} versus frequency offset.

is limited by the LNTA.

Fig. 4.15 shows the measured B_{1dB}, the blocker input power for which the in-band gain is 1dB compressed. The B_{1dB} is approximately –22dBm for a frequency offset $\geq$3MHz.

4.6.3 Adjacent Channel Rejection

The receiver's performance in presence of a blocker is characterized by the ACR. The ACR is measured with the desired signal strength at sensitivity+3dB and a blocker signal, modulated using the same standard with PRBS-15 sequence, at various offset frequencies. The wanted signal and blocker are generated with an R&S SMW200A and R&S SMBV100A, respectively. Fig. 4.16 shows the measured ACR.

The ACR is $\geq$63dB for BLE (1Mbps) at a frequency offset $\geq$3MHz. BT5.0 with double the data-rate has double the filter bandwidth. This shows in the ACR as $\geq$65dB ACR at $\geq$6MHz; double the frequency offset of BLE. The 802.15.4 ACR is $\geq$67dB for frequency offsets of $\geq$15MHz. 802.15.4 does not use Gaussian filtering of the transmitted signals and has therefore more transmitted spectral leakage in neighboring channels, which limits the maximal achievable ACR as confirmed here by the measurements. The filter alias at 16MHz/32MHz for 1Mbps/2Mbps is just visible by a small perturbation in the ACR rejection profile — indicating that the prefilter operates as desired.

In the following, we provide a short discussion regarding the ACR. From Fig. 4.16, we conclude that the ACR for BLE is limited to about 70dB. Various sources can

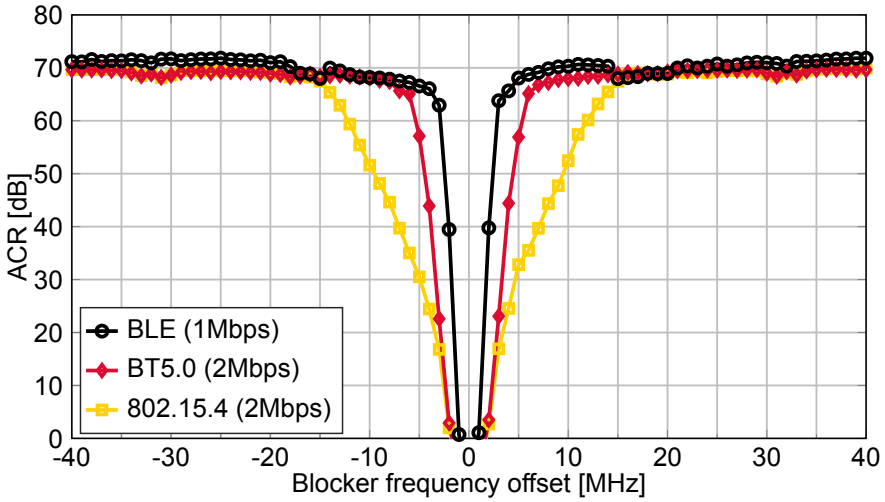


Figure 4.16: Measured adjacent channel rejection for different standards.

constrain the ACR performance:

- Limited blocker attenuation; the (small-signal) filtering.
- Reciprocal mixing; because of LO phase noise.
- Blocker gain compression; related to B_{1dB}.

The demodulation algorithm requires an SNR as derived from

$$\begin{aligned} \mathrm{SNR}_{\min} &\approx 174 + \mathrm{Sensitiviy} - \mathrm{NF} - 10\log(\mathrm{BW}) \\ &\approx 10\mathrm{dB} \end{aligned} \tag{4.13}$$

where NF is measured noise figure and BW the bandwidth. Therefore, 70dB of ACR requires about 80dB of attenuation to still demodulate the wanted signal. The phase noise of the mixer clock will result in an in-band reciprocal mixing product. The receiver's blocker noise figure (BNF) can be estimated as [32]

$$\mathrm{BNF} \approx -174 + P_b + \mathcal{L}(\Delta f) \tag{4.14}$$

where P_b is the blocker input power, which is

$$P_b = \mathrm{Sensitivity} + 3 + \mathrm{ACR} \tag{4.15}$$

at a given ACR level. From (4.13) to (4.15) the maximum allowed phase noise to achieve 70dB ACR is derived as

$$\begin{aligned} \mathcal{L}_{\max}(\Delta f) &\approx -\mathrm{SNR}_{\min} - 10\log(\mathrm{BW}) - \mathrm{ACR} \\ &\approx -140\mathrm{dBc/Hz} \end{aligned} \tag{4.16}$$

neglecting the circuit induced noise, i.e. BNF = NF + 3dB, as in [32]. The minimal required B_{1dB} for 70dB ACR is

$$\begin{aligned} B_{1dB,min} &\approx \text{Sensitivity} + 3 + \text{ACR} \\ &\approx -26\text{dBm} \end{aligned} \tag{4.17}$$

From a frequency offset of 5MHz onward, the BLE ACR is roughly constant at 70dB. Although, the analog FIR filter has constant rejection, the prefilter has more attenuation for larger frequency offsets. Hence, the ACR is not limited by the filter attenuation in this region. The simulated phase noise of the Windmill divider is –153.6dBc/Hz at 1MHz offset, which means that also the phase noise is not limiting. The ACR is most likely limited by blocker gain compression of –22dBm, which is somewhat more severe for a modulated blocker. This also explains that the 2Mbps ACR is slightly worse, because these standards have 3dB higher sensitivity and thus less "headroom" towards blocker gain compression.

At 2MHz offset, the ACR is 39dB — requiring a B_{1dB} of approximately –57dBm, which is much less than the measured –31dBm. The required filtering is roughly 49dB. The expected attenuation at 2MHz is about 70dB (10dB TIA + 60dB analog FIR [29, 30]). However, the blocker is modulated with 1Mbps covering a bandwidth of 1MHz, so that the filter attenuation from 1.5 to 2.5MHz offset is relevant. The worst case attenuation at 1.5MHz is only 46dB (6dB TIA + 40dB analog FIR [29, 30]), because of the steep FIR filter profile. At 3MHz offset the expected filtering is 76dB (16dB TIA + 60dB analog FIR [29, 30]). Therefore, the measured ACR of 39dB/63dB for 2MHz/3MHz offset can be explained by taking into account the blocker bandwidth. Consequently, the filter profile limits the ACR performance below approximately 5MHz offset when also taking into account the divider phase noise above.

The receivers frequency response was not measured here, as it is constrained by compression above 5MHz. Instead we report ACR performance, because this is what ultimately matters. The analog FIR filter response can be found in Chapter 3.

4.6.4 Power Consumption

The total power consumption is 370µW as shown in Fig. 4.17. The frequency divider power consumption is only 41µW, excluding the preceding buffer.

4.6.5 Comparison

The ACR in BLE-mode is compared to state-of-the-art IoT receivers in Fig. 4.18. The proposed receiver front-end has >20dB improved ACR for frequency offsets >2MHz. The prior art is measured with the wanted signal at –67dBm, which is similar to

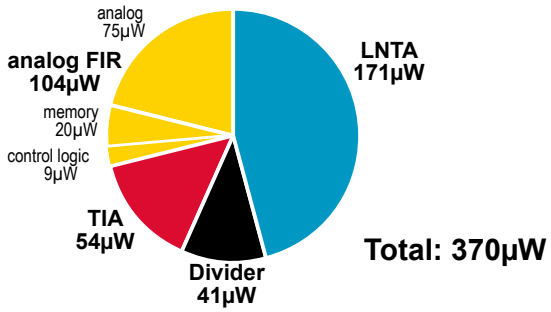


Figure 4.17: Power consumption breakdown.

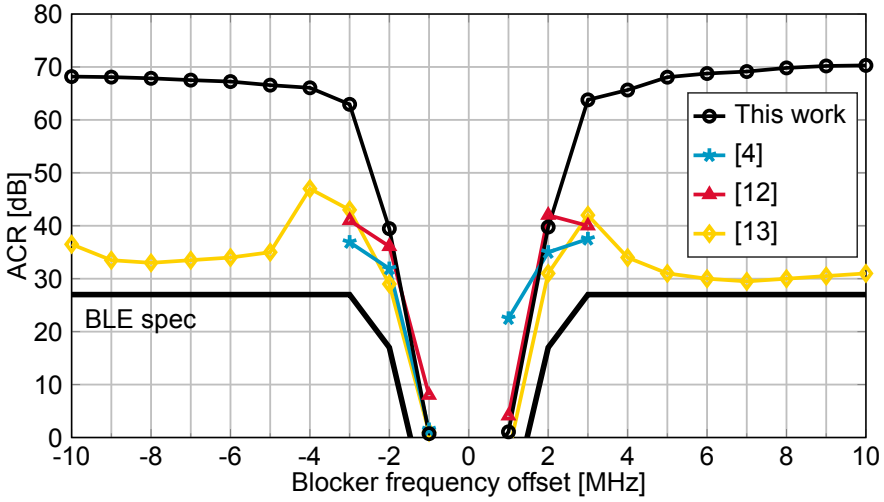


Figure 4.18: Comparison of the measured ACR for BLE (1Mbps).

placing a 29dB attenuator in front of the proposed receiver front-end. Alternatively, the feedback resistor can be reduced to avoid gain compression. The TIA feedback resistor is tunable in this design — allowing a 20dB gain reduction. Note that this is not an industrial product design, but rather an academic research work that has a broader scope: software defined ultra-low-power radio front-ends. Rather than choosing a standard specific sensitivity, we instead use a more general standard independent criterion: (actual NF based) sensitivity+3dB.

Table 4.2 summarizes the proposed receiver's performance and compares it to state-the-of-art 2.4GHz IoT receivers — only comparing the front-end. The power consumption of the receive chain is reduced by 2× or more, while achieving similar noise figure. The ACR is improved by more than 20dB at the 3rd channel offset. The IIP3 linearity is similar or higher than the prior art.

Table 4.2: Receiver Performance Summary and Comparison.

	This Work			[12] ISSCC'20		[20] ISSCC'20	[13] TMTT'19	[4] ISSCC'18	[5] ISSCC'18		[6][h] ISSCC'15		[10] ISSCC'13	[8] CICC'17
Standard	BLE	BT5.0	802.15.4[d]	BLE	BT5.0	BLE	BLE	BLE	BLE	BT5.0	BLE	802.15.4[d]	BLE	BLE
Data rate [Mbps]	1	2	2	1	2	1	1	1	1	2	1	2	1	1
On-chip Matching	Yes			Yes		Yes	No	Yes	Yes		No		Yes	Yes
P_{DC} [mW]	0.37	0.40	0.40	0.89[e]	-	5.3[g]	1.44[e]	1.2[e]	1.1[e]	-	1.95[e]	-	1.7	0.7[e]
NF [dB]	5.5			-		-	7.2	6	5.9		6.1		8.5	5.2
Sensitivity [dBm]	-99[b]	-96[b]	-96.5[b]	-96.4	-93.5	-94	-92	-94	-95	-92	-94	-91	-	-95.8
ACR 2nd/3rd channel[a]	39/63[b,c]	44/65[b,c]	52/67[b,c]	36.1/41.0[f]	36.3/45.0[f]	40/42[f]	29/42[f]	31/36[f]	18/30[f]	18/29.5[f]	25/35[f]	24/35[f]	-	-
IIP3 [dBm]	-7.5			-13.1		-	-17	-	-		-		-6	-19.7[i]
B_{1dB} [dBm]	-22			-		-	-	-	-		-		-	-
Gain [dB]	61	57	57	43.1		-	42	68	-		-		57	47-72
Supply Voltage [V]	0.7			0.5		0.8	1.2	1	0.8		1		0.6&1.2	1
Active Area [mm²]	0.5			1.9[g]		0.89[g]	0.7	1.64[g]	0.8[g]		1.3[g]		0.22	0.7[g]
Technology	22nm FDSOI			22nm FDSOI		40nm CMOS	130nm CMOS	65nm CMOS	40nm CMOS		40nm CMOS		65nm CMOS	40nm CMOS

[a]Channel spacing: BLE 1MHz; BT5.0 2MHz; 802.15.4 5MHz. [b]Demodulated using Matlab CPM demodulator (BLE, BT5.0) and MSK demodulator (802.15.4), both using a Viterbi algorithm with traceback depth of 16. [c]Measured with wanted signal at sensitivity +3dB. [d]Verified with 2Mbps raw data rate HS-OQPSK without de-spreading as in [6,7]. [e]Power consumption is estimated from power breakdown, e.g. w/o VCO/PLL. [f]Measured with wanted signal at -67dBm. [g]Includes more than RX path. [h]Some specifications of this work are found in [7]. [i]At minimal gain of 47dB.

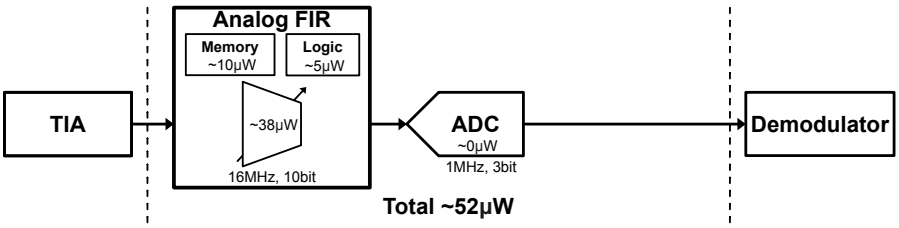


Figure 4.19: Overview of analog FIR baseband power consumption for BLE.

4.6.6 Full Receiver Discussion

In this section, the proposed design's performance is placed in the perspective of a full receiver design — including PLL and ADC.

In this design, all the channel filtering requirements are achieved by placing the high-order analog FIR filter after the TIA. This architecture choice significantly relaxes the dynamic range, sample rate and power consumption requirements of the ADC and down-stream digital signal processing functions, which only has to support demodulation and symbol detection.

In an application, the LO comes from an on-chip PLL with VCO and its phase noise could result in significant blocker induced noise which cannot be filtered — constraining the ACR. The phase noise of a state-of-the-art 0.5mW 5GHz VCO is –140dBc/Hz at 10MHz offset [33]. This corresponds to –140dBc/Hz at 5MHz offset when divided down to 2.5GHz using the frequency divider, which is sufficiently low for the achieved ACR.

It is useful to estimate the total power consumption of the entire receiver. A state-of-the art ADPLL consumes 673µW [34] and will consume roughly 910µW when implementing the low phase noise VCO design of [33] to obtain the ACR performance. The sampled output of the analog FIR filter, at 1Msample/s, can be used for ADC conversion. The ADC power consumption will be negligible if a SAR ADC is used. E.g., the 1Msample/s 10bit SAR ADC in [35] consumes only 3.2µW, more than sufficient for demodulation. Hence, the total power consumption excluding demodulation is estimated as 0.91+0.37=1.3mW.

4.7 Analog FIR Filter Discussion

Chapter 3 already showed that the proposed analog FIR has significant improved selectivity and power consumption compared to prior art continuous-time filters and discrete-time IIR filters. However, the requirements on the subsequent ADC are very low. The required sample rate is only 1Msample/s and roughly 3 to 4 bits are required for demodulation — resulting in negligible power consumption. This could give the

impression that a more digital approach can be beneficial. This section provides a discussion based on rough estimates. Architectural and technology improvements could significantly change the comparison results.

A single (I/Q) baseband path of the analog FIR approach is shown in Fig. 4.19. The total power consumption is about 52µW. An alternative is placing the FIR filter in digital and increasing the dynamic range and sample rate of the ADC. A 16Msample/s ADC is required to apply the FIR filter in digital. The state-of-the-art 12bit 12Msample/s ADC of [36] consumes 472µW and has 75.1dB spurious-free dynamic range (SFDR). These specifications are almost sufficient to allow 60dB of filtering — in a subsequent digital FIR filter — and demodulation. However, this approach still requires an amplifier upfront. Actually the charge domain sampler of the analog FIR approach would be good candidate as it uses efficient inverter-based transconductors, has low IRN and provides sinc filtering of sampling aliases. It would consume roughly 38µW. The digital FIR filter would also require the memory to provide the FIR coefficients (10µW). The digital FIR filter can be implemented using two time interleaved multiply-accumulate paths (Fig. 2.1b) — similar to the analog FIR approach. The multiplier FoM of 22nm FD-SOI is 4.6fJ/bit^2 [37]. Hence, the two multipliers combined would consume roughly 18µW for 12x10bit multiplication at 16MHz.

All in all, a digital approach will consume significantly more power consumption than the proposed analog FIR filter. Mainly, because the additional power of the analog FIR filter is only 5µW — from the logic buffers that drive the g_mDAC. The other blocks are also required when choosing a digital approach. Furthermore, switching to 2Mbps BT5.0 will double the power consumption of the digital circuitry. In case of the proposed analog FIR approach this means 15µW additional power for the memory + logic — as confirmed by the measurement results in Table 4.2. The digital approach will also roughly double the power consumption of the (already high power) ADC and digital FIR filter.

4.8 Conclusions

A 2.4GHz IoT receiver front-end is proposed and characterized for BLE, BT5.0 and IEEE802.15.4. The entire receive chain is optimized to minimize power consumption and improve selectivity.

Several techniques are proposed that achieve a 370µW power consumption — almost 2× lower than the state-of-the-art — in combination with a competitive 5.5dB NF. The LNTA has a push-pull inductive degenerated common-source architecture and is optimized using brute-force search on a simplified, though accurate, model. A single gate Windmill frequency divider has almost half the power dissipation concurrent with a phase noise improvement of 2dB or more compared to prior art. An

analog FIR filter is implemented with prefilter. Its 10bit transconductor DAC contains push-pull transconductors, 5bit thermometer coding and a low (16MHz for BLE) FIR-coefficient update-rate to optimize its power consumption while also achieving very sharp transition band. The receiver has ≥63dB ACR at ≥3 channels offset improving the state-of-the-art by >20dB. The analog FIR filter incorporates high selective filtering in a receiver baseband amplifier with negligible additional power consumption.

The proposed architecture and implementation techniques result in very low power consumption combined with outstanding selectivity, which makes the receiver front-end design ready for future IoT standards.

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Insanity: doing the same thing over and over again and expecting different results.

Albert Einstein

5

Phase Noise Cancellation Exploiting a Sub-Sampling Phase Detector

Clocks with low phase noise are a prerequisite for highly selective receivers. The >20dB improvement in selectivity of the receiver in Chapter 4 makes the phase noise requirement more stringent, as IoT receivers preferably do not use RF filters to reduce the cost. This chapter proposes a technique to reduce the phase noise by feedforward cancellation. The proposed technique reduces the phase noise of an integer-N PLL as verified by simulations. However, it can also be employed in fractional-N PLLs when a digital-to-time converter (DTC) is used in the reference path to align the edges at the phase detector — a common technique for fractional-N sub-sampling phase-locked loops (SSPLLs) [1, 2]. The contents of this chapter were previously published in the IEEE Transactions on Circuits and Systems II: Express Briefs [3], which is an extension on [4]. The proposed phase noise cancellation concept is patented in [5]. Section 5.6 and the last paragraph of Section 5.7 are added to discuss the phase noise cancellation technique in the context of the IoT receiver.

The author is aware that the content of this chapter partially overlaps with Chapter 1. However, the author preferred minimal modification of the already reviewed and accepted papers.

5.1 Introduction

Clocks with low phase noise and jitter are required in many applications — e.g. analog-to-digital converters, optical data communication and RF front-ends. SSPLLs [2, 6–8] have superior phase noise performance compared to conventional phase-frequency detector (PFD) PLLs. However, SSPLLs only reduce the close-in phase noise. The overall phase noise reduction is still limited to the maximal stable bandwidth of the PLL. For 3$^{\text{rd}}$ order type-II PLLs this is around the so-called Gardner's limit $f_{ref}/10$ [9].

A different method to reduce phase noise is by cancellation. This is a feedforward method and has therefore no stability limitations. Recently, several phase noise cancellation approaches have been published [10–14]. In [11], the delay in a ring oscillator is exploited for a delay-discriminator phase noise detection. The cancellation is performed by a variable delay block. Although showing 12.5dB phase noise improvement at $0.1f_{ref}$, the detection gain is constrained by limited inverter delay and the jitter performance is not state-of-the-art. [12] is also delay-line discriminator based and uses expensive off-chip components. The work in [13, 14] does not affect the clock phase noise, but the result of phase noise. In [13], the reciprocal mixing product as a result of phase noise is canceled and [14] cancels the phase noise in the digital domain — which does not improve the blocker noise figure.

Injection-locked PLLs [15–17] and PLLs with cascaded sub-sampling delay-locked loops (SSDLLs) [18] are also promising techniques to improve clock phase noise. In injection-locked PLLs the VCO edge is aligned to the reference clock edge by injection. In the PLL with cascaded SSDLL, the phase error of a PLL is measured by a sub-sampling phase detector (SSPD) and corrected in a DLL; a feedback method. Recently, a feedforward phase noise cancellation architecture was proposed that also exploits an SSPD [19]. All these techniques have ring oscillator implementations with state-of-the-art performance — a PLL FoM [6] around –235dB.

In this chapter, we analyze the fundamental limitations of a sub-sampling phase noise cancellation PLL (SSPNC-PLL) that we developed simultaneously but independently of [19]. Our analysis shows that the phase noise improvement is limited by aliasing and the SSPD hold operation. The SSPNC-PLL can achieve significantly lower root mean square (rms) jitter than an SSPLL alone.

The structure of this chapter is as follows. First, in Section 5.2, the PLL transfer characteristics are introduced. In Section 5.3, the fundamental limitations of the feedforward phase noise cancellation system exploiting an SSPD are analyzed. Section 5.4 introduces the SSPNC-PLL. The theoretical results are verified by simulation in Section 5.5 and conclusions are presented in Section 5.7.

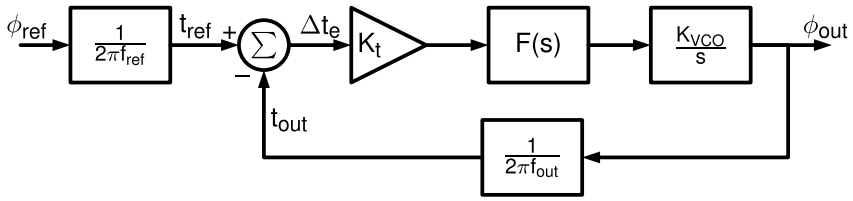


Figure 5.1: Unified linear PLL model for timing error based phase detectors.

5.2 Phase-Locked Loops

PFDs and SSPDs both measure the timing difference of two incoming clock signals. The linear model of Fig. 5.1 allows for a *unified analysis* of PLLs with timing error detectors. It models the phase detector with jitter detection gain K_t, the loop filter with transfer function $F(s)$ and the VCO with transfer function K_{VCO}/s. The phase detector is often implemented including a charge pump [2, 6–9, 11]. The relation between output frequency f_{out} and reference frequency f_{ref} is

$$N \equiv \frac{f_{out}}{f_{ref}} \tag{5.1}$$

Note that we explicitly model the phase detector as a *timing error detector*, in contrast to the conventional approach of a phase detector [6, 9]. A divide-by-N — and multiply-by-N in case of an SSPLL [6] — are not explicitly present in the model, because a frequency divider does not alter the timing instance of the clock signal zero crossings. Only the frequency of zero crossings is changed. In this chapter, we use the following transfer functions of the PLL:

$$G(s) \equiv \frac{t_{out}(s)}{\Delta t_e(s)} = K_t F(s) \frac{K_{VCO}}{s} \cdot \frac{1}{2\pi f_{out}} \tag{5.2}$$

$$H(s) \equiv \frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{1}{2\pi f_{ref}} \cdot \frac{K_t F(s) \frac{K_{VCO}}{s}}{1 + G(s)} \tag{5.3}$$

$$E(s) \equiv \frac{\Delta t_e(s)}{t_{ref}(s)} = \frac{1}{1 + G(s)} \tag{5.4}$$

5.2.1 PLL Phase Noise Spectrum

The output phase noise spectrum of the PLL can be derived given the additive noise at the different nodes in the model. Suppose, the charge pump noise $S_{i,CP}(f)$ and VCO phase noise $S_{\phi,VCO}(f)$ are the dominating components in the PLL output noise.

The output phase noise spectrum can be determined as

$$S_{\phi,out}(f) = \left|\frac{2\pi f_{ref}}{K_t}\right|^2 |H(f)|^2 S_{i,CP}(f) + |E(f)|^2 S_{\phi,VCO}(f) \tag{5.5}$$

5.2.2 SSPD versus PFD

The linear model of Fig. 5.1 can directly be applied to both SSPD and PFD based PLLs. Both phase detectors measure the timing difference of the two input clocks. The key distinction is in the timing detector gain [8]

$$K_{t,PFD} \propto f_{ref} \tag{5.6}$$

$$K_{t,SSPD} \propto \left.\frac{\mathrm{d}v(t)}{\mathrm{d}t}\right|_{t=t_{ref}} \approx 2\pi f_{out}\hat{v} \tag{5.7}$$

assuming a sinusoidal VCO output $v(t)$. In (5.7), $\hat{v}$ is the amplitude of $v(t)$ and t_{ref} the sampling instant. The slope of $v(t)$ is finite and known — e.g. provided by a constant slope generator [1]. The SSPD gain is approximately N times higher than of the PFD. Therefore, the charge pump's phase noise contribution is reduced by N^2. The result is superior jitter performance of SSPLLs compared with PFD PLLs — e.g. [1] demonstrated 0.16ps rms jitter while consuming only 8.2mW.

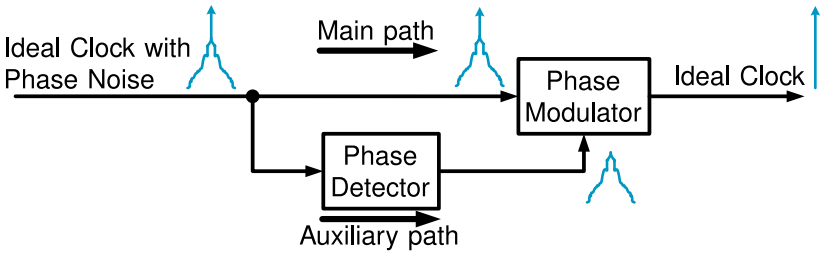
5.2.3 SSPD Hold Delay

The SSPD introduces a delay of $0.5T_{ref}$ when it is implemented using an ideal sample-and-hold circuit. The result is 18° less phase margin for an SSPLL with bandwidth $f_{ref}/10$ — considerably reducing the loop stability. SSPLLs are often implemented with a pulser to reduce the SSPD gain and thereby reducing the required capacitor size for stable operation [6]. An added bonus is the reduced hold delay of the pulser implementation. This increases the phase margin and improves the SSPLL stability. The SSPD characteristics are further analyzed in Section 5.3.1.

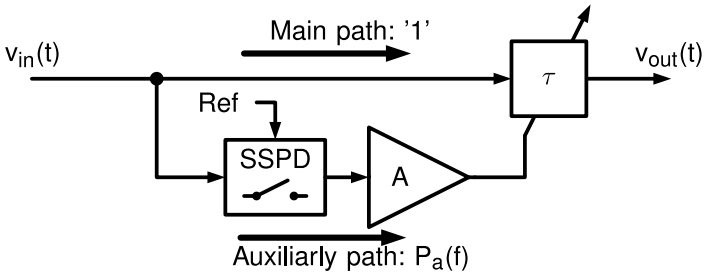
5.3 Feedforward Phase Noise Cancellation

Feedforward phase noise cancellation relies on the principle shown in Fig. 5.2a [10–12]. The phase noise of the input clock is detected in the auxiliary path and subtracted from the phase noise of the clock in the main path by a phase modulator. Ideally, the result is a clock without phase noise.

[19] proposed the implementation of Fig. 5.2b. It consists of an SSPD as phase detector, variable delay τ and an appropriate gain A. The SSPD bandwidth is constrained by the Nyquist limit $f_{ref}/2$. This potentially allows for phase noise reduction



(a)



(b)

Figure 5.2: Feedforward phase noise cancellation. (a) Basic principle [10–12]. (b) Block implementation [19].

up to 5 times the maximal PLL bandwidth. We refer to frequencies up to $f_{ref}/2$ as in-band and outside this range as out-of-band. Sub-sampling phase noise cancellation can be cascaded to any generated clock signal as long as the reference and input clocks are aligned — e.g. realized by an SSPLL (Section 5.4).

In this section, we discuss the fundamental limitations of feedforward phase noise cancellation employing an SSPD. The variable delay and gain are assumed ideal. A possible implementation of the variable delay is e.g. with a current-starved inverter [19].

5.3.1 SSPD Analysis

An SSPD converts the timing error of input clock signal $v_{in}(t)$ into a sampled voltage, according to

$$v_{sam}(t_{ref}) = \Delta t_e \cdot \left.\frac{\mathrm{d}v_{in}(t)}{\mathrm{d}t}\right|_{t=t_{ref}} \tag{5.8}$$

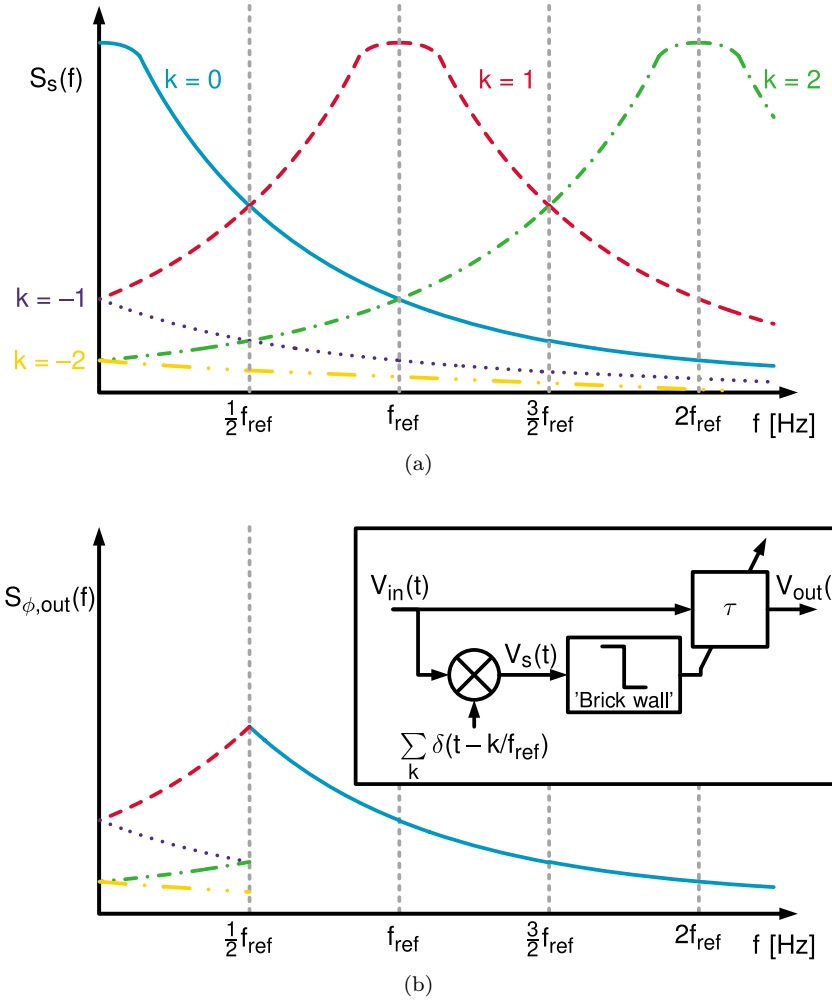


Figure 5.3: Phase noise spectral components up to $k = \pm 2$. (a) After sub-sampling detection. (b) After cancellation with ideal reconstruction filtering.

where t_{ref} is the sampling instant. The timing error is

$$\Delta t_e = t_{ref} - t_{in} \tag{5.9}$$

where t_{in} and t_{ref} are the time instances corresponding to the zero crossings of the input clock and reference signal, respectively. The derivative of $v_{in}(t)$ is approximated as constant within time interval Δt_e.

Two mechanisms impair the phase noise detection performance: Aliasing during phase detection and the filtering of the hold function. During detection the clock

phase noise aliases around every $f_{ref}/2$. The detected — sub-sampled — spectrum is

$$S_s(f) = f_{ref} \sum_{k=-\infty}^{\infty} S_{\phi,in}(f - kf_{ref}) \tag{5.10}$$

This spectrum is illustrated in Fig. 5.3a. We assume a stationary input phase noise spectrum with bounded total rms jitter; e.g. the output of a PLL. The aliased spectral components are illustrated by color. The sum of these components is the actual detected spectrum. In addition to the wanted solid ($k = 0$) spectral component, several other spectral components alias towards the $[0, f_{ref}/2]$ band. Suppose an ideal brick-wall filter with cut-off at $f_{ref}/2$ is applied as reconstruction filter. As the filter comes after the sampler, the unwanted aliased components remain present in-band and are uncorrelated with the solid ($k = 0$) component that we wish to cancel. The resulting output phase noise spectrum $S_{\phi,out}(f)$ after cancellation is shown in Fig. 5.3b and can be approximated by

$$S_{\phi,out}(f) \approx \begin{cases} S_{\phi,in}(f_{ref} - f) & 0 \leq f < f_{ref}/2 \\ S_{\phi,in}(f) & f \geq f_{ref}/2 \end{cases} \tag{5.11}$$

The aliased components up to $f_{ref}/2$ fundamentally limit the cancellation performance. Fortunately, the VCO phase noise shows a $1/f^2$ roll-off. This colored spectrum allows for phase noise detection even after aliasing, because in-band the non-aliased phase noise dominates the output of the SSPD.

In practical systems, a zero-order hold is applied to the sampled signal. The hold operation transfer function $H_h(f)$ is

$$H_h(f) = T_h \,\mathrm{sinc}(fT_h) e^{-j\pi f T_h} \tag{5.12}$$

Several limitations arise due to the hold filter function:

- The hold attenuation limits the in-band cancellation.
- The delay of the zero-order hold impairs the cancellation performance, especially at high frequency offsets.
- The out-of-band aliases are only moderately filtered.

5.3.2 Phase Noise Cancellation Output Spectrum

Suppose, that the gain A and delay sensitivity K_τ are ideal, linear and with bandwidth $\gg f_{ref}/2$. The cancellation condition is

$$P_a(f) = f_{ref} T_h \,\mathrm{sinc}(fT_h) e^{-j\pi f T_h} A K_\tau = 1 \tag{5.13}$$

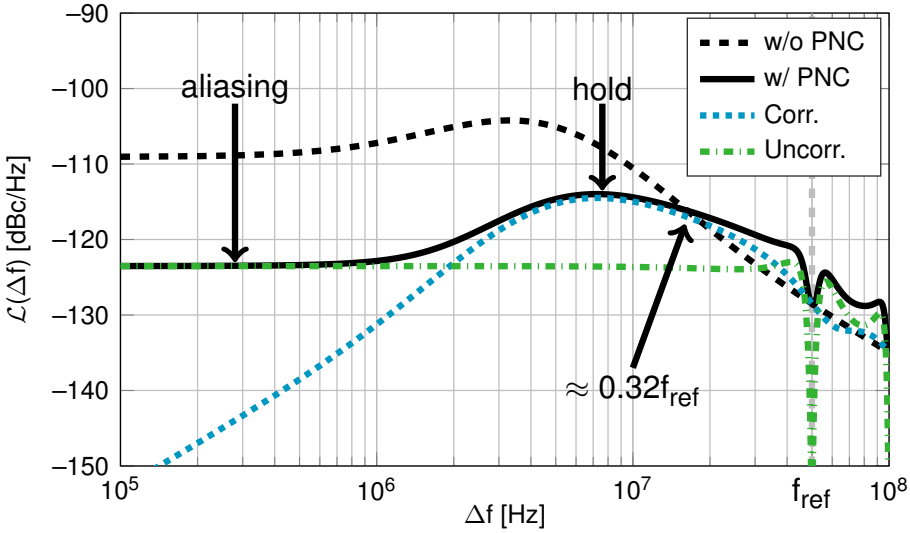


Figure 5.4: Modeled phase noise cancellation (PNC) output spectrum.

where $P_a(f)$ is the transfer function of the auxiliary path. $P_a(f)$ is frequency dependent, which means it is practically impossible to cancel at every frequency. The output spectrum of the phase noise cancellation system $S_{\phi,out}(f)$ using (5.10) and (5.13) is

$$S_{\phi,out}(f) = \underbrace{|1 - P_a(f)|^2 \, S_{\phi,in}(f)}_{\text{correlated PN}} + \underbrace{|P_a(f)|^2 \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,in}(f - k f_{ref})}_{\text{uncorrelated PN}} \tag{5.14}$$

In (5.14), we recognize two terms: The correlated phase noise ($k = 0$) and uncorrelated phase noise that is introduced by aliasing ($k \neq 0$). An equation with similar structure was also found for a feedback system analyzing sampling effects in a PFD PLLs [20].

Fig. 5.4 illustrates the phase noise cancellation performance for a clock with the phase noise spectrum of the Section 5.5 SSPLL; assuming $T_h = 1/f_{ref}$. The phase noise is canceled up to $0.32 f_{ref}$, more than 3× Gardner's limit. The reduction is limited by: aliasing at low frequency offsets, the hold operation at intermediate offsets and both correlated and uncorrelated phase noise contributions outside the cancellation bandwidth. (5.14) explains also the phase noise increase above roughly 10MHz in [18]. Since, a wide bandwidth SSDLL does not provide filtering of aliased phase noise nor delayed phase noise that is introduced by the SSPD.

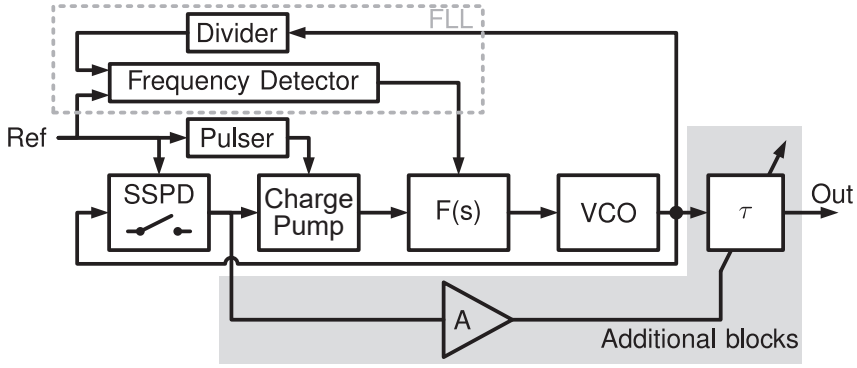


Figure 5.5: Sub-sampling phase noise cancellation PLL [19].

5.3.3 Practical Implementation Limitations

The total gain of the auxiliary path G_a should be 1. Mismatch between the main and auxiliary paths results in imperfect cancellation, as expressed by

$$\text{Cancellation Limit} = 20 \log |1 - G_a| \tag{5.15}$$

The required specification for maximal cancellation can be obtained from the fundamental limits. 90% accuracy limits the reduction to 20dB, sufficient for the spectrum of Fig. 5.4. This also imposes the required linearity in the auxiliary path.

The phase noise cancellation performance is in-band ultimately limited by the reference phase noise, which is directly present at the output. The noise contribution of A is small, because of the high SSPD detector gain; typically >1GV/s. An SSPD phase offset introduces a delay offset in the variable delay. However, a fixed delay offset has no influence on the output phase noise — it just introduces clock skew. The input clock jitter should be constraint to avoid saturation of the variable delay. The variable delay τ can be part of an existing buffer [11], because the required delay is small; in the order of picoseconds, much smaller than the buffer rise/fall time. Therefore, the added jitter of the variable delay is marginal, since this is proportional to the delay [21].

5.3.4 Spur Cancellation

In addition to phase noise, other spurs introduced in the PLL loop are canceled as well. E.g. supply variations might introduce spurs at the VCO. In [19] it is shown that a spur at 100kHz offset can be reduced by 19.5dB.

5.4 Sub-Sampling Phase Noise Cancellation PLL

The phase noise cancellation system of Section 5.3 requires aligned zero-crossings of the reference and input clock. This is accomplished by cascading a PLL with phase noise cancellation. In this way, the PLL aligns the clocks. The PLL is implemented by an SSPLL for minimal jitter. The SSPD error signal in the SSPLL can be reused for phase noise cancellation, because both signals are the same — the SSPLL output phase error. The schematic of this sub-sampling phase noise cancellation PLL (SSPNC-PLL) is shown in Fig. 5.5 [19]. It consists of a regular SSPLL with VCO, SSPD, charge pump, pulser and loop filter with transfer $F(s)$. The frequency-locked loop (FLL) is required to frequency lock the SSPLL [6]. Additionally, an appropriate gain and variable delay element for phase noise cancellation are implemented. The SSPD is part of the SSPLL and reused for phase noise cancellation.

The large detection gain of the SSPD results in only little required gain A in the auxiliary path, typically in the order of 1. Furthermore, the required bandwidth of A is small — approximately $5f_{ref}$ — and an existing buffer can be reused as variable delay. Therefore, we expect little additional power consumption compared with a conventional SSPLL.

To verify the derivations of Section 5.3, the widely used 3$^{\text{rd}}$ order type-II PLL is applied, with loop filter [9]

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1(s\tau_3 + 1)} \tag{5.16}$$

The bandwidth of the SSPLL can be estimated by [9]

$$K = K_t K_{VCO} \frac{\tau_2}{\tau_1} \cdot \frac{1}{2\pi f_{out}} \quad \text{[rad/s]} \tag{5.17}$$

From (5.5) and (5.14), the output phase noise spectrum of the SSPNC-PLL can be determined as

$$S_{\phi,out}(f) = |1 - P_a(f)|^2 \, S_{\phi,SSPLL}(f) + |P_a(f)|^2 \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,SSPLL}(f - kf_s) \tag{5.18}$$

5.5 Simulation Results

The theory of Sections 5.3 and 5.4 is verified in simulation. The assumptions of the simulations are listed below

1. The output frequency of the PLL is 2.5GHz with a 50MHz reference, ($N = 50$) and pulser on time of 1ns.

2. The PLL is locked. The steady-state is achieved.

3. The charge pump noise and VCO phase noise are dominant. The VCO phase noise is purely $1/f^2$ and is modeled as additive white noise on the VCO input. The loop noise is modeled as additive white noise to the charge pump current. $1/f$ noise is neglected.

4. The reference is assumed clean; without phase noise.

5. The SSPLL is a 3^{rd} order type-II PLL with loop parameters $K\tau_2 = 3$ and $\tau_2/\tau_3 = 9$. These normalization parameters fully characterize the PLL steady-state behavior and are identified as nearly optimum [9] when maximum bandwidth, good damping and as much filtering of the 3^{rd} pole as possible is required.

6. The VCO phase noise is based on a 1mW, –163dBc/Hz FoM oscillator — close to the theoretical limit of –165dBc/Hz for ring oscillators [22].

7. The loop noise power is chosen such that the loop noise and VCO phase noise equally contribute to the total rms jitter; i.e. the bandwidth is chosen as the optimum bandwidth given the loop noise and VCO phase noise power [23].

8. Both the gain A and variable delay τ are ideal.

9. The noise spectra are obtained by averaging 200 (transient noise) simulations in Matlab Simulink.

Fig. 5.6 shows the output phase noise with and without phase noise cancellation for both a PLL bandwidth of $f_{ref}/10$ and $f_{ref}/50$. We first discuss $f_{ref}/10$. The phase noise is reduced at low frequency offsets up to 15dB. At 5MHz offset ($f_{ref}/10$), the phase noise reduction is 8dB. The phase noise reduction bandwidth is 14MHz ($f_{ref}/3.6$). Outside the reduction bandwidth the phase noise is slightly increased as expected. The model of (5.14) is in accordance with the simulated phase noise spectrum. We define the cumulative rms jitter $\sigma_t(f_u)$ as

$$\sigma_t^2(f_u) = \frac{1}{(2\pi f_{out})^2} \int_0^{f_u} 2\mathcal{L}(\Delta f)\mathrm{d}\Delta f \tag{5.19}$$

The total rms jitter $\sigma_t(\infty)$ is improved by 3.2dB.

The phase noise cancellation system allows for novel loop filter designs to improve the jitter even further. Most of the jitter contribution is around the PLL bandwidth. Reducing the PLL bandwidth re-positions the phase noise bump to lower offset frequencies.

This is illustrated by the $f_{ref}/50$ plots in Fig. 5.6. At low offset frequencies the SSPLL phase noise slope is +20dB/decade, so the VCO phase noise contribution is

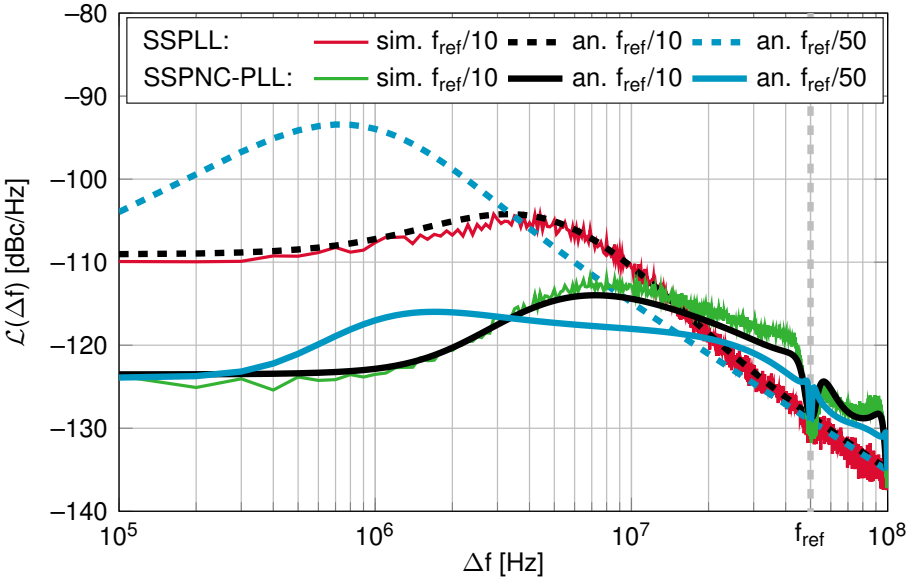


Figure 5.6: Simulated (sim.) and analytical (an.) phase noise w/ (SSPNC-PLL) and w/o (SSPLL) phase noise cancellation for different PLL bandwidths using (5.5) and (5.18).

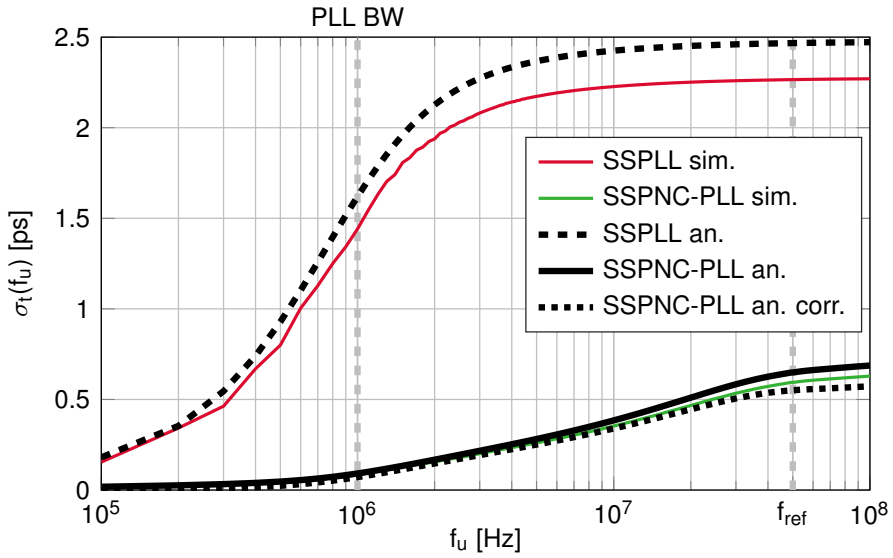


Figure 5.7: Simulated (sim.) and analytical (an.) cumulative rms jitter w/ (SSPNC-PLL) and w/o (SSPLL) phase noise cancellation, the SSPLL bandwidth is $f_{ref}/50$.

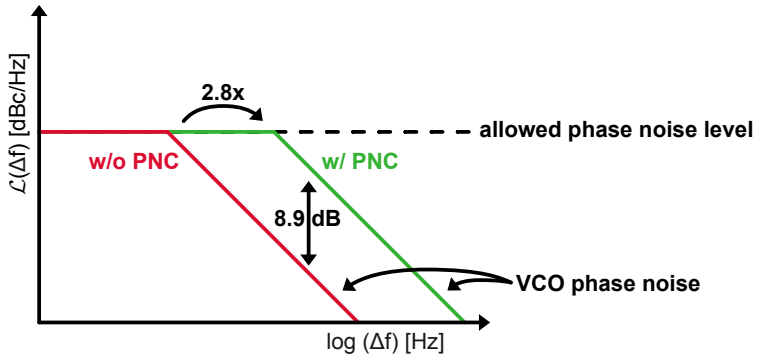


Figure 5.8: PLL phase noise w/ and w/o sub-sampling phase noise cancellation for a receiver application.

dominant. The phase noise reduction bandwidth is $0.3f_{ref}$. 9dB phase noise reduction is achieved at a frequency offset of $f_{ref}/10$. The out-of-band phase noise is 4dB lower than in the case of $f_{ref}/10$. The corresponding cumulative jitter is shown in Fig. 5.7. The jitter contribution is much more spread across frequencies than without phase noise cancellation. The aliased components have only a minor effect on the total rms jitter as illustrated by the jitter of the correlated part. The total rms jitter is significantly reduced: 11dB and 7.2dB compared with the SSPLL with bandwidth $f_{ref}/50$ and $f_{ref}/10$, respectively.

Our analysis shows that the state-of-the-art performance of [19] can still be enhanced. The phase noise reduction bandwidth can be improved from roughly $f_{ref}/10$ [19] to $f_{ref}/3.6$ by increasing the auxiliary path bandwidth; significantly reducing the jitter.

5.6 IoT Receiver Context

The proposed phase noise cancellation architecture is developed as a general purpose technique to increase the effective PLL phase noise reduction bandwidth and to reduce the jitter of a PLL for a given power consumption. In the context of the highly selective IoT receiver, sub-sampling feedforward phase cancellation can allow for a reduced power consumption of the PLL as illustrated in Fig. 5.8. The baseband analog FIR filter has a flat stop-band at a very small frequency offset. This flat stopband requires a certain phase noise level to avoid corruption of the desired signal by reciprocal mixing of a nearby blocker: the allowed phase noise level. The increase of the effective PLL bandwidth allows for a higher VCO phase noise in the PLL, since this phase noise is reduced by cancellation. The phase noise reduction bandwidth is

increased by 2.8×. Hence, the VCO power consumption can be reduced by roughly 7.7× (8.9dB) for the same VCO FoM. The PLL power consumption will be reduced considerably as the VCO is a major contributor to its total power consumption, e.g., 39% in [24].

5.7 Conclusions

Feedforward phase noise cancellation can reduce the phase noise and jitter of clocks without stability limitation. A sub-sampling phase detector is attractive, because of its linearity and high detection gain. The performance of this detector is fundamentally limited by aliasing, hold delay, in-band hold attenuation and limited out-of-band attenuation of the aliases. A sub-sampling phase noise cancellation PLL architecture that reuses the error signal of a sub-sampling PLL is discussed for feedforward phase noise cancellation. Moreover, it cancels spurs that are introduced in the PLL loop. Analytical expressions are derived that predict the output phase noise given an input phase noise spectrum to the cancellation technique. These expressions are verified by simulations for a given wideband sub-sampling PLL design. The phase noise reduction bandwidth is increased to $f_{ref}/3.6$ by the phase noise cancellation technique. The phase noise is improved by more than 9dB at a frequency offset of $f_{ref}/10$. The total rms jitter of the PLL is improved by 7.2dB compared with a sub-sampling PLL with maximal bandwidth.

The proposed phase noise cancellation technique increases the effective phase noise reduction bandwidth of the PLL. This allows for a higher VCO phase noise for the same reciprocal mixing products. The VCO power consumption could roughly be reduced by 7.7×. The proposed technique is simulated for an integer-N PLL but a DTC in the reference clock path can allow fractional-N operation [1, 2].

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One worthwhile task carried to a successful conclusion is better than 50 half-finished tasks.

Bertie Charles Forbes

6

Conclusions

This chapter presents the conclusions of this dissertation. The main innovations of this work are listed in the Section Original Contributions. In addition, recommendations are given for future research.

6.1 Conclusions

Wireless connectivity is essential to enable the Internet-of-Things (IoT). The increasing number of devices challenges the requirements on the wireless specifications as well as the power consumption. This dissertation focuses on improving the wireless receiver selectivity and reducing the power consumption while maintaining low noise figure (NF) and good linearity. The target applications are 2.4GHz IoT standards as Bluetooth Low Energy (BLE) and IEEE802.15.4. Reducing the receiver power consumption will improve the battery lifetime, since it reduces the average and peak power consumption. This dissertation proposes analog finite impulse-response (FIR) filtering to improve the receiver selectivity and introduces several power optimizations across the receive chain — including a Windmill frequency divider architecture. Furthermore, a feedforward phase noise cancellation architecture is suggested to reduce phase-locked loop (PLL) phase noise at little additional power consumption.

Analog FIR filters can be implemented using a simple architecture. The output is sampled and can be at a low sample rate, because the analog FIR circuit filters the unwanted spectral components substantially. Analog FIR filters with symmetric

coefficients introduce a pure time delay and have therefore a linear phase response, which does not phase distort the desired signal. The inherent sinc filtering of the filter aliases relaxes the requirements of a prefilter and allows a low FIR coefficient update rate. Analog FIR circuits have been investigated prior to this work, but not as channel selection filters for an IoT application, which requires low power consumption as well as steep and strong filtering. (Chapter 2).

An analog FIR filter architecture that uses two 10bit pseudo-differential transconductance digital-to-analog converters (g_mDACs) and four integration capacitors is proposed. It implements a 128tap FIR. Several performance impairments are analyzed, including the g_mDAC output impedance and mismatch. The parasitic g_mDAC output impedance is compensated in the filter coefficients. The effect of transconductor mismatch is reduced by partially thermometer coding the g_mDAC. The filter is designed and fabricated in a 22nm fully-depleted silicon-on-insulator (FD-SOI) process. Its bandwidth is accurately tunable from 0.06 to 3.4MHz. The filter combines steep and strong filtering (f_{-60dB}/f_{-3dB}=3.8) with low power consumption (92µW) and low input-referred noise (IRN) (12 nV/$\sqrt{\text{Hz}}$). The low power consumption is accomplished by: the single switchable transconductor design, a low filter update rate of 64MHz and 5bit thermometer coding of the g_mDAC. The blocker 1dB compression point (B_{1dB}) is –3.4dBm and a consistent attenuation of >60dB is obtained for unwanted signals up to –4dBm. (Chapter 3).

A zero-IF receiver architecture is proposed with power optimizations across the receive chain. It employs a push-pull inductive degenerated low-noise transconductance amplifier (LNTA) which was optimized using brute-force search on a simplified model. The LNTA combines a low NF with low power consumption. The LNTA output current is downconverted by a passive mixer and converted to voltage using a transimpedance amplifier (TIA). This TIA is used as prefilter to reduce the filter aliases of the subsequent analog FIR channel filter. The combined inherent attenuation of analog FIR filter and TIA prefilter result in 80dB attenuation of the filter aliases, while allowing a reduction in the FIR coefficient update rate to 16MHz — which further reduces the analog FIR filter power consumption. A Windmill 25% duty-cycle frequency divider architecture is proposed. It reduces the power dissipation by almost 2× while reducing the phase noise by 2dB or more compared with prior art designs as verified by simulations. The receiver front-end was designed and fabricated in a 22nm FD-SOI process. It has more than 63dB adjacent-channel rejection (ACR) at three channels offset or more, a competitive 5.5dB NF and –7.5dBm input-referred third-order intercept point (IIP3) at maximum gain — while consuming only 370µW. (Chapter 4).

Improvements on the receiver filtering specifications bring more stringent demands on the local oscillator (LO) phase noise performance. A feedforward phase noise cancellation structure employing a sub-sampling phase detector (SSPD) is proposed to

reduce the phase noise without a (significant) increase in the power consumption of the LO generation. This phase noise cancellation structure can be implemented in a sub-sampling phase-locked loop (SSPLL) and the inherent SSPD can be reused. Furthermore, spurs that are introduced in the PLL loop are reduced as well. Analytical expressions are derived and verified by simulations to qualify the performance improvement. The phase noise cancellation technique increases the phase noise reduction bandwidth to $f_{ref}/3.6$. The phase noise at $f_{ref}/10$ is reduced by 10dB and the total rms jitter of the PLL is improved by 7.2dB using phase noise cancellation. (Chapter 5).

Several techniques are proposed and verified that allow to significantly improve the performance of IoT receivers while reducing their power consumption — granting improved selectivity along with increased battery life-time. These innovations help to pave the way to an all connected world. Not just connecting *everyone*, but connecting *everything*.

6.2 Original Contributions

Several original contributions are proposed in this dissertation:

- The inverter-transconductor capacitor analog FIR filter architecture to provide minimal input referred noise for a given power consumption.
- A transconductor analog FIR filter with dynamically switched coefficients in combination with a continuous time common-mode feedback, resulting in a stable transconductor output common mode voltage.
- Low-update rate in the analog FIR filter in combination with a simple prefilter to reduce power consumption.
- Partially thermometer bit analog FIR coefficients for;
  - reduced power consumption of the analog FIR DAC;
  - reduced coefficient mismatch effect on the filter transfer.
- The analysis of the following practical implementation impairments of analog FIR filters;
  - the effect of the g_mDAC output conductance on the filter transfer and its compensation;
  - the effect of parasitic g_mDAC output capacitance on the filter transfer;
  - the effect of analog FIR coefficient mismatch on the filter stopband attenuation for binary and (partially) thermometer coded designs.

- A receiver architecture with analog FIR channel selection filter suitable for low power IoT applications.
- The Windmill 25% duty-cycle frequency divider architecture that employs only a single gate between input clock and four 25% duty-cycle output phases.
- The feedforward phase noise cancellation architecture employing an SSPD and analytical analysis of its performance;
  - as a stand-alone technique;
  - when reusing the SSPD in an SSPLL.

6.3 Recommendations

After the considerable improvement in power consumption and ACR in the receive chain, new bottlenecks arise. The main recommendations for future research are shortly discussed.

Since the proposed receiver front-end's power consumption is 2× lower than a state-of-the-art *LC*-based PLL, the next challenge is to further reduce the power consumption of the PLL. However, it is important to note that this should not come at an increase of phase noise, because of the very strong ACR performance.

The proposed receiver front-end has very high linearity compared to other state-of-the-art 2.4GHz IoT receivers. However, it is desirable to improve the linearity further — without increasing the power consumption — to fully benefit from the increased filtering performance.

The proposed analog FIR filter approach has shown its merits for IoT receivers. It is highly selective, low power, very flexible and is very suitable to implement in new technology nodes that have reduced digital power consumption and supply headroom. The concept has great potential and is not limited to low power receivers. It is therefore important to continue research on analog FIR implementations for other applications. Analog FIR circuits could shape the (analog) signal processing future.

List of Publications

Peer-Reviewed

[1] **B. J. Thijssen**, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "2.4GHz Highly-Selective IoT Receiver Front-End with Power Optimized LNTA, Analog FIR Filter and Frequency Divider Architecture," *IEEE J. Solid-State Circuits*, 2020, (Early Access).

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[4] **B. J. Thijssen**, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "A 0.06–3.4-MHz 92-μW Analog FIR Channel Selection Filter With Very Sharp Transition Band for IoT Receivers," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 171–174, 2019.

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Patents

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Acronyms

ACR adjacent-channel rejection

ADC analog-to-digital converter

ADPLL all-digital phase-locked loop

AFIR analog finite-impulse-response

AWG arbitrary waveform generator

B_{1dB} blocker 1dB compression point

BBD bucket-brigade device

BCCD bulk channel charge coupled device

BER bit-error-rate

BLE Bluetooth Low Energy

BNF blocker noise figure

BPF bandpass filter

CCD charge coupled device

CID charge injection device

CMFB common-mode feedback

CMOS complementary metal-oxide-semiconductor

DAC digital-to-analog converter

DC direct current, but also used to refer to the zero-frequency of a signal

DDFS direct-digital frequency systhesis

DFT discrete Fourier transform

DTC digital-to-time converter

ECG electrocardiogram

ESD electrostatic discharge

FD-SOI fully-depleted silicon-on-insulator

FET field-effect transistor

FIR finite impulse-response

FoM figure-of-merit

g_mDAC transconductance digital-to-analog converter

GFSK Gaussian frequency-shift-keying

HS-OQPSK half-sine shaped offset quadrature phase shift keying

I/Q in-phase/quadrature-phase

IDT interdigital transducer

IF intermediate frequency

IIP3 input-referred third-order intercept point

IIR infinite-impulse response

IM3 third-order modulation

IoE Internet-of-Everything

IoT Internet-of-Things

IRN input-referred noise

ISM industrial, scientific and medical

LNA low-noise amplifier

LNTA low-noise transconductance amplifier

LO local oscillator

LPF low-pass filter

LSB least-significant bit

MSB most-significant bit

MSK minimum-shift keying

NF noise figure

NFET n-channel field-effect transistor

OIP3 output-referred third-order intercept point

OOB out-of-band

OP_{1dB} output-referred 1dB compression point

PCB printed circuit board

PCCD peristaltic charge coupled device

PFD phase-frequency detector

PFET p-channel field-effect transistor

PLL phase-locked loop

PRBS pseudo-random bit-stream

PVT process voltage temperature

QFN quad-flad no-leads

RF radio frequency

rms root mean square

RX receiver

SAR successive-approximation register

SAW surface acoustic wave

SCT surface charge transistor

SFDR spurious-free dynamic range

SNR signal-to-noise ratio

SSDLL sub-sampling delay-locked loop

SSPD sub-sampling phase detector

SSPLL sub-sampling phase-locked loop

SSPNC-PLL sub-sampling phase noise cancellation phase-locked loop

TIA transimpedance amplifier

V→I voltage-to-current

V→Q voltage-to-charge

VCO voltage-controlled oscillator

ZIF zero insertion force

About the Author

Bart J. Thijssen was born in Ede, The Netherlands, in 1992. He obtained the B.Sc. degree *(cum laude)* in advanced technology and M.Sc. degree *(cum laude)* in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2014 and 2016, respectively.

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Bart Thijssen has authored six technical journal and conference papers and holds two patents. He is recipient of the "Analog Devices Outstanding Student Designer Award".