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Short-Channel Vertical Organic Field-Effect Transistors with High On/Off Ratios

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A unique vertical organic field-effect transistor structure in which highly doped silicon nanopillars are utilized as a gate electrode is demonstrated. An additional dielectric layer, partly covering the source, suppresses bulk conduction and lowers the OFF current. Using a semiconducting polymer as active channel material, short-channel (100 nm) transistors with ON/OFF current ratios up to 10^6 are realized. The electronic behavior is explained using space-charge and contact-limited current models and numerical simulations. The current density and switching speed of the devices are in the order of 0.1 A cm^{-2} and 0.1 MHz, respectively, at biases of only a few volts. These characteristics make the devices very promising for applications where large current densities, high switching speeds, and high ON/OFF ratios are required.

Organic semiconductors are attractive materials due to their flexibility, solution processibility, low cost, light weight, and they are utilized in a number of widely investigated electronic devices spanning organic light-emitting diodes, organic field-effect transistors (OFETs), organic photodetectors (OPDs), and organic photovoltaic cells.[1–5] Currently, great attention is directed toward combining these components in a single (all-) organic integrated device.[6] However, when integrated with another organic component, despite efficient operation, OFETs present architectural challenges.[7] Therefore, for integration purposes, not only the performance but also the architecture of an OFET must be critically analyzed and designed.

The performance of a transistor can be quantified by two attributes, current density and switching speed.[8] Since organic semiconductors are a low-mobility class of materials, an OFET requires a large transistor width and a short transistor channel length in order to excel in the mentioned attributes.[7–10] From the architectural perspective, in an integrated pixelated device, transistors should also have small footprints so that light-emitting/-sensing devices can occupy larger areas on each pixel. Yet for planar OFETs, the device area increases with the width and decreasing the channel length demands high-resolution patterning. A vertical geometry allows reduced area requirements by employing a submicrometer thick organic film as the transistor channel.[11,12] However, when the channel length of an OFET approaches the 100 nm regime, high electric fields result in large bulk current densities that cannot be modulated efficiently via a gate-field.[13–15] This phenomenon is known as the short-channel effect and it restricts further improvement of vertical OFETs (VOFETs).

In this report, a novel VOFET geometry is demonstrated addressing the short-channel effect, in particular by suppressing the undesired bulk current. It is based on a gate electrode consisting of massively parallel highly doped silicon nanopillars (**Figure 1**). Crucially different from other VOFETs, an insulating layer is deposited on top of the bottom contact in order to force injection of the charge carriers only from the sides of the bottom metal, and current flow within a thin layer close to the gate dielectric, minimizing space-charge limited current through the bulk semiconductor. Thanks to this unique geometry, ON/OFF ratios up to 10^6 can be realized, i.e., at least three orders of magnitude larger than in previously reported short-channel (100 nm) VOFETs.[11,15]

In order to fabricate the nanopillars with a high areal density (≈10^6 pillars mm^{-2}), optical resist dots (100 nm radius) arranged in a hexagonal lattice (250 nm lattice constant) are created using displacement Talbot lithography (DTL). It allows for fast wafer-scale patterning.[16] This resist dot pattern acts as an etch mask during etching of about 300 nm into the underlying silicon. Since the silicon is highly doped p-type (resistivity of 0.010–0.025 Ω cm), it can be directly used as a massively parallel nanopillar gate electrode for a single device (≈7×10^5 pillars per device of total size 0.7 μm^2). In our experiments, we use bulk silicon wafers, but silicon-on-insulator wafers can be used in order to electrically separate individual many-pillar devices. A stoichiometric low-pressure chemical-vapor-deposited (LPCVD) 45 nm silicon nitride (Si_3N_4) isolates these

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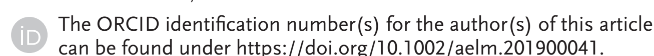
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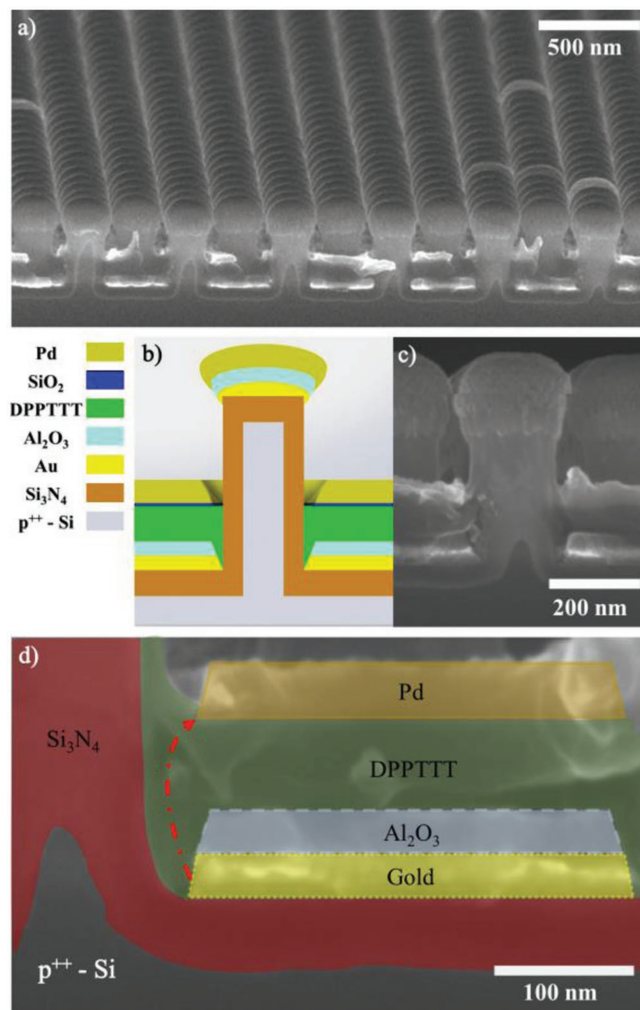

Figure 1. Fabrication of VOFETs with massively parallel nanopillars as gate. a) Overview SEM image of the nanopillars. b) Schematic representation of a single pillar gate. c) SEM image of a single nanopillar. The p-Si pillar core is not visible due to the off-center cross section. d) Zoom-in to the vertical junction next to a nanopillar gate. The red arrow schematically indicates the most likely conduction path.

pillars from the rest of the device (Figure 1a–d). LPCVD Si_3N_4 has a high relative dielectric constant (≈8), withstanding high electric fields without deterioration. After deposition of Si_3N_4 the bottom electrode is evaporated, during which material on top of the pillars accumulates, increasing the pillar radius, and causing a mushroom-like shape (Figure 1a–c). This property stimulates formation of a trapezoidal bottom contact in between the pillars (Figure 1d). Additionally, if a subsequent layer is evaporated, the enlarged top diameter causes an increased distance to the base of the pillars (see Figure 1b,c). Here, we utilize this property to our advantage and evaporate an isolating layer (25 nm Al_2O_3) onto the 25 nm gold bottom contact. As illustrated in Figure 1d, the gold surface is only exposed at the sides of the trapezoidal bottom contact. Eventually, this architecture creates a conduction path (schematically indicated by the red arrow in Figure 1d) close to the gate pillar surface, minimizing the undesired bulk current.

For the organic semiconducting layer, we use the conjugated polymer [poly-[2,5-bis(2-octyldodecyl)-3,6-di(thiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dionel-alt-thieno[3,2-b]-thiophene] (DPPTTT). This polymer is chosen because it has a high highest occupied molecular orbital (HOMO) level (5.2 eV – comparable to the work functions of Au and Pd), it is stable in air and is reported to have a reasonably high mobility of 0.1 cm^2 V^{-1} s^{-1}.[17] Before deposition of this polymer, the substrate is treated with UV/ozone and functionalized with self-assembled monolayers (SAMs) of trimethoxy(octadecyl)silane (OTS) and perfluorodecanethiol (PFDT) on the Si_3N_4 dielectric and Au surfaces, respectively. DPPTTT is spin coated on the nanopatterned wafer, resulting in a ≈60 nm thick layer on Al_2O_3, while being ≈100 nm thick around the pillars (Figure 1d). Finally, a 40 nm palladium top electrode (Pd) with a 3 nm thin intermediate layer of silicon dioxide (SiO_2) is evaporated onto the organic material. This SiO_2 layer plays a crucial role, since it forms an interlayer that blocks metal atoms and stops diffusion into the soft organic matter.[18] In addition, a sufficiently thin (2–3 nm) insulating layer between the metal and organic semiconductor stimulates Fermi-level depinning and promotes quasi-Ohmic injection of charges.[19]

The asymmetry between the electrodes and the work functions is reflected in the current density–voltage (J_D–V_{DS}) characteristics. Unless stated otherwise, the Au bottom electrode (source, S) is grounded, while a voltage is applied to the Pd top electrode (drain, D). **Figure 2**a shows the J_D–V_{DS} curve for a potential sweep between +1 V and −1 V at a gate voltage V_{GS} = 0 V. Since DPPTTT is a p-type semiconductor, injection of holes occurs from the electrode with the highest potential. For $V_{DS} < 0$ V, i.e., hole injection from the bottom, the current is much smaller than for $V_{DS} > 0$ V, due to the limited contact area of the bottom electrode. Figure 2b shows J_D–V_{DS} curves for $V_{DS} < 0$ V at different gate voltages (from +2 to −6 V). The current density does not saturate when $|V_{GS}| >> |V_{DS}|$, implying that the short-channel effect is not fully suppressed. When a gate sweep is performed for fixed $V_{DS} = -1$ V, the current density ON/OFF ratio reaches 10^6, see Figure 2c. We note that the ON/OFF ratios of several working devices (≈20) lie within the 10^4–10^6 range. For comparison, devices without Al_2O_3 insulating layer and with a thinner organic layer of 50 nm were measured as well. All devices gave ON/OFF ratios of 10^2, which clearly demonstrate the advantage of the optimized architecture. Additionally, thanks to the thin interfacial SiO_2 layer, none of the fabricated devices were shorted. The sweep rate in above measurements is 0.2 V s^{-1}, and hysteresis is observed in all measurements particularly for slower sweep rates (not shown here). We attribute this behavior to a threshold voltage shift that is caused by electrochemical reactions involving unavoidable traces of water, turning holes into protons.[20]

In order to estimate the hole mobility, a fit to the linear regime of the J_D–V_{DS} curve is performed for the following equation

$$\mu = \frac{L}{WCV_{DS}}\left(\frac{\partial I_D}{\partial V_{GS}}\right) \tag{1}$$

where μ is the mobility, W is the transistor width, L is the channel length, and C is the capacitance per unit area.[21]

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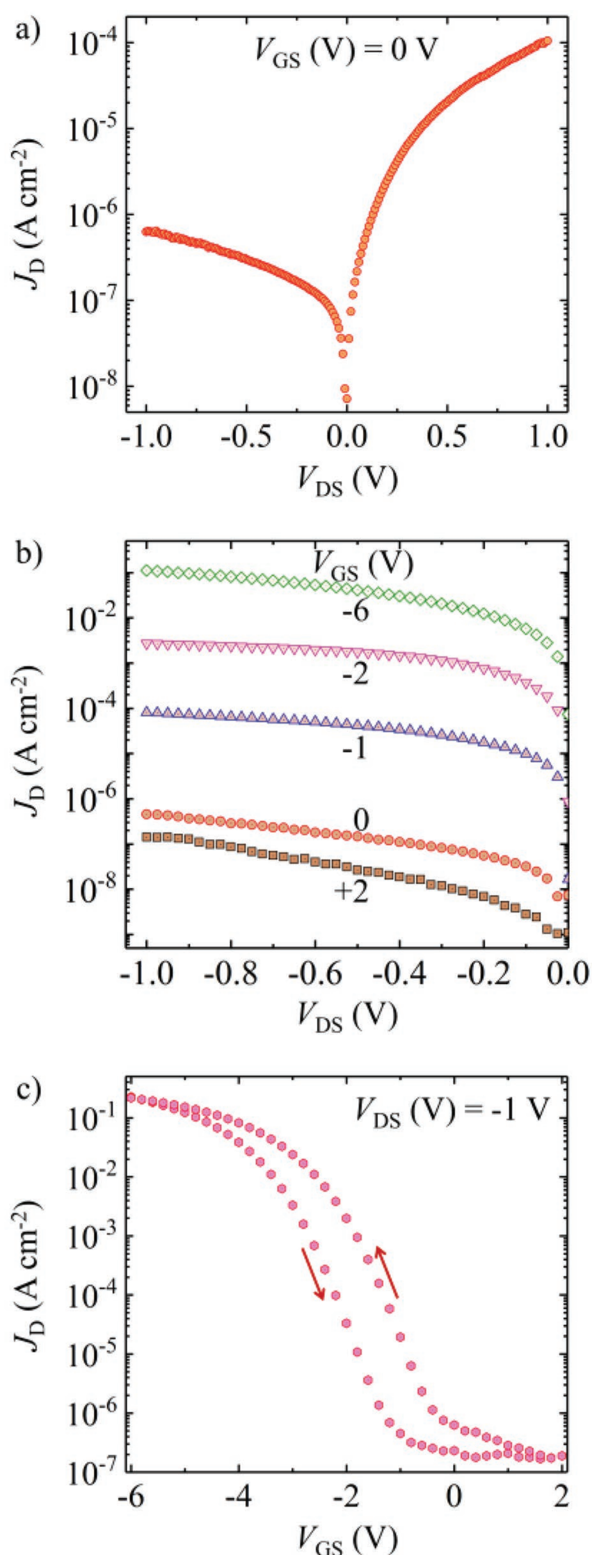

Figure 2. Transistor characteristics. a) Current density J_D for a device with an area of 0.6 mm^2 (7 × 10^6 pillar gates) is measured by sweeping the voltage applied at the top electrode while grounding the gate and bottom electrodes. b) J_D as a function of top electrode voltage V_{DS} for different gate voltages V_{GS}. c) J_D as a function of V_{GS} for V_{DS} = −1 V, for a forward (2 to −6 V) and backward (−6 to 2 V) sweep (0.2 V s^{-1} sweep rate).

The drain current I_D can be found by multiplying the current density J_D by the device area A (0.6 mm^2). The effective transistor channel width W of the total device can be extracted by multiplying the circumference of one pillar P by the number of pillars per device. The number of pillars in a single device can be found from the pillar density D and the total area A, yielding

$$W = P \times D \times A = 250\ \frac{\text{nm}}{\text{pillar}} \times 7 \times 10^6\ \frac{\text{pillars}}{\text{mm}^2} \times 0.6\ \text{mm}^2 \approx 1\ \text{m} \tag{2}$$

It should be noted that such a large width enables a high current at a small areal footprint, ergo high current density. The current contribution per pillar gate is around 3 nA. Using Equation (1) with L = 100 nm derived from the scanning electron microscope (SEM) images, and C = 132 nF cm^{-2} from the Si_3N_4 capacitance measurements, we calculate an effective mobility of $\mu = 4 \times 10^{-4}$ cm^2 V^{-1} s^{-1}.

The extracted mobility is much lower than the 0.1 cm^2 V^{-1} s^{-1} value reported in the literature for optimized long channel, planar thin-film transistors (TFTs).[17] In order to verify the extracted mobility, the J_D–V_{DS} measurements are further analyzed by fitting to the space-charge-limited-current (SCLC) model at $|V_{GS}| >> |V_{DS}|$, and to the contact-limited-current (CLC) model at V_{GS} = 0 V. The following two equations are used to fit the data in order to extract the SCLC mobility and the potential barrier at the source electrode, respectively

$$\text{SCLC}:\ J_D = \frac{9}{8}\varepsilon_0\, \varepsilon\mu \frac{V_{DS}^{\ 2}}{L^3} \tag{3}$$

where ε_0 and ε are the vacuum and relative permittivities, respectively[22]

$$\text{CLC}:\ J_D = \frac{q\mu N_0}{L} V_{DS} \exp\left[-\frac{q}{kT}\left(\varphi_b - \sqrt{\frac{q\,V_{DS}}{4\pi\varepsilon_0\varepsilon L}}\right)\right](1-\text{FF}) \tag{4}$$

where q is the elementary charge, N_0 is the effective density of localized states in the polymer in between which charge hopping takes place, k is the Boltzmann constant, T is temperature, φ_b is the potential barrier, and FF is the filling factor, which defines the percentage of the area not contributing to the conduction.

In order to fit to SCLC, an individual J_D–V_{DS} curve at V_{GS} = −6 V is used (**Figure 3**a). A mobility value of $\mu_{SCLC} = 3.3 \times 10^{-4}$ cm^2 V^{-1} s^{-1} is extracted from this fitting, where $\varepsilon = 3$ is used.[23] This value is consistent with the mobility calculated above. For the CLC fit, the filling factor must be determined. The edge of the bottom electrode next to the pillar, which is the only part contributing to the conduction, has a lateral width of 7 nm (Figure 1c). Considering that this edge is 100 nm away from the center of the pillar and that the unit area around one pillar is (270 nm)^2, 1-FF is estimated to be only 6%. Inserting this value, the estimated effective localized state density $N_0 = 10^{19}$ cm^{-3} and kT = 26 meV into Equation (3) results in a fitting that gives a barrier height of φ_b = 0.19 eV (Figure 3b).[24] This potential barrier is attributed to the difference between the work function of the SAM-modified gold and the DPPTTT HOMO level. In order to test whether the conduction is affected by the change of the contact resistance, a

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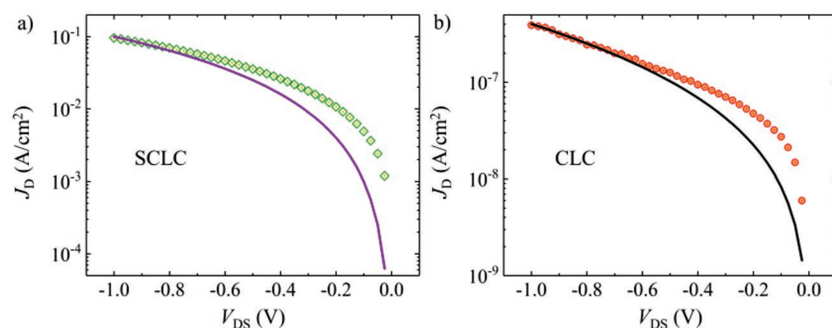

Figure 3. a) Space-charge limited current fit (purple line) to J_D–V_{DS} sweep at V_{GS} = –6 V (green diamonds). b) Contact limited current fit (black line) to J_D–V_{DS} sweep at V_{GS} = 0 V (orange circles), yielding a barrier height of φ_b = 0.15 eV.

vertical device without pillars is produced. The current density stayed constant (not shown here) irrespective of the gate voltage applied to the substrate, confirming that the field-effect mechanism (channel resistance) is responsible for the gate response. Additionally, the approximate channel length is extracted from this fit to be $L \approx 95$ nm.

Measurements and fittings consistently show that the mobility of the devices is far lower than expected. The interface between the dielectric layers and the semiconductor or the morphology of the polymer could cause this large deviation. First, the untreated dielectric materials (Si_3N_4 and Al_2O_3) have high surface energy and contain trapped charges.[25] The OTS SAM, used in this study, might be insufficient to diminish this reactive nature of the insulators. Second, fibers within the spun polymer tend to form π–π stacking along the in-plane direction, while the conduction occurs in the vertical (out-of-plane) direction.[17] In other words, anisotropy in the mobility could occur as a result of horizontally lying polymer fibers. Lastly, the top interfacial layer of SiO_2 could be degrading the organic semiconductor. Even though the high evaporation rate (0.5 nm s^{-1}) is used to minimize intercalation into the polymer, there could be a diffuse interface that decreases the overall mobility.[26] Additionally, e-beam evaporation of SiO_2 results in oxygen vacancies in the eventual composition, forming a defective SiO_x (x = 1.9) layer, which could introduce charge traps for the organic polymer.[27] A different combination of SAM, polymer, and insulators could possibly improve the device performance. We stress, however, that although the mobility is lower than expected, this does not impair the main result of this paper, which is the high ON/OFF ratio facilitated by the suppression of the bulk current.

Although the bottom electrode is partly covered with an insulating layer, the top electrode still has a large contact area with the organic material. This means that the charges can be injected from anywhere along the top electrode, unlike for the bottom electrode, where only the edges are available for injection. Additionally, the top electrode is further away from the pillars due to the shadowing effect of the mushroom-topped pillars, which causes the trapezoidal contact formation. Considering these two features, gate manipulation of the charges that are injected from the top electrode is expected to be difficult. This effect can be observed when the polarity of the device is reversed (**Figure 4**).

For a device different from the one shown in Figures 2 and 3, Figure 4a shows the J_D–V_{DS} curves for opposite polarities. While the accumulation at $V_{GS} < 0$ affects both cases similarly, injection from the bottom electrode allows better control during depletion at $V_{GS} > 0$. This is a consequence of the different contact areas and the different distances of the contacts to the pillar. Simulations for a simple geometry with the device simulation software ATLAS are performed in order to confirm this finding.[15] Figure 4b–e shows how the hole concentration is affected by the gate for different polarities. When charges are injected into the polymer from the bottom contact through a small window adjacent to the gate electrode, the overall concentration can be decreased drastically when a positive gate voltage is applied (Figure 4c). However, for the opposite case, charges are distributed more evenly in the polymer since there is a much larger injection area. Figure 4e clearly shows that the concentration within the polymer stays high even when a positive gate voltage is applied.

For the fabricated 100 nm short-channel VOFET devices, switching speed measurements were also performed. The setup for these measurements is shown in **Figure 5**a. Square voltage pulses between 0 and –6 V with a switching time of 5 ns were applied to the gate electrode for 1 ms with a repetition of 2 ms and a top electrode voltage of –1 V (Figure 5b). The amount of current that is drawn from the source is converted into a voltage through a 270 Ω resistor and measured with an

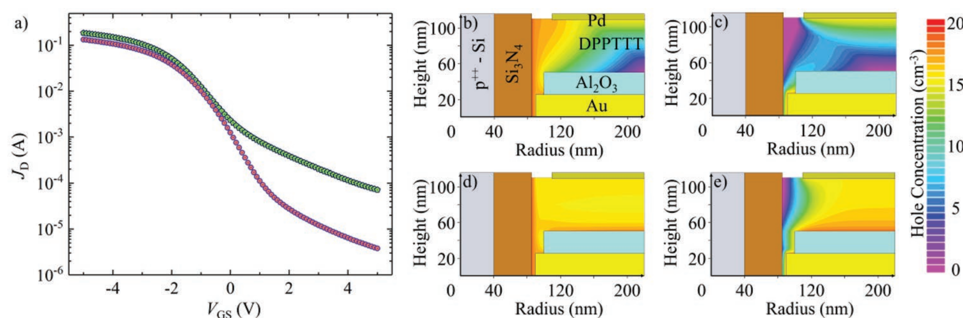

Figure 4. a) J_D–V_{GS} curves for opposite polarities. Bottom injection: bottom electrode is grounded (purple circle). Top injection: top electrode is grounded (green diamonds). b,c) Simulated hole concentrations for bottom injection, $V_{GS} \ll 0$ and $V_{GS} \gg 0$, respectively. d,e) Simulated hole concentrations for top injection, $V_{GS} \ll 0$ and $V_{GS} \gg 0$, respectively.

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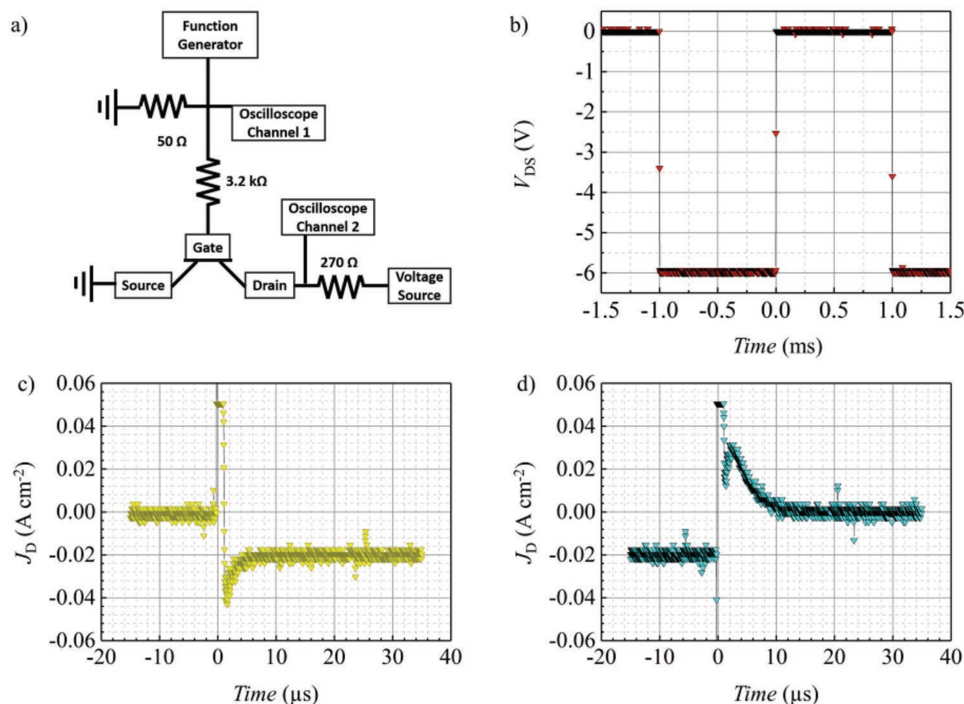

Figure 5. Switching characteristics. a) Circuit diagram of the setup that is used to obtain the switching times. b) Input signal. c) Transistor switch-on plot. The rise time is around 5 µs. d) Transistor switch-off plot. The fall time is around 10 µs.

oscilloscope. Switch-on and switch-off responses are plotted in Figure 5c,d. Measured rise and fall times (time it takes for the signal to saturate/flatten) are ≈5 and 10 µs, respectively, which translates into 0.2 and 0.1 MHz switching speeds. The contrast between the switching times stems from the difference in accumulation mechanisms. For the rise time, the gate field directly attracts charges to the dielectric surface, while for the fall time charges relax into the bulk material in the absence of any field. Even though the mobility is low (≈10^{-4} cm^2 V^{-1} s^{-1}), the switching speeds are approaching the MHz range. Considering that switching speed directly scales with mobility, higher switching speeds are expected when higher mobilities are realized. Additionally, the parasitic capacitance between bottom electrode and the silicon substrate might also be affecting the transit frequency. Reduction of this capacitance would require a thicker insulating layer between the source and the gate contacts.

In this report, the substrate is a silicon wafer and the fabrication flow starts with a well-established silicon machining process. Therefore, all of the considered steps are designed and applicable for large-area production on silicon. With proper materials selection, it could be possible to produce this type of VOFETs on conducting organic substrates (or organic-coated glass substrates) instead of highly doped silicon wafers. However, there are multiple steps where analogous methodologies for organic processing are yet to be established. For instance, fabrication steps that involve developers and solvents should not damage the organic substrate. Additionally, the high-temperature LPCVD process should preferably be replaced with an alternative method such as room-temperature spatial atomic layer deposition.[28] Therefore, several advancements are needed in order for this technology to allow fabrication on organic substrates.

In conclusion, we have shown that nanopillar gates and evaporation of an insulating layer on top of the bottom electrode makes fabrication of VOFETs with 100 nm channel length feasible. The insulating layer allows high ON/OFF ratios up to 10^6 even for such short channel lengths since it decreases the overall bulk current. Despite the low effective field-effect mobility in the present device, switching speeds approaching the MHz range are measured, made possible by the short transistor channel length. In addition, ON currents can reach up to mA range for device areas less than 1 mm^2, which equals to a current density of 0.1 A cm^{-2}. These results suggest a promising pathway for future integrated light-emitting/-sensing VOFET devices where short-channel effects are minimized while maintaining functional device characteristics.

Experimental Section

Device Fabrication: The fabrication started with a heavily doped p-type wafer (0.010–0.025 Ω cm). The wafer was spin coated with Bottom Anti Reflective Coating (BARC, AZ BARLi-II 200, 3000 rpm, 45 s, baked at 185 °C for 1 min), after which PFI-88 diluted in 1:1 propylene glycol monomethyl ether acetate was spin coated (4000 rpm, 45 s, baked at 95 °C for 1 min). The wafer was first exposed to EVG 620 with 60 mJ cm^{-2} to define 2.5 × 5 mm^2 areas that were separated by 1 cm. Immediately after this, DTL exposure was performed twice (the second exposure was performed after the wafer was rotated by 60°) in Eulitha PhableR 100C using a phase-shift line mask with 500 nm periodicity. Exposure parameters are Energy = 75 mJ cm^{-2}, DTL range-gap = 3–65 µm, target cycle = 20 s with 1 precycle. A postexposure bake was done at 120 °C for 2 min. The resist was developed in OPD

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4262 for 1 min. First, the underlying BARC was etched using home-built directional reactive ion etching (50 sccm N_2, 25 Watt, 10 mTorr, 340 V_{DC}). Before the silicon was etched, the wafer was dipped into buffered hydrofluoric acid for 30 s. Silicon etching was performed in a commercial Oxford Instruments PlasmaPro 100 Estrelas machine (35 s, 40 sccm C_4F_8, 35 sccm SF_6, inductively coupled plasma (ICP) power 800 W, high-frequency (HF) power 35 W, 22 mTorr). After this process, the resists were stripped and the wafer was cleaned in 99% HNO_3 at 20 °C and 69% HNO_3 at 95 °C. 45 nm stoichiometric LPCVD Si3N4 was deposited in an Amtech Tempress furnace (800 °C, 22 sccm SiH_2Cl_2, 66 sccm NH_3, 200 mTorr, 9 min). The bottom electrode materials were evaporated through a shadow mask (1×2.5 mm^2) in a Balzers BAK 600 E-beam evaporator (successively 10 nm Al_2O_3, 2 nm Cr, 25 nm Au, and 25 nm Al_2O_3). After that, the chips were cut to 1×1 cm^2 and cleaned in UV/ozone for 5 min. A monolayer of OTS was vapor deposited on the surface at 100 °C for 30 min in a desiccator. A self-assembled monolayer of PFDT was deposited on the Au contact by dipping the chips in a 3×10^{-3} M isopropanol (IPA) solution for 15 min. After the chips were rinsed, DPPTTT was spin coated (1000 rpm) using a 10 mg mL^{-1} dichlorobenzene solution that was stirred at 120 °C for 2 h. Finally, 3 nm SiO_2 and a 40 nm Pd top electrode were (successively) deposited through shadow mask using the BAK evaporator.

Device Characterization (DC): DC measurements were performed using Keithley 2400 and 2401 sourcemeters. The gate capacitance was measured with a Tenma 72–7732A multimeter by connecting the top and bottom electrodes to one end while connecting the gate to the other end of the multimeter. The measured capacitance was divided by the total overlapping area of the electrodes with the Si_3N_4 gate dielectric to obtain capacitance per unit area (C). For switching speed measurements, a Tenma 72–8690 power supply, an Agilent 33250A Function Generator, and a Keysight DSOX2004A Oscilloscope were used. All measurements were performed in dark and vacuumed chamber.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

organic electronics, polymer semiconductors, short-channel effects, vertical organic field-effect transistors

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