A Baseband-Matching-Resistor Noise-Canceling Receiver With a Three-Stage Inverter-Only OpAmp for High In-Band IIP3 and Wide IF Applications

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***Abstract*—In this article, we propose a baseband noise-canceling receiver architecture to increase in-band linearity. A key feature of the architecture is that all active circuits are in baseband, including the low-noise transconductance amplifier (LNTA). The LNTA operating at baseband frequencies allows the use of feedback to increase the linearity. This article analyzes a tradeoff that exists between in-band linearity and noise in mixer-first receivers and shows how the proposed architecture breaks such tradeoff. The receiver targets high IF bandwidths, enabled by a transimpedance amplifier (TIA) composed of an OpAmp using only inverters. This article describes the stabilization mechanism of this OpAmp with a unity-gain bandwidth (UGB) of 7.6 GHz. The receiver is fabricated in 22-nm FDSOI CMOS. The measured results show an in-band IIP3 of > 9 dBm for an IF bandwidth of 175 MHz with sub-5-dB noise figure (NF) across 1–6-GHz local oscillator (LO) frequencies.**

***Index Terms*—Base station, high unity-gain bandwidth (UGB), in-band linearity, inverter-only OpAmp, low-noise transconductance amplifier (LNTA), noise-canceling, stabilization, transimpedance amplifier (TIA), wideband IF.**

I. Introduction

RECENTLY, increasing in-band linearity has become an important focus in many sub-10-GHz receiver applications, mainly those where the band of interest may contain many signals, such as cognitive radio [1], base station applications [2], and intraband carrier aggregation scenarios [3]. Other emerging areas where high in-band linearity is necessary include self-interference cancellation for in-band full-duplex receivers with significant cancellation in the digital domain [4], [5] and MIMO applications involving beamforming that takes place (partly) in the digital domain [6].

Most of the abovementioned applications are increasingly targeting higher IF bandwidths, mainly driven by higher data-rate demands. For instance, Jiang *et al.* [1] targeted high IF bandwidth for cognitive radio and 5G wireless applications. Pini *et al.* [7] also aimed at high IF bandwidth for 5G bands below 6 GHz. Similarly, works on base-station receiver designs [8], [9] have targeted high IF bandwidth to support all 3GPP bands.

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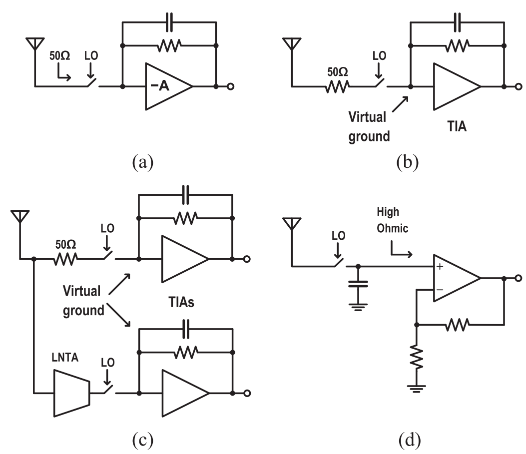


Fig. 1. Representative mixer-first receiver architectures (a) [10], (b) [2], (c) [12], and (d) [13] for comparing their in-band linearity along with noise, matching, and OoB linearity performances.

Therefore, receivers with both high in-band linearity and wide IF-bandwidth are desired for many applications. It is also desired that other receiver performances, such as noise figure (NF), out-of-band (OoB) linearity, and input matching, are not degraded.

To achieve high linearity, mixer-first topologies have been popular, as they can postpone voltage swing to the end of the receive chain. A few of those architectures are shown in Fig. 1.

Receivers as in Fig. 1(a) ([10], [11]) generally rely on the impedance at the input of the baseband amplifier [$-A$ in Fig. 1(a)] for input matching to achieve low NF. There will be significant swing at the input of the baseband amplifier in these receivers. Hence, such receivers trade-off in-band linearity for low NF. The topology in Fig. 1(b) [2] is a good choice for high in-band linearity due to the virtual ground at the input of the transimpedance amplifier (TIA). However, it is more noisy due to the 50-Ω matching resistor. The receiver shown in Fig. 1(c) [12] achieves virtual ground at the input of the TIAs and also cancels the noise of the matching resistor. However, the low-noise transconductance amplifier (LNTA) operating at RF frequencies either limits the input matching or the linearity. Fig. 1(d) [13] is another good choice to increase in-band linearity because of the virtual short between the inputs of the baseband amplifier. However, due to its lack of input matching, it is not practical in many applications.

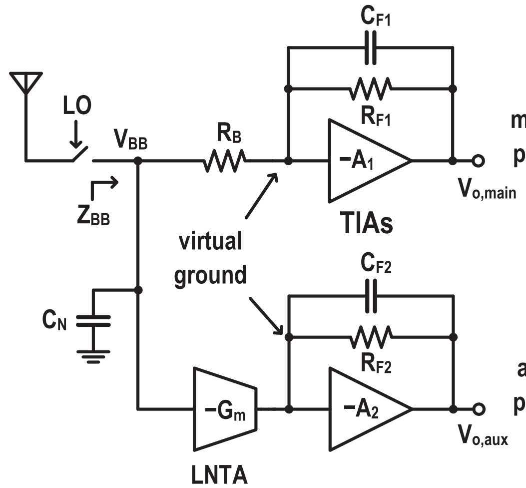


Fig. 2. Proposed baseband-matching-resistor noise-canceling receiver architecture.

In [14], we proposed a baseband noise-canceling (BBNC) receiver architecture targeting both high in-band linearity and high IF bandwidth without compromising on other performances, such as NF, OoB linearity, and input matching. Compared with [14], in this article, we provide a more detailed analysis of the various properties of the architecture, as well as more mathematical analysis and design guidelines. We also provide analysis and design guidelines for the 7.6-GHz unity-gain bandwidth (UGB) three-stage inverter-only OpAmp.

The rest of this article is organized as follows. The proposed receiver architecture is presented and briefly described in Section II. In-depth analysis of the various properties of the architecture and tradeoffs is given in Section III. Section IV shows the full circuit implementation and circuit design details. This section also includes prior art on wideband TIA design and a detailed analysis of the three-stage inverter-only OpAmp. Section V deals with the experimental results and comparison with prior art. Section VI concludes this article.

II. Architecture

The proposed receiver is shown in Fig. 2. It is a noise-canceling architecture with the feature that all active circuits operate in baseband, including the LNTA. Input matching is provided by R_B, whose impedance is frequency translated to the input by the passive mixer. Both the TIAs have virtual ground at their input.

The proposed receiver achieves higher in-band linearity mainly because of the virtual ground at the input of the TIAs and the LNTA operating in baseband. The virtual ground at the input of the TIAs not only reduces the swing at their inputs but also allows the loop gain to be > 1 unlike in the case of the architecture shown in Fig. 1(a). Higher loop gain further reduces the distortion produced by the TIAs.

Furthermore, operating the LNTA in baseband enables the use of feedback to achieve the desired linearity. Feedback not only increases the linearity of the LNTA but also makes the linearity robust to process, voltage, and temperature (PVT) changes. Most RF LNTAs do not have this luxury such that they dominate the overall non-linearity, with linearization

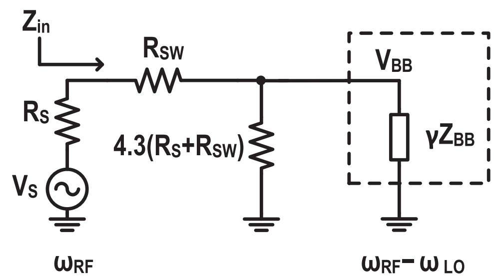


Fig. 3. Simplified circuit model for mixer-first receiver analysis [11], [16].

techniques suffering from variation across PVT as explained in [15].

The N-path filter formed by the source impedance and the capacitor C_N rejects OoB interferers. Unlike [12], where the LNTA operates at RF, the input capacitance of the LNTA only (slightly) affects the bandwidth of the N-path filter and hence does not degrade input matching at high frequencies. Also, it is a noise-canceling architecture where the noise of the matching resistor R_B is canceled by an auxiliary path containing an LNTA with transconductance G_m. We analyze all the properties in greater detail in Section III.

III. Architecture Analysis

Fig. 3 shows a circuit model for mixer-first receivers mainly simplifying the frequency translation effects of the mixer switches in the receiver analysis [11], [16]. This model greatly simplifies the analysis of input matching, noise, and conversion gain. Note that Z_{in} is the input impedance in the RF domain, which has to be matched to 50 Ω. Z_{BB} inside the dashed box is the same as Z_{BB} in Fig. 2, which is the impedance toward the baseband part of the mixer switches. Similarly, the voltage V_{BB} inside the dashed box represents the downconverted voltage on the baseband part of the mixer switches. The value of γ in Fig. 3 depends on the number of paths and mixer switch duty cycle and is approximately 0.2 for the four paths, 25% we will use here. Similarly, $4.3(R_S + R_{\text{SW}})$ models the shunting impedance (Z_{sh} in [16]) for this case.

A. Input Matching

To simplify the input matching analysis, Fig. 3 can be rewritten as shown in Fig. 4(a), considering only the resistive part (R_{BB}) of the Z_{BB}. Since the input of the auxiliary path (LNTA) in Fig. 2 is capacitive and only visible out-of-band, only the main path is considered as shown in Fig. 4(b) to calculate R_{BB}. The effect of the reactive part of Z_{BB} is studied later in Section III-D. Also, the switch resistance R_{SW} is neglected since its value is designed to be low because its noise cannot be canceled. Nevertheless, switch resistance is considered later for noise analysis.

The analysis starts with the matching resistance R_{in} that should be equal to 50Ω. Then, R_{BB} should be [17]

$$R_{\text{BB}} = \frac{4.3}{3.3} \times \frac{R_s}{\gamma} \tag{1}$$

where R_S is 50 Ω and γ is approximately 0.2 for four-path filtering. Also, from Fig. 4(b), R_{BB} can be written as

$$R_{\text{BB}} = R_B + R_v \tag{2}$$

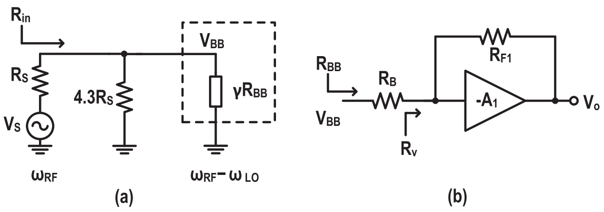


Fig. 4. (a) Circuit model for input matching. (b) Circuit to calculate R_{BB}.

where

$$R_v = \frac{R_{F1}}{1 + A_1}. \tag{3}$$

Thus, from (2), it is a design freedom how to distribute R_{BB} between R_B and R_v.

Furthermore, from (3), it appears that for a chosen value of R_v, there are multiple sets of values of R_{F1} and A_1 available as design freedom. However, there is an additional design constraint coming from the required conversion gain from the antenna input to the output of the TIA, which generally feeds the ADC. It can be seen from Fig. 4(a) that the conversion gain from V_S to V_{BB} is a constant since R_{BB} is fixed. If the gain from V_{BB} to V_O as shown in Fig. 4(b) is fixed to $-A_0$, it can be written as

$$\frac{V_O}{V_{\mathrm{BB}}} = -\frac{R_v \times A_1}{R_B + R_v} = -A_0. \tag{4}$$

Since $R_B + R_v$ is fixed due to matching constraint (2), $R_v \times A_1$ also becomes fixed due to gain constraint (4). Hence, only one of R_B, R_v, $-A_1$, or R_{F1} becomes an independent variable as varying one of them fixes the value of the others. R_v is chosen here as the independent variable for the forthcoming analysis as it appears in all the three equations, i.e., (2)–(4).

B. In-Band Linearity

The value of R_{BB} can be calculated to be 321 Ω from (1) for four-path filtering. Hence, R_v can be varied from 321 to 0 Ω according to (2) while varying R_B by the same amount in the other direction. The equation to calculate noise factor from [17] is rewritten as follows to analyze the variation of NF when R_v is varied from 321 Ω to 0 Ω:

$$F = 1 + \frac{R_S}{4.3 \times R_S} + \frac{R_B \times R_S}{\gamma \times {R_{\mathrm{BB}}}^2}. \tag{5}$$

Note that to simplify the analysis, noise due to only R_B of total R_{BB} is considered in (5) as the noise due to R_v [equivalently noise due to R_{F1} in Fig. 4(b)] can be made negligible as illustrated in [17]. Also, $-A_1$ is assumed to be noiseless and the assumption that R_{SW} is zero is continued.

Now, the variation in R_v from 321 to 0 Ω results in an NF variation from 0.9 to 3 dB, as shown in Fig. 6. Hence, most mixer-first architectures as in Fig. 1(a) depend on achieving $R_v = 321$ Ω to achieve low NF [11]. However, this is not the optimal choice for in-band linearity, as we will show next.

Consider the I^+ slice of Fig. 5(a) which is the main path of the architecture in Fig. 2. To understand the effect of different values of R_v on in-band linearity, the loop gain T_0 (of the TIA with amplifier $-A_1$) will be formulated as a function of R_v. For this, R_{ES} in Fig. 5(a) is determined first.

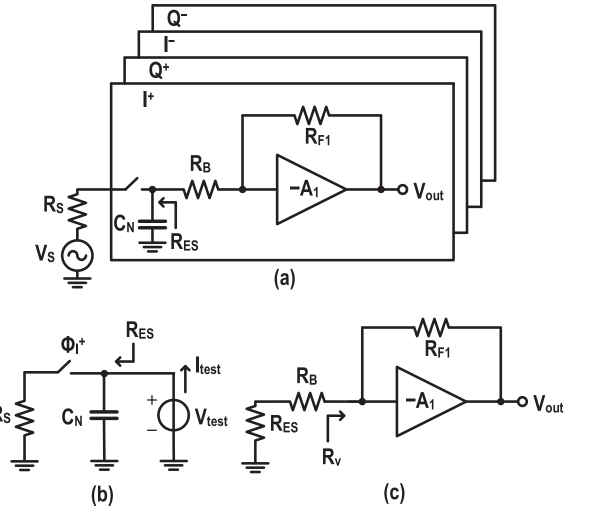


Fig. 5. (a) I^+ slice of Fig. 2 to calculate R_{ES}. (b) Equivalent circuit to evaluate R_{ES}. (c) Circuit model to analyze loop gain.

R_{ES} can be evaluated using the circuit in Fig. 5(b) following similar steps as in [2]. R_{ES} is obtained from calculating the average current I_{test} for the applied dc voltage V_{test}. ϕ_{I^+} represents the local oscillator (LO) signal that controls the mixer switch in the I^+ path. Since both the switching frequency of ϕ_{I^+} and -3-dB frequency due to $R_S C_N$ are higher than the in-band frequencies of interest, R_{ES} evaluated at dc can be used for all in-band frequencies. For 25% duty cycle ϕ_{I^+}, average I_{test} is equal to $V_{\mathrm{test}}/4R_s$, resulting in $R_{\mathrm{ES}} = 200$ Ω.

Now, considering Fig. 5(c), the loop gain T_0 of the TIA can be calculated as

$$T_0 = A_1 \left(\frac{R_{\mathrm{ES}} + R_B}{R_{\mathrm{ES}} + R_B + R_{F1}} \right) \tag{6}$$

which can be rewritten using (2)–(4) in terms of constants and the independent variable R_v as

$$T_0 = \frac{A_0 R_{\mathrm{BB}}}{R_v} \times \left(\frac{R_{\mathrm{ES}} + R_{\mathrm{BB}} - R_v}{R_{\mathrm{ES}} + R_{\mathrm{BB}} + A_0 R_{\mathrm{BB}}} \right). \tag{7}$$

Fig. 6 shows the graph of T_0 as a function of R_v for $A_0 = 10$. It can be observed that T_0 increases with the decreasing of R_v. The higher the loop gain T_0, the higher the in-band linearity will be, since the coefficients[1] of the nonlinear terms in the polynomial defining the nonlinear transfer function are suppressed by the loop gain T_0 [18], [19]. Thus, a lower value of R_v leads to higher in-band linearity. Note that this increase in in-band linearity generally comes at the cost of power, since according to (4), the gain A_1 has to be increased to obtain lower R_v.

Thus, a clear tradeoff between NF and in-band linearity can be observed for the mixer-first architecture of the form in Fig. 1(a), given the matching and conversion gain constraints. However, the noise-canceling architecture proposed in Fig. 2 breaks this tradeoff. Since high in-band linearity is

[1]The coefficients of the polynomial defining the nonlinear transfer function may also depend on the loop gain T_0 depending on the implementation of $-A_1$.

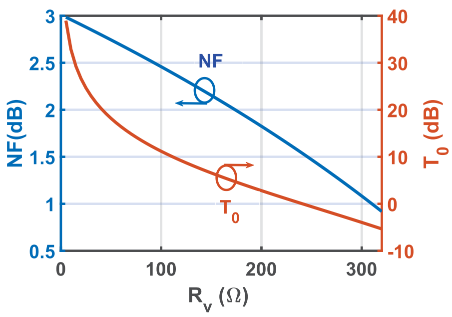


Fig. 6. NF and loop gain T_0 as a function of R_v.

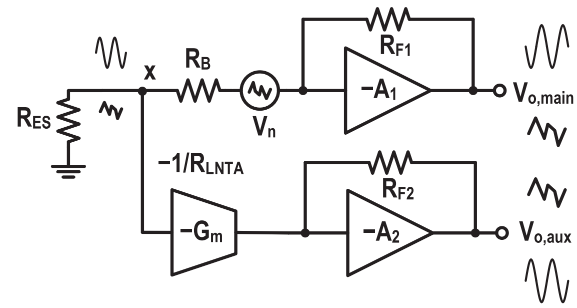


Fig. 7. Circuit to illustrate noise-canceling mechanism of R_B.

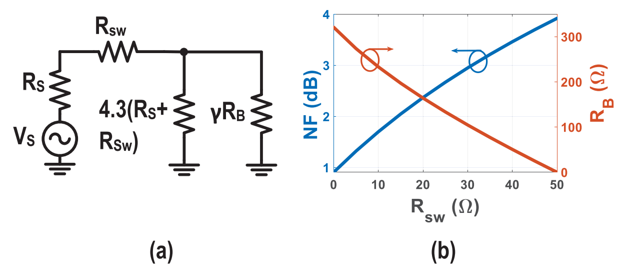


Fig. 8. (a) Circuit model and (b) plot to include R_{SW} effect on NF and R_B.

targeted in this work, a low R_v value is required, which gives rise to degraded NF performance in the main path because all matching resistance must be provided by R_B. However, the auxiliary path cancels this noise, breaking the tradeoff.

The analysis above also holds for the TIA in the auxiliary path. However, since the output resistance of the LNTA is generally higher than the feedback resistance of the TIA, loop gain in the auxiliary path is >1 in most cases and hence linear.

The LNTA is another block that can limit the linearity of receivers, especially LNTAs operating at RF frequencies such as the one in Fig. 1(c). In Section IV-A, about the circuit design, we will show that because the LNTA can work in baseband in our topology, we can use more feedback for higher linearity.

C. Noise

Consider Fig. 7 to analyze the noise-canceling mechanism. Since the receiver is designed for high in-band linearity, virtual ground is assumed at the input of the TIAs. The noise voltage of matching resistor R_B is represented by the voltage source V_n. Signal voltage and noise due to V_n are pictorially represented at node x and the output of main and auxiliary path. It can be seen that the noise voltages at the output of both paths are in phase, while the signal voltages are out of phase. The condition for noise canceling of the matching resistor R_B is

$$V_n \times \frac{R_{F1}}{R_{\mathrm{ES}} + R_B} = V_n \times \frac{R_{\mathrm{ES}}}{R_{\mathrm{ES}} + R_B} \times \frac{R_{F2}}{R_{\mathrm{LNTA}}} \tag{8}$$

which can be simplified to

$$\frac{R_{F1}}{R_{\mathrm{ES}}} = \frac{R_{F2}}{R_{\mathrm{LNTA}}}. \tag{9}$$

The different resistors in (9) also impact various other specifications of the receiver. As calculated in Section III-B, R_{ES} is fixed by R_S. It will be shown in Section IV-A that R_{LNTA} is chosen to obtain low noise in the LNTA. The resistor R_{F1} determines the gain of the main path. In this design, R_{F2} is adjusted to satisfy (9). The choice of R_{F2} also sets the gain of the auxiliary path. Note that R_{ES} depends on external R_S and does not follow the rest of the on-chip resistors in (9) across PVT variations. However, to simplify the design, calibration circuits are not included since a significant noise cancellation is obtained even without such fine-tuning.

To include the effect of switch resistance R_{SW} on noise, Fig. 4(a) is rewritten as shown in Fig. 8(a). The resistance R_{BB} is approximated to R_B in this model since a low R_v is chosen for high in-band linearity. Note that the R_B also depends on R_{SW} due to the input matching constraint

$$R_B = \frac{4.3}{\gamma} \frac{\left(R_S{}^2 - R_{\mathrm{SW}}{}^2\right)}{3.3 R_S + 5.3 R_{\mathrm{SW}}}. \tag{10}$$

Assuming that the noise due to R_B can be canceled, the effect of R_{SW} on noise factor F can be calculated from [17] as

$$F = \left(1 + \frac{R_{SW}}{R_S}\right)\left(1 + \frac{1}{4.3}\right). \tag{11}$$

Fig. 8(b) shows the plot of NF and R_B for R_{SW} between 0 and 50 Ω. It can be observed that NF increases from 0.9 to 3.9 dB in this range. R_{SW} of 8Ω is chosen in this work. This value guarantees $<$1.5-dB NF when R_B noise is canceled. R_{SW} is not decreased beyond this point as this would degrade input matching at higher frequencies due to parasitic capacitances. Moreover, there are other sources of noise, such as the LNTA and the TIAs.

D. N-Path Filtering and Conversion Gain

The N-path filtering and conversion gain of Fig. 2 are analyzed as follows. First, the transfer function of the down-conversion of the antenna voltage to V_{BB} is calculated, and then, the transfer functions from V_{BB} to both the outputs ($V_{o,\mathrm{main}}$ and $V_{o,\mathrm{aux}}$) are analyzed. Since the UGB of $-A_1$ is high, a virtual ground can be assumed at its input at near-out-of-band frequencies. Hence, Z_{BB} in Fig. 2 is a parallel combination of R_B and C_N.

Consider Fig. 3 to calculate $V_{\mathrm{BB}}(s)/V_S$. For this, the voltage transfer from V_S to the voltage across γZ_{BB} is determined first, and then, the resulting transfer is multiplied by $1/(4\gamma)^{1/2}$ to include the downconversion effect [11]. To simplify the

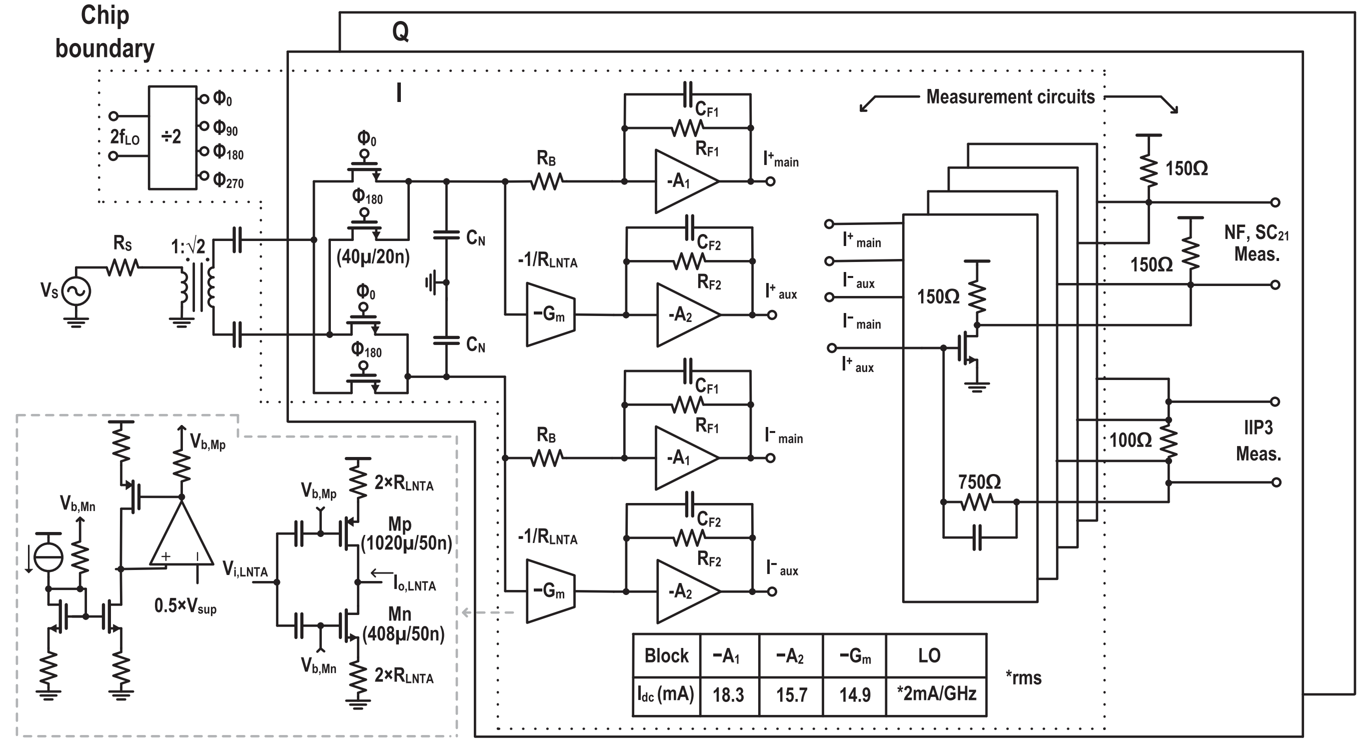


Fig. 9. Circuit implementation of the BBNC receiver.

analysis, R_{SW} is assumed to be zero, as a small R_{SW} is chosen in the design and has little effect in this calculation.

Now, $2 \times V_{BB}(s)/V_S$ can be written as [11], [16]

$$\frac{V_{BB}(s)}{V_S/2} = \frac{4.3\sqrt{\gamma}\,R_B}{\left(4.3R_S + 5.3\gamma\, R_B\right)\left(1 + \frac{s(4.3/5.3)R_S R_B C_N}{(4.3/5.3)R_S + \gamma\, R_B}\right)}. \quad (12)$$

Since the above transfer function from RF source voltage to baseband side of the mixer switches is a first-order low pass in nature, the bandpass N-path filter formed at the RF side of the mixer switches is second order in nature. Note that the dc gain of (12) is 0.9 dB and the pole is a parallel combination of the resistors R_S, $4.3R_S$, $\gamma\, R_B$, and capacitor C_N/γ.

Now, again assuming virtual ground at the inputs of $-A_{1,2}$ (in Fig. 2) at near-out-of-band frequencies, it can be observed that the transfer functions from V_{BB} to output of the main ($V_{o,\mathrm{main}}$) and auxiliary ($V_{o,\mathrm{aux}}$) paths are also first-order low pass in nature with poles due to TIAs at $1/R_{F1}C_{F1}$ and $1/R_{F2}C_{F2}$, respectively.

Thus, the transfer functions of the overall conversion gain from RF voltage to output voltages of both main and auxiliary paths are second-order low pass in nature. Also, note that both the poles, i.e., N-path pole and TIA pole are at real frequencies. In this work, to simplify the design, TIA poles are designed at 200 MHz and the N-path filter pole is placed at a sufficiently higher frequency of 475 MHz such that N-path filter pole does not strongly affect the overall IF bandwidth (175 MHz) of the receiver.

IV. Circuit Design and Implementation

Fig. 9 shows the circuit implementation of the proposed receiver in a 22-nm FDSOI CMOS process. An external balun with $1:\sqrt{2}$ turns ratio is used to convert the single-ended RF input source into 100-Ω differential input of the receiver. Mixer switches are driven by a 25% duty-cycled clock operating at the LO frequency. On-chip amplifiers (to obtain square wave), ÷2, and 25% duty cycle generation circuits are used to generate such waveforms from a differential sinusoidal clock input operating at twice the LO frequency [20]. Fig. 9 also shows circuits to measure noise and linearity separately, which will be explained in Section V-A.

A. LNTA

As mentioned in Section III-B, LNTAs operating at RF frequencies can limit the linearity of the receivers. In this section, this limitation is explained and illustrated in the context of the source-degenerated inverter used as LNTA in this work.

Consider the LNTA shown in Fig. 10(a). For simplicity, let the matching be provided by the R_S shown. The value of R_{LNTA} ($2 \times R_{\mathrm{LNTA}} = 13\ \Omega$) is chosen such that noise due to R_{LNTA} does not dominate the NF of the receiver. For a source-degenerated inverter, the $g_m R_{\mathrm{LNTA}}$ product indicates the amount of feedback, where $g_m = g_{m,Mp} + g_{m,Mn}$ in the circuit considered. From [19], P_{IIP3} of the LNTA increases by increasing the $g_m R_{\mathrm{LNTA}}$ product. In this simulation, $g_m R_{\mathrm{LNTA}}$ is increased by impedance scaling g_m, i.e., scaling the width of the transistors and current through the transistors together. Increasing g_m also leads to higher capacitance at the input of the LNTA, which will degrade input matching and lower the −3-dB corner frequency ($\omega_{-3\ \mathrm{dB}}$) for the transfer function V_i/V_s. Note that the effect of C_{gs} of the input transistor on $\omega_{-3\ \mathrm{dB}}$ becomes constant with increase in $g_m R_{\mathrm{LNTA}}$ product

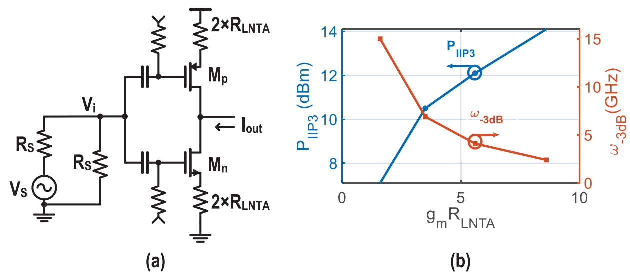


Fig. 10. (a) Simulation setup of source-degenerated LNTA operating at RF considered to demonstrate (b) tradeoff between P_{IIP3} and $\omega_{3\text{ dB}}$ as a function of $g_m R$ product.

due to the degeneration; however, the effect of C_{gd}, which is approximately half of that of C_{gs} in saturation region, increases.

Fig. 10(b) shows P_{IIP3} and $\omega_{-3\text{ dB}}$ as a function of the $g_m R_{\text{LNTA}}$ product. The tradeoff between P_{IIP3} and $\omega_{-3\text{ dB}}$ can be clearly observed. Hence, operating LNTA in baseband as proposed in this work (see Fig. 2) breaks this tradeoff and allows for various feedback-based architectures for LNTA to not only to increase linearity but also make them robust across PVT, which is not possible in architectures that do not have feedback [15].

The transistor length is chosen at 50 nm for the above simulation. The length is not decreased below this, even though a lower length improves $\omega_{-3\text{ dB}}$ for a given $g_m R_{\text{LNTA}}$ product as it also degrades P_{IIP3} due to short-channel length effects.

Fig. 9 shows the LNTA and its replica bias circuit implemented in this design. $2 \times R_{\text{LNTA}}$ is chosen to be 13Ω for low-noise performance. A g_m $(g_{m,Mp} + g_{m,Mn})$ value of 500 mS $(g_m R_{\text{LNTA}} \approx 3.2)$ results in an IIP3 of 9 dBm. Note that g_m is not increased beyond this point as this not only leads to higher power but also to higher supply voltage requirements. The receiver is powered by a single supply voltage of 0.83 V.

The gates of the transistors Mp and Mn are biased with different voltages to increase g_m/I_{dd} and g_m/V_{dd} of the LNTA, where I_{dd} and V_{dd} refer to the dc current and supply voltage of the LNTA, respectively. The −3-dB corner frequency of the high-pass filter formed by the ac coupling is 100 kHz. The replica bias circuit is a 12 times scaled-down version of the LNTA. The output of the LNTA is biased around midsupply, identical to the input of the TIA.

B. TIA

Designing for a wide IF-bandwidth in mixer-first receivers boils down to the design of a wideband TIA. In mixer-first receivers where input matching is achieved by the feedback resistor of the TIA such as in [10] and [11], stability is not a major concern since loop gain T_0 is less than 1. However, in receiver architectures where the input of the TIA needs to act as a virtual ground, T_0 greater than 1 is desired. Hence, stability becomes a major challenge, especially when wide IF bandwidth is also desired along with high in-band linearity.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR ART OPAMPS TARGETING WIDEBAND LINEAR TIA

	Unit	JSSC18 [21]	TCASI19 [1]	TCASI20 [22]	This Work
Bandwidth	MHz	20	200	80	175
In-band IIP3	dBm	33	15.1‡	19.4	14◇
Supply	V	1.8	1.8	1.8	0.83
UGB	GHz	1.6	1.1	1.3	7.6
Noise†	μV	21.1	11.7 △	49.7	4.6
Power	mW	5.4	18	14.2	13

‡ IIP3 of overall receiver

◇ Simulated overall receiver IIP3 with ideal LNTA block

† Input referred integrated (over respective IF bandwidth) noise of OpAmp

△ Integrating 0.83nV/$\sqrt{Hz}$ (at 10MHz) over the IF bandwidth

Therefore, there is a revived interest in the design of OpAmps with high UGB in such receiver applications.

Table I shows three recent works on such high UGB OpAmps. Pini *et al.* [21] utilized pole-zero compensation to achieve high UGB. Pini *et al.* [21] achieved in-band IIP3 as high as 33 dBm; however, note that the IF bandwidth is only 20 MHz and it benefits from a 1.8-V supply. Jiang *et al.* [1] and Jung *et al.* [22] employed feedforward-based compensation to achieve high UGB. They report an in-band IIP3 of 15.1 and 19.4 dBm in the respective bandwidths of 200 and 80 MHz and also benefit from a 1.8-V supply.

In our design, the OpAmps used in the TIAs of both main and auxiliary paths are designed using only inverters (dc coupled). The first major advantage of inverter-based analog design is that the design scales with the process, for example, inverter-based OpAmp designed in this work uses the same supply (0.83 V) as that of digital circuits, whereas OpAmps designed in [1], [3] [21], and [22] need a higher supply voltage compared to that used by the digital circuits. Second, the inverters avoid unnecessary internal nodes ([23]) such that the bandwidth can be high—this is reflected in the UGB reported in this work (7.6 GHz). Other advantages include high SNR due to current reuse and linearity benefits because of rail-to-rail output swing even though power supply rejection ratio (PSRR) is poor. The result is an OpAmp with state-of-the-art performance that can work at this low supply voltage.

The performance summary in Table I is for the OpAmp in the auxiliary path. For this OpAmp, the feedback factor is one because the output impedance of the LNTA is higher than the impedance of the feedback network. Analysis and design considerations can be extended to the OpAmp in the main path by considering the different feedback factor.

C. Three-Stage Inverter-Only OpAmp

The stabilization mechanism and design considerations for the OpAmp are explained with the help of Fig. 11. For simplicity, no external load capacitor is assumed, which had little effect on the stabilization technique or design considerations as explained later in the section. The OpAmp needs to be designed for a certain loop gain T_0 to achieve the desired

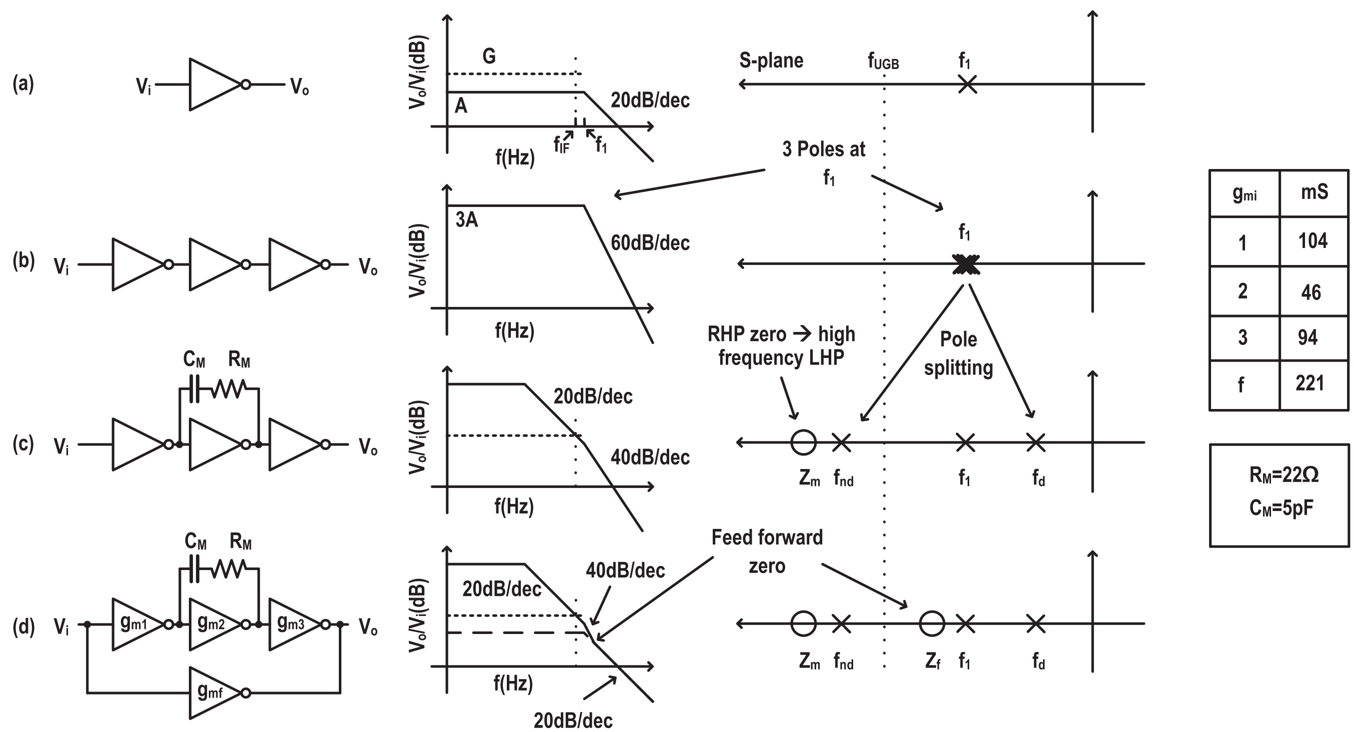


Fig. 11. Circuit, Bode plot, and pole-zero plots to explain OpAmp stabilization. (a) Single-stage inverter has insufficient self-gain. (b) Three-stage cascaded inverters roll-off at −60 dB/decade through ω_{UGB}. (c) Miller compensation with RHP zero removal improves roll-off at ω_{UGB} to 40 dB/decade and still has potential for instability. (d) Feedforward path introduces a zero and takes over high frequency response, hence 20-dB/decade roll-off through ω_{UGB}, and hence stabilizes OpAmp.

in-band linearity. Hence, a minimum gain G is desired until the frequency f_{IF} (Hz) as shown in the dotted lines in the Bode plot of Fig. 11(a).

A simple choice is to use an inverter as the OpAmp. However, as shown in the Bode plot in Fig. 11(a), gain A of the inverter is lower than the gain G desired for linearity. Without loss of generality, the location of f_1, the pole frequency of the inverter, is assumed to be at higher frequency than f_{IF}.

Since the overall OpAmp needs to be inverting, the next option in a single-ended design is a cascade of three inverters, as shown in Fig. 11(b). Without loss of generality, each inverter stage is assumed to have a gain of AdB and a single pole at frequency f_1 as shown in the corresponding Bode and pole-zero plots. The gain rolls off with 60 dB/decade through the UGB, so the OpAmp is unstable when used in feedback.

As a first step toward stabilizing the three-stage inverter in Fig. 11(b), a Miller capacitor with right half-plane (RHP) zero removing resistor is added parallel to the middle inverter stage, as shown in Fig. 11(c). Due to the Miller compensation, the poles at input and output of the second-stage inverters split into a dominant pole at frequency f_d and a nondominant pole f_{nd}, which is pushed outside the UGB as shown in the pole-zero plot. The Miller capacitor value needs to be chosen such that the gain required at f_{IF} (as shown in the dotted line of Bode plot) is sufficient to achieve the desired in-band linearity. R_M is chosen such that the RHP zero is brought to the left half-plane and is pushed far away from the UGB. However, note that circuit in Fig. 11(c) still has potential for instability as the magnitude in the Bode plot crosses f_{UGB} with 40-dB/decade roll-off due to f_d and f_1 which reside below f_{UGB}.

A feedforward path as shown in Fig. 11(d) is added as a final step toward stabilization. The feedforward path adds a zero,[2] so there are two poles and one zero below f_{UGB}. Hence, the Bode plot goes through f_{UGB} with 20-dB/decade roll-off as a first-order system. The dashed line shown in the Bode plot is the magnitude response of the feedforward path. Overall magnitude response is dominated by the three-stage cascaded inverter path until the zero is introduced, and then, the feedforward path takes over at high frequencies.

Fig. 11 shows the values of the g_m of the inverters of various stages of the OpAmp. g_{m1} is chosen such that its thermal noise contribution is low. The length of the transistors of this stage is also chosen higher compared with other stages to reduce its flicker noise. g_{m2} is chosen to be lower compared with other stages to reduce the power as it does not affect the performance of the OpAmp significantly. g_{m3} is chosen such that it can source/sink sufficient linear current to the LNTA for the maximum input power level. g_{mf} is chosen to adjust the feedforward zero location to obtain the desired phase margin.

The OpAmp is loaded by the input capacitance of the measurement circuits (1.1 pF), as shown in Fig. 9. This pushes the pole at the output of g_{m3} to lower frequencies than f_1. In this design, this pole still remains higher than f_{IF}, as shown

[2]The zero Z_f due to feedforward path is located at higher frequencies than f_{IF} and does not severely degrade the settling characteristics of the OpAmp.

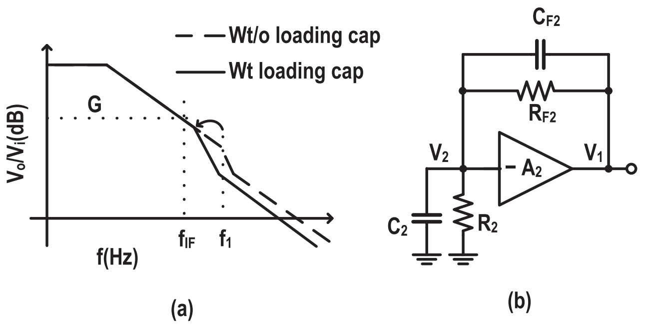


Fig. 12. (a) Bode plot showing the effect of capacitive loading at the output of the OpAmp. (b) Circuit to model pole and zero due to the feedback network.

in Fig. 12(a). Even though f_{UGB} of the OpAmp is decreased due to the capacitive loading at its output, the gain of the OpAmp at f_{IF} does not change.

Another practical consideration is that the feedback factor of the OpAmp is not exactly one and has a frequency dependence. This does not change the above analysis significantly as long as the output impedance of the LNTA is much higher than the impedance of the feedback network. However, this nonideality introduces an additional pole and zero in the loop gain. Fig. 12(b) shows the circuit model to include this effect. $-A_2$ in Fig. 12(b) is the OpAmp in the auxiliary path analyzed in Fig. 11. R_2 denotes the output resistance of the LNTA and C_2 represents the total capacitance at the output (input) of LNTA ($-A_2$). The transfer function of the feedback network can be written as

$$\frac{V_2(s)}{V_1(s)} = \frac{R_2}{R_2 + R_{F2}} \times \frac{1 + sR_{F2}C_{F2}}{1 + s(R_{F2} \parallel R_2)(C_{F2} \parallel C_2)}. \quad (13)$$

Thus, there will be one pole (f_{fb}) and zero (Z_{fb}) each in addition to the poles and zeros in the pole-zero plot of Fig. 11(d).

Fig. 13 shows the simulation results of magnitude and phase response of the loop-gain T_0 of the OpAmp when placed in the TIA of the auxiliary path, as shown in Fig. 9. The pole (f_{fb}) and zero (Z_{fb}) added by the feedback network along with f_1 and Z_f are located between the dashed lines marked in the phase response of Fig. 13. It can be observed that Z_{fb} at around 175 MHz starts to improve the phase response; however, poles f_{fb} and f_1 at slightly higher frequencies start to degrade the phase response. However, feedforward zero (Z_f) added at higher frequencies improves the phase response again.

Fig. 13 also includes the stability plots for extreme conditions with respect to process and temperature along with nominal conditions. It can be observed that the phase margin is > 75° in all the cases. Location of the dominant pole due to Miller compensation can be seen at around 1 MHz such that a loop gain of 38.2 dB is available at the band edge to achieve the desired in-band linearity. The UGB is located at around 7.6 GHz as marked in the simulation.

Since the UGB of the OpAmp is 7.6 GHz, high routing inductance during layout can lead to instability. Specifically, the routing inductance in the feedback path causes phase

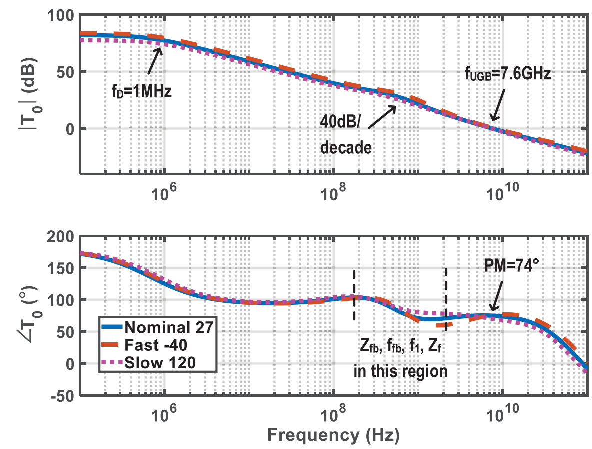


Fig. 13. Simulation of the magnitude and phase response of the Bode plot of the OpAmp designed and placed in the auxiliary path of Fig. 9 with process corner results.

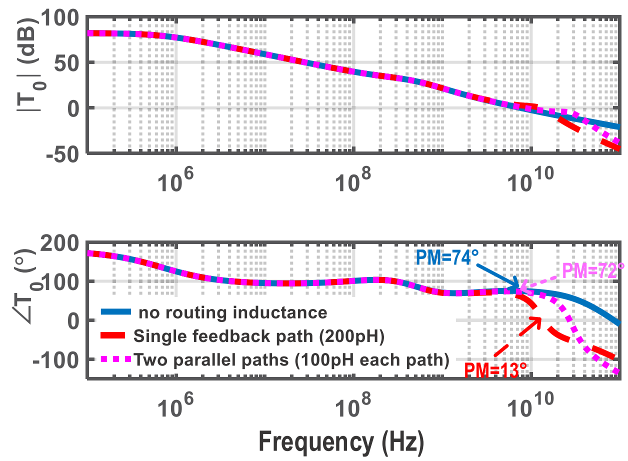


Fig. 14. Bode plot showing the stability degradation due to routing inductance.

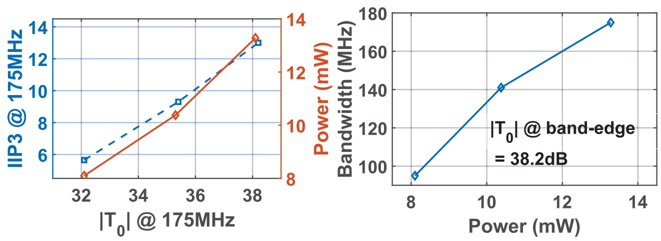
margin deterioration due to the series resonance of this inductance with C_{F2}.

Fig. 14 shows the simulation results explaining this effect. The solid line with 74° phase margin shows the stability plot of the OpAmp without considering routing inductors. The dashed line shows the stability plot when the feedback path with R_{F2} and C_{F2} is routed as a single path. The large dimension of C_{F2} (13.7 pF) in the feedback path results in a routing length of 200 μm with equivalent routing inductance of 200 pH (assuming 1-nH/mm routing inductance). This results in a phase margin of 13°, hence potential for instability. Series resonance can be observed as a bump in the magnitude plot and a sharp phase degradation in the phase plot. Splitting the feedback path up in two parallel ones reduces the inductance and pushes the resonance to higher frequencies, improving the phase margin to 72° (dotted line).

Note that common-mode control is not necessary since the OpAmps work independently and there is no coupling between any of the I/Q/+/−/main/aux paths.

D. Linearity, Bandwidth, and Power Tradeoff of the OpAmp

The high in-band IIP3 and wide IF bandwidth targeted in this work leads to an increased power consumption. A tradeoff



(a) (b)

Fig. 15. Simulation results of the tradeoff between the power and (a) band-edge IIP3 and (b) bandwidth of the OpAmp.

between power and in-band IIP3 of the LNTA was discussed in Section IV-A. Here, first, the tradeoff between the linearity and power consumption of the OpAmp is analyzed. The OpAmp in the auxiliary path is considered for the analysis and the same can be extended to the OpAmp in the main path.

In this analysis, the band-edge IIP3 of the OpAmp is simulated for various values of the loop gain T_0 (at the band edge). For every T_0, the power consumption of the OpAmp is optimized. This gives a relationship between the IIP3 and power consumption of the OpAmp. Note that the IIP3 of the OpAmp is characterized by simulating the IIP3 of the auxiliary path keeping the LNTA as an ideal block.

The dashed line in Fig. 15(a) shows the simulation results of the IIP3 at the band edge (175 MHz) for varying values of T_0 (at the band edge). T_0 at the band edge is varied as follows. First, the Miller capacitor is changed to change T_0 at the band edge. This results in a change in the stability conditions. Then, the power consumptions in g_{m2}, g_{m3}, and g_{mf} stages of the OpAmp are optimized such that the stability conditions are similar (constant phase margin) for all T_0. Note that g_{m1} is not varied such that thermal and flicker noise characteristics of the OpAmp are not varied significantly.

It can be observed from the solid line of the simulation result [Fig. 15(a)] that a higher IIP3 (at higher T_0) at the band edge comes at the cost of increased power consumption.

The tradeoff between the bandwidth and power dissipation of the OpAmp can be analyzed with a similar simulation setup with one key change. In the previous analysis, the IIP3 of the OpAmp is simulated against its power consumption (T_0) at one frequency (band edge). However, in this analysis, the frequency up to which $T_0 > 38.2$ dB is valid is simulated against the power consumption of the OpAmp. This frequency indicates the IF bandwidth up to which the desired IIP3 can be obtained (as T_0 determines the IIP3). The simulation results in Fig. 15(b) show that an increase in bandwidth also comes at the cost of power consumption. T_0 of 38.2 dB is chosen for this simulation since this value is used as T_0 in the final design.

E. Power Consumption Breakdown

Table II shows the breakdown of the power consumption of the receiver calculated using the current consumed by various blocks, as shown in Fig. 9. The OpAmp of the main path consumes more power than the OpAmp of the auxiliary path. This is because the feedback factor of the main path is lower than that of the auxiliary path. Though a low R_{SW} is required

TABLE II

POWER CONSUMPTION BREAKDOWN OF THE RECEIVER

Block	OpAmps of main path	OpAmps of Aux path	LNTAs	LO	Total
Power (mW)	15.2×4	13×4	12.4×4	1.7 mW/GHz	162.4mW + LO

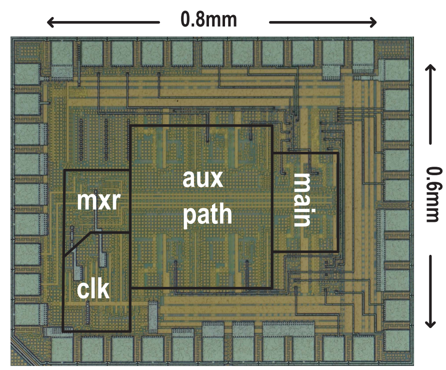


Fig. 16. Chip photograph showing various receiver blocks.

in the mixer switches for low noise, compared with baseband circuits, i.e., LNTA and TIAs, much lower power is dissipated in the LO generation circuits. This is because the mixer switches benefit from minimum length transistors (20 nm). The reduced capacitance for a given R_{SW} and the reduced supply voltage due to lower transistor length greatly decreases the power dissipation in LO generation circuits compared with those designed with higher transistor length processes [11].

V. EXPERIMENTAL RESULTS

The receiver was realized on chip in a 22-nm FDSOI CMOS process and has an active area of 0.48 mm^2. A single supply voltage of 0.83 V powers the chip. Fig. 16 shows a chip photograph with the placement of the various receiver blocks. Mixer switches are placed near to the bond pad so that RF routing is minimal. The four capacitors involved in N-path filtering are placed near the mixer switches to provide short return paths for the high-frequency currents. The clk block includes a $\div 2$ circuit and a four-phase 25% duty-cycle generation circuit.

A. Test Setup

The interface of the receiver inputs and outputs for the measurement can be seen in Fig. 9. The measurements were performed with a single-ended source, followed by a passive balun driving the receiver. The differential output voltage is measured by an active differential probe. The receiver has circuits at the output to measure NF and IIP3 separately. Common-source amplifiers and all-pass voltage attenuator circuits are used at the output to measure NF and IIP3, respectively, such that noise and distortion of the active differential probe do not dominate the respective measurements. The corresponding gain and attenuation were deembedded. Note that Fig. 9 also shows the addition of the main path and auxiliary path signals.

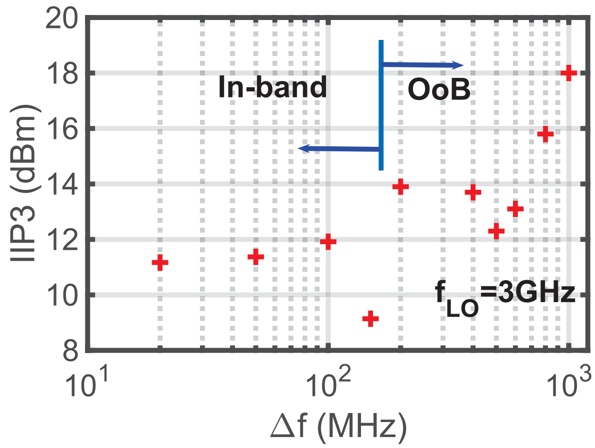


Fig. 17. Measured IIP3 across interferer offset frequencies.

B. Measurement Results

The measured IIP3 for both in-band and OoB is shown in Fig. 17. Two tones f_1 and f_2 are at $\Delta f - 2$ MHz and $\Delta f + 2$ MHz, respectively, for the case of in-band IIP3 measurement. Note that Δf represents the offset from the LO frequency (f_{LO}) and $f_{\mathrm{LO}} = 3$ GHz in this case. IIP3 is >9 dBm for all Δf within the measured TIA bandwidth of 175 MHz. For the OoB IIP3 measurement, two tones f_1 and f_2 are at Δf and $2\Delta f - 50$ MHz such that the IM3 products are always at 50 MHz. An approximate increase of 6 dB can be observed for OoB IIP3 from Δf of 500 MHz–1 GHz indicating the effect of N-path filtering that has a −3-dB frequency of 475 MHz. Since this −3 dB frequency is more than two times away from the IF bandwidth, the advantage of OoB N-path filtering is not observed near the band edge. The measured IM3 curve for $\Delta f = 20$ MHz is shown in Fig. 18(a). This measurement shows that the IIP3 is valid until an input power of −20 dBm, which is approximately 600-mVp-p swing at each single-ended output.

It can be recollected from Section IV that the simulated in-band IIP3 of the LNTA is 9 dBm and that of the receiver considering the LNTA as an ideal block is 14 dBm. Hence, the overall in-band IIP3 of the receiver is limited by the LNTA. The measured in-band IIP3 of the receiver (11 dBm) as shown in Fig. 17 is slightly higher than the IIP3 limited by the LNTA because of the more linear main path that does not contain the LNTA. Although LNTAs such as [24] with more complex and stronger feedback can provide higher linearity, noise and power dissipation in such LNTAs increase due to the increased number of transistors. We use a source-degenerated inverter as the LNTA as it provided the best tradeoff among linearity, noise, and power of the circuits we considered.

S_{11} measured at $f_{LO} = 3$ GHz is shown in Fig. 18(b). Since the −3-dB frequency of the N-path filter is more than two times higher than that of the IF bandwidth, offset in S_{11} due to parasitics such as bondwire inductance [25], [26] and mixer input capacitance does not degrade the input matching significantly. Fig. 19 shows the measured conversion gain SC_{21} of the receiver. A dc gain of 22.4-dB and a −3-dB bandwidth of 174 MHz is measured, which matches closely with the design and simulations.

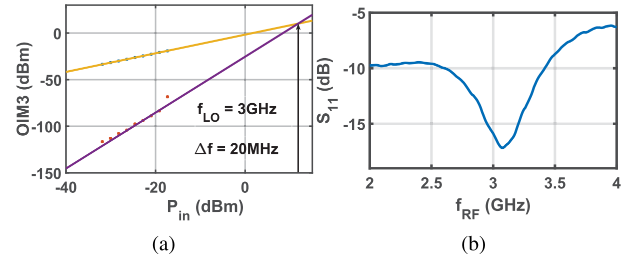


Fig. 18. Measured (a) OIM3 at 20-MHz offset and (b) S_{11} showing N-path filtering.

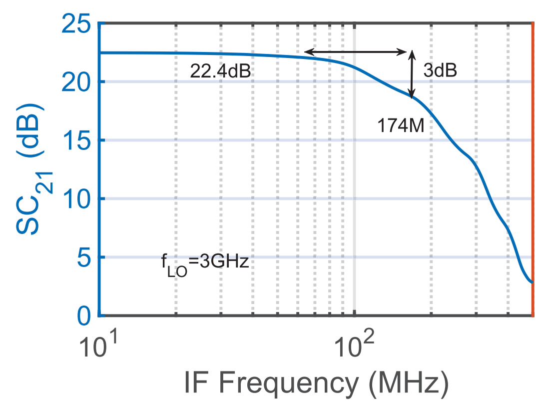


Fig. 19. Measured SC_{21} at 3-GHz LO.

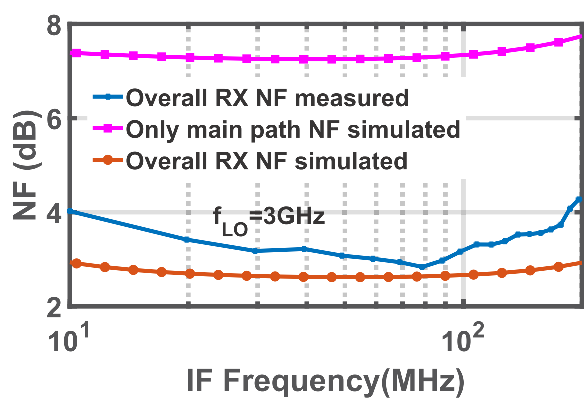


Fig. 20. Measured NF of the overall receiver at 3-GHz LO.

Fig. 20 shows the measured NF at 3-GHz LO frequency. The simulation result shows a close match with the measurement. The < 3-dB NF at 80 MHz confirms the noise-canceling property of the receiver. For comparison, the simulated NF of the receiver without noise-canceling path (only main path) is also shown in Fig. 20. Note that since the IF bandwidth is more than two times smaller than the $-3-dB$ frequency of the N-path filtering, the noise canceling is not affected by the N-path filtering across the IF bandwidth for a given LO frequency (3 GHz in Fig. 20).

Fig. 21 shows the key performances of the receiver across LO frequencies. It plots the in-band IIP3, NF, and SC_{21} measured at 50-MHz offset across LO frequencies from 1 to 6 GHz. In-band IIP3 stays between 9 and 11 dBm for the measured LO sweep. The NF of 2.5 dB at 1 GHz increases to around 5 dB at 6-GHz LO. This degradation in NF is mainly

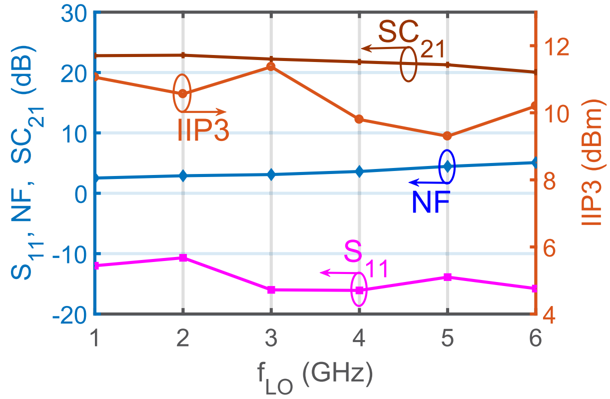


Fig. 21. Measured S_{11}, NF, SC_{21}, and IIP3 across LO frequencies.

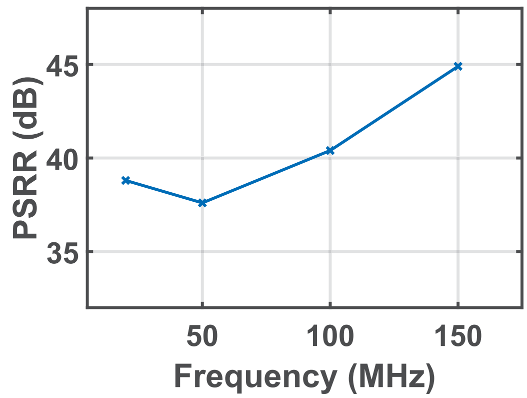


Fig. 23. Measured PSRR across IF frequency.

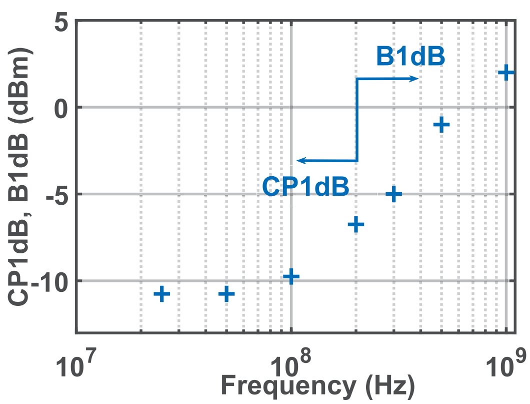


Fig. 22. Measured $\mathrm{CP_1dB}$ and $B_1\mathrm{dB}$ for various frequency offsets at 3-GHz LO.

due to an increase in the effective mixer switch resistances at higher frequencies. Routing parasitics between the drivers and the mixer switches degrade the signal strength driving the mixer switches at higher frequencies and hence increase the effective mixer switch resistances. Increase in R_{SW} not only degrades NF according to Fig. 8 but also increases R_{ES} in noise-canceling equation (9). Even though calibration to adjust the on-chip resistor values in (9) can improve the NF, such circuits are not included in this work. The S_{11} well below -10 dB across 1–6 GHz shows that large input capacitances of the LNTAs do not degrade the input matching at higher frequencies, as explained in Section IV-A. S_{11} improves at higher LO frequencies compared to that at 2 GHz due to the tuning effect of the mixer input capacitance by the series bondwire inductance [25], [26]. We measured the receiver until 6 GHz even though it is functional until 8 GHz in the extracted simulations due to the frequency limitation of the $2\times f_{\mathrm{LO}}$ source (12.75 GHz) feeding the clk block.

Fig. 22 shows the measured $\mathrm{CP_1dB}$ (in-band) and $B_1\mathrm{dB}$ (OoB). For the $\mathrm{CP_1dB}$ measurement, input power at which the gain compresses by 1 dB is observed for various in-band frequency tones. For $B_1\mathrm{dB}$ measurement, an in-band tone at 50-MHz offset and -25-dBm input power is monitored for a 1-dB gain compression in the presence of OoB blocker tones at different frequency offsets.

Because of quasi-differential nature of the active building blocks, the receiver is characterized for its susceptibility to power supply and common mode noise. Fig. 23 shows the measured PSRR at different frequencies. A bias tee network is used to superimpose sinusoidal tones at various frequencies over the dc supply voltage across the off-chip decoupling capacitor placed close to the chip. A PSRR of around 38 dB is measured. Note that the voltage transfer from the off-chip decoupling capacitor to the on-chip decoupling capacitor decreases due to the increasing impedance of the bondwire inductance at higher frequencies. Therefore, a higher PSRR is measured with respect to the off-chip decoupling capacitor above 100 MHz.

Due to the double balancing mixer used, the receiver rejects considerable common-mode noise. However, unlike PSRR measurement where the supply noise is fed to the singled-ended supply input of the chip at IF frequencies, the measurement accuracy of the CMRR is limited as the common-mode noise is fed to the differential inputs of the chip at RF frequencies. An overall CMRR of 27 dB is measured at 3-GHz LO limited by the low CMRR (35 dB) of the balun and differential cables that feed the chip inputs. It is worth pointing out that even a mismatch of 0.25 mm between two bondwires that feed the receiver differential inputs can already degrade the CMRR to 27 dB.

For similar reasons, i.e., mismatches and the limited CMRR, an in-band IIP2 of 33.9 dBm is measured (f_1 = 70.1 MHz, f_2 = 120.1 MHz, and f_{LO} = 3 GHz).

Therefore, to achieve high CMRR, PSRR, and IIP2 in such quasi-differential realizations, symmetric layout and large devices are needed to reduce mismatch. Common-mode rejection circuits in quasi-differential implementations as in [23] can be investigated to further increase the above performances.

C. Comparison

The focus of this work is to achieve high in-band linearity and wide IF bandwidth without compromising on other receiver performances, such as NF, OoB IIP3, and matching. Table III shows the in-band IIP3 and IF bandwidth (along with other performances) of the state-of-the-art receivers and compares it to our receiver performance. Reference [1] is a close comparison to our work as it also achieves both high in-band IIP3 and wide IF bandwidth. However, even though Jiang *et al.* [1] improved NF by cross coupling the gates of

TABLE III
RESULT SUMMARY AND COMPARISON WITH PRIOR ART

	This Work	TCASI19[1]	JSSC16[3]	RFIC19[5]	JSSC12[12]	ISSCC16[8]	ISSCC18[9]
Architecture	BBNC	RX with LNTA	Mixer-first	Mixer-first	FTNC	ZIF RX	ZIF RX
Technology	22FDX	40nm	28nm	65nm	40nm	45nm	65nm
In-band IIP3 (dBm)	9	15.1-16.7	7 *	6	-3 ‡	-4 ‡	12 †‡
IF bandwidth (MHz)	175	200	50	10	2	50	100
f_{RF} **(GHz)**	1-6	3-6	0.4-3.5	0.5-3.5	0.08-2.7	0.4-4	0.4-6
NF (dB)	2.5-5	5-5.8	2.4-2.6	3.3 △	1.9	2	12
Supply Voltage (V)	0.83	1.8/1.1	1.5/1.1	2.4/1.2	1.3	2.5/1.8/1.1	1.8/1.3
Power (mW)	172	64.1-69.6 ◇	38-75	38	35.1-78	200	6600 **
Area (mm^2)	0.48	1.2 ◇	0.23	1.5	1.2	49 **	68.7 **

* Measured for 20MHz bandwidth, baseband supply = 1.5V
† De-embedding off-chip LNA
◇ Only I-channel
‡ taken from band-edge IIP3
△ TDD operation mode
** Full SOC

a differential common gate LNTA, its NF is higher than 5 dB, whereas we achieve much lower NF due to the noise-canceling property of the receiver. Also, Jiang *et al.* [1] used a higher supply voltage of 1.8 V to increase IIP3 compared to 0.83 V used in our receiver. In addition, inductors used in the common-gate LNTA not only limits their low-frequency operation (3 GHz compared 1 GHz in our case) but also increases the chip area (1.2 mm^2 for only I channel compared to 0.48 mm^2 for both I and Q channels in our case). Nevertheless, due to the LNTA in the front end, Jiang *et al.* [1] does not possess the disadvantages of a mixer-first receiver [3], [27].

References [3] and [5] are two other receivers that achieve high in-band IIP3, but both report this for a lower IF bandwidth of 20 and 10 MHz, respectively, compared to 175 MHz in our work. Furthermore, they make use of higher analog supply voltages of 1.5 and 2.4 V, respectively, to increase linearity. McLaurin *et al.* [9] measured a band-edge IIP3 of 12 dBm, but this is after de-embedding the off-chip LNA, which is reflected in the higher NF of 12 dB. We mainly target base-station applications and our power numbers are lower compared to [8] and [9] which target the same application.

VI. CONCLUSION

The proposed receiver can achieve high in-band linearity over a wide RF frequency range of 1–6 GHz. This is mainly because all active circuits operate at baseband frequencies and can be designed using feedback, both the LNTA and the TIA. The input capacitance of the LNTA in baseband does not degrade the input matching unlike that of an LNTA operating at RF frequencies. A strong feedback (high loop gain) in the TIA in mixer-first receiver architectures increases their NF. The noise-canceling property of the proposed receiver breaks this tradeoff allowing both low NF and high in-band linearity. A high loop-gain of the TIA with wide IF bandwidth also demands for an OpAmp with high UGB. An inverter-only multistage OpAmp is designed for this.

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