Comparison of Selective Deposition Techiques for Fabricating p$^+$n Ultrashallow Silicon Diodes

Xingyu Liu, Shivakumar D. Thammaiah, Thomas L.M. Scholtes, and Lis K. Nanver

Abstract—**Ultrashallow diodes were fabricated using two different chemical-vapor deposition techniques: either a pure boron (PureB) deposition from diborane or boron-doped Si selective epitaxial growth (SEG) from dichlorsilane and diborane gases. They are evaluated with respect to the current-voltage diode characteristics. The PureB diodes have two decades lower saturation current, good uniformity and no significant leakage currents. In contrast the SEG diodes have leakage currents that cause a factor 10 spread in saturation current. A differential current measurement technique was applied to show that the high SEG-diode saturation currents are a result of high electron injection in the anode region and the spread is due to defect-related leakage currents originating in the vicinity of the p$^+$-region .**

Keywords— *boron; chemical vapor deposition; current-voltage characteristics; selective epitaxial growth; silicon; ultrashallow diodes*

I. Introduction

Reducing the junction depth of silicon diodes plays an important role in the shrinking of CMOS transistors. Also for increasing functionality of CMOS technology by integrating application specific devices, new low-temperature techniques for fabrication of ultrashallow junctions are continually being developed. One example is PureB p$^+$n junctions that are created by chemical-vapor deposition (CVD) of pure boron at temperatures below 700°C. These diodes can be fabricated with junction depths less than 10 nm [1]. Such shallow junctions will normally have much higher saturation currents than their deep junction counterparts because the integral number of p-dopants in the anode decreases as the junction depth decreases. However, in PureB diodes the hole concentration in the anode region is the result of a reaction at the boron-silicon interface giving a coverage of about one monolayer of holes. Among other experimental results, this has been concluded from the fact that the saturation currents in PureB diodes are comparable to those of deep p$^+$n junctions [1, 2]. In recent years these junctions have found use in high-sensitivity, robust photodiode detectors for very low-penetration beams such as VUV light and low-energy electron with energies down to 100 eV [1, 3]. A much more commonly used CVD method is the selective epitaxial growth (SEG) of highly-boron-doped Si layers. In this paper the current-voltage (*I-V*) characteristics of both these types of junctions are compared. A 2-diode measurement technique, presented in [4], was used here to separate leakage currents from the ideal electron and hole flows. In this way, the basic current flows in the diodes could be determined giving a better understanding of the processing parameters responsible for the *I-V* behavior.

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II. Experimental Procedures

The basic diode structure studied in this work is shown in Fig. 1. The substrates are (100) n-type Si with a resistivity of 2-5 Ω-cm and a thickness of 525 µm. A 750-nm-thick thermal oxide was grown and patterned with anode windows by HF wet etching to the Si. Immediately before transfer to the CVD equipment, a HF dip (0.55% HF) was performed followed by wafer cleaning with Marangoni drying as the last step [5]. The CVD was performed in an ASM Epsilon One reactor equipped with diborane (B_2H_6) for pure boron deposition and boron doping of the epitaxially grown Si layers. The Si was supplied by a dichlorsilane precursor and in both cases hydrogen was used as carrier gas. All depositions were performed at a wafer temperature of 700°C. The PureB thickness was controlled by the length of the B_2H_6 exposure time chosen here to be in the range of 30 s to 30 min. The target thickness for the Si epitaxial growth was 20 nm. Both the PureB and the Si:B deposition are selective, growing only on the c-Si and not on the oxide. This means that both depositions suffer from loading effects that may result in thicker layers in small windows surrounded by large oxide areas [6, 7]. The actual layer thickness in the diodes studied here was not measured directly but was estimated from other experimental results. A high B_2H_6 flow rate was used to obtain a maximum Si doping level of 2×10^{19} cm^{-3} as governed by the solid solubility of B in Si at 700°C.

Finally, the wafer was coated with a metallization layer of Al/(1%Si) sputtered directly after the CVD step and patterned on the front of the wafer for contacting of the diode anodes. The whole backside of the wafer was also metallized to give ohmic contact to the cathode. The completed wafers were alloyed in forming gas at 400°C for 30 min. The 1% Si content in the Al is necessary for avoiding spiking of the SEG regions. For PureB diodes the PureB layer itself forms a robust barrier between the Al and Si, so in this case pure Al is also often used [1].

III. Theoretical Considerations

The pure B deposition has already been extensively studied and is known to form a few-nm deep p$^+$n-like junction with current flows comparable to deep diffused junctions [5]. For the 700°C deposition used here, there is some boron doping of the Si surface to the solid solubility of 2×10^{19} cm^{-3}. This is, however, not enough to explain the very low saturation current. Therefore, to explain this and other properties of these diodes, a new bandgap model was proposed in [2]: the deposited B layer reacts with the Si forming a monolayer of acceptor states that fill with electrons, giving a monolayer of fixed negative charge. The PureB layer acts like a semi-insulator accumulating an inversion layer of holes in the Si as illustrated by the band diagram in Fig. 2a.

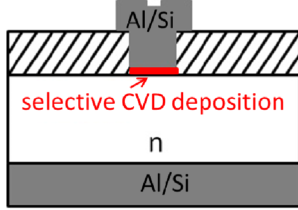

Fig. 1. Cross section of the basic p$^+$n diode structure where a CVD deposition of PureB or boron-doped Si is performed selectively in a window to the Si substrate.

In Fig. 2b the band diagram of a conventional Si ohmic-contacted p$^+$n junction is shown. In the ideal case with a lightly-doped n-substrate, the current in the p$^+$n diode is dominated by the injection of the holes from the p$^+$-region into the n-substrate. This can be verified experimentally by using the 2-diode test structure described in [4] and shown in Fig. 3a. The W_B is the distance between the 2 diodes named emitter and collector and W_E is the emitter width. Schematic cross-sections of the diodes displaying the expected current flows are shown in Figs. 3b and 3c for the biasing methods used here to study the emitter diode currents indicated as I_E and $I_{E//C}$.

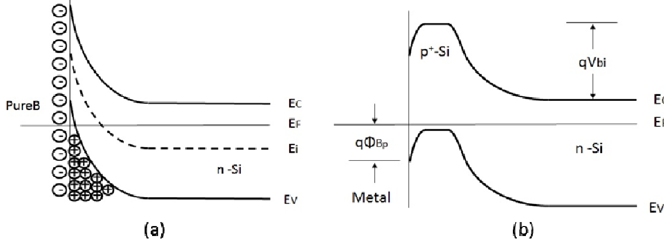

Fig. 2. Band diagram of (a) a PureB diode [2] and (b) a conventional p$^+$n diode all at zero bias.

To gain insight in the mechanisms governing the current flows in the different types of junction we first look at the ideal case, disregarding defect-induced currents and series resistance. The electron and hole currents over a junction can be expressed as [8]:

$$I = \mathrm{q}n_{\mathrm{i0}}^2 A\left[\frac{1}{G_{\mathrm{D}}}+\frac{1}{G_{\mathrm{A}}}\right]\left(\mathrm{e}^{\frac{\mathrm{q}V}{kT}}-1\right) \quad (1)$$

$$I_{\mathrm{h}} = \frac{\mathrm{q}n_{\mathrm{i0}}^2 A}{G_{\mathrm{D}}}\left(\mathrm{e}^{\frac{\mathrm{q}V}{kT}}-1\right) \quad (2)$$

$$I_{\mathrm{e}} = \frac{\mathrm{q}n_{\mathrm{i0}}^2 A}{G_{\mathrm{A}}}\left(\mathrm{e}^{\frac{\mathrm{q}V}{kT}}-1\right) \quad (3)$$

where q is the elementary charge, n_{i0} is the intrinsic carrier concentration, A is the diode area, G_D and G_A are the Gummel numbers of the n- and p-doped regions, respectively, and kT/q is the thermal voltage. The electron injection into the anode (here the emitter/collector) region is governed by the Gummel number G_E of the region. In a general formulation this can be defined as

$$G_{\mathrm{E}} = \int_{W_{\mathrm{QNE}}} \frac{N_{\mathrm{E}}(z)}{D_{\mathrm{n}}(z)}\frac{n_{\mathrm{i0}}^2}{n_{\mathrm{ie}}^2(z)}dz + \frac{N_{\mathrm{E}}}{S_{\mathrm{E}}}\frac{n_{\mathrm{i0}}^2}{n_{\mathrm{ie}}^2} \quad (4)$$

where W_{QNE} is the width of the p-type doped region of the Si, N_E is the active p-type doping concentration, i.e., hole concentration, $D_n(z)$ is the electron diffusion coefficient in the p-region as a function of depth z from the Si surface, and S_E is the surface recombination velocity. The $n_{ie}(z)$ is given by

$$n_{\mathrm{ie}}(z) = n_{\mathrm{i0}}\exp\left(\frac{-\Delta E_{\mathrm{G}}(z)}{2kT}\right) \quad (5)$$

where $\Delta E_G(z)$ is the bandgap difference with respect to the c-Si. Likewise, the hole injection into the substrate is governed by the Gummel number of the substrate, G_{sub}. In the simplest 1-D approximation the saturation current can be written as $I_{SE} \propto 1/G_{sub}$ with $G_{sub} = N_{sub}W_{sub}$, where N_{sub} and W_{sub} are the substrate doping and width, respectively [8].

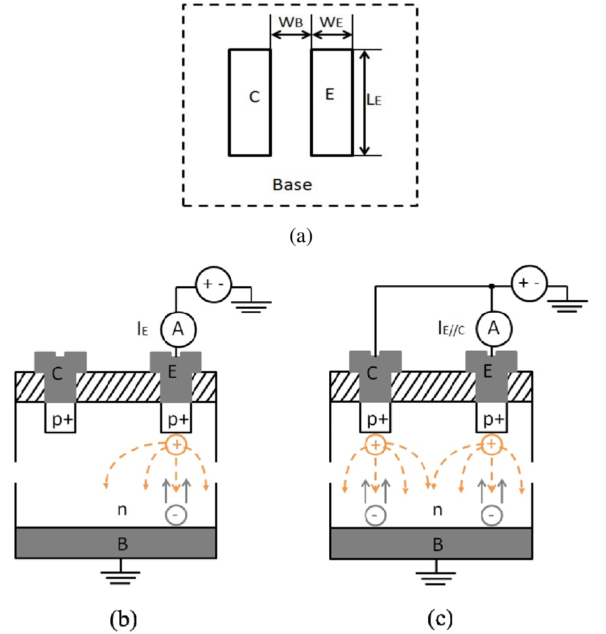

Fig. 3. (a) Basic layout of the 2-diode test structure. Schematic cross section of p$^+$n-like diodes with (b) only the emitter connected and (c) both emitter and collector connected in parallel. The emitter current is in both cases measured under forward bias.

For both the PureB and SEG diodes studied here, assuming a clean interface between the c-Si and the deposited material, the level of hole injection into the substrate would entirely be governed by the substrate doping profile and should therefore be the same for both diode types. The Gummel number of the emitter is, however, quite different in the two cases. For the PureB diode G_E is largely determined by the hole segregation at the interface, which corresponds to a concentration of about 10^{15} cm^{-2}, and the doping of the Si contributes no more than about 2×10^{12} holes/cm^2 [1]. For the SEG diode the thickness and doping of the Si is expected to lead to much lower G_E corresponding to about 10^{13} holes/cm^2. Due to loading effects that give a variation of the amount of deposited Si, as a function of both global and local patterning of windows, the exact integral doping of the emitter is difficult to predict. When the integral doping decreases the electron injection will increase and can start to dominate the diode current as is the case for Schottky diodes that have no p-doped region.

A fundamental difference between the electron and hole current injection is found in the volume of the region into which they are injected. The emitter region is limited in size to the designed area of the anode windows, give or take some variations that may be caused by the specific processing. Therefore the injected electron current is proportional to the emitter area. In contrast, the holes injected into the substrate can spread in all directions into the substrate [9]. In our case with a low-doped 525-µm-thick substrate, the perimeter hole current per micrometer readily becomes much higher than the laterally uniform current density being vertically injected across the surface area of the anode. The spreading of the holes will be attenuated by any hole injection from other diodes being operated in the vicinity. This effect is described in detail in [4, 10] and is used here to extract information on electron and hole current flows from 2-diode *I-V* measurements.

As shown in Fig. 3 the 2-diode test structure is operated in two ways. The forward diode current through the emitter is measured with and without the collector connected in parallel. Due to the effects of current spreading $I_E < I_{E//C}$ and the differential current $\Delta I_E = I_E - I_{E//C}$ can be defined.

While the PureB diodes can be fabricated with reproducibly ideal *I-V* characteristics [1], SEG diodes often suffer from non-idealities. The emitter current can then be expressed as follows:

$$I_E = J_A A_E + J_P P_E + I_{leak} = I_{SE}\left(e^{\frac{qV}{kT}} - 1\right) + I_{leak} \quad (6)$$

where A_E is the emitter area in which a laterally uniform current density J_A flows, P_E is the on-mask perimeter, J_P is the current per micrometer that then accounts for the current not included in $A_E J_A$, and I_{leak} is the non-ideal current component.

In view of the limited processing, it is to be expected that the leakage component originates from defects in or near the depletion region over the emitter junction and not in the bulk of the substrate. This leakage is therefore the same whether or not the collector is connected. By using an emitter area, A_E, that covers a laterally uniform current-flow region in both contacting situations, we can write:

$$I_E = J_E A_E + J_{PE} P_E + I_{leak} = I_{SE}\left(e^{\frac{qV}{kT}} - 1\right) + I_{leak} \quad (7)$$

$$I_{E||C} = J_E A_E + J_{PE||C} P_E + I_{leak} = I_{SE||C}\left(e^{\frac{qV}{kT}} - 1\right) + I_{leak} \quad (8)$$

Therefore ΔI_E follows the ideal *I-V* characteristic

$$\Delta I_E = J_{PE} P - J_{PE||C} P = (I_{SE} - I_{SE||C})\left(e^{\frac{qV}{kT}} - 1\right) \quad (9)$$

The above formulations are only valid for low currents where the series resistance through the Si substrate and the emitter contact are not playing a role. In [4] it is shown that for high electron injection in the emitter, the series resistance through the substrate will reduce I_E when the collector is connected. This is in contrast to the case where the electron injection level is much lower than the hole injection level. The I_E and $I_{E//C}$ are then attenuated by the series resistance but approach each other as the voltage increases. This behavior is indicated in Fig. 4 where also the effect on ΔI_E is illustrated.

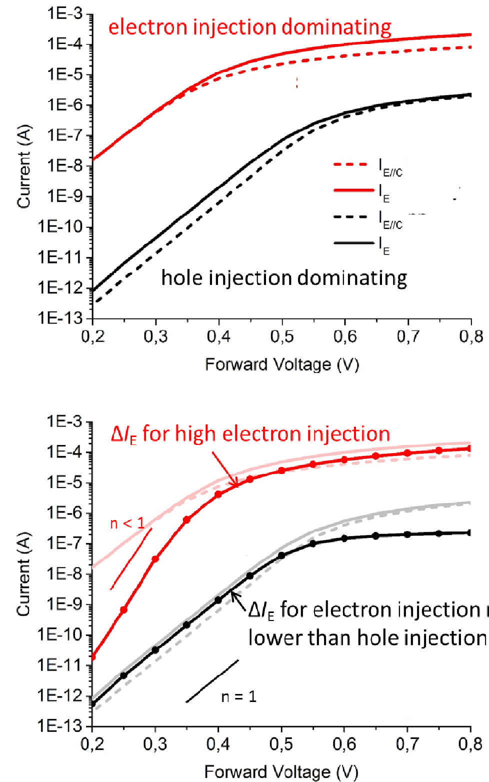

Fig. 4. Typical *I-V* characteristics for diodes for which either the electron injection in the anode or hole injection in the substrate dominates. Top: the currents I_E and $I_{E//C}$. Bottom: the resulting differential current ΔI_E.

IV. Results

The measured *I-V* characteristics of PureB and SEG diodes with an anode area of 20x1 µm^2 are compared in Fig. 5 for several measurements across the wafer. The PureB diodes

display uniformly low saturation current and an ideality factor n = 1. The SEG diodes have about 2 decades higher current with a decade spread and consistently have varying values of n > 1. This trend is also seen for other device geometries as shown by the measurement of the current at 0.4 V plotted for diodes up to 40x40 µm^2 in area in Fig. 6. No significant difference in the *I-V* behavior is seen for diodes measured at either the edge or center of the wafer. This suggests that both the PureB and SEG depositions are well-calibrated with respect to uniformity of the deposition over the wafer.

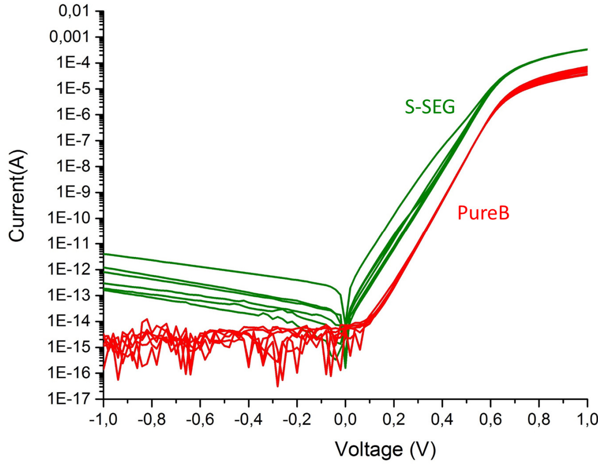

Fig. 5. Across-the-wafer measurements of diode *I-V* characteristics for PureB and SEG diodes with area 20x1 µm^2. The PureB layer thickness is about 3 nm.

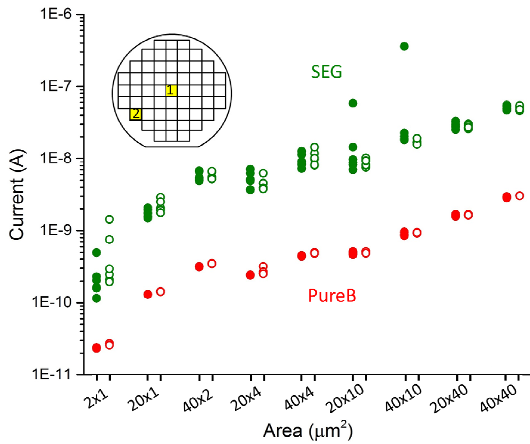

Fig. 7. Diode current spread at 0.4 V forward bias for PureB and SEG diodes with different areas. Measurements are performed on dies 1 and 2 (shown in inset) and 6 diodes per area are measured per die.

Despite the lower saturation current of the PureB diodes the attenuation at high forward voltage due to series resistance is much higher than for the SEG diodes. This is because the resistivity of the PureB layer is very high (> 500 Ω-cm [11]) so for a low series resistance a less than 3-nm-thick tunneling layer should be used. This is made clear in Fig. 8 where the *I-V* characteristics of devices with different PureB thickness are displayed. In this figure the differential current ΔI_E is also shown, revealing behavior characteristic of p$^+$n diodes where the hole injection into the substrate dominates. At low voltages the curves are equal with an n = 1. At high forward voltage the attenuation from series resistance is highest for the thickest PureB layer as would be expected. Even for the lowest series the deviations in ΔI_E typical of high electron current (n < 1) are not seen indicating that the electron injection in the emitter is much lower than the hole injection. The series resistance with the 2-nm-thick PureB layer is so low that the attenuation is no larger than what is seen for the SEG samples.

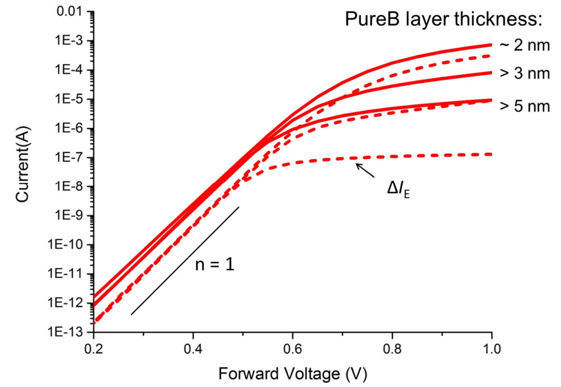

Fig. 8. *I-V* characteristics of diodes with different PureB layer thickness showing the emitter current I_E (solid line) and the differential current ΔI_E (dashed line). The anode area is 20x1 µm^2.

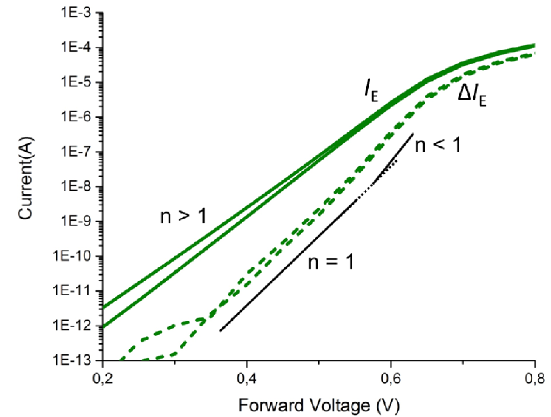

Fig. 9. *I-V* characteristics of 2 SEG diodes showing the emitter current I_E (solid line) and the differential current ΔI_E (dashed line). The anode area is 20x1 µm^2.

The *I-V* characteristics of 2 SEG diodes are shown in Fig. 9. At low voltages these diodes show the same ΔI_E level as is measured in the PureB diodes, i.e., the hole current is the same in both cases. The non-ideal diode leakage current does not appear in the differential current indicating that it is related to defects in the p$^+$ SEG region as expected. The effects of series resistance become visible when the current level increases with an n < 1. This is typical for high electron injection, i.e., the high SEG diode saturation current comes from high electron injection into the SEG emitter. A much higher integral doping in the SEG region would be needed to suppress this injection.

V. Conclusions

The results show that the PureB diodes have many advantages with respect to the boron-doped silicon-epitaxial-

growth diodes. Even though the PureB junction depth is only a few nm as compared to tens of nm for the SEG diodes, it provides a very efficient suppression of the electron injection level which is much lower than that of the hole injection. The SEG diodes allow a high electron injection giving a 2 decades higher saturation current than the PureB diodes. Moreover, unlike the PureB diodes, the SEG diodes are prone to non-ideal leakage currents that were seen for all the studied geometries from 2x1 μm^2 to 40x40 μm^2. The measurement of the differential current ΔI_E makes it clear that the high SEG saturation current is in first instance due to high electron injection and not the exclusive result of leakage currents. These do, however, give a significant spread in the diode *I-V* characteristics whereas the PureB diodes have excellent uniformity in this respect. For the PureB diodes one point of concern is the high resistivity of the PureB layer itself: for low series resistance a tunneling layer with thickness less than 3 nm should be applied. Such a thin layer is equally efficient in suppressing the electron injection as the thicker layers because the hole layer that forms at the PureB-to-Si interface is solely responsible for providing a very high anode Gummel number.

REFERENCES

[1] L. K. Nanver, L. Qi, V. Mohammadi, K. R. M. Mok, W. B. de Boer, N. Golshani, A. Sammak, T.L.M. Scholtes, A. Gottwald, U. Kroth, and F. Scholze, "Robust UV/VUV/EUV PureB photodiode detector technology with high CMOS compatibility," *J. Select. Topics Quantum Electronics*, vol. 20, No.6, pp. 1_11, Nov. 2014.

[2] L. Qi, and L. K. Nanver, "Conductance along the interface formed by 400℃ pure boron deposition on silicon," *IEEE Electron Device Letter*s, vol. 36, No.2, pp. 102-104, Dec. 2014.

[3] A. Sakic, G. Van Veen, K. Kooijman, P. Vogelsang, T. L. M. Scholtes, W. B. de Boer, J. Derakhshandeh, W. H. A. Wien, S. Milosavljevic, and L. K. Nanver, "High-efficiency silicon photodiode detector for sub-keV electron microscopy," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2707–2714, Oct. 2012.

[4] X. Liu and L.K. Nanver, "Comparing current flows in ultrashallow pn-/Schottky-like diodes with 2-diode test method," *29th International Conference on Microelectronic Test Structures (ICMTS) Proceedings,* Yokohama, Japan, March 28-31, 2016.

[5] F. Sarubbi, L. K. Nanver and T. L. M. Scholtes, "High effective Gummel number of CVD boron layers in ultrashallow p^+n diode configurations," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1269-1278, Jun. 2010.

[6] V. Mohammadi, W. B. de Boer, T. L. M. Scholtes, L. K. Nanver, "A Simple Model describing the kinetic of CVD Deposition of Pure-Boron Layers from Diborane," *ECS Transactions,* vol. 45, issue 31, pp. 57-65, May 2012.

[7] J. Hållstedt, E. Suvar, C. Menon, P.-E. Hellström, M. Östling, and H. H. Radamson, "Methods to reduce the loading effect in selective and non-selective epitaxial growth of SiGeC layers," *Materials Science and Engineering: B*, vol. 109, no. 1–3, pp. 122–126, 2004.

[8] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd edition, John Wiley & Sons, Inc., USA, 2007.

[9] P.-J. Chen, K. Misiakos, A. Neugroschel, and F. A. Lindholm, "Analytical solution for two-dimentional current injection from shallow p-n junctions," *IEEE Trans. Electron Devices*, vol. 32, no. 11, pp. 2292-2296, Nov. 1985.

[10] L. Qi, G. Lorito, L. K. Nanver, "Lateral-transistor test structure for evaluating the effectiveness of surface doping techniques" *IEEE Trans. Semiconductor Manufacturing*, vol. 25, no. 4, pp. 581-588, Nov. 2012.

[11] V. Mohammadi, S. Ramesh, L. K. Nanver, "Thickness evaluation of Deposited PureB Layers in Micro-/Millimeter-Sized windows to Si," *27th International Conference on Microelectronic Test Structures (ICMTS) Proceedings,* Udine, Italy, pp. 194-199, 2014.

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