Low-Power Highly Selective Channel Filtering Using a Transconductor–Capacitor Analog FIR

Bart J. Thijssen, *Student Member, IEEE*, Eric A. M. Klumperink, *Fellow, IEEE*, Philip Quinlan, *Member, IEEE*, and Bram Nauta, *Fellow, IEEE*

***Abstract*— Analog finite-impulse-response (AFIR) filtering is proposed to realize low-power channel selection filters for the Internet-of-Things receivers. High selectivity is achieved using an architecture based on only a single—time-varying—transconductance and integration capacitor. The transconductance is implemented as a digital-to-analog converter and is programmable by an on-chip memory. The AFIR operating principle is shown step by step, including its complete transfer function with aliasing. The filter bandwidth and transfer function are highly programmable through the transconductance coefficients and clock frequency. Moreover, the transconductance programmability allows an almost ideal filter response to be realized by careful analysis and compensation of the parasitic circuit impairments. The filter, manufactured in 22-nm FDSOI, has an active area of 0.09 mm^2. Its bandwidth can be accurately tuned from 0.06 to 3.4 MHz. The filter consumes 92 μW from a 700-mV supply. This low power consumption is combined with a high selectivity: $f_{-60\,dB}/f_{-3\,dB} = 3.8$. The filter has 31.5-dB gain and 12-nV/$\sqrt{\text{Hz}}$ input-referred noise for a 0.43-MHz bandwidth. The OIP3 is 28 dBm, independent of the frequency offset. The output-referred 1-dB-compression point is 3.7 dBm, and the in-band gain compresses by 1 dB for an −3.7-dBm out-of-band input signal while still providing >60 dB of filtering.**

***Index Terms*— Analog filters, analog FIR filter, FDSOI, filtering-by-aliasing, transconductance DAC (g_mDAC), Internet of Things, linear phase, low noise, low power, low-pass filter, software-defined-radio, tunable.**

I. Introduction

LOW-POWER highly selective channel filters become increasingly important. The trend to connect everyone and everything creates a need for highly selective wireless receivers since the radio environment becomes increasingly crowded. In addition, when targeting Internet-of-Things (IoT) applications, minimal power consumption is desired to increase battery life. A typical zero-IF receiver is shown in Fig. 1. It consists of a low-noise amplifier (LNA), mixer, local oscillator, low-pass filter (LPF), and analog-to-digital converter (ADC). In this article, we target a highly selective integrated LPF with minimal power consumption.

Manuscript received November 29, 2019; revised February 11, 2020; accepted March 17, 2020. Date of publication April 29, 2020; date of current version June 29, 2020. This work was supported by Analog Devices. This article was approved by Associate Editor Lucien J. Breems. *(Corresponding author: Bart J. Thijssen.)*

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Digital Object Identifier 10.1109/JSSC.2020.2987731

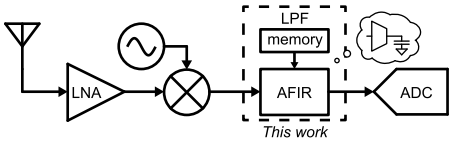

Fig. 1. This work in a receiver.

Conventionally, these LPFs have g_m-C [1], [2] or opamp R-C [3] implementations. Both require multiple transconductors to create higher order filters. These transconductors introduce noise that limits the signal-to-noise ratio (SNR) for a given power consumption. Alternatives are the time-discrete analog infinite-impulse-response (IIR) filters of [4]–[6], but they do not achieve a sharp filter transition.

Analog finite-impulse-response (AFIR) filters [7]–[11], some of which referred to as Filtering-by-Aliasing [12]–[14], have a very sharp filter transition and good out-of-band (OOB) rejection. The most straightforward AFIR filter implementation stores samples of the input signal, provides a weighting coefficient for every time step, and delivers an output sample at the input sampling rate [8], [10]. This requires a lot of storage capacitors for a high filter order. The AFIR filter can be implemented more efficiently by realizing that the output sample rate does not need to equal the input sample rate [7], [11]–[15]. As the filter removes the unwanted signal components (outside the filter bandwidth), the filtered signal can be downsampled without corrupting it by aliasing.

Previous AFIR implementations use a high FIR update rate [12]–[14], cascaded FIR stages [9], or a power hungry transconductor [15] and have, therefore, high power consumption. Reference [11] shows a low-power implementation but has limited OOB rejection and an unattenuated filter alias.

This article is an extension on [16] where we proposed a low-power AFIR filter implementation as a channel selection filter. It contains a single inverter-based g_m-C integrator for maximal SNR per power [17]. The transconductor is implemented as a digital-to-analog converter (DAC): g_mDAC. In the nominal operation mode, the filter bandwidth is 0.43 MHz, which roughly resembles the I/Q baseband bandwidth of a 1-Mb/s IoT-standard, e.g., Bluetooth low energy (BLE). The filter programmability allows for a tunable bandwidth from 0.06 to 3.4 MHz. The power consumption is only 92 μW because of a low FIR update rate, power efficient transconductor, and partially thermometer design. The filter's power consumption is an acceptable fraction of the total power consumption of state-of-the-art IoT receivers [18]–[21].

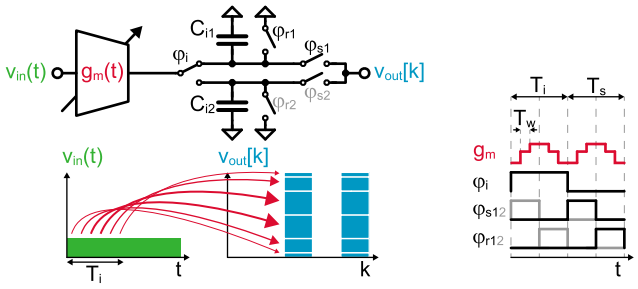

Fig. 2. Analog FIR filter with six filter coefficients.

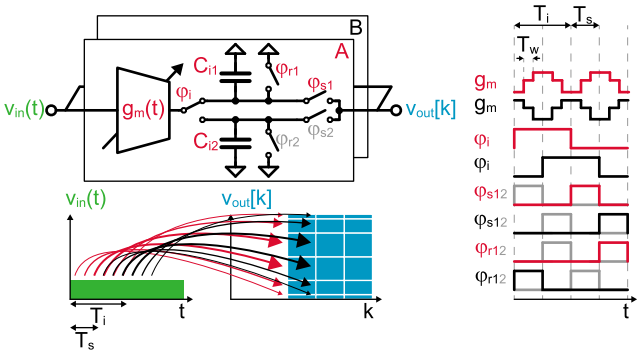

Fig. 3. Two-path time-interleaved analog FIR filter with six filter coefficients ($m = 2$).

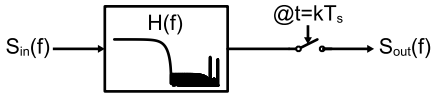

Fig. 4. AFIR filter model.

In this article, a detailed derivation of the AFIR transfer function—including all aliases—is provided. The proposed circuit is analyzed in detail, showing its parasitic impairments, but also providing solutions to mitigate these. Furthermore, additional measurements of the transfer function and distortion give a more complete picture of the filter's performance.

The structure of this article is as follows. In Section II, the AFIR filtering approach is analyzed in detail. Section III discusses the low-power AFIR implementation. A comprehensive analysis of the device impairments due to mismatch and parasitics is described in Section IV. Section V discusses the measurement results, and the conclusions are provided in Section VI.

II. Analog FIR Filtering

In this section, the AFIR filter theory is discussed. First, the architecture is introduced, followed by a detailed analysis of its transfer function and a simple mathematical model, a frequency-domain example, and a summary of how to tune the filter bandwidth.

A. Architecture

Fig. 2 shows a six-tap AFIR filter architecture. In [16], we provide a step-by-step explanation starting from a conventional digital FIR filter to the analog FIR filter of Fig. 2. Here, we just briefly summarize the working principle. For simplicity, the input signal is assumed constant. The input signal $v_{\text{in}}(t)$ is converted to current by a transconductance $g_m(t)$, which varies in time and provides the FIR weights at rate $f_w = 1/T_w$. Different time instances of $v_{\text{in}}(t)$ are weighted differently as in a textbook FIR filter [22]. Starting on an empty capacitor C_{i1}, the weighted current is summed on C_{i1} during the integration phase ϕ_i for integration time T_i. The output is sampled during ϕ_s creating an FIR filtered output voltage $v_{\text{out}}[k]$ sample. Afterward, the voltage on C_{i1} is reset during ϕ_r. Two integration capacitors are used to allow for simultaneous integration of the input and readout at the output. Fig. 2 illustrates the concept using a six-tap AFIR architecture, where the six coefficients are processed in one integration cycle.

B. Time-Interleaving

In Fig. 2, the output sample rate $f_s = 1/T_s = 1/T_i$ and is, thus, limited to the integration time. This constraint is broken by time-interleaving multiple paths: the output sample rate can be increased for the same filter shape and bandwidth. For m paths, this results in an output sample rate

$$f_s = \frac{m}{T_i}, \quad m = 1, 2, 3, \ldots \tag{1}$$

Fig. 3 shows a two-path ($m = 2$) six-tap time-interleaved AFIR filter. The output sample rate is doubled for the same filter transfer function (and FIR coefficients).

C. Filter Transfer Function

The filter transfer function is determined using the time-domain representation of Fig. 3. As illustrated by the different blocks in $v_{\text{out}}[k]$, an output voltage sample consists of N charge contributions. N is the number of filter taps and related to the integration time and weights update time according to $N = T_i/T_w$. The individual charge contributions $q[n]$ become available at

$$t = nT_w, \quad n = \ldots, -1, 0, 1, \ldots \tag{2}$$

The output charge is

$$q[n] = \overline{g_m} w[n] \int_{(n-1)T_w}^{nT_w} v_{\text{in}}(t)\mathrm{d}t \tag{3}$$

where $w[n] = g_m(nT_w)/\overline{g_m}$ is the time-dependent FIR coefficient and $\overline{g_m}$ is the average transconductance. The output voltage samples are available at

$$t = kT_s = k\frac{NT_w}{m}, \quad k = \ldots, -1, 0, 1, \ldots \tag{4}$$

The output voltage samples consist of the sum of N charge contributions during a single integration period

$$v_{\text{out}}[k] = \frac{1}{C_i}\sum_{a=0}^{N-1} q[kN - a]. \tag{5}$$

The input is, thus, integrated over time T_w, sampled at nT_w, weighted by an FIR coefficient, and summed and sampled at

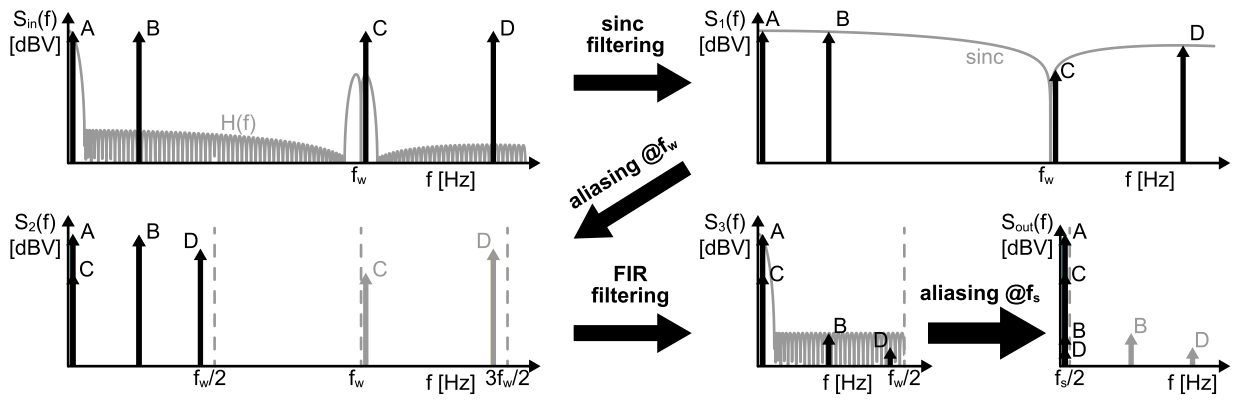

Fig. 5. AFIR filter frequency response example. The filter has four equal power input signals: A, B, C, and D.

kT_s. The reset is implicitly present in (5); output number k contains only charge contributions of one integration cycle.

Since f_w and f_s have an integer relationship and $f_w \geq f_s$, the two sampling actions can be seen as a single sampling action at the lower rate f_s—the first "sampling" by the weighting coefficients does not place the signal in a different position in the f_s Nyquist zones. The output spectrum $S_{\text{out}}(f)$ is derived from the input spectrum $S_{\text{in}}(f)$ by taking the Fourier Transform of (3) and (5)

$$S_{\text{out}}(f) = \sum_{k=-\infty}^{\infty} H(f - kf_s) S_{\text{in}}(f - kf_s) \tag{6}$$

where the harmonic transfer function $H(f)$ is

$$H(f) = \underbrace{\frac{\overline{g_m} T_i}{C_i}}_{\text{gain}} \underbrace{\text{sinc}\left(\frac{f}{f_w}\right) e^{-j\pi \frac{f}{f_w}}}_{\text{windowed } \int} \underbrace{\sum_{a=0}^{N-1} w_a z^{-a}\Big|_{z=e^{j2\pi \frac{f}{f_w}}}}_{\text{FIR}} \tag{7}$$

where

$$w_a = w[N-a], \quad a = 0, 1, \ldots, N-1 \tag{8}$$

are the FIR weighting coefficients, normalized to $\sum w_a = \sum^N w[n] = 1$. (7) was derived in [15] as the ideal FIR transfer function with windowed integration prefiltering. Note that the time varying code $w[n]$ resembles the time-inverse FIR impulse response w_a [12], [13].

Three components can be distinguished in (7): gain, sinc windowed integration, and FIR filter. The FIR filter provides very selective filtering with a sharp filter transition and can be designed to have a linear phase. The windowed integration acts as a prefilter, attenuating the FIR filter aliases at integer multiples of f_w. The gain is determined by $\overline{g_m}/C_i$, which is PVT sensitive. The normalized AFIR filter transfer function is only dependent on g_m ratios and clock frequencies, which is PVT independent (apart from mismatch).

The AFIR filter characteristics can be modeled, as shown in Fig. 4. The input spectrum is filtered by $H(f)$ and sampled afterward at $t = kT_s$.

D. Frequency-Domain Example

In this section, we give an example to provide more intuition of the AFIR filtering function. Fig. 5 shows the step-by-step AFIR filtering operation as indicated by the arrows. Consider an input spectrum $S_{\text{in}}(f)$ consisting of four equal power signals: a wanted signal A and three unwanted signals B, C, and D. The harmonic transfer function $H(f)$ shows the final gain of the input signals. All inputs have a non-zero bandwidth to ensure that they are not completely canceled by a spectral null. The AFIR filters as follows.

1) The signal is sinc filtered. Mainly, C is attenuated.
2) The signal is sampled at f_w resulting in aliasing of C and D. Hereafter, we only consider the signal in the first Nyquist zone: [0 $f_w/2$]. C and D are grayed out at their original positions.
3) The signal is FIR filtered, attenuating B and D considerably.
4) The signal is sampled at f_s resulting in aliasing of B and D to [0 $f_s/2$].

In $S_{\text{out}}(f)$, all signals are in the frequency band [0 $f_s/2$] and fall (almost) on top of each other. However, the previous filtering reduces the signal-to-interference ratio sufficiently not to corrupt the wanted signal A. C is filtered by the windowed integration sinc but is filtered less than B and D. Additional prefiltering is needed, but a first-order low-pass prefilter can significantly reduce this alias if f_w is sufficiently higher than f_s. The same output spectrum can directly be obtained by applying the model of Fig. 4, where the intermediate sampling at f_w is neglected.

E. Designing the Filter Bandwidth

The filter bandwidth and roll-off are determined by the shape of its coefficients and T_i. The filter coefficients can be designed using standard digital FIR filter theory. The number of time-interleaved paths is then determined by the desired f_s. The filter aliases are at integer multiples of f_w. Increasing f_w increases the number of coefficients for the same FIR filter.

The filter bandwidth can be tuned by changing $1/T_i$ proportionally. For example, the bandwidth is doubled by halving T_i; the other parameters can change in two ways.

1) *Double f_w and Constant N;* The frequency offset of the filter aliases, relative to the filter bandwidth, remains constant and, thereby, the sinc suppression of the aliases.

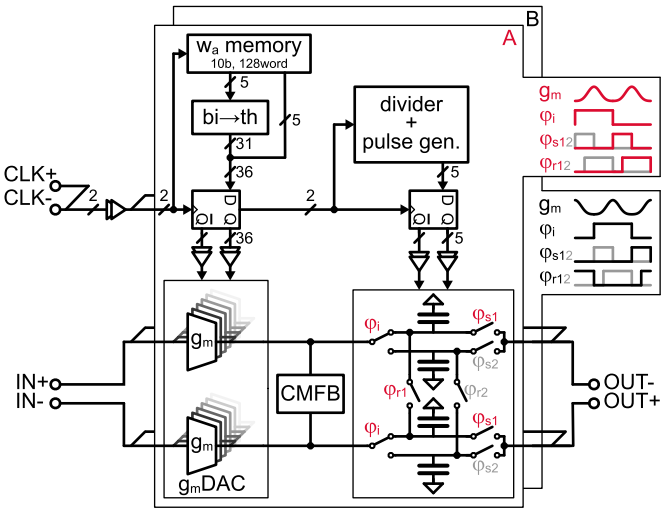

Fig. 6. AFIR circuit implementation.

2) *Constant f_w and Half N:* The frequency offset of the filter aliases, relative to the filter bandwidth, reduces and, thereby, the sinc suppression of the aliases.

Most often, it is desirable to keep the sample-rate to bandwidth ratio constant so that the close-in aliasing at f_s is not changed.

III. Circuit Implementation

Fig. 6 shows the proposed circuit implementation. Two time-interleaved paths (A and B) are implemented to double the output sample rate (1 MHz) for a 2-μS integration time. The nominal filter bandwidth is 0.43 MHz. The variable transconductance is implemented as a pseudo-differential 10-bit transconductance DAC (g_mDAC). The 10-bit g_m tunability is determined from the mismatch analysis, including the number of bits (see Section IV-C). The AFIR g_mDAC code and control logic are reclocked by a differential clock at 64 MHz. The maximum integration time of 2 μS for a 64-MHz g_mDAC update rate requires 128 filter coefficients (FIR taps), which are provided by an on-chip memory for each time-interleaved path. The sample and reset phases partially overlap to ensure that the parasitic capacitances of the PCB and measurement probe are also reset.

The implemented integration capacitor is 20 pF. In this prototype, the capacitor value can be increased 4× by differentially implemented capacitors (not shown) to (partially) compensate for gain variation when changing the bandwidth. The integration capacitors could be reused as a sampling capacitor of an SAR ADC, removing the need for an intermediate buffer. The circuit implementation is described block by block in the following.

A. Digital Control and Memory

The g_m-code and integration capacitor control signals are reclocked in D-flip-flops by a pseudo-differential clock at 64 MHz. The digital power consumption is significantly reduced due to this relatively low update rate compared with previous AFIR designs [8], [9], [14], [15]. However, the filter has aliases around integer multiples of this 64 MHz, as illustrated in Fig. 5. By careful design, we choose to allow these aliases, as they are severely suppressed by the sinc notches. Furthermore, a simple first-order prefilter can sufficiently attenuate these aliases for the 0.43-MHz bandwidth.

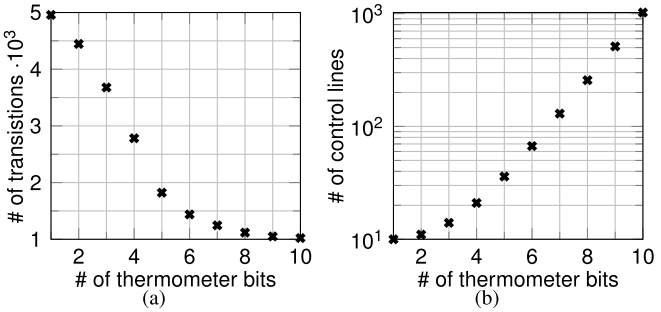

Fig. 7. Partially thermometer implementation of a 10-bit DAC. (a) Number of transitions per output sample. (b) Number of control lines.

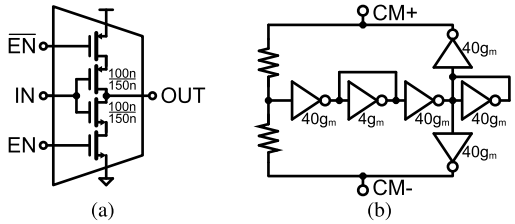

Fig. 8. Circuit implementations. (a) Unit g_m-cell. (b) Common-mode feedback.

When observing a single integration phase, the g_m-value monotonically increases to the g_mDAC maximum, and afterward, it monotonically decreases to the minimum value—the g_mDAC is effectively only turned on/off once during a single integration phase. Therefore, the power consumption of the buffers driving the g_mDAC enable switches can be significantly reduced by implementing the g_mDAC (partially) thermometer coded. Fig. 7(a) shows the number of code transitions versus the number of MSB thermometer bits for a 10-bit g_mDAC; a fully binary-coded DAC contains one thermometer bit. A 5-bit thermometer coded g_mDAC reduces the number of transitions—and, thus, the buffer power consumption—by 2.7× compared with a fully binary design. Furthermore, Fig. 7(b) shows that the complexity of a 5-bit thermometer design is manageable.

Each g_mDAC is controlled by a 10-bit 128-word memory, making the filter code highly reconfigurable.

B. g_mDAC

The g_mDAC is split: 5-bit thermometer and 5-bit binary weighted as determined from the digital control power consumption and g_m-cell mismatch analysis (see Section IV-C). It is constructed from unary g_m-cells of 1.3 μS, which are implemented as shown in Fig. 8(a). The g_m-cell is turned on/off by the enable signal EN. The g_m-cells have a push–pull architecture to double the supply current efficiency. In addition, the g_mDAC current consumption is proportional to the

FIR code—resulting in higher SNR per power consumption than for the current steering design of [15]. The inverter transconductor architecture is very suitable for modern CMOS processes with a low supply voltage.

C. Common-Mode Feedback

The common-mode feedback (CMFB) circuit is shown in Fig. 8(b). The g_mDAC output common mode is set to the voltage of a self-biased inverter, roughly $V_{DD}/2$. The switching of the g_mDAC results in the common-mode charge injection to the output, which is suppressed by the CMFB. The dominant pole of the CMFB loop is placed at CM+ and CM− because the parasitic output capacitance of the g_mDAC is ill-defined. Therefore, C_i is implemented single-ended although a differential implementation would save area. The CMFB circuit has three nondominant poles. Two nondominant poles are at $f_t/2$ and $f_t/10$, which can be very high in a state-of-the-art CMOS process.[1] The third is determined by the CM sensing resistors and the inverter parasitic input capacitance. High CM sensing resistors are chosen, for which the CMFB-loop is stable across PVT in extracted simulations, to minimize charge loss during integration. The power penalty is small: only 20% of the total g_mDAC power consumption. The noise of the center transconductors is the common mode and has no effect on the differential output signal. The noise contribution of the last transconductors is small since g_m is only 40 unit g_m's, ten times smaller than the average g_mDAC code of roughly 400.

D. Practical Considerations

In this work, the AFIR filter is designed with a BLE IoT receiver in mind although the AFIR concept is not limited to this application. In this section, we show that the proposed implementation fits within a BLE receiver design.

The noise factor of the receiver in Fig. 1 is

$$F = 1 + \Delta F_{\text{LNA}} + \Delta F_{\text{Mixer}} + \frac{\overline{v_{\text{in},n}}^2}{A_v^2 kT R_{\text{ant}}} < 4 \tag{9}$$

where ΔF is the respective noise factor contribution, $\overline{v_{\text{in},n}}$ is the input-referred noise voltage of the AFIR filter, A_v is the voltage gain from the antenna to the AFIR filter input, and R_{ant} is the antenna impedance, typically 50 Ω. The noise figure of the state-of-the-art BLE receivers is sub-6 dB ($F < 4$) [18]–[21].

An estimate of the filter's input-referred noise voltage is

$$\begin{aligned}\overline{v_{\text{in},n}}^2 &\approx \frac{\overline{i_n}^2|_{g_m\text{DAC}} + \overline{i_n}^2|_{g_m\text{CMFB}}}{\overline{g_m}^2|_{g_m\text{DAC}}} \cdot 2 \cdot \frac{1}{m} \\ &\approx \frac{4kT\gamma \cdot (400+40) g_m}{(400 g_m)^2}\end{aligned} \tag{10}$$

where k is Boltzmann's constant, T is the absolute temperature, γ is the noise excess coefficient, and $\overline{i_n}$ is the respective average single-ended output noise current from the g_mDAC and CMFB. When assuming $\gamma \approx 2$, the AFIR filter noise factor contribution is about 0.34 for 30-dB LNA + mixer gain and 1.3-μS g_m-cells, which is reasonable for $F < 4$.

[1]In this article, f_t is defined as the unity-gain frequency of an inverter with a self-biased inverter load.

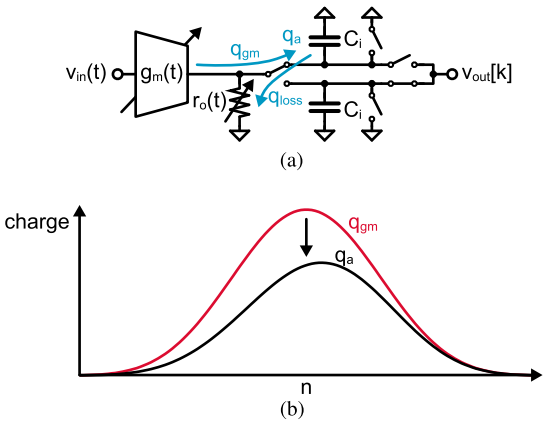

Fig. 9. Effect of limited output impedance. (a) Schematic. (b) Ideal charge q_{g_m} and actual integrated charge q_a at the end of T_i.

The AFIR filter gain can be estimated from (7) as 34 dB for 20-pF integration capacitors. The 34-dB gain is well below the intrinsic gain ($g_m r_o = 162$ in simulation) of the g_mDAC. Therefore, the g_mDAC output impedance has limited effect on the filter's transfer function.

IV. Circuit Analysis and Solutions

The circuit implementation has several practical impairments compared with the theoretical model of Section II. This section analyzes these impairments and provides practical solutions.

A. Output Impedance

A limited output impedance of the g_mDAC results in charge loss during the integration phase. This effect is illustrated in Fig. 9. During integration, previously integrated charge leaks away through parasitic resistance $r_o(t)$. Hence, the effective charge q_a (FIR coefficient) is smaller than the programed charge q_{g_m} of the g_mDAC, more so, for earlier applied coefficients. Although, the effect on the filter transfer function is limited in this design because the dc gain is lower than the g_mDAC intrinsic gain, it is still desirable to compensate for it. The net charge contributions with and without a limited output impedance are shown in Fig. 9(b). The effective FIR code is skewed. The charge contribution q_a to the total charge at the end of integration is

$$q_a = w_a \overline{g_m} r_{o,a} \overline{v_{\text{in}}} C_i \left(1 - e^{\frac{-T_w}{r_{o,a} C_i}}\right) \prod_{b=0}^{a} e^{\frac{-T_w}{r_{o,b} C_i}} \tag{11}$$

where w_a is the coefficient number ($a = 0, 1, \ldots, N-1$) of the g_mDAC and $\overline{v_{\text{in}}}$ is the average input voltage during T_w. The corresponding output resistance $r_{o,a}$ is

$$r_{o,a} = R_{\text{fixed}} \parallel \frac{\mu}{w_a \overline{g_m}} \tag{12}$$

where μ is the transconductor intrinsic voltage gain and $\parallel$ denotes the parallel configuration of the impedances. It contains a fixed component R_{fixed}, from the CMFB sensing

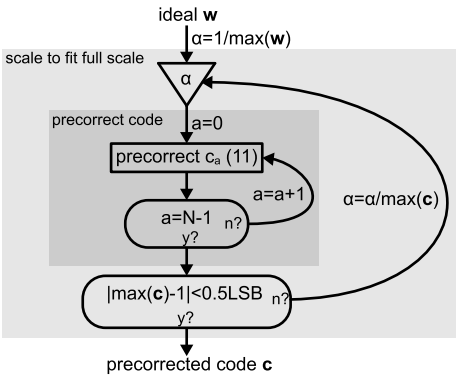

Fig. 10. Algorithm to calculate r_o-precorrected code.

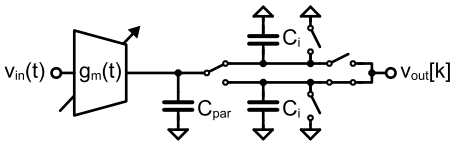

Fig. 11. Parasitic capacitance at the g_m output.

resistors, and the g_mDAC output impedance that varies in accordance with the transconductance value. When high CMFB resistor values are chosen, the fixed term can be neglected.

Fortunately, the filter shape is determined by the relative size of the coefficients. Therefore, a precorrected code can be determined, which takes into account the charge loss and can be applied to the AFIR memory to closely match the effective charge profile with the ideal profile.

The algorithm to calculate the precorrected code $\mathbf{c}$, with coefficient c_a, is shown in Fig. 10. First, the ideal weights are scaled by α. This scaling factor ensures that $\mathbf{c}$ matches the g_mDAC full-scale (normalized to 1) to minimize the quantization error. Therefore, α starts from $1/\max(w_a)$. Starting from $a = 0$ (the last code in time, first of the impulse-response), code c_a is precorrected for all future charge loss. In addition, the instantaneous charge loss during its own integration period has to be corrected. The required coefficient can be derived as

$$c_a = -\frac{\mu C_i}{g_m^{\dagger} T_w} \ln\left(1 - \alpha w_a \frac{g_m^{\dagger} T_w}{\mu C_i} \underbrace{\prod_{b=0}^{a} e^{\frac{T_w}{r_{o,b} C_i}}}_{\text{future loss}}\right) \tag{13}$$

where $g_m^{\dagger}$ is the maximum transconductance. The future loss is corrected by the product of exponentials and the rest compensates for the loss during its own integration period, neglecting R_{fixed} only for its own period. c_a is calculated for all N coefficients. Afterward, $\mathbf{c}$ is compared with the g_mDAC full scale, and α is varied until the precorrected code exactly fits within. The correction can even be applied to a purely resistive transconductor with $\mu = 1$. A similar code precorrection approach, for a purely resistive transconductor with source resistance, is provided in [13].

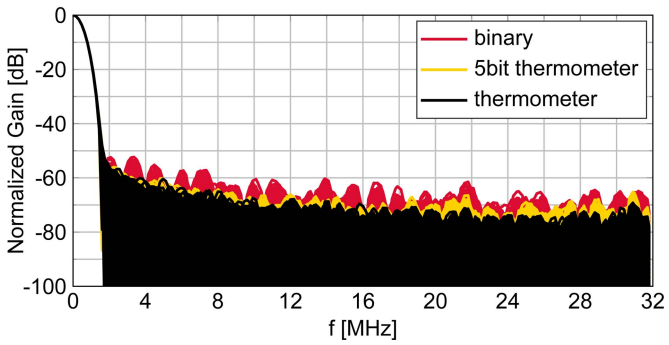

Fig. 12. Transfer function of 500 g_mDAC mismatch realizations for different g_m-code controls.

B. Parasitic Capacitance

The filter transfer function can be affected by the g_mDAC parasitic output capacitance C_{par}, as shown in Fig. 11. The charges of subsequent output samples are shared though C_{par} because this charge is not reset. This results in an additional IIR filtering according to

$$H_{C_{\text{par}}}(f) = \left.\frac{1}{1 - \frac{C_{\text{par}}}{C_{\text{par}}+C_i} z^{-1}}\right|_{z=e^{j2\pi f T_i}}. \tag{14}$$

The extra filtering is at the output of the model in Fig. 4. If significant, this effect can be easily mitigated by resetting the parasitic capacitance during the first T_w integration period, at the loss of only a single filter coefficient.

C. g_m-Cell Mismatch

The filter stopband attenuation is limited by the g_m-cell mismatch of the g_mDAC. Given the simulated mismatch of a single unary g_m-cell ($\sigma_{g_m}/g_m = 10.7\%$), the transfer function is determined for numerous g_mDAC mismatch realizations; neglecting sinc filtering and aliasing. The aggregation of these transfer functions provides an estimate of the worst case filter transfer function, which is shown in Fig. 12 for 500 realizations and a different g_mDAC control. The filter bandwidth and roll-off are unaffected by the mismatch—only the stopband floor level is impacted. The binary controlled transfer functions show spurious responses, which are reduced by >8 dB in the (5-bit) thermometer controlled g_mDAC realizations.

The mismatch realizations of Fig. 12 allow for a more detailed analysis of the implications of the filter transfer function. Fig. 13 shows the cumulative distribution of the g_mDACs that have a certain $f_{-60\text{ dB}}$; for frequencies $f \geq f_{-60\text{ dB}}$, the attenuation is ≥60 dB. The binary coded g_mDACs have unwanted filter spurs as can be recognized from the steps in Fig. 13. The performance is significantly improved when implemented as a thermometer-coded g_mDAC. The 5-bit thermometer coding has similar performance as a fully thermometer coded g_mDAC but adds significantly less complexity. The stopband attenuation can further be improved by mismatch calibration, as done in [12], [13].

Fig. 13 also shows the cumulative distribution for an 8-bit fully thermometer coded g_mDAC with the same MSB g_m size. The performance is clearly reduced compared with

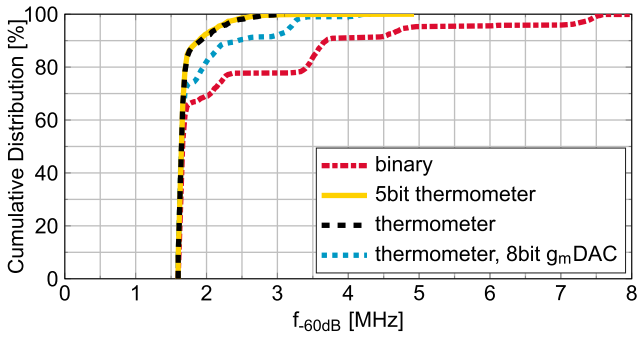

Fig. 13. Cumulative distribution of the 10-bit g_mDACs versus $f_{-60\ \mathrm{dB}}$.

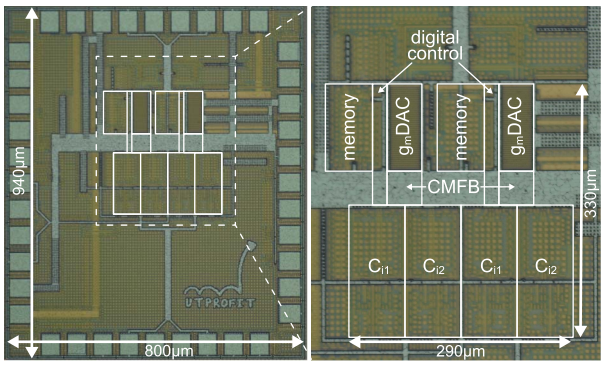

Fig. 14. Chip photograph indicating filter blocks.

a 10-bit design. The 9- and 10-bit designs have similar filter suppression, including mismatch. A 10-bit design is chosen to ensure that the filter performance is not limited by the number of bits.

D. g_mDAC Transient Behavior

The dynamic switching of the g_m-cells in the g_mDAC has an effect on the AFIR filter's performance in terms of circuit and system level. The transient switching behavior has three contributing error sources: charge injection to the input (driving stage) of the filter, settling behavior of the g_m-value, and charge injection to the output. All three effects are common mode since the g_m for the pseudo-differential paths is identical. The injected charge does not, to the first order, disturb the differential wanted signal.

The charge injection to the input, or kickback, is of little concern in the receiver application. The simulated peak-to-peak and rms common-mode voltage variations are <1 mV and <0.1 mV, respectively, when assuming a parallel output impedance of about 24 kΩ and 2pF of the previous stage.[2]

The settling behavior of a switching g_m-cell changes its effective g_m-value. This effect can be compensated by taking into account the error in g_m-value in a transition and compensating for this in the code. Simulations showed that for the proposed design, this was not required.

The effect of charge injection to the output is alleviated by the time-continuous common-mode feedback circuit and by placing the integration capacitors to the ground—providing a low-impedance for the high-frequency common-mode switching signals—as verified by simulations.

Partially thermometer coding of the g_mDAC reduces all three effects by reducing the number of transitions, as discussed in Section III-A.

E. Time-Interleaving Gain Mismatch

The output sample rate is increased by time-interleaving two paths for the same filter shape, which allows for a flexible AFIR design. The g_mDAC mismatch in the two paths results in a gain mismatch—effectively multiplying the input signal with a square wave with frequency $0.5f_s$. The result is spurs at

$$f_{spur} = f_{\mathrm{in}} \pm n \cdot 0.5 f_s, \quad n = 1, 2, 3, \ldots \tag{15}$$

For in-band signals, this creates unwanted distortion components. In an IoT receiver, this is of minor concern. Typically, only low SNR (10–20 dB) is required for demodulation, yet strong suppression of (much larger) interferers is desired, which is realized by the strong filter suppression of >60 dB.

V. Measurement Results

The AFIR filter was designed and fabricated in a 22-nm FDSOI process. The chip operates at a 700-mV supply voltage and has an active area of 0.09 mm^2. Fig. 14 shows the chip micrograph, indicating its major blocks. The FIR code is a Chebyshev window with r_o-precorrection, where r_o is estimated from this simulation. The measurement setup is as discussed in [16]. The charge sharing between the integration capacitors and the measurement probe (and PCB) capacitors results in a gain reduction, which is de-embedded. The gain reduction was estimated as 3.1 dB from the capacitances of extracted simulations and the Teledyne LeCroy AP033 datasheet. The bandwidth is set at 0.43 MHz, unless specified otherwise.

A. Transfer Function

The filter has a dc gain of 31.5 dB. Fig. 15 shows the simulated and measured normalized filter transfer function without g_m-cell mismatch calibration. The measured transfer function is very close to the simulation result, including the very steep transition; the ratio between the 60- and 3-dB attenuation frequencies is only 3.8. The stopband attenuation is limited to about 60 dB at 2 MHz, which can be expected from the mismatch analysis of Section IV-C. The filter aliases at 64 and 128 MHz are suppressed by >45 dB—as expected from the windowed integration sinc filter (7).

The effect of r_o-precorrection is shown in the measurement of Fig. 16(a). The transfer function error is mainly in the transition band. Here, the input varies slowly in comparison to the integration time, requiring the "long-term" accuracy of the coefficients. High offset frequencies are locally canceled during integration and are, thus, affected less by the skewed

[2]12 kΩ is the input impedance of the self-biased g_m-cells that provide the input bias.

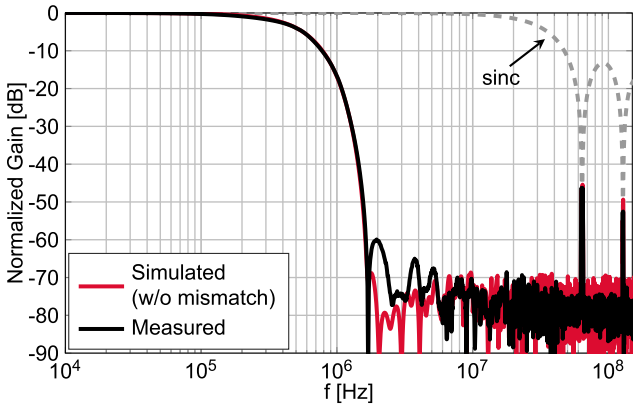

Fig. 15. Measured normalized transfer function at a bandwidth of 0.43 MHz (without calibration).

effective impulse-response. r_o-precorrection clearly improves the filter transition.

The parasitic output capacitance of the g_mDAC was minimized in the design. The measured in-band attenuation is only 0.3 dB compared with the ideal transfer function (7), which is not a significant error in the targeted application.

Fig. 16(b) shows the measured transfer function with and without mismatch calibration of the g_m coefficients after characterizing g_mDAC. g_m-cell mismatch has little effect on the transfer function roll-off. The stopband depth is improved by 8 dB, indicating that the stopband suppression is indeed limited by the g_mDAC mismatch.

Fig. 16(c) shows the filter transfer function for different supply voltages; 700 mV ± 10%. The filter bandwidth is independent of the supply voltage as expected from (7). The transfer functions have only small deviations in the transition and stopband, especially, considering the gain variation of −9 dB (630 mV) and +7 dB (770 mV). All supplies use the same r_o-compensation code, which explains the reduced roll-off for the non-nominal cases. The stopband attenuation is limited for the 630-mV case by the error caused by g_m-cell transitions, while the relative mismatch improves for a larger overdrive voltage. Process and temperature variations will have a similar effect on the filter transfer function. In a practical application, it could be desirable to have some coarse trimming settings to reduce gain and supply current variations.

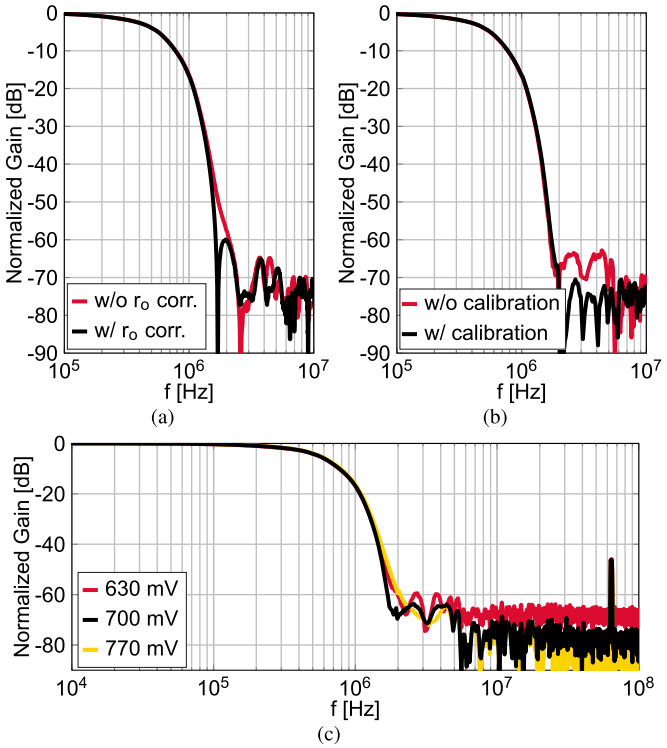

Fig. 16. Measured filter transfer function for 0.43-MHz bandwidth. (a) r_o-precorrection. (b) g_m-cell mismatch calibration. (c) Different supply voltages.

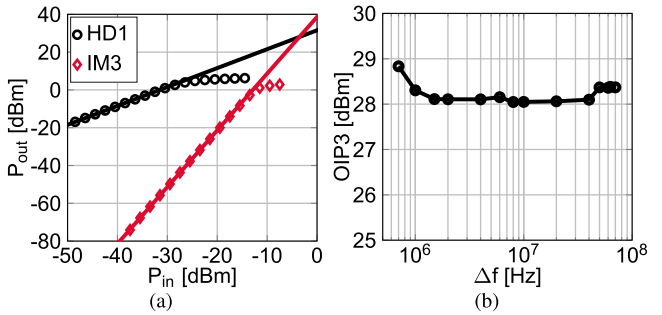

Fig. 17. Measured linearity. (a) In-band gain and out-of-band OIP3. (b) OIP3.

B. Noise and Distortion

In this section, the AFIR filter is characterized for several performance metrics. The measured input-referred noise (IRN) is 12 nV/$\sqrt{\text{Hz}}$, averaged across 0.01–0.43 MHz.

The in-band compression is characterized by the in-band gain shown in Fig. 17(a). The output-referred 1-dB compression point (OP_{1dB}) is 3.7 dBm, which corresponds to almost 1 V_{pp}—70% of the 1.4-V differential voltage range.

The small-signal nonlinearity is characterized by the output-referred third-order-modulation point (OIP3). The IM3 is measured by placing two tones at Δf and $2\Delta f$. In Fig. 17(a), the IM3 is shown for 5.01- and 9.98-MHz signals. The IM3-tone is at 40 kHz, which does not coincide with the aliases of the two input tones. Fig. 17(b) shows the OIP3 for various frequency offsets Δf. The measured OIP3 is 28 dBm and constant for different offset frequencies, which implies that the third-order nonlinearity is dominated by the transconductance rather than the output resistance.

Large OOB signals can degrade the filter performance; 60 dB of filtering is only useful when this dynamic range can also be handled for large blockers. Fig. 18(a) shows the measured in-band gain for a blocker at 5.14 MHz, where the blocker input power is swept. The B_{1dB} is −3.6 dBm, the blocker input power for which the in-band gain is 1-dB compressed. Fig. 18(a) shows a gain increase just before the B_{1dB}. The class-AB biasing of the g_mDAC increases the gain when a large (OOB) signal is applied.

Fig. 18(b) shows the gain of an OOB blocker at 5.14 MHz versus its input power; where the gain is normalized to the

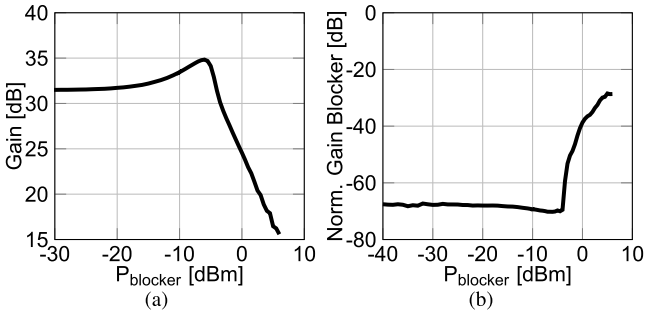

Fig. 18. Measured filter characteristics for a blocker at 5.14 MHz. (a) In-band gain. (b) Normalized gain blocker.

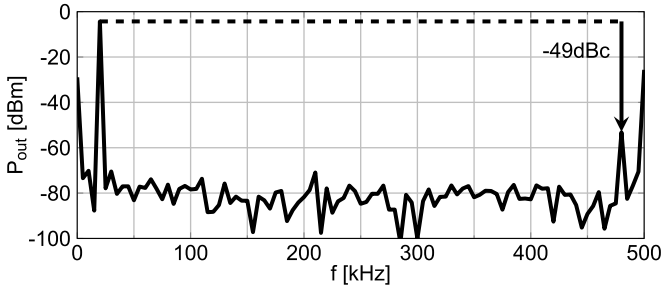

Fig. 19. Measured output spectrum for a 20-kHz input frequency.

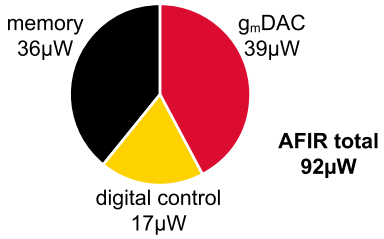

Fig. 20. Power consumption breakdown.

dc gain. The blocker remains attenuated by almost 70 dB up to an input power of −4 dBm, after that the filtering sharply degrades. The input range for OOB blockers is about 400 mV_{pp} differentially, concluding from the in-band gain and large signal filtering in Fig. 18.

Time-interleaving two paths double the output sample rate. However, a spur is expected due to the gain mismatch of the paths (see Section IV-E), which is a consequence of the g_m-cell mismatch. The output spectrum for a 20-kHz input signal is shown in Fig. 19. The time-interleaving spur at −49 dBc is in accordance with the simulated g_mDAC mismatch of about 0.33%. Calibration of the g_mDAC coefficients can reduce this spur. Underestimation, of the CMFB inverter mismatch manifests itself as a dc offset and a tone at 500 kHz of about 30 mV_{pp} differentially, which can be removed by calibration.

C. Power Consumption

Fig. 20 shows the power consumption breakdown. The total power consumption is 92 μW. The power consumption of the digital and analog (g_mDACs, including CMFB) is about equal.

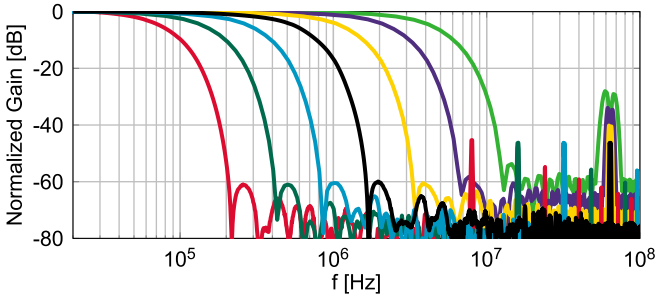

Fig. 21. Measured filter transfer function for different bandwidth settings.

The memory is not specially designed for this application, allowing of further power reduction.

D. Flexibility

The filter is highly reconfigurable. In this section, the flexibility is demonstrated without (significantly) increasing the power consumption. Fig. 21 shows the filter transfer function for bandwidths from 0.06 to 3.4 MHz.

The bandwidth is reduced by decreasing the g_mDAC update rate and g_mDAC output sample rate proportionally. This is accomplished by reducing the input CLK frequency (see Section II-E, option 1). The filter aliases are at lower frequencies because the g_mDAC update frequency is reduced.

The bandwidth is increased by reducing the number of coefficients while maintaining the same CLK frequency (see Section II-E, option 2). The filter alias remains at 64 MHz; the number of filter coefficients is reduced. The filter alias is attenuated less because it has a larger bandwidth for the same sinc windowed-integration filter. The power consumption is only increased by 10% for a filter bandwidth of 3.4 MHz.

E. Comparison

The proposed filter performance summary and a comparison to state-of-the-art power-efficient filters are shown in Table I. This work achieves the lowest power consumption in combination with a very sharp transition band. Reference [9] has a sharper filter transition but at >90× more power consumption. The filter IRN is low, and the linearity is competitive. The active chip area is relatively small.

When comparing the classical opamp R-C and g_m-C filters with the recent digitally controlled analog FIR and IIR filters, the FIR and IIR analog filters show very strong potential in modern CMOS processes. Digital control is attractive as it only consumes dynamic power, while its power consumption scales down with technology and low supply voltages. The proposed AFIR approach allows for a very steep filter with a single transconductor to maximize the SNR for given power consumption. The programmability of the proposed AFIR implementation not only allows for a flexible filter shape and bandwidth but can also be deployed to reduce the effect of circuit impairments, e.g., the limited output impedance of a transconductor.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[6] VLSI'17	[9] JSSC'13	[4] JSSC'14	[3] JSSC'09	[1] JSSC'10	[2] CICC'17	[5] TCAS-I'18
Topology	128-tap AFIR	Passive IIR	Cascaded AFIR	g_m-C IIR	Opamp RC	g_m-C	g_m-C	g_m-C IIR
Supply voltage [V]	0.7	1.2	1.2	1.2	0.55	2.5	1.3	1.8
Power cons. [mW]	0.092	0.15	8.4	1.98	3.5	1.26	0.65	4.3
$f_{-3\mathrm{dB}}$ [MHz]	0.06-3.4[a]	0.54	5-26	0.4-30	11.3	2.8	20	0.49-13.3
$f_{-60\mathrm{dB}}/f_{-3\mathrm{dB}}$	3.8	10[b]	1.5[c]	7.8[c]	-	5.9[b]	4.8[c]	7.5[c]
Gain [dB]	31.5	0[c]	41	9.3	0	15	0	17.6
IRN [nV/$\sqrt{\mathrm{Hz}}$]	12	23.3	12	4.57	33	23	15.3	6.54
OP_{1dB}[e][dBm]	3.7	-	-	10	−0.5	-	6.3	12.93
OOB OIP3[f][dBm]	28	55.1	13[d]	21	13	50.6	28.8[d]	32.63
B_{1dB} [dBm]	-3.7	-	-	-	-	-	-	-
Technology	22 nm FDSOI	130 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	90 nm CMOS	180 nm CMOS	180 nm CMOS
Active Area [mm^2]	0.09	0.06	0.52	0.42	0.43	0.5	0.12	2.9

[a] Other specifications are measured at 0.43MHz; [b] Extrapolated from figure; [c] Estimated from figure; [d] In-band;
[e] $OP_{1dB} = P_{1dB}$ + Gain - 1; [f] OIP3 = IIP3 + Gain;

VI. CONCLUSION

An analog FIR filter architecture is proposed to serve as a channel selection filter for low-power receivers. It employs a hardware efficient implementation that requires only two 10-bit pseudo-differential transconductor DACs (g_mDACs) and four integration capacitors to obtain a 128-tap FIR filter.

The bandwidth is accurately tunable from 0.06 to 3.4 MHz. Very sharp filtering is obtained, and the stopband attenuation at small frequency offsets—3.8× the −3 dB bandwidth—is 60 dB, without g_m-cell mismatch calibration. A low power consumption (92 μW) is achieved by the single transconductor (g_mDAC) design with a low update rate and 5-bit thermometer coding. The filter shows the constant in-band gain and filtering for blockers with an input power of up to −4 dBm.

The AFIR filter's low power consumption and high selectivity enable future IoT receivers in an increasingly crowded wireless environment. Furthermore, the programmability supports the software-defined IoT receivers.

ACKNOWLEDGMENT

The authors would like to thank G. Wienk for CAD assistance, H. de Vries and A. Rop for measurement support, and their other colleagues from the ICD Group for fruitful discussions. They would also like to thank Y. Sudarsanam and B. Uppiliappan from Analog Devices Boston for the memory and decoder design and GlobalFoundries for silicon donation.

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