ELECTRICAL CHARACTERISTICS OF B^+ AND BF_2^+ IMPLANTED POLY-Si AND POLY-Ge_xSi_{1-x} AS GATE MATERIAL FOR SUB-0.25μm APPLICATIONS

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ABSTRACT

The electrical properties of p-type doped poly-Si and poly-Ge_xSi_{1-x} (x~0.3) gate material were studied. The effect of dopant concentration and anneal temperature on the electrical behavior of these polycrystalline layers is investigated. A lower sheet resistance, higher Hall mobility and higher dopant activation is found for Ge_xSi_{1-x} compared to Si at equal doping levels. MOS capacitors with B^+ and BF_2^+ implanted gates were used to study boron penetration. Boron penetration is similar for $Ge_{0.3}Si_{0.7}$ and Si. Gate depletion is dependent on the dopant activation hence Ge_xSi_{1-x} offers the possibility for lower gate depletion compared to Si.

INTRODUCTION

The downscaling of devices in modern IC-technology gives rise to conflicting demands on the process steps used. Sub-0.25μm MOS technology requires both thin gate oxides (~5nm), shallow source and drain junctions (<0.1μm), highly doped gate material (> $10^{20}cm^{-3}$) and low temperature budgets. A severe problem is the penetration of boron from p^+-doped gates through thin gate oxides. This problem is even more severe when BF_2^+ is used as a dopant ion instead of B^+. Not only is the boron penetration larger with decreasing gate oxide thickness but also with increasing fluorine dose and higher anneal temperature [1]. Therefore low process temperatures are needed. However when the anneal temperature is too low gate depletion becomes a problem. Polycrystalline-Ge_xSi_{1-x} is an interesting gate material

for sub 0.25μm processes [2] because of its process compatibility, high dopant activation at low temperatures and possibility to manipulate the workfunction. In this paper results of a study on the use of poly-Ge_xSi_{1-x} as gate electrode will be reported.

EXPERIMENTAL

Polycrystalline Si and Ge_xSi_{1-x} layers (500 nm) were grown in a conventional hot wall Low Pressure Chemical Vapor Deposition (LPCVD) reactor using SiH_4 (silane) and GeH_4 (germane) as reactive gasses. These layers were deposited on n-type Si(100) wafers covered with either a thick isolating SiO_2 layer (Hall experiments) or a thin (10 nm) gate oxide layer. The samples were doped with B^+ or BF_2^+ by means of ion implantation and than further processed to obtain van der Pauw structures and MOS capacitors. The anneals were performed in an furnace using an N_2 ambient. The Hall measurements were performed using a 0.1T magnet.

RESULTS

Resistance and activation

The B^+ doped samples show a lower sheet resistance for poly-$Ge_{0.3}Si_{0.7}$ than for poly-Si after an anneal of 800 °C for 60 min. This is caused by both higher activation and higher mobility, as can be seen in figure 1. The hole mobility is related to the Hall mobility by a scattering factor r_H. The BF_2^+ doped samples have a higher sheet resistance than their B^+ doped counterparts, see figure 2.

After the activation of the dopants, usually other process steps follow ,e.g. deposition of an oxide isolation layer. The temperature budget of these steps has to be as low as possible for compatitive silicidation etc. However lower temperatures can lead to deactivation of the dopants. Figure 3 shows the dopant deactivation by measurement of the sheet resistance after the second anneal at 750 °C. The first anneal of 5 min 950 °C led to almost 100% activation. The increase is caused by deactivation only and is 50% for Si and only 10% for $Ge_{0.3}Si_{0.7}$. After an additional anneal of 5 min 950°C the deactivation is completely undone.

Gate depletion

Although boron diffusion in poly-Ge_xSi_{1-x} is more difficult than in poly-Si after 60 min 800 °C a flat doping profile is found, the first demand to minimize gate depletion. The higher dopant activation of poly-Ge_xSi_{1-x} at equal implantation dose and temperature budget leads to less gate depletion. Simulations of gate depletion

were done to study the impact of higher activation on gate depletion, see figure 4. The 50% activation of the 10^{20} cm^{-3} boron concentration for Si (see figure 1) leads to e.g. 9 and 4% gate depletion for 6 and 10 nm gateoxide thicknesses respectively. An 80% dopant activation as can be seen for $Ge_{0.3}Si_{0.7}$ leads to 7 respectively 3.5% gate depletion. Hence Ge_xSi_{1-x} offers a significant reduction in gate depletion and offers possibilities to lower temperature budgets.

CV-measurements

Using BF_2^+ as a dopant atom instead of B^+ has the advantage that shallow junctions can be created. A high concentration of fluorine in the gate however leads to enhanced boron diffusion through thin gate oxide especially at higher process temperatures. For any type of gate material is therefore, essential that the diffusion of boron through the gate oxide is as low as possible. From figure 5 it can be seen that using $Ge_{0.35}Si_{0.65}$ the boron diffusion problem occurs at approximately equal anneal conditions as for poly-Si. In this figure we also see the expected change in flatband voltage due to the manipulation of the workfunction, when Ge is added to form the Ge_xSi_{1-x} alloy. Since the activation of dopants can be achieved at lower temperature budgets for the GeSi alloy than for Si the change of having boron diffusion is diminished when using a poly- Ge_xSi_{1-x} gate.

CONCLUSIONS

We have shown that the use of p-type doped poly-Ge_xSi_{1-x} gate material does not only give the possibility to change the work function but could lead to lower process temperatures and still achieve good activation and reduce gate depletion and boron diffusion through thin gate oxides.

ACKNOWLEDGMENTS

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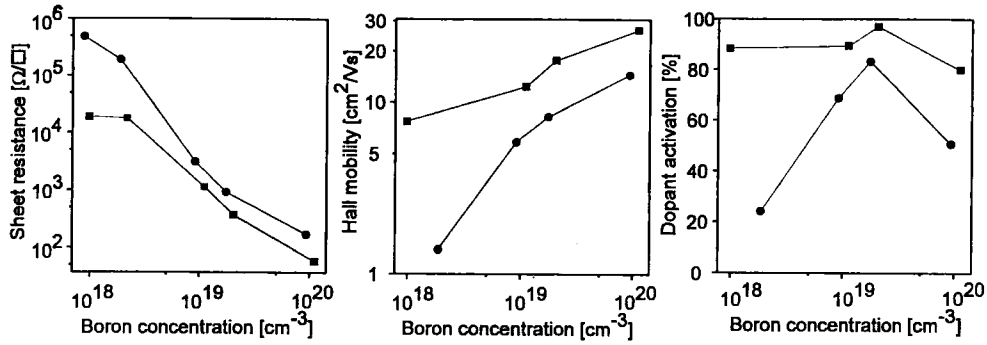

Figure 1: Sheet resistance (left), Hall mobility (middel) and Hall dopant activation (right) of 500 nm thick B^+ doped poly-Si (●) and poly-$Ge_{0.3}Si_{0.7}$ (■) after 60 min 800 °C anneal.

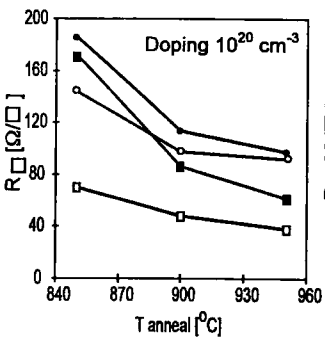

Figure 2: $R_{\square}$ for B^+ (open) and BF_2^+ (filled) Si (dots) and $Ge_{0.35}Si_{0.65}$ (squares). Anneal time 30 min.

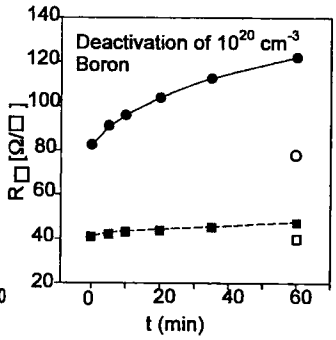

Figure 3: $R_{\square}$ after 5 min 950°C and t min 750°C for Si (●) and $Ge_{0.3}Si_{0.7}$ (■). Additional 5 min at 950°C (open symbols).

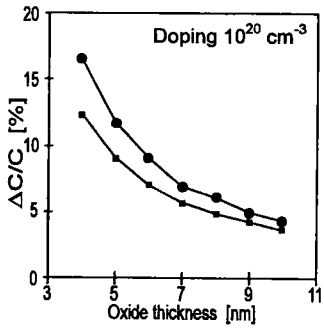

Figure 4: Simulation of gate depletion of Si(●) and $Ge_{0.3}Si_{0.7}$(■) after 800°C 60 min.

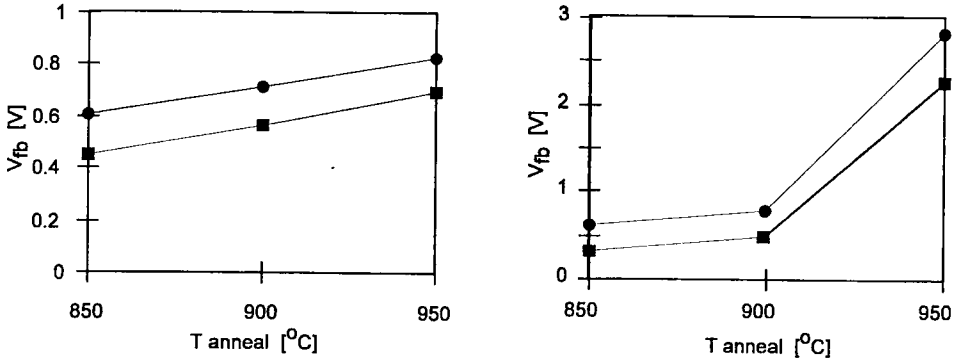

Figure 5: Flatband voltages for B^+ (left) and BF_2^+ (right) doped Si (●) and $Ge_{0.35}Si_{0.65}$ (■) in MOS capacitors with 10 nm gateoxide thickness. Dope level 10^{20} cm^{-3}.