A low-voltage CMOS Op Amp with a rail-to-rail constant-g_m input stage and a class AB rail-to-rail output stage

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Abstract - **In this paper a low-voltage two-stage Op Amp is presented. The Op Amp features rail-to-rail operation and has an input stage with a constant transconductance (g_m) over the entire common-mode input range. The input stage consists of an n- and a p-MOS differential pair connected in parallel. The constant g_m is accomplished by regulating the tail-currents with the aid of an MOS translinear (MTL) circuit. The resulting g_m is constant within 5%.**

The common-source output stage employs a feedback circuit which also contains an MTL circuit. This feedback circuit ensures class AB operation and prevents the transistors in the output stage from cutting off.

The Op Amp will be realized in a semi custom CMOS process with minimum channel lengths of 10μm. Simulations show that the minimum supply voltage is less than 2.5 V. A unity gain bandwidth of 550 kHz and a DC voltage gain larger than 80 dB are feasible. The input range exceeds the supply rails, whereas the output range reaches the rails within 130 mV.

I. INTRODUCTION

In this paper a low voltage two stage CMOS Op Amp is presented. The structure of the Op Amp is depicted in fig. 1.

In order to obtain an input stage with a rail-to-rail input range, an n- and p-channel pair have to be driven in parallel. Without precautions the small signal transconductance (g_m) of such a combination depends on the common input voltage because the differential pairs will cut off nearby one of the supply rails. This is an unwanted phenomenon as it prevents an optimal frequency compensation. A constant transconductance is realized by common input voltage dependent biasing of the input pairs using an MOS translinear (MTL) circuit [1]. Furthermore, offset differences between the n- and the p-pair and the fast transition between both pairs on and one pair on can result in a poor CMRR [2]. An improvement of the CMRR is achieved by making the transition range as large as possible. Besides the parallel input pairs with constant g_m circuit the input stage contains two cascode stages in parallel which drive the output transistors.

An output stage which combines a rail-to-rail output range and a low quiescent power consumption requires class AB controlled output transistors in a common-source configuration. The output stage presented in this paper employs an MTL circuit in a local feedback loop so as to ensure class AB operation and to prevent the output transistors from switching off. This has to be avoided because it will deteriorate the HF behaviour and the step response. Unlike other solutions, e.g. [3], this feedback circuit does not contain any transistors that may cut off. The feedback circuit senses the currents through the output transistors and drives a differential pair (M_{d1}/M_{d2}) which in turn controls the voltages at the gates of the output transistors (fig. 1).

II. A CONSTANT-g_m INPUT STAGE

An input stage with a constant transconductance and an improved CMRR with input pairs operating in weak-inversion has been presented previously [2]. However, input pairs in weak-inversion often have the drawback of a smaller transconductance which results in a lower cut-off frequency. The input stage presented in this paper therefore employs input pairs operating in strong-inversion. A constant trans-conductance in strong-inversion requires the following relation between the tail currents I_{sn} and I_{sp} of the differential pairs:

$$\sqrt{K_n \cdot I_{sn}} + \sqrt{K_p \cdot I_{sp}} = \text{constant} \qquad (1)$$

$$\text{with: } K = \mu C_{ox} \frac{W}{L}$$

Assuming that $K_p = K_n$ this relation becomes:

$$\sqrt{I_{sn}} + \sqrt{I_{sp}} = \text{constant} \qquad (2)$$

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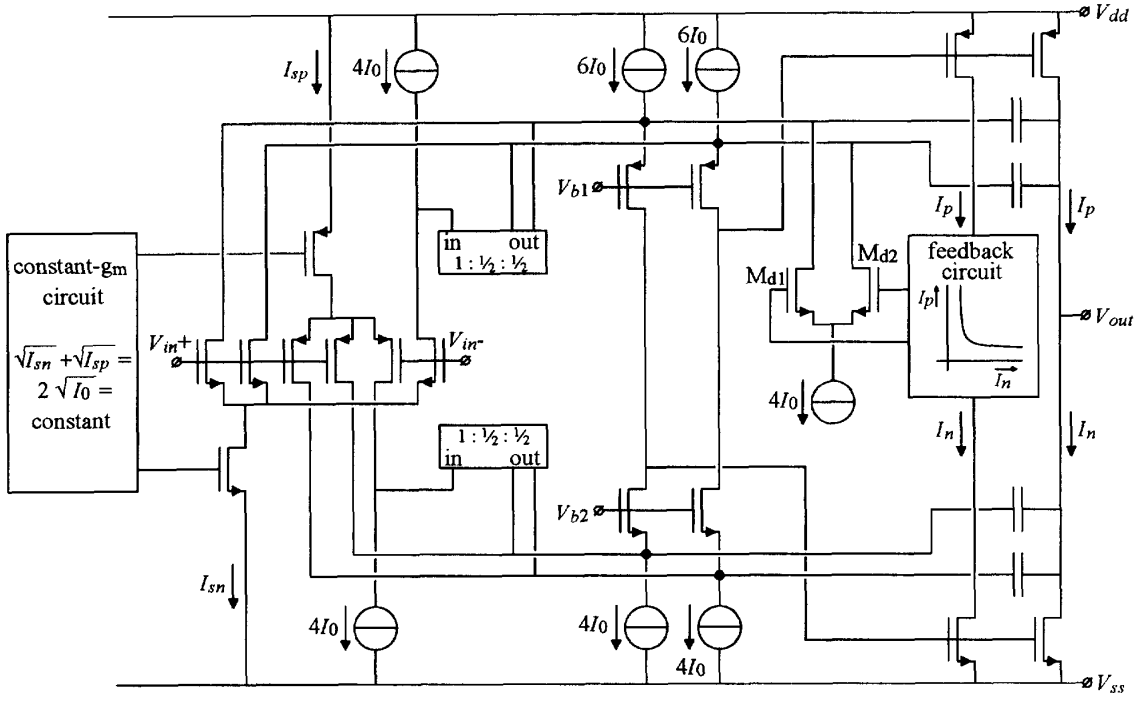

Fig. 1. The structure of the realized Op Amp.

A circuit that forces this relation is shown in fig. 2. The transistors M1, M2, M3 and M4 are connected in an MOS translinear loop [1] and the following relation between the drain currents can be derived:

$$\sqrt{I_{sn}} + \sqrt{I_{sp}} = \sqrt{I_0} + \sqrt{I_0} \qquad (3)$$

Therefore, equation (2) is satisfied. The actual value of I_{sn} and I_{sp} are defined by a second condition, which is forced by the differential pair M5/M6 and a current mirror:

$$I_{sp} - I_{sn} = 4\alpha \cdot I_0 \qquad (4)$$

$$\text{with: } -1 \le \alpha \le 1$$

The factor α is dependent on the differential input voltage of the differential pair M5/M6, and thus on the common-mode input voltage of the complete Op Amp. Note that I_{sn} - I_{sp} never exceeds the value $4I_0$, which is the tail-current of the differential pair M5/M6. The transition range can be adjusted by choosing the aspect ratios of M5 and M6.

Instead of forcing the difference I_{sp}-I_{sn} into the translinear loop, we could also sense I_{sn} and use the translinear circuit to create I_{sp} (or vice versa) [4]. However, a problem arises when I_{sn} becomes very small. Transistor M3 will then start to operate in weak inversion resulting in a much lower gate-source voltage than expected. The gate-source voltage of M1 will now become too large and as a result Isp will also be too large. This problem does not occur in the presented solution because I_{sp}-I_{sn} is limited to $4I_0$ (4). In the final realization the input pairs are partly split (fig. 1) to enable the feedback circuit to control the gates of the output transistors seperately.

III. A Class AB Output Stage

The purpose of the class AB control circuit is to prevent the output transistors or any other transitors in the circuit from switching off, as this would deteriorate the step response of the stage. If the drain current of the n-channel output transistor (I_n) becomes very large the current through the p-type output transistor (I_p) has to be limited to a minimum value (I_{min}) and vice versa. The computer program MTLPLOT [5] was used to find the following equation, that can be implemented in an MTL circuit:

$$\sqrt{\frac{1}{2} I_{min}} + \sqrt{I_n + I_p - I_{min}} = \sqrt{I_n - \frac{1}{2} I_{min}} + \sqrt{I_p - \frac{1}{2} I_{min}} \qquad (5)$$

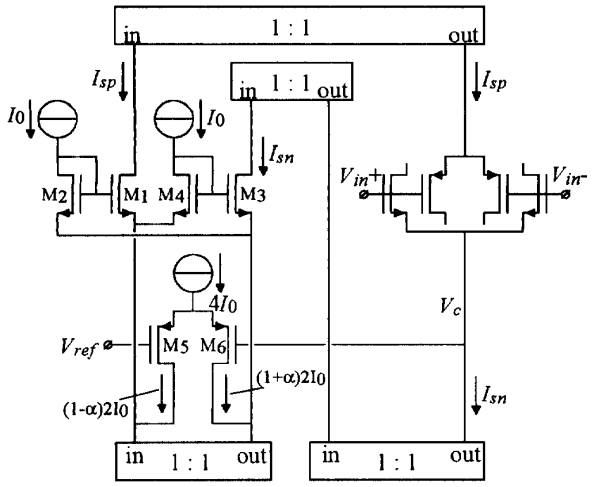

Fig. 2. The constant-g_m input stage.

Figure 4 shows a plot of the resulting relation I_p versus I_n. An implementation of equation (5) prevents the output transistors as well as any transistor in the feedback circuit from switching off.

An output stage using an MTL loop based on equation (5) is depicted in fig. 3. The actual MTL loop is formed by M_{o1}, M_{o2}, M_{o3} and M_{o4}. If the loop is in equilibrium (i.e. the loop equation (5) is valid) then the differential input voltage of the differential pair M_{d1}/M_{d2} will be zero. If I_n or I_p becomes smaller than I_{min}, which does not agree with the loop equation (5), V_2 will become larger than V_1. The differential pair M_{d1}/M_{d2} is connected to the cascode stage in such a way that this will result in larger gate-source voltages of the output transistors and the equilibrium will be restored.

IV. Simulation and Measurement Results

A two stage Op Amp using the above mentioned stages has been simulated and will be realized in our semi-custom CMOS process with minimum channel lengths of 10μm and threshold voltages of 0.63V (n-channel transistors) and -0.77V (p-channel transistors). Simulations show that the transconductance of the input stage is constant within 5%.

The complete Op Amp was frequency compensated using four Miller capacitors as is shown in fig. 1. The specifications of the complete Op Amp are shown in table 1. The unity gain frequency of 550 kHz is mainly limited by the minimum channel lengths used (10 μm).

V. Conclusions

An Op Amp has been realized with a unity gain frequency of 550 kHz which is limited because of the minimum channel lengths of 10μm. The Op Amp contains a constant-g_m input

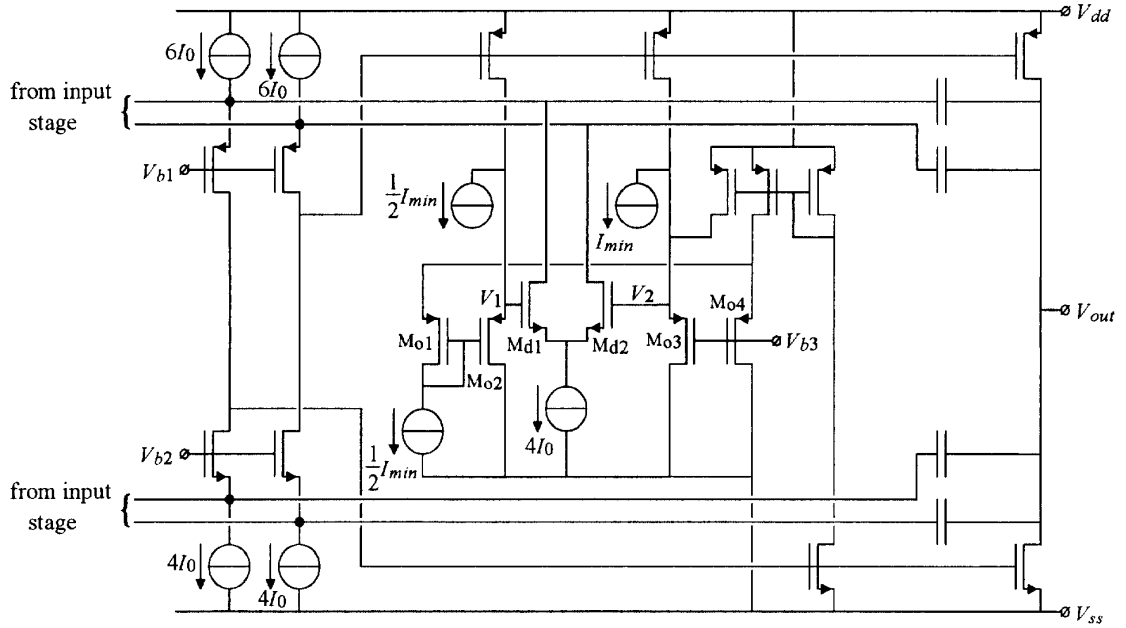

Fig. 3. The class AB output stage.

Simulated specifications V_{supply}=3V, R_{load}=1kΩ, C_{load}=15pF,Temp.=27°C	
GBW	550 kHz
PM	65°
DC-gain	> 80 dB
Input voltage range	exceeds V_{ss} and V_{dd}
Output voltage range	V_{ss}+0.13V...V_{dd}-0.13V
Min. supply voltage	< 2.5 V
Total supply current	650 µA

Table 1. Specifications of the complete Op Amp.

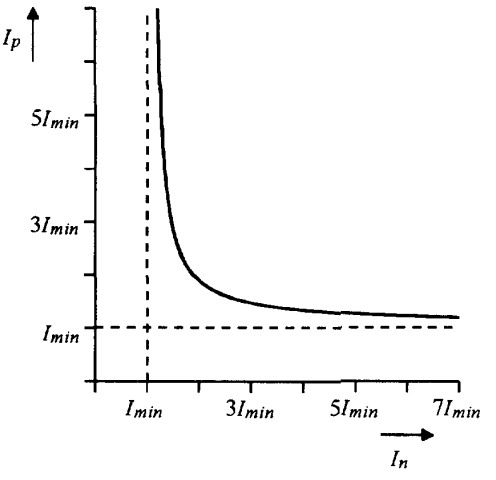

Fig. 4. The relation between I_p and I_n resulting from (5).

stage and the transconductance shows a deviation of less than 5% throughout the input range. The class AB output stage prevents its transistors from cutting off. This improves the high frequency behaviour and the step response of the stage.

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