Analysis of Switched Capacitor Losses in Polar and Quadrature Switched Capacitor PAs

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***Abstract*—This paper derives the efficiency limitations of switched capacitor power amplifiers (SCPAs) due to switched capacitor (SC) losses during charging and discharging of their capacitor arrays. Polar modulation is covered, as well as quadrature modulation both with clock duty cycles of 50% (Q50) and 25% (Q25). Closed form expressions are derived for both the maximum output power and SC power loss for signals with arbitrary phase and amplitude. These expressions are verified by simulations using ideal switches and capacitors, and 22 nm CMOS transistor models. These results are used to analyze the SCPA efficiency for 64QAM signals using a statistical model. It is shown that for a given array capacitance and supply voltage, the polar architecture is the most power efficient. Compared to polar modulation, the SC loss for 64QAM is fundamentally 18% higher for Q50 and 46% higher for Q25 SCPAs, whereas the generated output powers are fundamentally 6 and 3dB lower, respectively.**

***Index Terms*—Class-D power amplifier (PA), SCPA, radio frequency digital-to-analog converter (RF-DAC), digital PA, polar transmitter, quadrature transmitter**

I. Introduction

SWITCHED capacitor (SC) circuits have been popular since the 1970's for processing signals with high precision due to the accurate matching of capacitors and their good linearity [1]. More recently, SC circuits have been employed in radio frequency (RF) power amplifiers (PAs) [2]–[9]. These switched capacitor power amplifiers (SCPAs) offer a very good linearity and moderate power efficiency. Multiple SCPA architectures have been proposed.

Figure 1a indicates a polar SCPA [2] with a total array capacitance C divided over N uniformly sized slices. These are controlled by the thermometer coded differential base band (BB) input signals n_+ and n_- with common mode level $N/2$. This is upconverted to RF using a digital mixer with a phase modulated local oscillator (LO). This way, the input codes control the number of toggled slices and the LO determines the switching moment, giving a modulation in relative amplitude α and phase ϕ_0 of the RF output signal, respectively.

Alternatively, the RF output signal can be generated using a quadrature architecture as in Figure 1b. n_1 to n_4 are the thermometer coded differential quadrature BB input signals with common mode level $N/2$. An SCPA using quadrature modulation with a clock duty cycle of 50% (Q50) is made by connecting the outputs of two sub-SCPAs with $C/2$ capacitance each and 90° phase shifted LOs. This yields a capacitive divider, combining the quadrature signals [3].

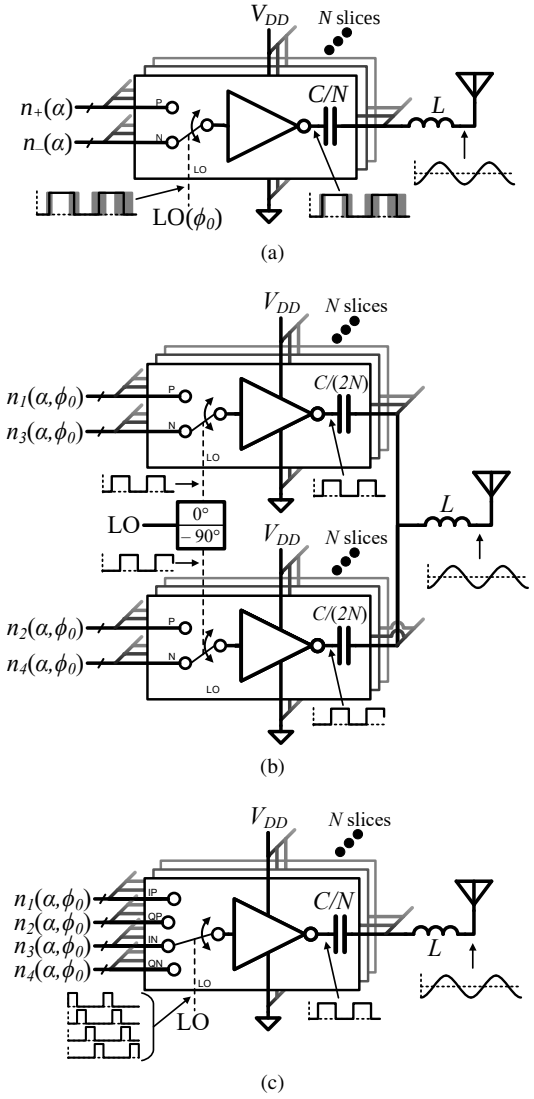

Fig. 1. Single ended implementations of common SCPAs architectures. (a) Polar SCPA. (b) Q50 SCPA consisting of two sub-SCPAs with $N/2$ slices each. (c) Q25 SCPA.

A quadrature architecture could also be implemented using I/Q sharing [4] using a four-phase mixer and a single sub-SCPA as in Figure 1c. This will be referred to as a quadrature modulation with a clock duty cycle of 25% (Q25) SCPA.

The Thévenin equivalent output voltages for the different SCPAs up to the series inductor are indicated in Figure 2a to

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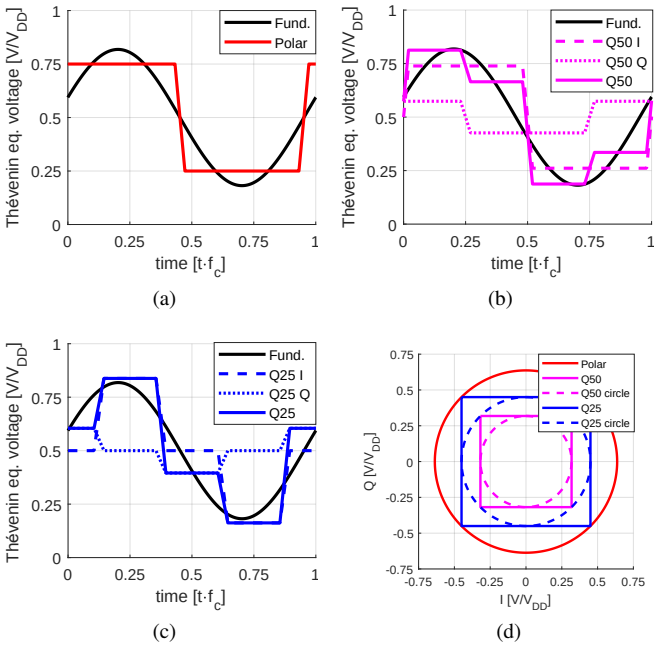


Fig. 2. Waveforms resulting in the same fundamental for (a) polar (b) Q50 and (c) Q25 SCPAs. (d) Maximum instantaneous output amplitudes in the complex plane.

2c. In Figure 2d, their maximum instantaneous output amplitudes are indicated, along with the inscribed circle, indicating the maximum output amplitude that can be generated at an arbitrary phase.

For all architectures, a sinusoidal signal is generated to model narrow-band communications around angular carrier frequency ω_c, with an instantaneous phase ϕ_0 and amplitude $\alpha\hat{A}$, where α is a value between 0 and 1, indicating the back-off from maximum output amplitude $\hat{A}$:

$$v_{out}(t) = \alpha\hat{A}\sin(\omega_c t + \phi_0) \tag{1}$$

In section II, III and IV, a set of equations is derived for the output power and SC losses in polar, Q50 and Q25 SCPAs, respectively. Section V relates these loss models to efficiency enhancement techniques. In section VI, these relations are verified using simulations with both ideal switches and transistor models and efficiency for 64QAM is analyzed using a statistical model. Section VII concludes this work.

II. Polar SCPAs

The output power $P_{out,pol}$ and SC loss $P_{SC,pol}$ for polar SCPAs have been discussed in [2] and are summarized here for reasons of comparison.

A. Polar input codes and output power

The open-circuit output voltage v_{pol} and array input capacitance C_{in} for the polar SCPA in Figure 1a are modeled in Figure 3a, with $\Delta n = n_+ - n_-$ toggled slices. Here:

$$v_{pol}(t) = \begin{cases} \frac{n_+}{N}V_{DD}, & \text{for } 0 < \omega_c t - 2k\pi + \phi_0 < \pi \\ \frac{n_-}{N}V_{DD}, & \text{otherwise} \end{cases} \tag{2}$$

where $k \in \mathbb{Z}$

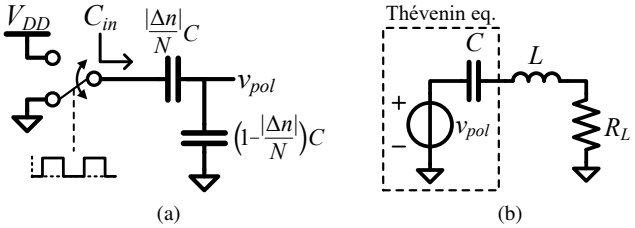


Fig. 3. (a) Open-circuit model for the capacitive divider in a polar SCPA. (b) Thévenin equivalent circuit with tuning inductance and load.

The loaded output voltage can be found using the Thévenin equivalent circuit of the SCPA in Figure 3b. The LC tank in the SCPA is designed to form a band-pass filter around f_c, such that the output voltage can be approximated by the fundamental of the Fourier series of Equation 2 [2]:

$$v_{pol,1}(t) = \left(\frac{n_+}{N} - \frac{1}{2}\right)\frac{4V_{DD}}{\pi}\sin(\omega_c t + \phi_0) \tag{3}$$

By equating this to Equation 1, it can be found:

$$\hat{A}_{pol} = \frac{2V_{DD}}{\pi} \tag{4a}$$

$$n_\pm = \left(\frac{1}{2} \pm \frac{\alpha}{2}\right)N \tag{4b}$$

The resulting output power is:

$$P_{out,pol} = \frac{(\alpha\hat{A}_{pol})^2}{2R_L} = \frac{2\alpha^2 V_{DD}^2}{\pi^2 R_L} \tag{5}$$

B. Polar switched capacitor loss

During a code transition, the inductor blocks instantaneous current changes, and the current through the inductor and load can be neglected. This renders the circuit in Figure 3a adequate for modeling SC loss. For a polar SCPA, the number of toggled capacitors relates to back-off as $|\Delta n| = \alpha N$. The input capacitance follows as:

$$C_{in,pol} = \frac{|\Delta n|}{N}\left(1 - \frac{|\Delta n|}{N}\right)C = \alpha(1-\alpha)C \tag{6}$$

During the two switching moments in a carrier period $1/f_c$, an average energy of $\frac{1}{2}C_{in,pol}\Delta V^2$ is dissipated in the switches, where ΔV is the $\pm V_{DD}$ voltage step applied to the input capacitance. The SC loss follows as:

$$P_{SC,pol} = 2f_c \cdot \frac{1}{2}C_{in,pol}\Delta V^2 = \alpha(1-\alpha)f_c C V_{DD}^2 \tag{7}$$

III. Q50 SCPAs

The Q50 Cartesian SCPA was introduced in [3] and was indicated in Figure 1b. In this section, its output power $P_{out,Q50}$ and SC loss $P_{SC,Q50}$ are derived. Whereas [3] assumes equal I and Q signals, this section analyzes the more realistic case with arbitrary phase and amplitude modulation.

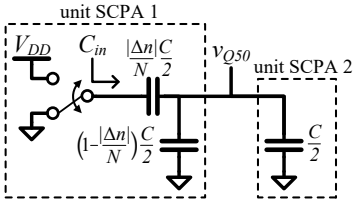


Fig. 4. Open-circuit model for the capacitive divider in a Q50 SCPA

A. Q50 input codes and output power

The open-circuit output voltage of the Q50 SCPA can be analyzed using Figure 4 and follows as:

$$v_{Q50}(t) = \begin{cases} \frac{n_1+n_2}{2N}V_{DD} & \text{if } 0 \le \omega_c t - 2k\pi < \frac{\pi}{2} \\ \frac{n_1+n_4}{2N}V_{DD}, & \text{if } \frac{\pi}{2} \le \omega_c t - 2k\pi < \pi \\ \frac{n_3+n_4}{2N}V_{DD}, & \text{if } \pi \le \omega_c t - 2k\pi < \frac{3\pi}{2} \\ \frac{n_3+n_2}{2N}V_{DD}, & \text{if } \frac{3\pi}{2} \le \omega_c t - 2k\pi < 2\pi \end{cases} \tag{8}$$

The fundamental of Equation 8 is:

$$\begin{aligned} v_{Q50,1}(t) = &\frac{2V_{DD}}{\pi}\left(\left(\frac{n_1}{N}-\frac{1}{2}\right)\sin\omega_c t \right. \\ &\left. + \left(\frac{n_2}{N}-\frac{1}{2}\right)\cos\omega_c t\right) \end{aligned} \tag{9}$$

When Equation 9 is equated to the desired output voltage in Equation 1, the input codes can be solved to:

$$n_p = \frac{\alpha N}{2}\sin\left(\frac{p\pi}{2}-\phi_0\right)+\frac{N}{2} \tag{10}$$

Where p is an index for inputs 1 to 4. By substituting Equation 10 into Equation 9, the maximum output amplitude and instantaneous output power can be derived to be:

$$\hat{A}_{Q50} = \frac{V_{DD}}{\pi} \tag{11a}$$

$$P_{out,Q50} = \frac{(\alpha\hat{A}_{Q50})^2}{2R_L} = \frac{\alpha^2 V_{DD}^2}{2\pi^2 R_L} \tag{11b}$$

Due to phase shift between I and Q, the maximum number of capacitors that can be switched at once is $N/2$. The maximum amplitude achievable at arbitrary phase can be seen as the inscribed circle in Figure 2d. This occurs e.g. when the I phase is at maximum amplitude, and the Q phase is at zero amplitude. The output voltage $v_{Q50}(t)$ then is a square wave from $V_{DD}/4$ to $3V_{DD}/4$, i.e. half the supply voltage in swing, as opposed to the full supply voltage for the polar SCPA, decreasing the output power by 6 dB.

B. Q50 switched capacitor loss

The array input capacitance is modeled in Figure 4 and is:

$$C_{in,Q50} = \frac{|\Delta n_{p,Q50}|}{2N}\left(1-\frac{|\Delta n_{p,Q50}|}{2N}\right)C \tag{12a}$$

Where the number of toggled capacitors is:

$$\Delta n_{p,Q50} = n_p - n_{p-2} = \alpha N \sin\left(\frac{p\pi}{2}-\phi_0\right) \tag{12b}$$

The probability density function (PDF) for the instantaneous phase ϕ_0 of a transmitted signal depends on the used modulation scheme. For noise-like baseband signals, a uniform PDF is expected. For quadrature amplitude modulation (QAM) signals, the square constellation has peaks in the PDF around $\frac{\pi}{4}+\frac{k\pi}{2}$, especially at higher amplitudes. Upsampling and filtering of the baseband signals however smoothens the transitions between symbols and therefore the transition in phase. The peaks are thus decreased, albeit not completely removed.

When assuming that ϕ_0 has a uniform PDF from 0 to 2π, the average input capacitance over ϕ_0 and p can be calculated with the aid of the identity in Appendix A:

$$\overline{C}_{in,Q50} = \frac{1}{8\pi}\sum_{p=1}^{4}\int_0^{2\pi} C_{in,Q50}(\phi_0,p)d\phi_0 = \alpha\left(\frac{1}{\pi}-\frac{\alpha}{8}\right)C \tag{13}$$

During each of the four switching moments in a carrier period, an average energy of $\frac{1}{2}\overline{C}_{in,Q50}\Delta V^2$ is dissipated in the switches, resulting in a SC loss of:

$$P_{SC,Q50} = 4f_c\cdot\frac{1}{2}\overline{C}_{in,Q50}\Delta V^2 = \alpha\left(\frac{2}{\pi}-\frac{\alpha}{4}\right)f_c C V_{DD}^2 \tag{14}$$

IV. Q25 SCPAs

The Q25 SCPA was introduced in [4] and is indicated in Figure 1c. In this section, its output power $P_{out,Q25}$ and SC loss $P_{SC,Q25}$ are derived.

A. Q25 input codes and output power

The open-circuit output voltage can be analyzed using the same model as the polar SCPA in Figure 3a:

$$v_{Q25}(t) = \begin{cases} \frac{n_1}{N}V_{DD}, & \text{for } \frac{\pi}{4} \le \omega_c t - 2k\pi < \frac{3\pi}{4} \\ \frac{n_2}{N}V_{DD}, & \text{for } \frac{-\pi}{4} \le \omega_c t - 2k\pi < \frac{\pi}{4} \\ \frac{n_3}{N}V_{DD}, & \text{for } \frac{5\pi}{4} \le \omega_c t - 2k\pi < \frac{7\pi}{4} \\ \frac{n_4}{N}V_{DD}, & \text{for } \frac{3\pi}{4} \le \omega_c t - 2k\pi < \frac{5\pi}{4} \end{cases} \tag{15}$$

The fundamental of Equation 15 is:

$$\begin{aligned} v_{Q25,1}(t) = &\frac{2\sqrt{2}V_{DD}}{\pi}\left(\left(\frac{n_1}{N}-\frac{1}{2}\right)\sin\omega_c t \right. \\ &\left. + \left(\frac{n_2}{N}-\frac{1}{2}\right)\cos\omega_c t\right) \end{aligned} \tag{16}$$

When equating this to Equation 1, the input codes can be found to equal to the Q50 SCPA in Equation 10. The maximum instantaneous output amplitude and output power then are:

$$\hat{A}_{Q25} = \frac{\sqrt{2}V_{DD}}{\pi} \tag{17a}$$

$$P_{out,Q25} = \frac{\alpha^2 V_{DD}^2}{\pi^2 R_L} \tag{17b}$$

As the Q25 quadrature waveforms have double peak-to-peak amplitude and half duty cycle w.r.t. Q50, follows: $P_{out,Q25}(\alpha) = 2P_{out,Q50}(\alpha) = \frac{1}{2}P_{out,pol}(\alpha)$.

TABLE I
SIMULATION PARAMETERS FOR THE SCPAS.

Parameter	f_c	f_{BB}	C	L	R_L	V_{DD}
Value	1.0	20	5.0	5.07	50	0.9
Unit	GHz	MHz	pF	nH	Ω	V

B. Q25 switched capacitor loss

The input capacitance for Q25 can be modeled with the circuit in Figure 3a. The average input capacitance can be found similar to the method for Equation 13. Using the identity in Appendix A, the resulting average input capacitance is:

$$\begin{aligned}\overline{C}_{in,Q25} =& \frac{1}{8\pi}\sum_{p=1}^{4}\int_0^{2\pi}\frac{|\Delta n_p|}{N}\left(1-\frac{|\Delta n_p|}{N}\right)C d\phi_0 \\ =& \alpha\left(\frac{\sqrt{2}}{\pi}-\frac{\alpha}{4}\right)C\end{aligned} \tag{18a}$$

Where number of switched elements is:

$$\Delta n_p = n_p - n_{p-1} = \frac{\sqrt{2}\alpha N}{2}\sin\left(\frac{p\pi}{2}-\frac{\pi}{4}+\phi_0\right) \tag{18b}$$

The total power loss to drive the capacitive divider at four switching moments per carrier period with average SC loss each of $\frac{1}{2}\overline{C}_{in,Q25}\Delta V^2$, is:

$$P_{SC,Q25} = 4f_c\cdot\frac{1}{2}\overline{C}_{in,Q25}\Delta V^2 = \alpha\left(\frac{2\sqrt{2}}{\pi}-\frac{\alpha}{2}\right)f_c C V_{DD}^2 \tag{19}$$

The SC loss is proportional to $f_c C V_{DD}^2$ for all investigated architectures. Hence, their relative quantities are a fundamental property of the architecture and α only.

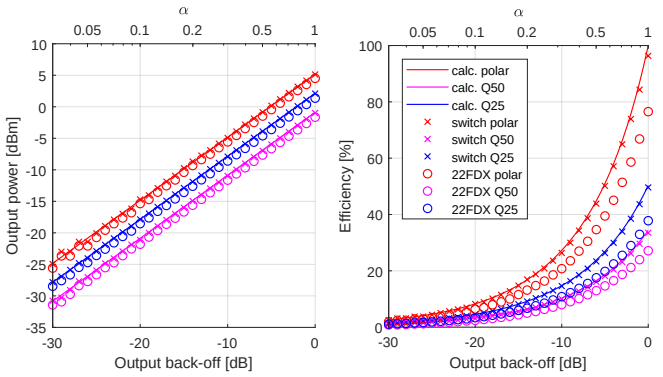
V. EFFICIENCY ENHANCEMENT TECHNIQUES

To improve SCPA efficiency, multiple techniques have been proposed, such as class G [3], [5], Doherty [6], sub-harmonic switching (SHS) [7] or combinations [8], [9]. The common characteristic of these techniques is that they all achieve back-off without driving the capacitive divider at a back-off code, maintaining the efficiency of $\alpha = 1$. At these levels, Equation 7, 14 and 19 hold, albeit with a lower V_{DD} for class G, peaking PA disabled for Doherty, and lower switching frequency for SHS. This renders efficiency for high α most important for system efficiency. A polar implementation is therefore favorable over Q50 and Q25 architectures.

Decreasing the load impedance can also improve system efficiency, as it does not affect the SC losses, but increases the output power. However, the insertion loss of the required impedance transformer will limit the efficiency improvement.

VI. SIMULATIONS

To verify the relations for P_{out} and P_{SC}, the SCPAs have been simulated using both ideal switches and transistor implementations for the switches. An implementation with $N = 255$, or 8-bits, is considered, rendering quantization noise negligible in the efficiency calculations. A 20MHz complex sine wave is used as baseband input signal. C is chosen 5 pF, in the order magnitude of the values in [2] and [3]. An overview of all design variables is given in Table I. No efficiency enhancement techniques are used.



(a) (b)

Fig. 5. Calculated and simulated results for the different SCPA architectures. (a) Output power. (b) Efficiency.

A. Ideal switches

The SCPAs have been implemented using ideal switches without series resistance and parasitic capacitances. This allows to investigate maximum efficiency without technology related parasitic losses, which decrease with Moore's law. The simulated and calculated output power are shown in Figure 5a. Some deviation can be seen at large back-off due to quantization. The simulated and calculated power efficiency have been plotted in Figure 5b. Additional power is lost in harmonics of f_c delivered to the load, which were assumed to be filtered out in calculation, slightly decreasing the efficiency.

B. Switches in 22nm technology

Implementations for the SCPAs have been made in Global Foundries 22 nm FD-SOI (22FDX) technology, and resistance, capacitance and cross-capacitance extraction is done on the unit cell in Figure 6. 22FDX offers a high transition frequency, making it suitable for efficient switching at GHz frequencies. The transistors are scaled such that the SCPA output impedance is approximately $R_L/10$, such that neither resistive nor capacitive losses in the switches are dominant. Loss due to gate capacitance is taking into account by driving the input using an ideal switch. As both SC loss and output power scale with V_{DD}^2, the low supply voltage does not impact efficiency. The output power is evaluated in Figure 5a. In the simulation, the output power decreases with 0.4 dB for all architectures due to the SCPA output resistance resulting from the transistor on-resistance, and finite transition time t_{tr} of the loaded drivers. The latter results in a transition time for the open-circuit output voltage as well. This can be modeled using a convolution with a rectangular impulse response $h_{tr}(t) = \frac{1}{t_{tr}}\text{rect}\left(\frac{t}{t_{tr}}-\frac{1}{2}\right)$, resulting in an attenuation of the output signal due to a sinc filter:

$$|H_{tr}(f)| = \frac{\sin(\pi f t_{tr})}{\pi f t_{tr}} \tag{20}$$

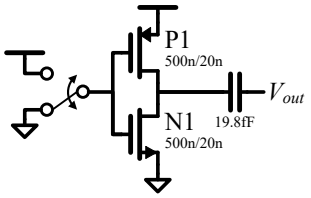


Fig. 6. Single slice for the SCPA cells in 22FDX technology.

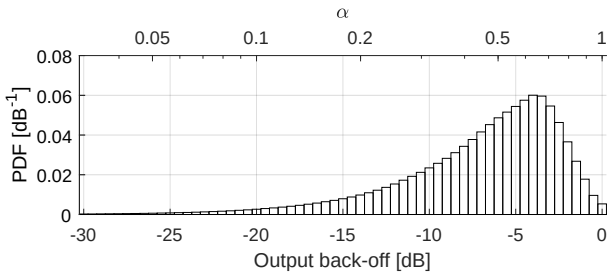


Fig. 7. PDF for the instantaneous amplitude of a 64QAM signal.

TABLE II
SCPA EFFICIENCY FOR 64QAM SIGNALS.

	P_{out} [mW] calc.	P_{loss} [mW] calc.	η [%] calc.	η [%] switch	η [%] 22FDX
Polar	0.957	0.837	53.4	52.3	41.3
Q50	0.239	0.989	19.5	18.9	15.3
Q25	0.479	1.226	28.1	27.7	20.7

Power efficiency is evaluated in Figure 5b and has decreased w.r.t to the ideal switch SCPA due to the charging of parasitic capacitances in the transistors and the unit cell layout, and the switch on-resistance. This deviation is always within 18% of the theoretical value, indicating the dominant loss mechanism is modeled.

C. Modulated cariers

The system performance for a 64QAM signal has been evaluated using a statistical model. A 64QAM signal is generated and clipping is applied to limit the peak-to-average power ratio (PAPR) to 5.4dB. The PDF of this signal versus the instantaneous value for α is indicated in Figure 7. With these statistics and the output power and efficiency versus α in Figure 5a and 5b respectively, the average power efficiency has been analyzed, indicated in Table II. These efficiencies are high compared to published SCPAs, even those with efficiency enhancement techniques, as losses in the matching network are not taken into account and a relatively small technology node has been used. By comparing the calculated loss and output power in Table II, the SC loss for polar SCPAs is the least, and is 18% and 46% higher for Q50 and Q25 SCPAs, while producing 6 and 3 dB less output power, respectively.

VII. CONCLUSIONS

Analytic expressions have been found for the output power and SC losses of polar, Q50 and Q25 SCPAs, using a statistical model for instantaneous phase. These relations show that w.r.t. polar SCPAs, Q50 and Q25 SCPAs have a 6 dB and 3 dB lower peak output power for equal supply voltage and load, respectively. These results have been verified using simulation of an 8-bit SCPA with ideal and 22FDX transistor switches. Efficiency calculations match to simulation using ideal switches and transistor models within 3% and 24% margin, respectively. In transistor implementations, power efficiency decreases due to switch on-resistance, parasitic capacitance and finite transition times. For 64QAM signals, the SC losses are analyzed to be 18% and 46% higher than for polar SCPAs, for Q50 and Q25 SCPAs, respectively. The results are applicable to SCPAs with efficiency enhancement techniques as well. As these architectures operate at lower back-off code, they favor polar implementations for maximum power efficiency.

APPENDIX A
IDENTITY FOR AVERAGE INPUT CAPACITANCE

The following equation is considered:

$$A = \sum_{p=1}^{4} \int_0^{2\pi} |\sin(\theta(p) \pm \theta_0)| \left(1 - B\,|\sin(\theta(p) \pm \theta_0)|\right) d\theta_0 \tag{21}$$

As the integrand is periodic in π due to the absolute value operators, the integral in Equation 21 can be taken over a single period of π when the total is multiplied by two. The phase offset $\theta(p)$ can be removed due to the integration over a full period. As p drops out of the equation, summing over p from 1 to 4 is the same as multiplying by four:

$$\begin{aligned} A =& 8 \int_0^{\pi} |\sin(\pm\theta_0)| \left(1 - B\,|\sin(\pm\theta_0)|\right) d\theta_0 \\ =& 8 \int_0^{\pi} \sin\theta_0 \left(1 - B \sin\theta_0\right) d\theta_0 = 16 - 4\pi B \end{aligned} \tag{22}$$

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