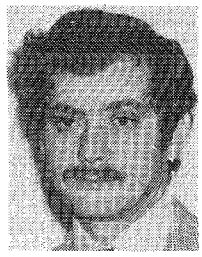

Victor Blatt was born in Cordoba, Argentina, on December 29, 1943. He received the maximum degree of Ingeniero Electricista Electronico from the University of Cordoba, Cordoba, Argentina, in 1970.

While at the University of Cordoba, he was engaged in research on system automation. From 1970 to 1971 he was employed at Lennox, Cordoba, as a Development Engineer in industrial electronics and system automation. He was with Philips, Eindhoven, The Netherlands, from 1971 to 1973 where he designed integrated circuits in I^2L. In 1973 he joined the Allen Clark Research Centre, The Plessey Company Ltd., Caswell, Towcester, Northants., England, working on research and development in the field of monolithic integrated circuits. At present he is Head of a Digital Design Group there.

Geoffrey W. Sumerling, for a photograph and biography, see this issue, p. 127.

Polycrystalline Silicon as a Diffusion Source and Interconnect Layer in I^2L Realizations

JAN MIDDELHOEK AND ARIE KOOY

Abstract—**Boron-doped polycrystalline silicon is applied as a diffusion source for the p-type regions of I^2L devices. The polysilicon also serves as a conductive level which requires no contact windows in the p-type regions. Compared to conventional processing a higher fan-out, size reduction, and a greater layout flexibility are reported.**

I. The Structure of the I^2L Device with Polysilicon

A polycrystalline silicon layer doped during the deposition with boron, can be applied as a diffusion source while it serves, at the same time, as a conductive layer to the diffusion area. IC processes which are based on this combined use of polycrystalline silicon result in a considerable size reduction of the p-type region [1]. This is mainly due to the fact that the interconnections of the diffusion areas require no contact windows. The performance of the devices also benefits from this size reduction. The design of the layout of an IC is greatly facilitated by the extra conduction level.

The principle of self-alignment is applicable in the fabrication because oxide regions adjacent to the polysilicon are formed simultaneously with the indiffusion from the polysilicon after the polysilicon layer has been etched. A technique, known as IDOPOS [2], has in principle the same possibilities as the technique reported in this paper.

Fig. 1 compares the cross sections of the base regions of two n-p-n bipolar transistors. One is a conventional type, the other is made with polysilicon. The area of the base region and the base-collector capacitance of the polysilicon type are smaller. The base surface remains partly covered with highly boron-doped polysilicon, resulting in a boron concentration under the polysilicon which is higher than directly around the emitter. The polysilicon on the surface forms more or less an aequipotential ring around the emitter. The polysilicon track connecting the base may be led in any direction independent of the aluminum track from the emitter.

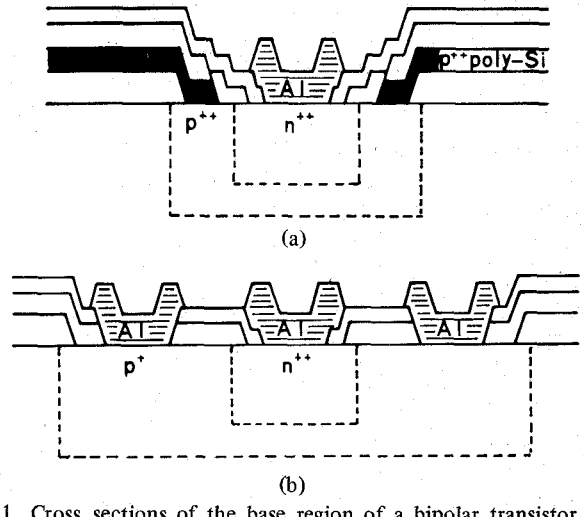

Fig. 1. Cross sections of the base region of a bipolar transistor. (a) Polysilicon technique (poly-Si base). (b) Conventional processing (standard base).

Fig. 2 shows a cross section of an I^2L device. The use of polycrystalline silicon helps to increase the number of collectors, which may be accommodated in the base regions in two

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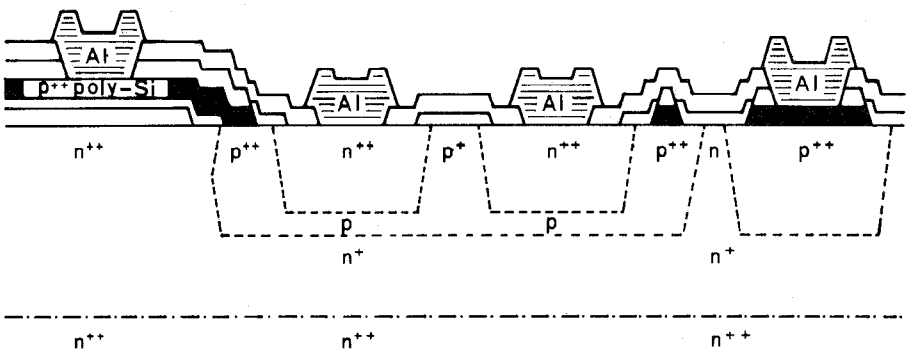

Fig. 2. Cross section of an I^2L device in the polysilicon technique.

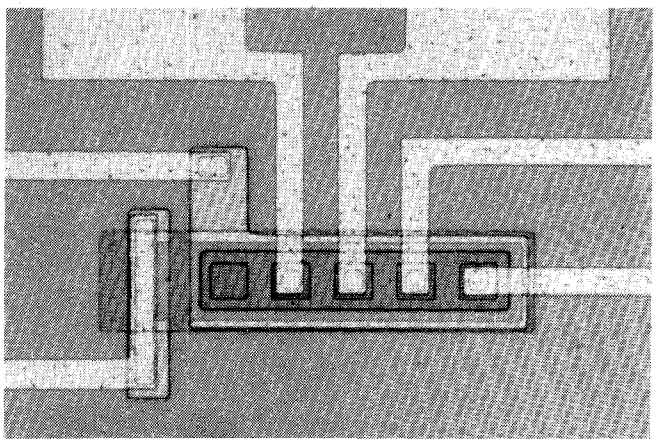

Fig. 3. Top view of an I^2L gate with five collectors and an external base contact.

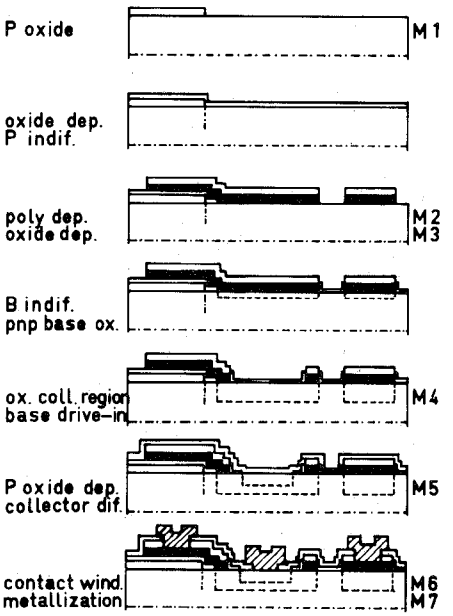

Fig. 4. Illustration of the polysilicon I^2L process.

ways. First the area which is normally needed for a base contact window is now available for a collector and secondly the polysilicon which remains on the surface of the base region reduces the series resistance in the lateral direction. The performance of the p-n-p transistor may benefit from the polysilicon because the concentration in the p-region is higher than that in the conventional processing.

Fig. 3 shows a photograph of a device with five collectors. The contact windows are $10 \times 10\ \mu m^2$. Further size reduction would appear possible.

II. The Device Technology

The deposition of polycrystalline silicon on monocrystalline silicon differs from the deposition on silicondioxide as applied in the silicon gate MOST technique. It is extremely difficult to completely avoid whisker growth on the monocrystalline surface. Reduction of the deposition temperature to 625°C [1] proved to be a good solution in the case of boron-doped polysilicon. In the case of phosphorus-doped polysilicon the deposition rate becomes very low at 625°C [2].

The etching of the polycrystalline silicon just as far as the monocrystalline substrate can be carried out reproducibly by calibration of the etching rate.

III. Process Description

Fig. 4 illustrates the process description.

Starting material: an n-type epitaxial layer of 0.6 Ω · cm and 6-μm thickness on an n^{++} substrate of ⟨100⟩ orientation.

1) Phosphorus doped silane-oxide deposition; $PH_3/SiH_4 = 0.064$; $T_{deposition} = 325°C$; $t_{ox} = 2000$ Å (doped) + 1000 Å (pure).

2) Mask 1 for the isolated area; negative resist; [HF (49 percent), sat. NH_4F] : $H_2O = 1:20$.

3) Deposition of pure silane-oxide; $T_{deposition} = 325°C$; $t_{ox} = 1500$ Å.

4) Deep n^{++} type diffusion in N_2 ambient. $T_{dif} = 1150°C$; $t_{dif} = 30$ min.

5) Mask 2 for the active area; negative resist; HF (buf.): $H_2O = 1:6$.

6) Doped polysilicon deposition: $B_2H_6/SiH_4 = 4 \cdot 10^{-4}$. $T_{deposition} = 625°C$; $t_{poly} = 3500$ Å.

7) Deposition of pure silane-oxide. $T_{dep} = 325°C$; $t_{ox} = 4000$ Å.

8) Mask 3 for the outer edges of the polysilicon layer. Positive resist; HF (buf.):H_2O = 1:20; poly-Si etchant [300 ml HNO_3 (65 percent), 10 ml HF (49 percent), 100 ml CH_3COOH, 150 ml H_2O]; $t_{etching\ poly} = 2$ min.

9) Indiffusion in oxygen ambient. $T_{dif} = 1150°C$; $t_{dif} = 15$ min; $t_{ox\ p\text{-}n\text{-}p\ base\ region} = 700$ Å; $x_{j\ mono} = 1.0$ μm; $R_{s\ mono} = 219$ Ω.

10) Mask 4 for the inner edges of the polysilicon layer. Negative resist; HF (buf.): H_2O = 1 : 6; poly-Si etchant [see 8)]; $t_{etching}$ = 2 min.

11) Drive-in diffusion in oxygen ambient. T_{dif} = 1150°C; t_{dif} = 75 min. $t_{ox\ collector\ region}$ = 2000 Å; $x_{j\ mono}$ = 3.4 μm; $R_{s\ mono}$ = 200 Ω.

12) Mask 5 for the collector areas. Negative resist; HF (buf.): H_2O = 1 : 6.

13) Deposition of phosphorus doped silane-oxide. PH_3/SiH_4 = 5.1 10^{-2}; T_{dep} = 325°C; t_{ox} = 2000 Å (doped) + 1000 Å (pure).

14) Indiffusion in N_2 ambient. T_{dif} = 1100°C; t_{dif} = 120 min; x_j = 2.7 μm; R_s = 5.9 Ω.

15) Mask 6 for contact windows. Negative resist; HF (buf.): H_2O = 1 : 6.

16) Al evaporation (E-gun). t_{Al} = 1.3 μm.

17) Mask 7 for metal delineation. Positive resist; [75 ml H_3PO_4, 15 ml CH_3COOH, 5 ml HNO_3 (65 percent), 15 ml H_2O].

18) Anneal in wet N_2. T = 450°C; t = 60 min. Sheet resistances. $R_{s\ poly\ on\ SiO_2}$ = 115 Ω; $R_{s\ poly\ on\ Si}$ = 51 Ω.

IV. Results and Discussion

The current amplification factors have been determined with the structure, as shown in Fig. 3. The results should not be considered as the optimum, which can be reached with this poly-Si technique, but as proof of the feasibility of the process.

First the collector currents into each of the four connected collectors were measured at a constant base current of 100 μA and with the injector grounded.

Collector	I_C (μA)	Ratio	log ratio × 60 mV/n
2	726	1.098	2.44/3 = 0.81 mV
3	661	1.066	1.66/2 = 0.83 mV
4	620	1.037	0.94/1 = 0.94 mV
5	598		

In the first place these measurements show that the upward current gain per collector is about 7. The collector current decreases when the collector is at a greater distance from the base contact. If it is assumed that the base current is equally divided over the base region, then the voltage drop from collector to collector in the base region can be estimated. The collector current may be expressed as

$$I_C = \beta_{up} I_{BO} \exp\left((qV - nI_B R_{cc})/kT\right).$$

n depends on the position of the collector and can be found with the help of Fig. 5.

The resistance from collector to collector R_{cc} can be estimated as 0.86 mV divided by the fifth part of the total base current. This gives R_{cc} = 43 Ω. The same measurement on a conventionally made device gives R_{cc} = 220 Ω. This result is a clear indication that the polysilicon process reduces the lateral series resistance in the base region.

Even for a high base current of 100 μA the collector current ratio of the first to the fifth collector is only 1.40. The conventional process gives a factor 4.

The inverse current gain of the p-n-p transistor $\beta_{I,\ p\text{-}n\text{-}p}$ of the perpendicular gate (see Figs. 3 and 6) is 0.76. The inverse current gain of the p-n-p transistor of the parallel gate (see Fig. 6) is 2.05. The downward β_d of the n-p-n transistor was determined to be 280. A more profound study of the current amplification and of the contributions to base current has not yet been made. It requires a large variety of test structures [3].

Fig. 6 shows a photograph of two ring oscillators. The largest oscillator has 49 stages, the other 17. From the oscillating period T as a function of the supply current I_{supply}, the plot of Fig. 7 is determined. The delay time per stage was calculated according to the expression $T/2 \times n$. The power-delay pro-

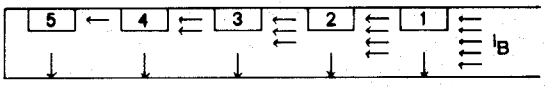

Fig. 5. Schematic representation of the base current distribution.

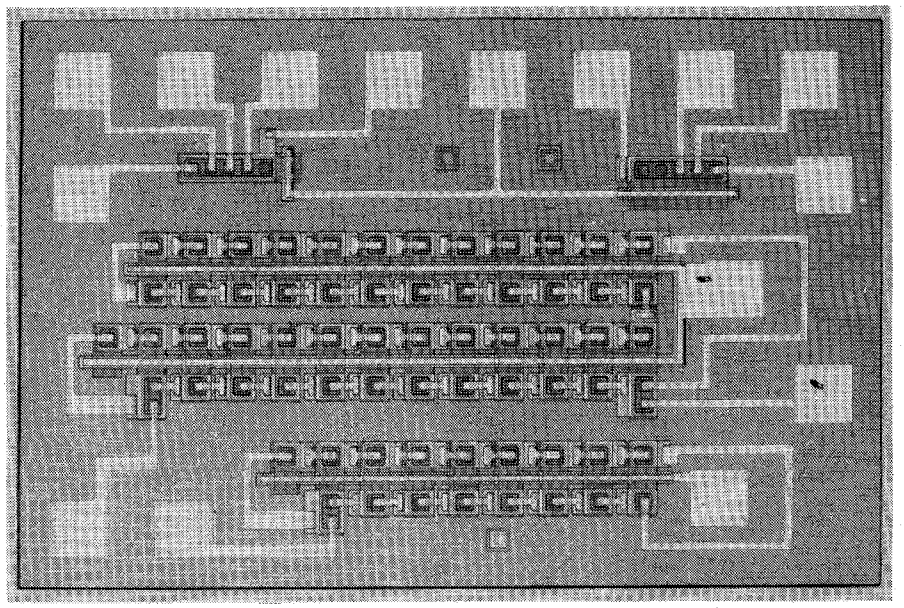

Fig. 6. Photograph of the test chip, which contains two gates and two ring oscillators. The number of stages are 17 and 49, respectively.

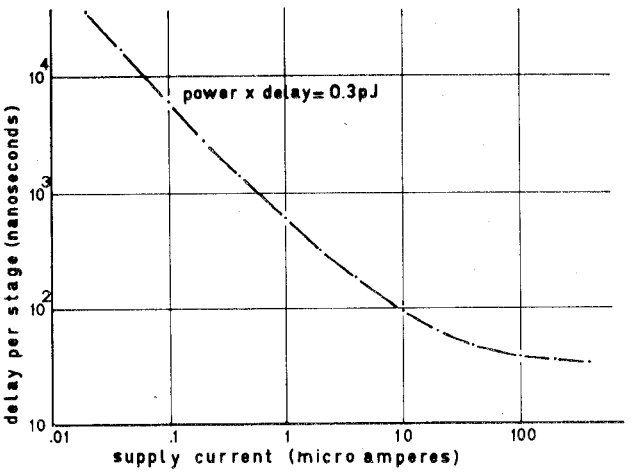

Fig. 7. Average propagation delay per gate versus the supply current per single collector gate.

duct per stage is $I_{\text{supply}} \times n^{-1} \times V_{\text{supply}} \times T \times (2n)^{-1}$, where n is the number of inverters, 49 or 17.

At last we show in Fig. 8 a photomicrograph of a 4-bit programmable accumulator [5], successfully realized in the new technology. It contains 172 gates on a chip area of 4 mm^2.

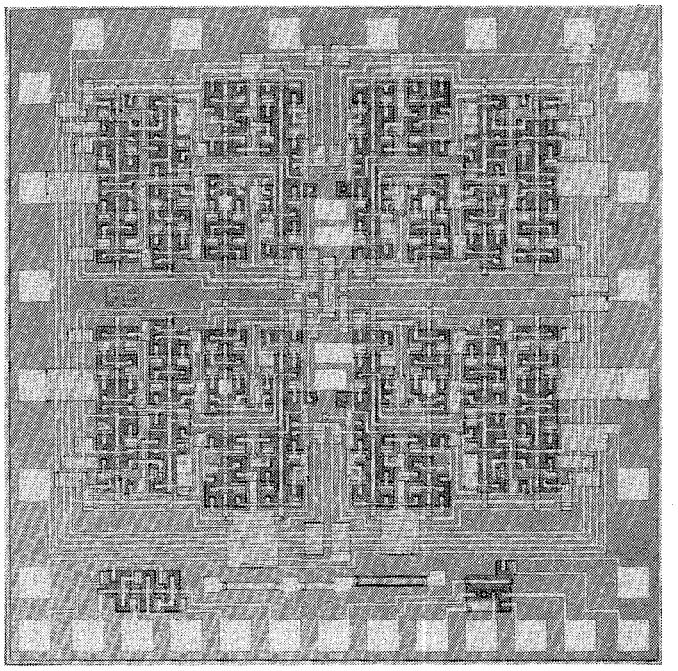

Fig. 8. Photograph of a 4-bit programmable accumulator realized in the polysilicon I^2L technique. The chip of 4 mm^2 contains 172 gates and two test devices.

Acknowledgment

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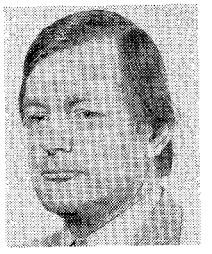

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He joined the staff of the Physical Chemistry Laboratory of the State University of Leiden in 1961, where he worked on the dielectric behavior of liquids. In 1967 he became a member of the staff of the Solid State Electronics Group at the Twente University of Technology, Enschede, The Netherlands, where he has been in charge of the IC processing laboratory and where he also teaches IC technology.

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