case, no minority carriers were generated because the light energy was lower than the band gap.

All the results mentioned had good reproducibility provided the measurement conditions were fixed. The bias-temperature treatment at −5 V for 2 h at 170°C had no influence on the characteristics of an MOS diode [4].

From the results, we can draw the following conclusions: 1) The resistivity and the breakdown field are sufficiently high. 2) There exist almost no interface states which follow the RF signal from 100 Hz to 1 MHz. 3) In the anodic oxide film, there are deep electron trap centers near the GaP surface into which electrons tunnel on application of positive voltage. At negative bias, trapped electrons are slowly emitted into the GaP conduction band. The emission is accelerated by shining light with energy higher than 1.8 eV. 4) There may exist another trap level of $9 \times 10^{11}/cm^2$, which is responsible for the hysteresis observed in the dark. The energy of the level may be shallower but the time constant is longer than 10 ms.

These characteristics are similar to those of an MNOS diode. One can infer that the oxidized film has a two-layer structure and some structural defects act as trap centers between the two layers.

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A Polysilicon Source and Drain MOS Transistor (PSD MOST)

J. MIDDELHOEK AND A. KOOY

***Abstract*—An MOS transistor is described in which the source and drain areas are obtained by diffusion from doped polycrystalline silicon. Polysilicon tracks form the interconnect with the diffusion areas without the need for contact windows. As a result transistor and junction sizes are reduced by a factor 2 or 3 over a normal structure. Polycrystalline silicon tracks in this new technique are of greater advantage as interconnect layers than in the silicon gate technique.**

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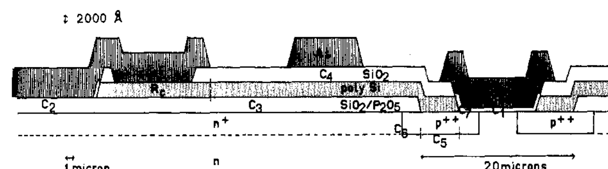

Fig. 1. Cross section of most important structures in PSD technique. Note different scales in vertical and horizontal directions.

I. The Structure of the PSD MOS Transistor

A large fraction of the total area of standard Al gate or Si gate MOS transistors is taken by the source and drain areas. This is mainly due to the minimum spacings, as required by the photo–etch technique. The crosssection of a polysilicon source and drain MOST given in Fig. 1 shows that if polysilicon lines serve as a diffusion source as well as the conductive path to the source and drain, an appreciable reduction in transistor length can be achieved. A reduction in the capacitance of the diffused areas to the substrate is also a useful result.

The fabrication of the PSD MOS transistor requires 4 masks and less processing steps than the "standard" silicon gate technique. The first mask delineates the active area. The field oxide consists of thick thermally grown SiO_2 or, as we used, a lightly phosphorus-doped silane–oxide to provide for a "channel stop" n-type surface layer outside the active regions. With the second mask, the gate area is etched out of the boron-doped polysilicon. The third mask provides windows in order to make contact between aluminium and polysilicon lines. The fourth mask delineates the aluminium. Stabilization of the MOS structure is achieved in the usual way with phospho-silicate glass. Insulation of the Al lines from the polysilicon lines is achieved by thermally grown oxide and/or deposited silane–oxide layers.

The junction depth and the diffusion under the thin gate oxide are related to the thickness of the gate oxide because indiffusion and gate oxidation take place simultaneously. The thin oxide gate overlap capacitance and the channel length reduction by underdiffusion are not dependent on the alignment of masks. The process is self-aligning with regard to these parameters.

II. The Technology of the PSD MOS Transistor

The main problem of the technology is the prevention of polysilicon whisker growth during the deposition of polysilicon on the bare parts of the monocrystalline silicon substrate. This problem has been completely overcome by codoping the polysilicon with boron. The addition of B_2H_6 to SiH_4 considerably increases the deposition rate [1]. Therefore, the deposition temperature can be chosen as low as 625°C. The deposition rate is then 900 Å/min at a B/Si ratio of 33×10^{-4}. At 625°C, the deposited polysilicon layer shows no whisker growth and forms a mirror-like layer. Even on the oxide step edge of the active area, no whisker growth could be detected.

Complete etching of the polysilicon in the gate area causes no problems because the etching is continued after the color of the field oxide has appeared, so that a thin layer of the monocrystalline silicon in the gate area is also removed.

Another problem found was staining in the contact holes on the polysilicon. It was found that staining occurred on those polysilicon tracks which also made contact with the diffused areas of the substrate. Contact holes on polysilicon tracks which were completely isolated from the substrate by an oxide

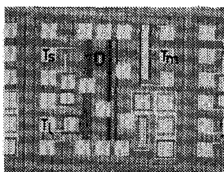

Fig. 2. Photograph of test chip. Bonding pads are $100 \times 100\ \mu^2$.

layer did not show staining. Staining occurred when the wafer was taken out of the etch-solution for checking, whether the contact holes were completely open or not. Currently the only practical solution for this problem consisted of etching the holes long enough in darkness and rinsing quickly and thoroughly.

III. Process Description

1) Standard cleaning.
2) Silane–oxide deposition; $PH_3/SiH_4 = 7 \times 10^{-5}$; $T_{deposition} = 325°C$; $t_{ox} = 4000$ Å.
3) Mask 1 for active area; neg. resist; $HF{:}H_2O = 1{:}20$.
4) Doped polysilicon deposition, $B_2H_6/SiH_4 = 1.7 \times 10^{-3}$; $T_{deposition} = 625°C$; $t_{poly} = 3500$ Å.
5) Pure silane–oxide; $T_{deposition} = 325°C$; $t_{ox} = 3500$ Å.
6) Mask 2 for gate area; pos. resist; SiO_2 etch; poliSi etch (300 ml HNO_3 (65 percent), 100 ml H_3PO_4 (85 percent), 10 ml HF, 150 ml H_2O).
7) Gate oxidation and diffusion at 1150°C, $t_{ox} = 1000$ Å; 250 Å PSG; anneal 15 min at 1050°C in N_2.
8) Mask 3 for contact-windows; neg. resist; $HF{:}H_2O = 1{:}6$.
9) Al metallization.
10) Mask 4 for metal delineation; pos. resist; H_3PO_4/H_2O. Anneal.

IV. Results and Discussion

A photograph of the chip manufactured for evaluation of the PSD process is shown in Fig. 2. The chip contains 3 MOS transistors, resistive tracks of polycrystalline silicon, various capacitive structures, and diodes.

A. Resistors

The boron-doped polycrystalline layer was 3500 Å thick and the resistance per square was 49 Ω. The spread of the resistances over a wafer was ±2 percent. The contact resistance R_c between a 15-μm wide metal line and a 15-μm wide polysilicon track with a contact hole of $10 \times 10\ \mu m^2$ was found to be 24 Ω ± 4 Ω. The resistance in the longitudinal direction of a 15-μm wide polysilicon track, in parallel to a p^+ diffusion as used for the source and drain of T_M is 2.5 Ω/μm.

B. Capacitors

In Fig. 1 the different capacitive structures are indicated by a number. The capacitances are determined on mounted and encapsulated chips with a ratio-transformer bridge according to the three terminal method which eliminates the parasitic capacitances of the housing and the bonding pads. The spread in the capacitances is 2 percent or less except for C_6 for which the determination could not be done with an accuracy of better than 25 percent because the design of one of the diodes was unfavorable.

C_1 (t_{ox} = 1250 Å) $= 2.73 \times 10^{-4}$ pF/μm^2

C_2 (t_{ox} = 3950 − 50 + 125 + 250 Å) $= 0.81 \times 10^{-4}$ pF/μm^2

C_3 (t_{ox} = 3950 Å) $= 0.86 \times 10^{-4}$ pF/μm^2

C_4 (t_{ox} = 3050 Å) $= 1.08 \times 10^{-4}$ pF/μm^2

C_5 ($N_D = 5.10^{14}$ at/cm^3; V_j = 0 V) $= 0.87 \times 10^{-4}$ pF/μm^2

C_6 (p^+ side wall versus stopper diff.) $= 6 \times 10^{-4}$ pF/μm

C_7 (gate versus p^+ diff. overlap) $= 8.25 \times 10^{-4}$ pF/μm.

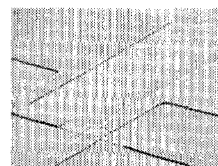

Fig. 3. SEM photograph of small PSD MOS transistor T_S. Magnification 800 times.

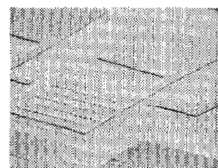

Fig. 4. SEM photograph of the large PSD MOS transistor T_L. Magnification 500 times.

TABLE I

Transistor	T_S	T_M	T_L
μ_o		193 cm^2/V. sec.	
E_{GC}	3×10^6 V/cm		
V_T (10^7 ohm)	− 2.9 V	− 2.75 V	− 2.7 V
V_T (1 μ A, 5	− 3.7 V	− 2.95 V	− 2.68 V
R_S	175 Ω (calc)	909 Ω	312 Ω
R_{on} (min)	3500 Ω	1470 Ω	371 Ω
W/L (actual)	1.39	8.45 (calc)	80
W/L (designed)	1	7.8	51

Note: The process may be further optimized with respect to the dimensions of the metal and the polysilicon tracks and of the contact-windows. Also the thickness of the deposited layers can be independently changed. The threshold voltage may be adjusted by ion implantation.

C. Diodes

The breakdown voltage of the diodes was 28 V ± 1 V. From this value it may be derived that the surface concentration of phosphorus was about 3×10^{16}/cm^3.

D. MOS Transistors

A SEM photograph of the smallest transistor is shown in Fig. 3. This transistor is marked T_s in Fig. 2. This transistor requires no greater area than that provided by the crossing of the 15-μm wide metal and polycrystalline-silicon tracks. The designed channel length and width of this minimum size transistor are both 10 μm. These dimensions are reduced by underdiffusion.

Fig. 4 shows an SEM photograph of a PSD MOST designed for output stages. It is an interdigitated structure of about the same size as a bonding pad. The designed width of the polysilicon fingers is 5 μm. The designed gate length is 10 μm. This transistor is marked T_L in Fig. 2.

The evaluation of the transistor parameters was done according to the following equations for the MOS transistor in the linear region, $(V_{DS}/(V_{GS} - V_T)) < 0.01$, taking into account high gatefield mobility and series resistance [2].

$$I_{DS} = \frac{\mu_0 (W/L)(\epsilon_{ox}/t_{ox})}{1 + (V_{GS} - V_T)/(E_{GC} t_{ox})} \times (V_{GS} - V_T)(V_{DS} - I_{DS} R_S). \quad (1)$$

After some rearrangements this equation leads to

$$\frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_0 (W/L)(\epsilon_{ox}/t_{ox})} \times \frac{1}{(V_{GS} - V_T)} + \frac{1}{\mu_0 (W/L) \epsilon_{ox} E_{GC}} + R_S \quad (2)$$

in which μ_0 denotes the low field mobility in the inversion layer, E_{GC} denotes the critical field perpendicular to the inversion layer in the oxide, and R_S represents the total measured series resistance from the bonding pads to the source and drain sides of the channel.

μ_0, E_{GC}, and R_S cannot be evaluated independently for the three transistors. μ_0 is assumed to be equal for all three types. It is determined for transistor T_M from the slope of (2) because inaccuracies in the determination of the underdiffusion in the gate area and inaccuracies caused by the etch definition of the gate area contribute least to the inaccuracy of the calculation of the actual (W/L) ratio of transistor T_M. E_{GC} is derived from the intercept of (2) with the vertical axis for the case of transistor T_S, because R_S is relatively small for T_S and can be calculated from the results with the resistors.

If μ_0 is also known, the actual W/L for T_S and T_L can be calculated from the slope of (2). If E_{GC} is known, the R_S of T_M and T_L can be calculated from the intercept of (2) with the vertical axis.

The threshold voltages have been determined in two ways. First, as the gate voltage necessary to induce a channel sheet resistance of 10^7 Ω [3]. Second, as the gate voltage required for a drain current 1 μA at $V_{DS} = 5$ V.

The results of the evaluation of the transistor parameters are given in Table I.

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Effective Defect Density for MOS Breakdown: Dependence on Oxide Thickness

S. P. LI AND J. MASERJIAN

Abstract—**A procedure is introduced for measuring an effective density of defects that takes into account time-dependent dielectric breakdown in MOS devices. Measurements are obtained that show a surprising exponential decrease in this density with decreasing oxide thickness.**

Statistical methods have been developed in previous work for determining the density of defects in SiO_2 films responsible for premature (secondary) dielectric breakdown [1]–[6]. The general procedure entails 1) the use of a voltage ramp for observing the voltage at the onset of breakdown for each of a large number of MOS capacitors, and 2) counting primary (intrinsic) breakdowns as those occurring within some specified voltage interval below the maximum, and secondary (and tertiary) breakdowns as those at lower voltages. Using this distribution, the defect density is then calculated from statistical theory. This procedure suffers serious limitations, especially in light of more recent findings.

First, the voltage-ramp method does not allow sufficient time to account for time-dependent secondary breakdown. Recent work by the authors [7] shows that this time dependence can involve the major part of secondary breakdowns, and that even at moderately high fields (>4 MV/cm), times greater than 10^3 s are required at room temperature. Therefore, a large number of defects would go undetected with the voltage-ramp technique and would count only as primary breakdowns. Second, the so-called primary breakdown strengths observed by previous investigators are ill-defined and their range and magnitudes depend loosely on the particular investigation and the MOS process used. If the primary breakdowns are to be interpreted as intrinsic or free of defects, it seems reasonable to expect a much more sharply defined distribution.

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Although one is still free to interpret the results derived from the above procedure as an effective defect density relating to only a particular class of defects, a more reliable method of evaluating oxide quality with respect to breakdown is needed. The following describes a new method for measuring an effective defect density that takes into account time-dependent breakdown.

A time-dependent breakdown probability $P(t)$ is obtained by applying a constant field stress to a statistically sufficient number of MOS capacitors [8]. The fraction of the capacitors showing at least one breakdown event, self- quenching or otherwise, at time t after simultaneous application of electric field, is defined as $P(t)$. Let us specify a sufficiently large electric field F, a final time t_f, and a temperature T which accounts for a major portion of time-dependent breakdowns. More precisely, the value of $P(t_f)$ includes the effect of all defects encompassed by the specified F–t_f–T stress. On the basis of our previous work [7], for fields greater than 4 MV/cm, we may choose a time t_f—for example, 3000 s at room temperature—which is ample to include most time-dependent breakdowns and yet not excessive for practical measurements. This time-dependence has been explicitly related to Schottky emission of mobile ions from Al–SiO_2 interfaces with an activation energy of 1.4 eV. Osburn and Bassous [9] have recently shown a larger activation energy for poly Si electrodes (2.4 eV), and thus we anticipate that a correspondingly larger F–t_f–T stress would be required for these structures.

On the assumption that the effective defects are randomly distributed along two dimensions and are thus indistinguishable, the analysis of Price [10] applies (Bose–Einstein statistics) [4]. Using our definition of $P(t_f)$, the corresponding effective defect density $D(t_f)$ is given by

$$D(t_f) = \frac{1}{A} \frac{P(t_f)}{1 - P(t_f)} \qquad (1)$$

where A is the area of the MOS capacitor. Therefore, a plot of $P(t_f)/[1 - P(t_f)]$ versus A should yield a straight line through the origin with slope $D(t_f)$.

To apply the above procedures, arrays of MOS capacitors of different areas were patterned on single wafers. Measurements of $P(t_f)$ were obtained from 198 capacitors of each area, by making two 99-point-probe measurements for each area. Small areas were probed from pads extending over thick field oxides. The measurements used fields of 6.5 and 8 MV/cm and $t_f = 3000$ s. A total of eight silicon wafer in three groups were processed, embracing a range of oxide thickness d_{ox} (325–917 Å) and some changes in process conditions which affect the Si–SiO_2 interface. These changes are summarized in Table I. In all cases, the starting wafers were 6–8 Ω/cm n-type Si and Cu-ion-polished. Standard processing included cleaning, 5000-Å preoxidation and HF strip, oxidation in dry O_2 at 1175°C, and Al metallization by e-beam evaporation. Except when noted otherwise, postoxidation anneals were carried out in dry N_2 at 1175°C for 30 min, and postmetallization anneals in dry N_2 at 475°C for 15 min.

The effective defect densities $D(t_f)$ tabulated in the last column of Table I were obtained from the plots in Fig. 1. The experimental points in Fig. 1 are seen to fit the straight lines reasonably well for all the wafers tested, and thus the values of $D(t_f)$ appear to be statistically significant. A comparison of