HIGHLY-DOPED BULK SILICON MICROHEATERS AND ELECTRODES EMBEDDED BETWEEN FREE-HANGING MICROFLUIDIC CHANNELS BY SURFACE CHANNEL TECHNOLOGY

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ABSTRACT

Surface Channel Technology is widely used as the fabrication process to make free-hanging microchannels in various microfluidic devices. In this extended abstract, we report an innovative fabrication method to embed highly-doped silicon electrodes between the adjacent free-hanging microfluidic channels using the SCT process. Essentially, two parameters are used to tune the final cross-sectional geometry and size of the bulk silicon electrodes. One is the distance between two adjacent rows of slits and the other is the width of flat membrane above the microchannels. The advantageous physical features make bulk silicon electrodes suitable for many sensing and actuation applications. When the bulk silicon electrodes are used as microheaters, they allow higher power dissipation. This is because of their larger cross-sectional areas compared to the commonly used thin film metal microheaters. Moreover, as sensing electrodes, bulk silicon electrodes are located between the sidewalls of two adjacent microchannels. This makes them applicable as the sidewall resistive or capacitive readout in e.g. flow sensors.

KEYWORDS

Surface Channel Technology (SCT), free-hanging microfluidic channels, embedded sidewall bulk silicon electrodes, highly-doped bulk silicon microheaters.

INTRODUCTION

The original SCT process

Free-hanging microfluidic channels with the hydraulic diameter between approximately $20\,\mu m$ to $100\,\mu m$ can be fabricated by Surface Channel Technology (SCT) [1]. These microchannels have very thin channel walls of a few μm thick and are made of dielectric materials such as silicon nitride. The dielectric channels can be completely released free from the bulk silicon wafer and become free-hanging. These free-hanging microchannels are useful for different micro-electro-mechanical systems (MEMS) devices, such as fluid parameter sensors [2], control valves [3], micro-Coriolis flow sensors [4], pressure sensors [5], thermal flow sensors [6], and micro-gas-burners [7], The SCT fabrication method have become the technology platform for various microfluidic applications. Therefore, SCT is suitable as the microfluidic platforms for fabricating multi-parameter sensors [2].

The demands to develop sidewall electrodes

The original SCT process shows that as long as the channels are completely released, the microchannels become free-hanging and allow mechanical movement for sensing or actuating purposes [1]. All the electrical functionalities are realized by the thin film metal wires placed on the top surface of the microfluidic channels. For example, thin film microheaters and temperature sensors, resistive strain gauges and capacitive readout. In most cases, it is only possible for sensing and actuation from the topside of the channels. The demand of electrical functionalities in the micro-devices cannot be always fulfilled by the top surface thin film metal interconnects fabricated from the original SCT process.

In practical applications, there are great demands of sidewall sensing and actuation, which can be realized by embedding the electrodes on the sidewalls of the microfluidic channels. For example, the in-line relative permittivity sensors was realized with the SCT process by isolating two silicon electrodes at the sidewalls of the microfludic channel [8]. Accurate capacitance readout was demonstrated suggesting the viability of silicon electrodes for capacitive readout. However, a SOI wafer is needed to electrically insulate the device layer silicon electrodes from the bulk handle layer.

The concept of sidewall silicon electrodes have another potential application as the robust and reliable sidewall microheaters. For the micro-gas-burners [7], $200\,nm$ thick platinum resistors were patterned on the top surface of the micro-channel and function as topside microheaters and temperature sensors. However, thin film platinum resistors degraded morphologically and

electrically at high temperatures above 600 °C [7, 9]. More powerful heaters are necessary to reach 600 °C for the initiation of methane/air autoignition reaction for the micro Wobbe Index meter. It was previously reported that sidewall silicon microheaters can be embedded between the channel walls fabricated by Trench-assisted Surface Channel Technology and function as sidewall microheaters [10].

These reported approaches to integrate silicon electrodes have been proposed before using SOI wafers [4, 8] and/or refilled trenches [10], but these options require SOI wafers and add more complexity to the fabrication process.

Here we propose to integrate heavily-doped bulk silicon electrodes between the adjacent free-hanging channels, as illustrated in Figure 1(H2). The proposed fabrication scheme is completely based on the core concept of SCT in a silicon wafer, with special designs in the slits pattern and the release window location, in-plane silicon electrodes can be embedded between free-hanging surface channels. In the following sessions, firstly, the new SCT fabrication scheme will be explained. Next, the fabrication results will be presented. Lastly, the application of bulk silicon as microheaters will be discussed.

FABRICATION SCHEME

The new SCT fabrication scheme requires a highly-doped silicon wafer to make the sidewall bulk silicon electrodes electrically conductive. The schematic new SCT process is illustrated in Figure1 from A2 to H2. In comparison, the original SCT process using a silicon wafer is illustrated in Figure1 from A1 to G1.

In details, the new SCT process starts with (A2) a highly-doped silicon wafer; (B2) transfer the slit array patterns into the SiO_2 hard mask, where d is the spacing between two rows of slits; (C2) semi-isotropically etch the silicon wafer through the slit openings and form the semi-circular channel cavity with a flat top membrane. With properly designed d, there is silicon remained between two adjacent channels; (D2) conformal deposition of low-stress LPCVD silicon-rich Si_xN_y (SiRN) to seal the slit openings and form the thin dielectric channel walls; (E2) etch away the dielectric top layers until the highly-doped silicon; (F2) deposit thin film metal layers and pattern the metal wires to form electrical interconnects. This step enables electrical interconnections from external power supply to the embedded silicon electrode;

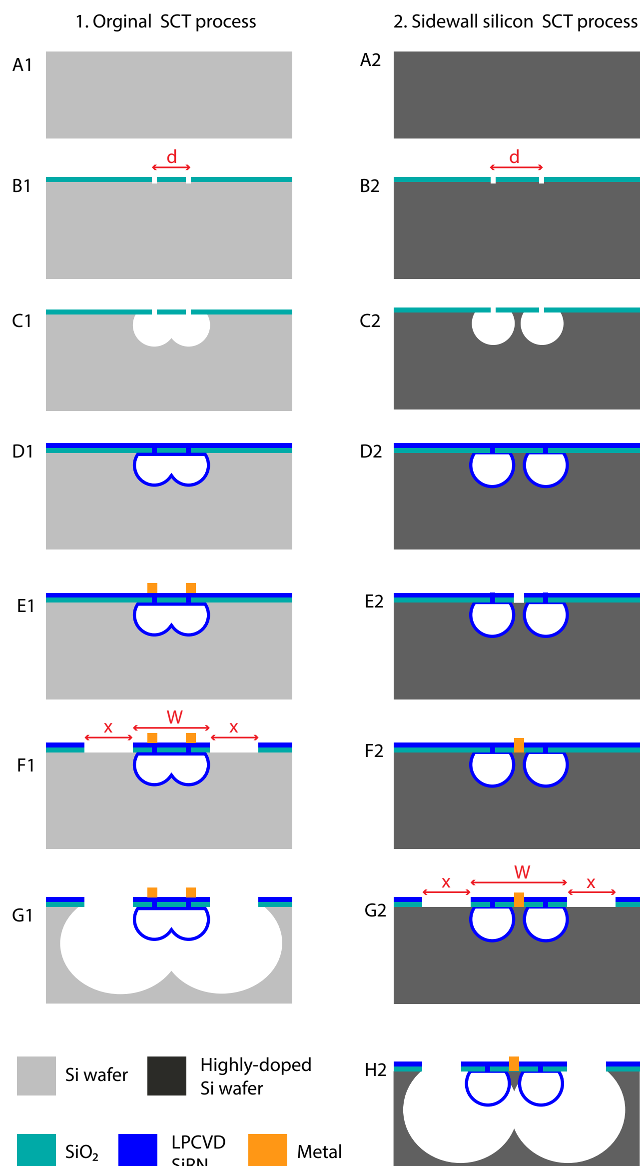

Figure 1: From A1 to G1 shows the schematic fabrication steps of the original SCT process in a silicon wafer to make free-hanging microchannels with topside electrical functionalities. From A2 to H2 shows the schematic fabrication steps of the new SCT process in a highly-doped silicon wafer to fabricate sidewall silicon electrode between two free-hanging adjacent microchannels. The original (1) and new (2) SCT fabrication process share the same sequences: (B1 and B2) etch slit arrays in the hard mask; (C1 and C2) semi-isotropically etch the channel cavity through the slit openings; (D1 and D2) deposit LPCVD SiRN to seal the slits and form channel walls; (E1 and E2, F2) deposit and pattern the metal thin films for electrical functionality. The new process requires the extra step (E2) to etch open the hard mask and uncover the highly-doped silicon between the two adjacent microchannels for metal connection; (F1 and G2) etch the front release window with width x and the flat membrane above the channel with width W in the hard mask; (G1 and H2) release etch the channel through the front release windows.

Next, design the top flat membrane above the channels with the width W, and (G2) etch frontside release window with the width x in the dielectrics top layers; (H2) release etch the channel through the frontside release mask. Use the same release etch recipe (i.e. etching method and etching time) from the original SCT process [1], by properly design the parameters x and W, there will be silicon remained between two adjacent channels after the release etch.

By controlling the release etch, the electrically conductive silicon become isolated from the bulk substrate, which is crucial for electrodes and microheaters.

RESULTS AND DISCUSSIONS

There are two parameters playing vital roles in determining the amount of the remained silicon. One is the distance between two rows of slits d, and the other is the width of the flat membrane above the channels W. In order to test the parameters to obtain the bulk silicon electrode between adjacent microchannels, structures were fabricated according to the new SCT process scheme described in the Figure 1(A2-H2). Each process recipe was kept the same as used in the original SCT process.

Firstly, different values of d between two rows of slits can result in either two separate channels or a single connected channel with larger width. In the new SCT process, larger d results in two separated channels (Figure 1(D2)). Whereas in the original SCT process, two closely placed rows of slits hence a smaller d results in one merged channel with a ridge at the bottom of the wider channel (Figure 1(D1)). Scanning electron microscope (SEM) photographs of the test structures show that, for two rows of slits with row distance $d = 60\,\mu\text{m}$, two separate channels are formed (Figure 2(A-F)). For $d = 55\,\mu\text{m}$, a single wider channel with bulk silicon electrode embedded inside the channel (Figure 2(G)).

Secondly, for a fixed release window width $x = 200\,\mu\text{m}$, the width of the flat membrane above the channels W defines the hard mask for the channel release etch. The SEM photographs of the fully released channels with certain amount of silicon remained between the channels are shown in Figure 2. If the release windows are close to the channels hence a small W, channels are completely released and the silicon in between is completely removed (Figure 2(B)). For $W = 100$, 140 and $250\,\mu\text{m}$, an increasing amount of silicon remains between the channels, as shown in Figure 2(C), 2(D), and 2(E) respectively. For even larger W the channels are no longer completely released.

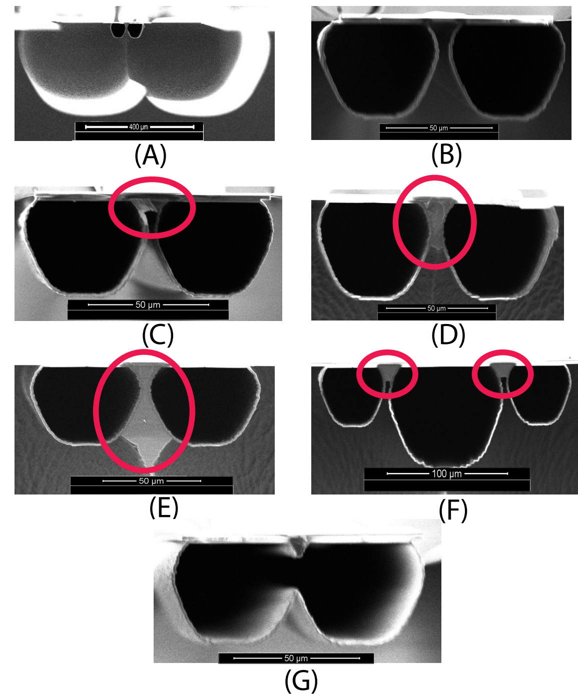

Figure 2: SEM photographs of (A) a fully released two separated channel structure, and close-ups of two channels (B) with no remaining silicon, (C) with a small ($\sim 35\,\mu\text{m}^2$) silicon electrode, (D) with a medium ($\sim 230\,\mu\text{m}^2$) silicon electrode, (E) with a large ($\sim 720\,\mu\text{m}^2$) silicon electrode; (F) a three-channel structure with two silicon electrodes, and (G) silicon electrode embedded inside the wider channel when $d = 55\,\mu\text{m}$.

The resistance of the silicon electrode depends on the doping level and cross-sectional area. We used boron-doped silicon wafers with resistivity ranging from 0.01 to $0.02\ \Omega \cdot \text{cm}$. The results in Figure 2 show that the cross-sectional area can be designed from approximately $35\,\mu\text{m}^2$ (Figure 2(C)) to $720\,\mu\text{m}^2$ (Figure 2(E)). Table 1 lists the calculated properties of the resulting silicon electrodes in comparison to a typical $10\,\mu\text{m}$ wide, $200\,\text{nm}$ thick platinum electrode on top of the channel. Especially when used as heaters the silicon electrodes provide a clear advantage. Supplying the same current density through the electrodes a factor of 10^4 to 10^5 more power can be dissipated due to the combination of higher resistance and larger cross-section. Figure 2(F) shows that it is also possible to embed two electrodes between three adjacent channels. This could for example be used to realize a relative permittivity sensor.

1 mm long microheaters	Resistivity [Ω cm]	Area [μm^2]	Resistance [Ω]	Power per unit length [$W m^{-1}$] (supply 1 mA)	Power per unit length [$W m^{-1}$] (supply 5×10^8 A m^{-2})
200 nm thick platinum	1×10^{-5}	2	50	5×10^{-2}	5×10^{-2}
Small silicon electrode	1×10^{-2}	35	2857	2.86	8.75×10^{2}
Medium silicon electrode	1×10^{-2}	230	435	4.35×10^{-1}	5.75×10^{3}
Large silicon electrode	1×10^{-2}	720	139	1.39×10^{-1}	1.8×10^{4}

Table 1: Comparison between platinum and silicon electrodes for Joule heating. For current density of 5×10^8 A m^{-2}*, silicon electrodes with large cross-sectional area and resistance can dissipate more power per unit length.*

CONCLUSIONS

Surface Channel Technology can be upgrade to become a more diverse microfluidic technology platform, simply by introducing the bulk silicon electrodes between the adjacent channel sidewalls. Different size and geometry of bulk silicon electrodes can be customized and optimized by tuning parameters d and W. It offers advantages for various microfluidic applications, such as much higher power dissipation when used as microheaters, higher sensitivity when used as strain gauges due to the piezoresistivity of silicon, and the possibility of sidewall capacitive sensing.

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