# FABRICATION METHOD OF MICROFLUIDIC CHANNELS WITH CIRCULAR CROSS SECTION FOR MICRO-CORIOLIS MASS FLOW SENSOR

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## ABSTRACT

This paper presents a new fabrication method to realize a channel underneath the surface of a single silicon substrate for micro Coriolis flow sensing application, as well as other multiparameter systems, such as thermal flow sensors. It allows to fabricate channels with a nearly perfect circular cross section without bonding of two wafers. With this technology, problems such as leakage, deformation of channels due to pressure and temperature that affect the performance of micro Coriolis flow sensor can be reduced significantly. Moreover, it leaves only very little topography on the surface of substrate, hence integration of actuation and readout systems by metal deposition can still be followed easily afterwards.

## KEYWORDS

Circular cross section, Buried channel technology, Wet etch, HNA, Flow sensors, Microfluidics

## INTRODUCTION

The concept of this new method for fabricating microfluidic channels for micro Coriolis flow sensing application is based on the combination of Buried Channel Technology (BCT) [1, 2] and silicon isotropic wet etching, which is known as HNA etching [3]. With this combination, it allows to fabricate a channel buried in Si substrate. With a starting point of etching at the bottom of a trench instead of at the substrate surface, a channel with a circular cross section can be realized by isotropic etching of Si. Compared to the Surface Channel Technology (SCT), which was used as a standard technology for the fabrication of Coriolis mass flow meter and other microfluidic devices [4, 5, 6], this new method has the potential to achieve much larger micro structures.

### Buried Channel Technology

Buried Channel Technology, or so called BCT, derived from the well-known SCREAM process, was invented in 1999 at MESA+ Institute to fabricate micro structures for fluidic applications in silicon substrate [1, 2, 7]. It allows to fabricate channels buried in the silicon substrate. The main steps of this process are trench etching, coating, bottom coating removal and etching of channel. Figure 1 shows the cross section of channel fabricated by BCT. By adjusting the width and depth of trenches, different sizes of channels can be realized in one substrate with only one step of lithography, which gives the possibility to integrate multi microfluidic devices with one lithographic mask.

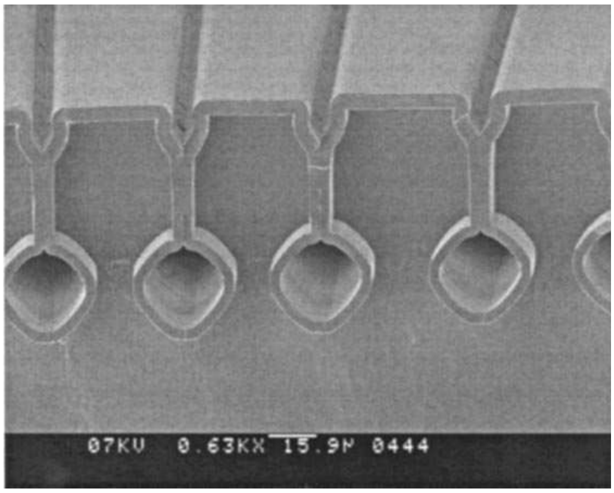


*Figure 1: SEM image of cross sections of channels fabricated by BCT [1].*

### Si Isotropic Wet Etching

Silicon isotropic wet etching, also known as HNA etching, is a chemical etching of silicon by a mixture of hydrofluoric acid (H), nitric acid (N) and acetic acid (A), while some researchers like to use water instead of acetic acid. It is proceeded by a sequential oxidation-followed-by-dissolution process [3, 8]. The complete reaction can be described as:

$$Si + 2\,HNO_3 + 6\,HF \longrightarrow H_2SiF_6 + 2\,HNO_2 + 2\,H_2O$$

The factor that limits the etch rate is highly dependent on the composition of mixture. When the concentration of nitric acid is low and hydrofluoric acid is high, the etch rate of process is limited by the oxidation step. When in opposite situation, the limit is then the dissolution of $SiO_2$. B. Schwartz *et al* investigated and explained in detail the etching mechanism behind this process in [3]. Figure 2 shows a semi-circular cross section of etched silicon substrate through a 10μm-wide line.

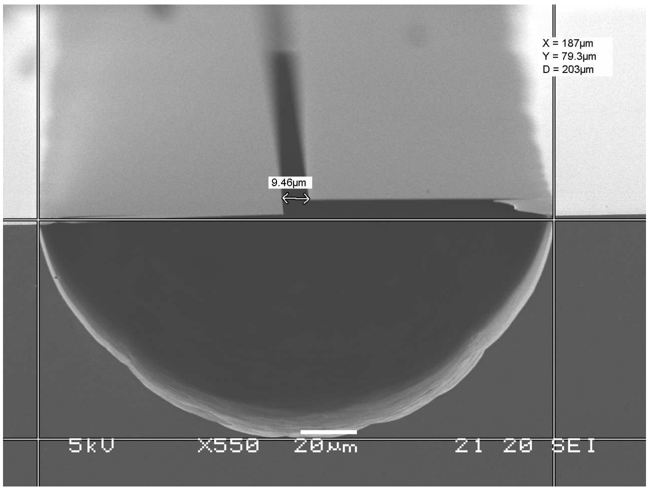


*Figure 2: SEM image of cross sections of channels etched in HNA solution (69%$HNO_3$:50%HF:$H_2O$=2:1:2) for 60*min *with SiRN mask.*

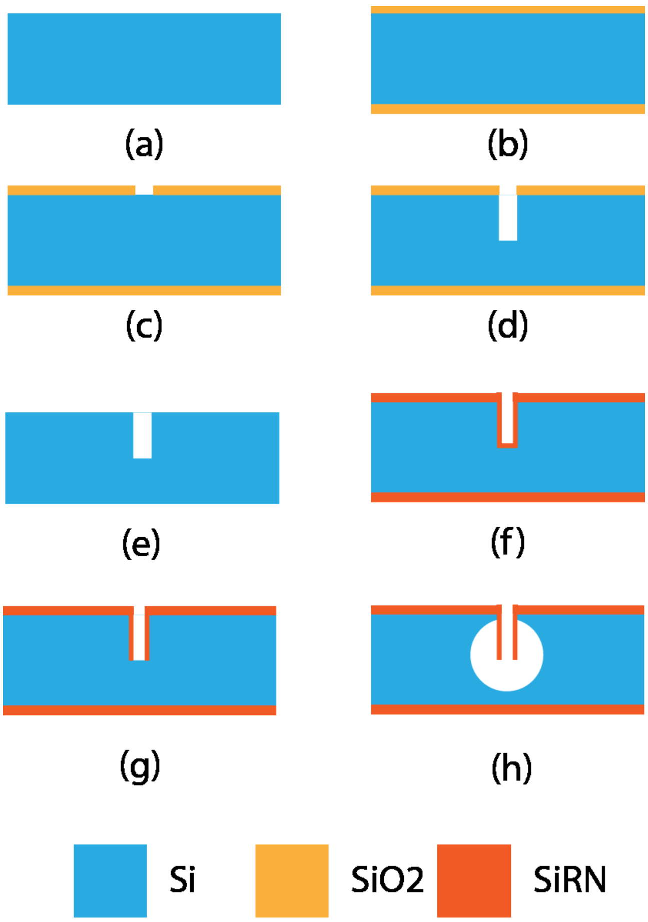


*Figure 3: Cross section view of fabrication steps for creating buried channels. (a): Bare silicon wafer. (b): Silicon wafer with 500*nm *$SiO_2$. (c): Patterning of line openings. (d): Trench etching. (e): Stripping of $SiO_2$. (f): SiRN coating. (g): Trench bottom coating removal. (h): Channel etching.*

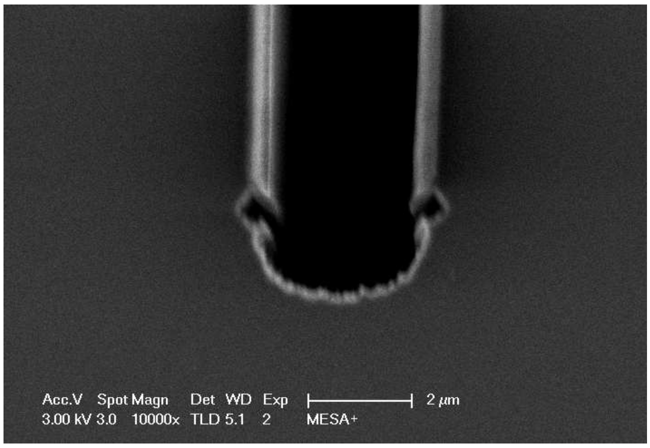


*Figure 4: SEM image of bottom coating removed trench (3*μm *wide) from early test to optimize the recipe of process.*

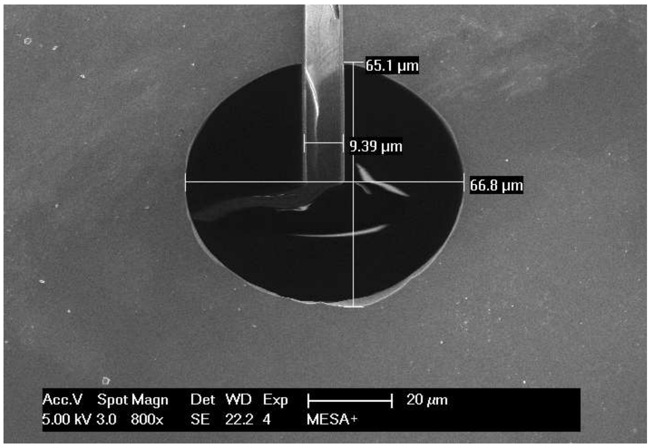


*Figure 5: SEM image of cross section of a channel after 65*min *etching in HNA (69%$HNO_3$:50%HF:$H_2O$=2:1:2).*

## FABRICATION

An overview of fabrication process can be seen in Figure 3. The steps are all done with standard recipe in the cleanroom of MESA+. First, silicon substrate is cleaned and oxidized to obtain a layer of 1μm $SiO_2$ (Figure 3b), serving as hard mask for Si etching in later steps. Lines with width of 10μm are etched through this layer (Figure 3c) and then followed by BOSCH process to produce trenches (Figure 3d). After that, $SiO_2$ layer is stripped by HF (Figure 3e) and coating of trenches is done by LPCVD 1μm low stress silicon rich nitride (SiRN) (Figure 3f). To remove the coating at the bottom of trenches, a PECVD $SiO_2$ layer is used as mask to protect SiRN on substrate surface. Due to the fact that trenches are of high aspect ratio and PECVD is a non-conformal deposition, bottom of the trench is not covered by this $SiO_2$ layer. Thus by running a plasma etching of SiRN, coating at bottom of trenches can be removed while substrate surface and sidewall of trenches stay. Figure 4 shows the bottom of trench after removing the coating layer. After successfully removing the bottom coating of trenches, the substrate is then etched in HNA solution (69%$HNO_3$:50%HF:$H_2O$=2:1:2) for 65mins. The cross section is shown in Figure 5.

## DISCUSSION

Compare the result shown in Figure 5 to Figure 2, the etch rate of silicon decreases significantly, this is due to the fact that diffusion of etching product and etchant through the deep trench is more difficult than through line openings on the substrate surface. A magnetic stirrer or ultrasonic bath can be the solution to achieve a higher etch rate. Together with a sufficient supply of etchant, the maximum diameter of etched channels will be limited only by the depth of trench and thickness of SiRN mask. From the earlier test, SiRN is a good material serves as mask for HNA solution, with an etch rate of approximately 2$\sim$3nm per minute. A thicker layer of SiRN can stand longer during etching, however, as a trade-off it also becomes more difficult to remove the layer at the bottom of trenches. Thus an alternate material can be considered to serve as mask for HNA solution for the future.

## CONCLUSION & OUTLOOK

A brief introduction of how to fabricate channels buried in a silicon substrate with a nearly perfect circular cross section is presented. The result is preliminary but shows a potential for producing extra-large channels of diameters up to few hundreds µm with this technology. Compared to channels fabricated by standard SCT, the main advantages of this new method are: 1) Reduction of temperature and pressure dependency for micro Corilis flow sensing application due to the nearly circular cross section, 2) A wider flow range can be covered with different sizes of channels. Furthermore, the cost of fabrication can be reduced as well since channels are etched by wet chemicals instead of plasma. Next step of the work will be focused on optimizing fabrication steps to realize an extra-large channel, then followed by sealing and releasing to achieve a free suspended tube for micro Coriolis flow sensing application.

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