



AGEING AND EMBEDDED INSTRUMENT MONITORING OF ANALOGUE/MIXED-SIGNAL IPS

Jinbo Wan

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INVITATION

to attend the public defense
of my PhD thesis

AGEING AND EMBEDDED INSTRUMENT MONITORING OF ANALOGUE/ MIXED-SIGNAL IPS

by
Jinbo Wan

on Friday 1st November 2019
at 10:45 in Waaier,
4 - Prof.dr. G. Berkhoff-zaal,
University of Twente

Afterwards there will be a
reception to which you are
also cordially invited.

PARANYMPHS
Mark Theodoridis
Digeorgia Natalie Da Silva

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Jinbo Wan

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DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof.dr. T.T.M. Palstra,
on account of the decision of the Doctorate Board,
to be publicly defended
on the 1st of November 2019 at 10:45am

by

Jinbo Wan

born on the 2nd of February 1979
in Linyi, China

This dissertation has been approved by:

Supervisor:

dr.ir. H.G. Kerkhoff

Cover design: Ilse Modder

Photo by: Adi Goldstein

Printed by: Gildeprint BV

Lay-out: Jinbo Wan

ISBN: 978-90-365-4829-8

DOI: 10.3990/1.9789036548298

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	dr. J. Bisschop

Acknowledgements

My sincere thanks go to my wife, Jifeng Tang, for her countless efforts and time spent on taking care of family during my thesis writing. Without her help, I could not have made it. Also appreciation for my parents for their understanding when i was busy with my thesis and could not go back to visit them.

I would like to show my gratitude particularly to my supervisor Hans Kerkhoff for his mentorship and support throughout my PhD work. Furthermore for his great patience and tremendous amount of time spent on reviewing my thesis. Also thanks to Prof. Gerard Smit for his reviewing of my thesis. I also would like to thank my colleagues at the University of Twente: Andreina Zambrano, Yong Zhao, Aamir Khan, Ahmed Ibrahim, Hassan Ebrahimi, Ghazanfar Ali, Bert Helthuis, Marlous Weghorst, and so on. I keep great memories to know them and work with them at the University of Twente.

Great acknowledgements to Jaap Bisschop for providing me with the opportunity to co-operate with NXP Semiconductors during my PhD project. A lot of thanks to my colleagues from NXP Semiconductors for their understanding during my thesis writing: Johan Knol, Wim Nijland, Mari Vogels, Mark Theodoridis, Louis Zheng, Jeroen Jalink, Lei Peters Wu, Claud van Oers, Mary Ann C. Bautista, Peter Vullings etc.

Thank you everyone!

Abstract

(Dutch)

Door de toename van het aantal SoCs in veiligheidskritische applicaties zoals in zelfrijdende autos, is onderzoek naar de betrouwbaarheid van elektronische circuits een belangrijk onderzoeksonderwerp geworden. De meeste inspanning is tot op heden vooral gericht geweest op puur digitale blokken. Het meest kritische deel, namelijk het analoge voorste stuk (AFE) is echter tot op heden nauwelijks onderzocht. Om deze reden ligt de nadruk van dit promotie onderzoek op betrouwbare analoog/mixed-signal (AMS) AFEs in veiligheidskritische applicaties zoals in autos.

Dit promotieonderzoek geeft een overzicht van de betrouwbaarheid van CMOS AMS circuits. De nadruk ligt op betrouwbaarheidsverschijnselen op nanometer schaal CMOS transistoren (kleiner dan 65nm). Meer specifiek op de overheersende NBTI betrouwbaarheidseffecten: fysische mechanismen, modellen en simulaties worden in detail behandeld.

NBTI modellering, metingen en validatie worden in detail bediscussieerd. Twee originele bijdragen worden er in beschreven. Een bijdrage betreft een compact NBTI model. Dit model wordt gebruikt voor de simulatie van NBTI degradatie van analoog/mixed-signal schakelingen. Dit nieuwe compacte NBTI model is gebaseerd op het iteratief oplossen van reactie-diffusie vergelijkingen. Dit model kan overweg met willekeurige signalen en is hierdoor geschikt voor analoog/mixed-signal simulaties. Het model is geëvalueerd voor een (NXP) 140nm CMOS technologie. Hierbij is gebruik gemaakt van zowel een blok golf als willekeurige signaal belasting. Het model is geïmplementeerd in de Cadence ADE omgeving met behulp van Verilog-A. Het is geschikt voor het simuleren van zowel deterministische als ook stochastische NBTI verouderingseffecten. De simulatie snelheid is ongeveer duizendmaal sneller dan voor andere reactie-diffusie gebaseerde modellen en is op ongeveer hetzelfde snelheidsniveau als transient simulaties.

Een andere originele bijdrage is het MOS drain-stroom model. Dit model is gebruikt om een eenvoudig te ontwerpen low cost on-chip drempel-spanning (V_{th0}) meetinstrument te maken en grote hoeveelheden NBTI degradatie data te verzamelen. Het nieuwe gesloten vorm drain-stroom model maakt het mogelijk MOS V_{th0} metingen uit te voeren in nanometer CMOS technologie. Een embedded meetinstrument met een lage overhead geschikt voor het meten van veroudering geïnduceerde V_{th0} verschuiving wordt voorgesteld. Langdurige stress tests laten zien dat de on-chip V_{th0} meting een V_{th0} verschuiving kan karakteriseren met een nauwkeurigheid van 3mV.

Na het opzetten van een reliability model en simulatie methode worden verschillende IP-blokken gesimuleerd en bediscussieerd voor het betrouwbaar maken van analoge circuits. Het eerste test vehicle is een in een 65nm MOS technologie ontworpen analoge versterker (OpAmp). Deze OpAmp bevat een nieuwe gain-boost methode waarmee de OpAmp een versterking haalt van 104dB en een unity gain bandwith van 783MHz. NBTI simulaties tonen aan dat de versterker offset de meest verouderingsgevoelige parameter is. Embedded instrumentatie gebaseerd op een nieuwe meet theorie is ontwikkeld voor de versterker offset en gain. Het instrument beschikt over een digitale interne kalibratie functie voor interne offset. Het is ontworpen in een 65nm LP digitaal CMOS proces en beschikt over een IEEE 1687 interface. Voor het besparen van kosten is het mogelijk het instrument te gebruiken voor meerdere analoge OpAMPs. Als het instrument niet wordt gebruikt kan het worden uitgeschakeld voor het beperken van het stroomverbruik.

Na OpAmps behandelt dit promotieonderzoek het gebruik van embedded instrumentatie in actieve filters voor AFEs voor autos. Experimenten laten zien dat de in actieve filters gebruikte feed back in veel gevallen voldoende bescherming biedt tegen betrouwbaarheidsproblemen van AFEs onder zware auto missie profielen. In sommige gevallen is het echter mogelijk dat de filter karakteristiek dusdanig veranderd dat dit leidt tot een foutieve sensor uitlezing. Dit kan aanleiding geven tot mogelijke veiligheidsproblemen van het betreffende voertuig. Een voorbeeld hiervan is het beschreven voorbeeld van een OTA-C laagdoorlaat filter. Het gedurende de levensduur observeren van filters met behulp van embedded instrumenten maakt het mogelijk om te waarschuwen met een dashboard melding of direct corrigerende maatregelen te nemen.

Afsluitend is een 10-bits volledig differentieel SAR ADC ontworpen in 65nm CMOS technologie. Hiervan zijn aansluitend de NBTI betrouwbaarheidseffecten gesimuleerd. Deze simulaties tonen aan dat NBTI gerelateerde veroudering aanleiding kan geven tot vertragingen

in de asynchrone SAR logica met mogelijke timing fouten als gevolg. De laatste bits van de ADC zijn hierdoor zinloos. NBTI degradatie van de SAR ADC comparator kan leiden tot een extra offset met als mogelijk gevolg offset fouten in de ADC. Twee embedded instrumenten worden voorgesteld om zowel timing als offset problemen in de SAR ADC te detecteren. Dit maakt de beschikbaarheid van betrouwbare ADCs mogelijk.

Het verouderingsgedrag van alle essentiële IP blokken binnen een AFE zijn voor dit promotie onderzoek onderzocht. Aansluitend worden nieuwe methoden beschreven gebaseerd op embedded instrumentatie voor het betrouwbaar maken van deze systemen. Enkele algemene conclusies worden getrokken op basis van de hierboven beschreven informatie. Beperkingen van het huidige en toekomstig onderzoek worden ook aangestipt. Afsluitend is een lijst bijgesloten van alle door de auteur geschreven publicaties.

Abstract

(English)

With an increasing number of **SoCs** being used in safety-critical applications like automotive, highly dependable circuits become an important research topic. However, most of the effort until now was spent on pure digital blocks. The most critical part, the analogue-front-ends are hardly being dealt with. Therefore the focus of this thesis is on dependable **Analogue/mixed-signal Front-Ends** in safety-critical applications like automotive.

In this thesis, an overview of the dependability of **CMOS AMS** circuits is provided. Emphasis is put on the reliability phenomena of nano-meter **CMOS** transistors (65nm and below), especially on the dominating **NBTI** reliability effects. Since this thesis is dominated by **NBTI** simulations, **NBTI** physical mechanisms, modelling and simulations are treated in detail. The target **AFE** in the thesis is also introduced. Two main directions to improve dependability are discussed.

Subsequently, **NBTI** modelling, measurements, validation and simulation are discussed in detail. Two original works are described, dealing with models. One original contribution is a **NBTI** compact model, which is later on used to simulate **NBTI** degradation of analogue/mixed-signal circuits. This new compact **NBTI** model is based on iteratively solving the **Reaction-Diffusion** equations. This model can accurately handle arbitrary stressed waveforms for the up-limit envelope and is thus very suitable for analogue/mixed-signal simulations. It is subsequently evaluated for a (NXP) **CMOS** 140nm technology with square-wave stresses and arbitrary wave stresses. The model is implemented in the Cadence **ADE** environment with Verilog-A, and can simulate both deterministic as well as stochastic **NBTI** ageing effects. The simulation speed is about thousand times faster than for other **Reaction-Diffusion**-based models, and is at the same speed level as transient simulations.

Another original result is the **MOS** drain-current model which is used to build an on-chip V_{th0} measurement **Embedded Instrument** and gather a large amount of **NBTI** degradation data

which is more convenient to design as well as featuring low costs. The new closed-form model for the MOS drain current is provided to facilitate MOS threshold-voltage measurements in nanometer CMOS technologies. A low overhead on-chip Embedded Instrument for ageing-induced threshold-voltage shift measurement is proposed. Long-time stress tests show that the on-chip V_{th0} test can characterize a threshold-voltage shift with 3mV accuracy.

After setting up the reliability model and simulation method, different analogue IP blocks are simulated and discussed to make the analogue IPs dependable. The first vehicle is an analogue OpAmp. A test bench OpAmp is designed in 65nm CMOS technology. It incorporates a new gain-boosting method. Based on the method, the test bench OpAmp reaches 104dB with 783MHz as the unity-gain bandwidth. The NBTI effect is simulated next; based on the simulation results, we observed that the most ageing-sensitive parameter in the OpAmp is the offset. An offset and gain Embedded Instrument for OpAmp IPs is subsequently designed based on a new measurement theory. This Embedded Instrument can self-calibrate its resident offsets in the digital domain after each measurement. The monitor is designed in 65nm LP digital CMOS process and provides an IEEE 1687 interface. It can be shared with other analogue OpAmp IPs to reduce the cost and shut down in the case of an idle situation to save power.

After OpAmps, the thesis continues dealing with dependable active filters in automotive analogue front-ends in SoCs by using an embedded instrument. It is shown by experiments that the feed-back in many active filters provides sufficient protection against reliability issues in analogue front-ends even under harsh automotive mission profiles. However in some cases, like the second-order OTA-C low-pass filter example, the filter characteristics may change to the extend that they give erroneous sensor readings. This can potentially endanger the car safety. By monitoring the filter during lifetime using an Embedded Instrument, either car-console flagging or direct corrective counter actions can be taken.

Finally, a 10-bits fully differential SAR ADC is designed in 65nm CMOS technology. Next, the NBTI reliability effects are simulated. The NBTI simulations show that the NBTI can increase the delay in the asynchronous SAR logic and generate timing errors which can make the last bits of the ADC meaningless. For the comparator, NBTI degradation can induce an extra offset and cause offset errors in the ADC. Two embedded instruments are introduced to detect both timing as well as offset errors in the SAR ADC, which enable the availability of dependable ADCs.

All the essential **IP** blocks inside an **AFE** are investigated in this thesis for their ageing behaviour and subsequently new methods with **Embedded Instruments** are described to make them dependable. Based on the information above, some general conclusions are drawn. Limitations of the current and future research are also addressed. At the end of the thesis, all publications written by the author are listed.

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List of Abbreviations

$\Delta\Sigma$	Delta-Sigma. 136
ABS	Anti-lock Braking System. 116
AC	Alternating-Current. 34 , 49 , 51 , 77 , 102 , 163
ADC	Analogue-to-Digital Converter. xii , xvii , xviii , xxi , xxiii , 8 , 9 , 17 , 26 , 27 , 33 , 62 , 68 , 69 , 70 , 72 , 77 , 83 , 84 , 85 , 99 , 116 , 125 , 128 , 135 , 136 , 137 , 138 , 139 , 140 , 141 , 142 , 143 , 145 , 146 , 147 , 148 , 149 , 150 , 151 , 152 , 153 , 154 , 155 , 156 , 157 , 158 , 159 , 162 , 163 , 165 , 166 , 185 , 186 , 187 , 188
ADE	Analogue Design Environment. xi , xxv , 9 , 35 , 41 , 52 , 54 , 56 , 57 , 77 , 163
AFE	Analogue/mixed-signal Front-End. xi , xiii , xix , xxi , 1 , 2 , 3 , 4 , 6 , 8 , 13 , 17 , 25 , 26 , 28 , 77 , 83 , 84 , 115 , 116 , 125 , 135 , 136 , 138 , 161 , 162 , 165 , 166 , 167
AMS	Analogue/Mixed-Signal. xi , 3 , 6 , 7 , 13 , 24 , 25 , 26 , 27 , 28 , 33 , 34 , 35 , 36 , 52 , 77 , 81 , 82 , 98 , 161 , 162 , 163 , 166
BIST	Built-in-Self-Test. 17 , 27
BSIM	Berkeley Short-channel IGFET Model. xxi , 63 , 66 , 67 , 68 , 70 , 71
CHC	Channel Hot-Carrier. 166 , 167

CMOS	Complementary Metal Oxide Semiconductor. xi , xii , xvi , xvii , xix , 6 , 8 , 9 , 13 , 14 , 15 , 16 , 17 , 18 , 24 , 27 , 33 , 34 , 35 , 36 , 38 , 43 , 44 , 47 , 58 , 62 , 77 , 81 , 82 , 84 , 85 , 87 , 91 , 104 , 108 , 111 , 116 , 117 , 118 , 128 , 135 , 136 , 137 , 139 , 141 , 143 , 145 , 147 , 149 , 158 , 161 , 163 , 164 , 165 , 166
CPS	Cyber-Physical System. 1 , 2 , 4
CPU	Central Processing Unit. 17 , 57 , 69 , 185
DAC	Digital-to-Analogue Converter. xxiii , 62 , 69 , 70 , 72 , 97 , 127 , 129 , 136 , 137 , 143 , 145 , 185 , 186 , 188
DC	Direct-Current. xix , xxii , 34 , 37 , 39 , 42 , 43 , 44 , 48 , 49 , 51 , 53 , 60 , 77 , 82 , 84 , 88 , 89 , 94 , 106 , 117 , 118 , 124 , 125 , 126 , 127 , 163
DNL	Differential Non-linearity. 147
DSP	Digital signal processor. 185
DUT	Device Under Test. xxi , 36 , 58 , 62 , 73 , 74 , 75 , 76 , 99 , 100 , 102 , 103 , 104 , 109 , 111 , 164
EDA	Electronic Design Automation. 117
EI	Embedded Instrument. xi , xii , xiii , xvi , xvii , xviii , xxi , xxii , xxiii , xxv , 9 , 13 , 26 , 27 , 28 , 33 , 36 , 58 , 59 , 61 , 63 , 65 , 67 , 68 , 69 , 71 , 73 , 75 , 77 , 81 , 82 , 96 , 98 , 99 , 100 , 102 , 103 , 104 , 105 , 106 , 109 , 110 , 111 , 115 , 116 , 117 , 125 , 126 , 127 , 128 , 129 , 131 , 135 , 154 , 155 , 156 , 157 , 158 , 161 , 162 , 164 , 165 , 166 , 167
EKV	C. C. Enz, F. Krummenacher and E. A. Vittoz. 63 , 64
ELESIS	European Library-based flow of Embedded Silicon test Instruments. xv , 7 , 8 , 9 , 25
ENOB	Effective-Number-of-Bits. 84
EOT	Equivalent Oxide Thickness. 41
EPS	Electric Power Steering system. 116

FinFET	Fin Field-Effect Transistor. 16 , 166 , 167
FVF	Flipped-Voltage-Follower. xxii , 91 , 106 , 107
HAST	Highly Accelerated Temperature/Humidity Stress Test. 3 , 158
HCI	Hot-Carrier Injection. 15 , 24 , 34 , 71 , 118
HTOL	High Temperature Operating Life. 3 , 158
HTSL	High Temperature Storage Life. 3 , 158
IC	Integrated Circuit. 1 , 2 , 3 , 4 , 6 , 14 , 117 , 167
INL	Integral Non-linearity. 147
IoT	Internet of Things. 1 , 2
IP	Intellectual Property. xii , xiii , 2 , 4 , 6 , 7 , 8 , 16 , 17 , 25 , 26 , 27 , 28 , 81 , 82 , 98 , 111 , 135 , 154 , 161 , 162 , 164 , 165 , 166
JEDEC	Joint Electron Device Engineering Council. 3 , 44 , 60 , 63
LDD	Lightly-Doped-Drain. 15
LP	Low-Pass. xvii , xxii , 116 , 117 , 118 , 119 , 120 , 121 , 122 , 123 , 124
LSB	Least Significant Bit. 138 , 142 , 145 , 147 , 148 , 150 , 152 , 157 , 158 , 185
LSM	Least Squares Method. 47 , 66
MOS	Metal Oxide Semiconductor. xi , xii , xxi , 58 , 64 , 75 , 116
MOST	Metal-Oxide-Semiconductor Field-Effect Transistor. xvi , xviii , xxi , 8 , 9 , 15 , 27 , 33 , 35 , 36 , 58 , 59 , 62 , 63 , 66 , 67 , 68 , 69 , 70 , 71 , 72 , 73 , 74 , 76 , 77 , 87 , 89 , 137 , 149 , 163 , 164
MSB	Most Significant Bit. 138 , 146
MSM	Measurement-Stress-Measurement. 35 , 59
MTBF	Mean Time Between Failures. 3

NBTI	Negative Bias Temperature Instability. xi , xii , xvi , xviii , xix , xx , xxi , xxii , xxv , 9 , 13 , 14 , 15 , 16 , 17 , 18 , 19 , 20 , 21 , 22 , 23 , 24 , 25 , 26 , 27 , 28 , 33 , 34 , 35 , 36 , 37 , 38 , 39 , 40 , 41 , 42 , 43 , 44 , 45 , 46 , 47 , 48 , 49 , 50 , 51 , 52 , 53 , 54 , 55 , 56 , 57 , 58 , 59 , 60 , 61 , 62 , 64 , 66 , 68 , 70 , 71 , 72 , 74 , 75 , 76 , 77 , 81 , 82 , 84 , 93 , 94 , 96 , 102 , 111 , 115 , 118 , 119 , 120 , 124 , 125 , 126 , 127 , 128 , 135 , 136 , 147 , 148 , 149 , 150 , 151 , 153 , 154 , 158 , 161 , 162 , 163 , 164 , 165 , 166 , 167 , 169
NMOS	N-type Metal Oxide Semiconductor. xx , xxi , 15 , 66 , 67 , 68 , 69 , 149
NMOST	n-type Metal-Oxide-Semiconductor Transistor. 15 , 85 , 87 , 88 , 89 , 90 , 106 , 139 , 148
OpAmp	Operational Amplifier. xii , xvi , xvii , xviii , xxi , xxii , xxv , 7 , 8 , 9 , 26 , 27 , 81 , 82 , 83 , 84 , 85 , 86 , 87 , 89 , 90 , 91 , 92 , 93 , 94 , 95 , 96 , 97 , 98 , 99 , 101 , 102 , 103 , 105 , 107 , 108 , 109 , 110 , 111 , 117 , 118 , 119 , 120 , 121 , 125 , 126 , 129 , 138 , 139 , 147 , 155 , 162 , 164 , 165 , 166
OTA	Operational Transconductance Amplifier. xii , xvii , xviii , xxii , 115 , 116 , 117 , 121 , 122 , 123 , 124 , 125 , 126 , 127 , 128 , 129 , 131 , 162 , 165
OTF	On-The-Fly. 22 , 35 , 44 , 59 , 60
PBTI	Positive Bias Temperature Instability. 15 , 16 , 148 , 149 , 152 , 166 , 167
PC	Personal Computer. 1
PDK	Process Design Kit. 117
PFB	Positive-Feedback. xxi , 90 , 97 , 98
PLL	Phase-Lock-Loop. 17 , 155
PMOS	P-type Metal Oxide Semiconductor. xix , xxi , 14 , 18 , 19 , 20 , 21 , 34 , 35 , 43 , 44 , 45 , 48 , 55 , 57 , 69 , 73 , 74 , 75 , 76 , 118 , 124 , 148 , 163

PMOST	p-type Metal-Oxide-Semiconductor Transistor. xix , xxiii , 9 , 14 , 15 , 18 , 19 , 20 , 44 , 82 , 87 , 118 , 120 , 121 , 139 , 140 , 142 , 148 , 161
PPM	Parts per Million. 3
PSP	Philips Surface Potential. 63
PVT	Process, Voltage and Temperature. 86 , 129
RD	Reaction-Diffusion. xi , xvi , xix , 22 , 23 , 24 , 33 , 35 , 36 , 37 , 41 , 42 , 43 , 45 , 47 , 50 , 51 , 57 , 77 , 163 , 166 , 167
RL	Reaction-Limited. 22 , 23 , 24
SAR	Successive-Approximation Register. xii , xvii , xviii , xxi , xxiii , 9 , 83 , 135 , 136 , 137 , 138 , 139 , 140 , 141 , 142 , 143 , 144 , 145 , 146 , 147 , 148 , 150 , 151 , 152 , 153 , 154 , 155 , 156 , 158 , 159 , 162 , 165 , 166 , 185 , 186 , 187 , 188
SC	Switched-Capacitor. 115 , 116 , 117 , 120 , 126 , 131
SNR	Signal-to-Noise Ratio. 146
SoC	System-on-Chip. xi , xii , xxi , 2 , 4 , 6 , 7 , 8 , 25 , 36 , 62 , 63 , 68 , 69 , 70 , 72 , 77 , 81 , 98 , 106 , 115 , 116 , 135 , 155 , 162 , 163 , 164 , 165 , 166 , 167
SPICE	Simulation Program with Integrated Circuit Emphasis. 34 , 35 , 54 , 60 , 163
TC	Temperature Cycle. 3
TDDb	Time-Dependent Dielectric Breakdown. 15 , 34 , 71 , 118
TEM	Transmission Electron Microscopy. xix , 15 , 16
THB	Temperature Humidity Bias. 3 , 158
TOETS	Towards One European Test Solution. xv , 7 , 8 , 9 , 25
TSMC	Taiwan Semiconductor Manufacturing Company. xxi , 9 , 66 , 67 , 70 , 71 , 85 , 111 , 164 , 165
UT	University of Twente. 7

Chapter 1

Introduction

***Abstract-** Moore's law has driven the developments of [Integrated Circuits \(ICs\)](#) for more than 50 years. Not only the density of [ICs](#) has increased enormously, but also the computational power of [ICs](#) has improved dramatically. Due to these improvements, more and more functions are integrated into a single chip together with embedded software. The application areas have been extended beyond [Personal Computers \(PCs\)](#). Examples are smart phones, electrical cars, [Internet of Things \(IoT\)](#) and so on. Among these new application areas, many of them contain safety-critical applications. Therefore the [ICs](#) used in these safety-critical areas are required to be dependable, which include reliability but more than just reliability as will be described later. This thesis takes a first step in developing dependable [Analogue/mixed-signal Front-Ends \(AFEs\)](#). Being the starting chapter of this thesis, the background of the thesis is introduced first. Then the motivations for research are presented with several questions raised. The research frameworks which include two European projects are discussed next. Finally the outline of the thesis is presented.*

1.1 Introduction

Not so long ago, electric cars were still not yet driving on the road. [IoT](#) and [Cyber-Physical System \(CPS\)](#) were also not yet defined. Medical electronics such as implantable hearing-aids and internal temperature sensor capsules were still in their prototype phase. However, from the introduction of the smart phone, the development of the electronics already showed some trends, which is making more and more things smart and connected.

One of the examples is the automotive industry. More and more sensors are implemented in new cars, such as tyre-pressure sensors, wheel-rotation sensors, car radars, visual cameras and so on. To process the data from these sensors, more and more [ICs](#) are used in cars. Even

highly complicated chips like many processor [System-on-Chip \(SoC\)](#) are starting to be used in the automotive industry. These [ICs](#) or [SoCs](#) are required to be very dependable and have a long lifetime (10 to 15 years) [[Ker10](#)].

At the same time, the major market for semiconductor companies is the consumer market. The most important requirements of the consumer market are price, power consumption and performance. The dependability has a lower priority. A lifetime of 5 years is sufficient for most consumer products. These requirements have driven the semiconductor process into the nanometer range and heavy competition pushes the time-to-market period to a minimum [[Ely14](#)].

With the semiconductor process technology entering the nanometer region, many of the processing techniques are approaching their limits, like lithography and doping. [ICs](#) produced in the latest technology have many more failures than before and thus have lower yield [[Pre15](#)]. To find and analyse all failure modes, extra efforts and sufficient failure cases are required. These all take much time and hence increase costs.

Normally a semiconductor process technology for mass production needs at least two years to reach sufficient high yield, to be matured [[Sas03](#)]. Another few years are required to gather sufficient in-field returned failure samples for improving the process. Here the difference between consumer products and for instance automotive products becomes clear. For consumer products, one will not wait for the semiconductor process to be matured. Time-to-market has the highest priority. While for automotive products, quality and dependability are the most important considerations. Hence the safety-critical automotive products normally use older semiconductor process technologies than consumer products [[Pel13](#)]. The main reason is because they are required to be highly reliable and thus more dependable.

With time progressing, the automotive markets have become more and more attractive. Many semiconductor companies have entered this field. The competition becomes hot and time-to-market is critical. Using the latest semiconductor process (means small area and thus lower cost) for an automotive grade 0 product [[Aut07](#)], which means safety-critical products like all kinds of sensors in a car, while keeping the high dependability has become a very attractive topic. The same is also true nowadays for medical electronics, [IoT](#) and [CPS](#). Most of the research in highly dependable [ICs](#) is focused on digital [IP](#) blocks, like microcontrollers, microprocessors and logical function blocks. Very little related work can be found on dependable analogue/mixed-signal [IPs](#), especially the [AFE](#). In automotive [ICs](#), the [AFEs](#) are a critical part because they directly interact with the outside physical world.

In this thesis, the focus is on [AFE](#) blocks for safety-critical [ICs](#) in automotive applications. This chapter will introduce dependable systems, mission profiles, thesis motivation, project framework, the research questions, and thesis outline. In the following chapters, the author will subsequently deal in detail with the [Analogue/Mixed-Signal \(AMS\)](#) building blocks of dependable [AFEs](#).

1.1.1 Dependable Systems

For a chip used in a safety-critical system, common sense is that the quality of the chip is required to be very high. *Quality* refers to the number of chips which can deliver its specification when they reach customers (at 0 hour). It uses the number of failing samples in 1 million samples as an indication. For example, a 1 [Parts per Million \(PPM\)](#) quality means that on average there is one sample failing within one million chips delivered.

It is worth to mention that quality is used to describe a product at 0 operational hours (fresh state), not during the lifetime. To describe a product during its operational lifetime, another term called reliability is used instead. *Reliability* is the ability of a system or component to perform its required functions under stated conditions for a specified time [[Int06](#)]. The reliability can be characterized by the [Mean Time Between Failures \(MTBF\)](#). It is of vital importance for safety-critical systems. A product failure after a few years of usage is very difficult to predict during a fresh product test. Resulting from the efforts of the [Joint Electron Device Engineering Council \(JEDEC\)](#) [[Str08](#)], a lot of reliability tests have been developed and standardized to help estimating and improving the product reliability. These reliability tests include [Temperature Cycle \(TC\)](#) test, [High Temperature Operating Life \(HTOL\)](#) test, [Temperature Humidity Bias \(THB\)](#) test, [Highly Accelerated Temperature/Humidity Stress Test \(HAST\)](#) and [High Temperature Storage Life \(HTSL\)](#) test. With the help of these reliability tests, the silicon chip's early infant-failure rate can be reduced dramatically [[Pre15](#)].

On the other hand, reliability tests can be destructive and usually help to filter out the infant-failure samples. For improving the lifetime of products, especially wear-out time, these reliability tests only provide limited help [[Pre15](#)]. The samples used for reliability tests cannot be sold to customers anymore. They are used for study and improving the reliability of the product and process, but cannot guarantee that all products shipped to customers will have no reliability issues.

With the developments in technology, especially with the help of new smart and connected systems, one can even improve the product lifetime (wear-out) by self-monitoring or self-repair. *Dependability* is a kind of umbrella that spans several attributes (or views) like reliability,

availability, maintainability as well as safety and security [Int06]. A dependable system is often a fault-tolerant system. It is not only reliable but also knows how to proceed if the system (potentially) fails. Due to the computational capability of systems nowadays, the dependable system can not only adapt to changes in the outside world but also detect the failure in the system itself. If a failure occurs within the system, the dependable system could carry out a simple failure analysis to find the fault location. Corresponding counter actions (maintenance) like isolation, bypass, and replacing IPs with redundant resources can be implemented to emulate repair. The repair time is linked to the system availability [Int06].

A dependable CPS will totally change the way people interact with engineered systems – just as the Internet has transformed the way people interact with information [Nat16]. It will drive innovation and competition in many fields like autonomous driving, smart agriculture, smart energy grids, artificial intelligence robots, building design and automation, healthcare, and manufacturing.

In this thesis, our work is focussed on how to design dependable AFEs for automotive SoCs.

1.1.2 Mission Profiles

What are the requirements for a device in a dependable system? A simple answer is that it depends on the application domain. An IC used for smart phones has a totally different working environment as compared to an IC used for automotive safety purposes. The required lifetime is also different. If a failure occurs in the IC, the consequence will be totally different for a smart phone than for a safety system in a car.

In the semiconductor industry, these application differences are summarized and simplified into so-called mission profiles. A mission profile is a collection of relevant environmental stress and operational conditions. These conditions are the ones an IC is being exposed to during its full-life cycle [Pre15].

A mission profile could include:

- Lifetime in years.
- On-time in hours.
- Number of on-off cycles.
- Operational temperature.

Table 1.1: An example mission profile for a semiconductor device used in vehicles [Pre15].

Lifetime	On-time	On-off cycles	Temperature	Humidity
15 years (=131,400 hours)	12,000 hours	54,000	125°/ 150°C	95%

- Relative humidity.

The lifetime is defined as the time period between the completion of the manufacturing process of the product and the end-of-life of the system. For a portable device like smart phones, the lifetime is only considered to be 5 years. For a home applications like TVs, computers, radios and DVDs, the lifetime can be up to 10 years. For automotive applications, the lifetime is 15 years [Ely14, Pre15].

The on-time is defined as the total time during which the device is operating. The power-down mode is considered to be the case where the device is not operating and is thus not taken into account in the on-time. For a smart phone and TVs, the on-time is considered to be 6 hours per day. For a car, the on-time is assumed to be 2 hours per day [Ely14, Pre15].

The on-off cycles are defined as the times of switching on and switching off the device per day. For a portable device and home applications, the on-off cycles are counted as 4 times per day. For automotive products, the on-off cycles are defined as 10 times per day [Ely14, Pre15]. The previous data is coming from statistics of a large number of user cases.

The operational temperature is defined as the environmental temperature under which the device is operating. For portable devices, the operational temperature is set from -20°C to 55°C. For indoor home applications, the operational temperature is between 0°C to 40°C. For automotive products, the operational temperature is defined as -55°C to 125°C. Some extreme applications in automotive can go up to 150°C [Pre15].

The relative humidity is defined as the environmental humidity in which the device is working. For portable devices, home applications, automotive products, a humidity of 95% can be used for all.

Table 1.1 shows an example of the mission profile for a semiconductor device used in cars. The parameters in the profile will be normally used to determine the acceleration (reliability)

test conditions, like how many different reliability tests are required and what the temperature and time period are for each reliability test.

In our research, the target vehicles are the automotive AFEs. The focus is on the reliability behaviour during its lifetime and how to make it dependable under the automotive mission profile. The most important parameters in Table 1.1 are the lifetime and operational temperature.

1.2 Motivation

Most of the research in highly dependable SoCs are focussed on digital IP blocks, like microcontrollers, microprocessors and logic function blocks. The way of validation is normally assuming a special kind of failure happened or injecting an artificial fault into digital blocks. Subsequently it is verified if the proposed dependable system can handle the fault. Reliability simulations are rarely used. Even when implementing reliability simulations, it is normally carried out with a simple DC model without dynamic signals for the sake of simplicity [Kuf10].

However, in automotive ICs, the AFEs are the most critical (versus digital tolerancy) part because they directly interact with the outside physical world. Little publications can be found on dependable AMS IPs, especially for the AFEs.

The reason is that the study of the reliability behaviour over time, which is referred to as *ageing* in this thesis, are very difficult in analogue circuits as compared to digital circuits. It requires accurate reliability models which can handle arbitrary waveforms for analogue circuits. It also requires the simulation tools to support this kind of reliability models. One will need a transistor-level AFE design in advanced CMOS technologies to simulate ageing. And the parameters for the reliability model in advanced CMOS technologies are very difficult to obtain because they are often company-confidential information. As a result, dependable AMS IPs, especially the AFEs, are still open areas which are rarely touched.

The previous issues are our motivation to make a firm step in this area by studying the ageing of AFEs, finding weaknesses in AFE circuits and proposing solutions for designing highly dependable AFEs.

1.3 Industrial Platform in the TOETS and ELESIS Framework

Basis of this thesis is a European research project named “Towards One European Test Solution (TOETS)”. The TOETS project had the ambition to create a breakthrough in methods and flows used by the test technologies in terms of considering test in the whole value chain from design to application [Cat09].

The University of Twente was involved in two tasks defined in TOETS to develop dependable heterogeneous circuits and systems at both circuit level and system level. This thesis is partly the result of the project which targeted at the *circuit level*.

The TOETS project generated a lot of fruitful achievements. A dependable OpAmp has been designed and demonstrated in the project which can self-monitor and self-repair its ageing degradations. However, the solution that was demonstrated consumed a lot of power and much area overhead as the resulting circuits were complex. It is less attractive if an SoC has multiple of these dependable OpAmps. As a result it remained the question whether there was a better solution to reduce the overhead and make the solution both simple as well as generic.

The Eniac “European Library-based flow of Embedded Silicon test Instruments (ELESIS)” European project was successor of TOETS and provided a good opportunity to elevate the previous problems. The ELESIS European project was aimed to define and standardise built-in chip test features with a common interface that will enable the identification of faults relatively inexpensively and thus reduce production costs. The primary targets were IPs containing analogue, radio frequency and sensor components, as they are particularly difficult to isolate for an analysis of the test parameters [Eni12].

The University of Twente had a task in ELESIS which was the creation of embedded dependability instruments and their models operating on Analogue/Mixed-Signal (AMS) IPs. The instruments targeted the ageing monitoring of critical AMS blocks in SoCs. The instrument outputs could be used for adaptive correction of the building block performances over their operational lifetime.

Our contribution has been on circuit design, simulation and advancements in dependability technology methods as treated in this thesis. Three new embedded instruments developed by us have been added to the open European library for embedded instruments. They monitor

the ageing behaviour of an **OpAmp** (offset shift), **MOST** ageing behaviour (threshold shift) and **ADC** ageing (timing and offset shifts). The designed embedded instruments are general purpose **IPs** which not only can be used as online ageing monitor but can also be used in a final product test. The designed embedded instruments can be shared by several **IPs** in the **SoC** (*IP level*) and solve the power and area overhead problem as resulted from the **TOETS** project. The final results of the **ELESIS** project turned out to be very successful [Wan15].

1.4 Research Questions

Since there are only a few references to dependable **AFEs**, the project research is required to start from scratch. First, the ageing simulation platform for analogue circuits has to be established to evaluate analogue circuit-reliability. Furthermore, an **AFE** target vehicle (test circuit) is required to be designed for evaluation purposes. Next, solutions for highly dependable **AFEs** have to be proposed based on the previous evaluation results.

Overall, the following research questions have to be answered:

- What is the dominating ageing effect in advanced **CMOS** technologies?
- Can a ageing model be developed which can handle arbitrary stress waveforms in analogue circuits? How to obtain the model parameters?
- Is there a ageing simulation tool/environment which can incorporate our ageing model and how to perform validation?
- What should be is our target-vehicle **AFE** for carrying out ageing simulations and exploring weaknesses?
- What is best solution to construct a highly dependable **AFE**?

These questions will be answered in the remaining of this thesis and in particular in Chapter 7.

1.5 Outline of the Thesis

The organization of this thesis is now described in more detail.

Chapter 1 provided an introduction to the thesis: background, definition of dependable systems, and mission profiles of automotive products. The motivation for our research has been presented and this has distilled into a number of research questions. Two European projects, [TOETS](#) and [ELESIS](#), were the enablers for this thesis.

In the following Chapter 2, a thorough overview with respect to the current status of dependable analogue/mixed-signal research is given. The limitations and critical parts are being discussed. Based on chapter 2, the lack of tools for analogue circuit ageing simulation is seen as a major limitation for dependable analogue/mixed-signal circuit design.

As a result, a new [Negative Bias Temperature Instability \(NBTI\)](#) model is proposed to assist analogue circuit [NBTI](#) simulation in Chapter 3. A new simulation tool based on the proposed [NBTI](#) model is implemented in the Cadence [Analogue Design Environment \(ADE\)](#) while using the Verilog-A language. In order to measure [p-type Metal-Oxide-Semiconductor Transistor \(PMOST\)](#) threshold voltages and extract [NBTI](#) parameters, a new model for the nanometer [MOST](#) drain current is proposed. This new drain current model makes it possible to design an [Embedded Instrument \(EI\)](#) for on-line monitoring the [MOST](#) threshold voltage.

Chapter 4 focusses on analogue [OpAmps](#). Reliability simulations are carried out on a target [OpAmp](#) which is designed in [Taiwan Semiconductor Manufacturing Company \(TSMC\)](#) 65nm low power digital [CMOS](#) technology. Two repair strategies are shown in Chapter 4. The first one is by a programmable [OpAmp](#), while the second is employing an offset and gain [Embedded Instrument \(EI\)](#).

Chapter 5 deals with analogue active filters. The ageing simulations are carried out on three kinds of active filters in [TSMC](#) 65nm low power digital [CMOS](#) technology. The same two repair strategies as discussed in chapter 4 are demonstrated. We show the design of an active filter circuit and as well as an [EI](#) for enhancing its reliability.

In Chapter 6, mixed-signal [Successive-Approximation Register \(SAR\) ADCs](#) are the subject of interest. The ageing simulations are carried out on an own designed 10-bits [SAR ADC](#) and each of the sub blocks. All circuits are designed in [TSMC](#) 65nm low power digital [CMOS](#) technology. The circuit design effort for the [ADC](#) repair strategy as well as the [EI](#) effort are presented and the results are demonstrated.

Chapter 7 will provide the conclusions with respect to the research. The research questions as posed in Chapter 1 will be answered. Original contributions resulting from this research will be provided too. Also limitations of the current work will be dealt with. Recommendations for future works are also provided. Finally, all papers published by the author are listed explicitly.

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Chapter 2

Dependability Overview of CMOS Analogue/Mixed-Signal Circuits

***Abstract-** The dependability of [Analogue/Mixed-Signal](#) circuits will be defined at the beginning of this chapter. Emphasis will be put on the ageing of nanometer [CMOS](#) transistors. The history of different ageing phenomena and how these issues were solved in silicon process manufacturing will be reviewed. As the currently dominating ageing effect is [Negative Bias Temperature Instability](#), its physical mechanism will be treated in detail. The state-of-art in [Negative Bias Temperature Instability](#) modelling and simulations will be described. A target [Analogue/mixed-signal Front-End](#) is the focus in this thesis and will be introduced. There are two directions which can improve the dependability of [Analogue/mixed-signal Front-Ends](#), being an extra design effort and the [Embedded Instrument](#) approach. They will be presented at the end of this chapter.*

2.1 Introduction

In the original dependability definition [Int06], the system can consist of hardware, software, human elements, or a combination of any of these elements to perform the necessary functions. Dependability infers that the system is perceived to be trustworthy and has the ability to provide service upon demand as desirable performance attributes. The definition can be summarized in four concepts: reliability, availability, maintainability, and safety [Ker10a]. In principle, the dependability of analogue and mixed-signal circuits should answer the following questions:

- At what time the circuit is expected to be out of performance e.g. due to ageing? – **Reliability**
- How long is the circuit not available due to repair? – **Availability**

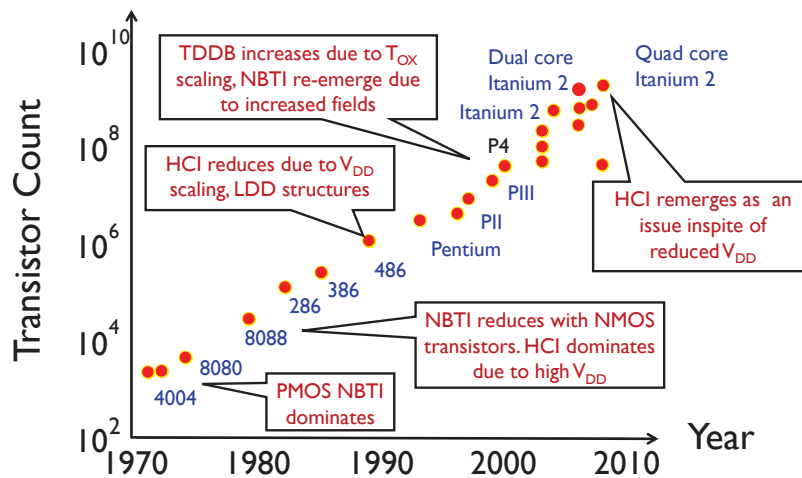


Figure 2.1: History of reliability issues in CMOS technologies [Ala13b].

- How to repair the circuit when it is out of performance? – **Maintainability**
- Will the circuit cause a safety problem due to its out-of-performance? – **Safety**

We will now discuss these dependability attributes in detail.

2.1.1 Reliability

Reliability represents the longevity of system operation without any incidents affecting system outage or impairment [Int06]. The reliability concerns the lifetime of the IC. The common definition for the IC lifetime is the time period after which the degradation of the IC performance is out of its tolerance band.

Reliability issues in CMOS technologies have existed for almost 40 years [Jep77], as shown in Figure 2.1. Although rarely noticed by circuit designers until recently, most of these reliability problems were solved at the manufacturing plants. With the technology entering the nanometer region, reliability issues cannot be easily solved in the old ways. Now more and more circuit designers are encouraged to take the reliability into account during design phase, otherwise it significantly reduces the product yield and lifetime [Gie08].

In the seventies, the **Negative Bias Temperature Instability (NBTI)** was the major reliability concern in PMOS technology. NBTI manifests itself as an increase in the threshold voltage and consequent decrease in the drain current and transconductance of a PMOST. Since the NBTI occurs under a negative gate-to-source voltage, it is only of concern to PMOSTs. With the

NMOS technology introduced in the eighties, NBTI turned out to be less a problem. Instead, another reliability phenomenon, referred to as Hot-Carrier Injection (HCI) became dominating.

HCI is a phenomenon in the MOST conducting channel where an electron or a hole gains sufficient kinetic energy to overcome a potential barrier which is necessary to break the interface state [Ogu80]. These high-energy electrons or holes are called “hot carriers”. They can be injected from the conducting channel into the gate-oxide. Finally they become trapped in the gate dielectric or tunnel out of the gate-oxide material. Resulting effects of HCI include increasing gate and substrate leakage currents, a decreasing drain-to-source current and increasing threshold voltage. HCI is more likely to happen in NMOSTs with a high drain-to-source voltage, because light-mass electrons are more easier to become "hot" than heavy-mass holes do. To reduce the HCI effect as well as power consumption, supply voltages of MOSTs were significantly reduced in the nineties from 5V to 3.3V. New process techniques like Lightly-Doped-Drain (LDD) helped further reducing the channel-to-drain electric field strength and also the HCI effect [Dho91].

As the scaling of the gate-oxide thickness continues, gate-oxide becomes so thin (already 2nm at 90nm CMOS technology) that a new failure mechanism named Time-Dependent Dielectric Breakdown (TDDB) occurs in both NMOSTs and PMOSTs. The TDDB is caused by formation of a conducting path through the gate-oxide due to an electron-tunnelling current if MOSTs are operated close to or beyond their specified operating voltages. Effects of TDDB in MOSTs can be a sudden increase in leakage current (hard breakdown) or continues to increase the threshold voltage and leakage current (soft breakdown) [Ala13a]. At the same time, to obtain sufficient charge in the channel with less gate capacitance, the electric field in the gate oxide is increased. As a result, NBTI re-emerged as a dominating issue in PMOSTs because of the increased electric field in the gate-oxide.

Intel introduced a new gate insulation material in its 45nm CMOS process, which is called high-K material [Boh07]. This material (combined of HfO_2 , ZrO_2 , Y_2O_3 , Al_2O_3 and so on) has a high dielectric constant K as compared to silicon dioxide (SiO_2) but is much thicker in dimension. The introduction of high-K materials reduced the TDDB issue efficiently. However, the high-K materials cannot contact with silicon directly. There needs to be a very thin layer SiO_2 between high-K and silicon. Due to the imperfection of this thin SiO_2 layer, both NBTI and Positive Bias Temperature Instability (PBTI) [Mar11] are dominating from 40nm CMOS technology and smaller. The PBTI effect can be treated in a similar way as NBTI and mainly occurs in NMOSTs. The transistor downscaling from 90nm to 32nm is shown in Transmission

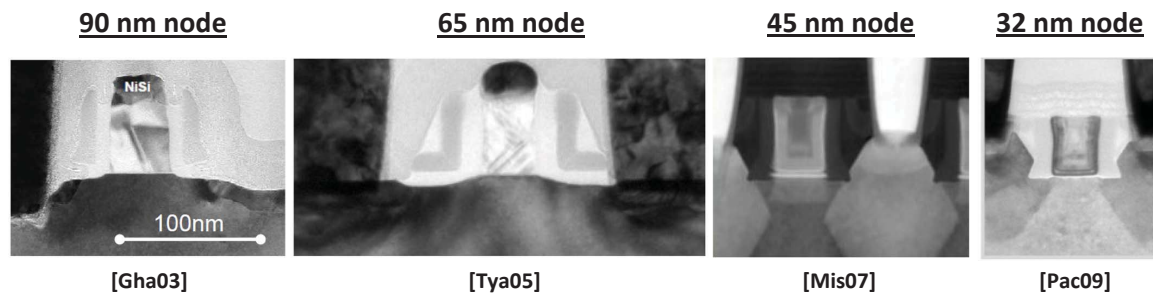


Figure 2.2: CMOS technology scaling in four technology nodes illustrated by Transmission Electron Microscopy (TEM) images [Gha03, Tya05, Mis07, Pac09]. They are scaled in the same dimensions [Sun08].

Electron Microscopy (TEM) cross-sections in Figure 2.2. Their physical sizes are scaled to be the same for comparison. For 90nm and 65nm nodes, the transistor gate oxides are so thin (around 2nm) that they are hardly visible in Figure 2.2. While the 45nm and 32nm transistors gate oxides can still be visible due to the increased thickness by the application of high-K materials.

Now the CMOS technology has entered the world of Fin Field-Effect Transistors (FinFETs) [Com13]. Many publications claim that NBTI and PBTI are still the most dominating reliability issue in FinFETs [Cho06, Lia05, Par07]. Due to our project limitation in time, in this thesis the study has been carried out on CMOS processing without high-K materials, such as 65nm, 90nm and 140nm technologies. Therefore the most dominating reliability mechanism in these technologies remains NBTI, which will be the focus of our attention.

2.1.2 Maintainability

Maintainability is the ease of access for system maintenance services, on-site or remote system restoration and recovery. In the case of transistor-level design in CMOS, maintainability or repairability in the classical sense is not feasible. If a defect in a transistor occurs, there is almost no way to repair the transistor. However, it is still possible in the sense that resulting faults at the circuit level can be internally detected, might be internally compensated, or if not feasible, the circuit or the whole IP could be isolated/bypassed and replaced by similar internal resources via electronic re-routing [Ker10b].

The maintainability at the circuit level asks for two requirements of the target circuit. The first requirement is that the circuit should be able to detect faults by itself. This will require

some function like [BIST](#). It has been successfully implemented in digital circuits like flash memories and [CPUs](#), as well as in analogue circuits like [Phase-Lock-Loops \(PLLs\)](#) and [ADCs](#).

The second requirement for maintainability is that the circuit should be capable to “repair” faults and restore its correct performance. The “repair” can be carried out locally by circuits via redundant re-routing and programmable tuning. It is also possible to carry out the repair at system level via compensation and recalculation in digital domains.

2.1.3 Availability

Availability exhibits the efficiency of system operation upon demand. For a transistor in [CMOS](#) technology with zero maintainability, meaning no repair is possible, the availability is actually equal to its lifetime. However for a circuit or [IP](#) with maintainability, the availability is the time period within its lifetime when the circuit is available and thus not under repair.

Maintainability and availability can be combined and characterized by the unavailability, which can be measured in time(s) in a year or after a fault event; it is the time over lifetime during which the system is being repaired (and hence unavailable). For safety-critical systems, the unavailability should be very low, for instance 10ms [[Ker10b](#)].

2.1.4 Safety

Safety is the occurrence or risk of injury, loss and danger to persons, property or environment. Safety can be described, among many others, by a percentage. In safety-critical systems, the safety should be 100%, meaning that no risk should exist under any conditions. For instance, the output of an [IP](#) should go to a predefined safe value (halt) in case of a non-repairable fault. In this thesis, the safety of analogue and mixed-signal circuits or [IPs](#) are treated as 100% safe and thus no safety issues will be discussed.

The dependability of an analogue or mixed-signal circuit or [IP](#) is described by characterizing the circuit’s reliability, availability, maintainability and safety. In the ideal case, the reliability of a fully dependable system should be 100% until the specified lifetime (e.g. 15 years), is never unavailable (0s) and features a 100% safety.

Aamir Khan wrote a thesis [[Kha14](#)] with the centre of interest in the maintainability and availability of [AFEs](#) at system level. In this thesis, the effort is focussed on reliability issues of analogue and mixed-signal circuits, especially with regard to the [NBTI](#).

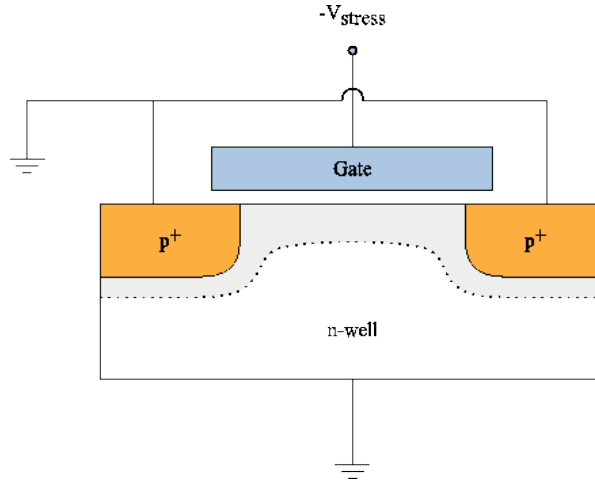


Figure 2.3: The **PMOST NBTI** stress conditions.

2.2 State-of-the-Art in NBTI

Among various reliability effects in nanometer **CMOS** transistors, which have been briefly introduced in Section 2.1, **NBTI** is the most dominating one in our case. **NBTI** occurs predominately in **PMOSTs**, where the source, drain and substrate of the **PMOS** transistor are connected together at a reference voltage. The gate of the **PMOST** is stressed by a negative voltage as compared to the drain, source and substrate. This is where the name “Negative Bias” comes from. Figure 2.3 shows the **NBTI** stress condition in a general form. In the real circuit, the **NBTI** stress can occur at any time under condition the source, drain and substrate of the **PMOST** are biased at power supply V_{dd} and the gate of the **PMOST** biased at any voltage lower than V_{dd} .

The **NBTI** effect increases the absolute threshold-voltage of the **PMOST** and decreases the mobility with time. Both phenomena get worse with increasing stress voltage and temperature. The overall effect is the reduction of drain currents and in return degrading the circuit performance gradually. An example is a reduced circuit-switching speed in digital circuits which can cause circuit failures.

2.2.1 NBTI measurement

Figures 2.4 and 2.5 show our measured **PMOST** threshold-voltage and mobility change over time due to **NBTI**. The stress voltage of V_{GS} is 1.15V and the stress temperature is 127°C. The changes are expressed in terms of a percentage. Due to both threshold-voltage and mobility degradations, the drain current reduces apparently after one week of stress, as shown in Figure 2.6. The drain current of the **PMOST** is measured by stepping the gate voltage in 24 steps and

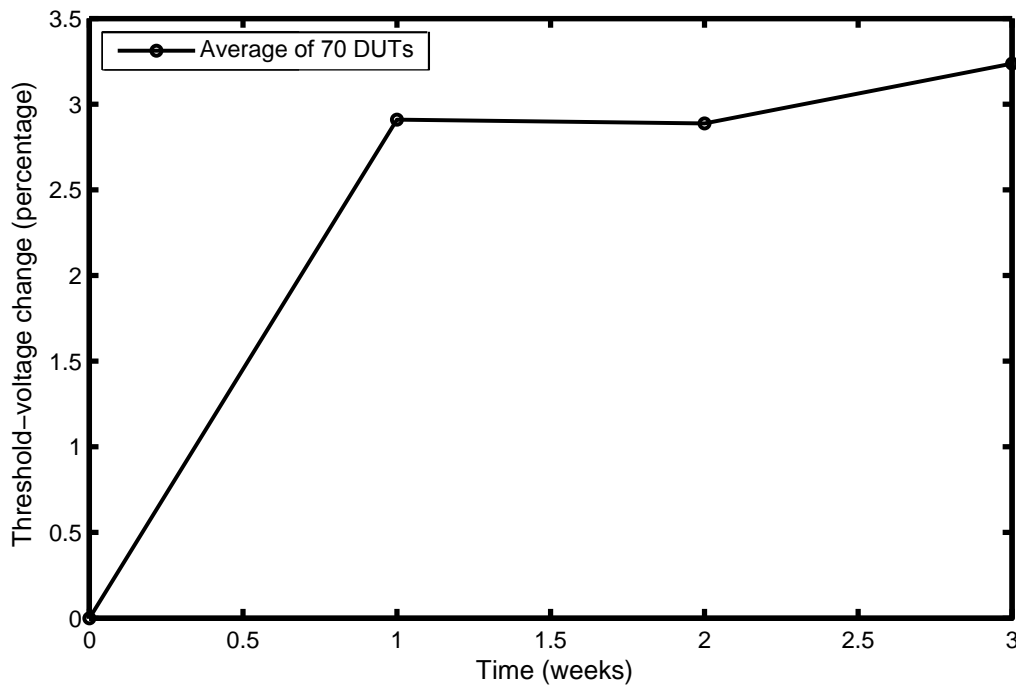


Figure 2.4: The 90nm PMOS transistor threshold increases due to NBTI. Our NBTI measurements have been carried out at $V_{GS} = 1.15V$ and $127^{\circ}C$.

sweeping the drain-to-source voltage. Chapter 3 will provide more detail of the measurement setup and results.

While both the threshold-voltage and mobility can be degraded by NBTI, most publications in NBTI research focus on threshold-voltage degradation exclusively. The reason is that the threshold degradation is the main factor for the drain current reduction and also easier to measure than mobility degradation. The same will hold for this thesis. As shown in Figures 2.4 and 2.5, the mobility change in percentage is also smaller as compared to the threshold-voltage.

As a result, the major degradation due to NBTI is the threshold-voltage increasing over time in PMOSTs under high voltage and high temperature stresses. Moreover, NBTI exhibits a partial recovery effect; it means the degradation in threshold-voltage can be partly recovered after the stress is removed, reduced or even inverted. An example is shown in Figure 2.7. With the stress voltage removed after 10000 seconds, the degraded threshold-voltage can recover more than 40%. It is this recovery effect which makes NBTI to be the most difficult reliability phenomenon for both measurements as well as modelling.

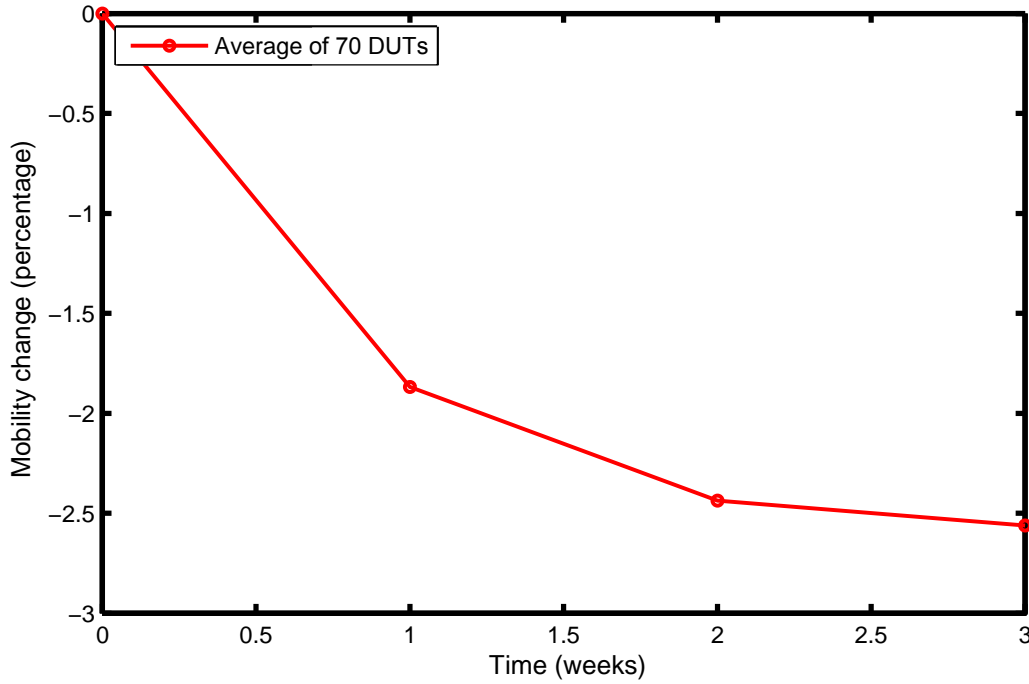


Figure 2.5: The 90nm PMOS transistor mobility decreases due to NBTI. Our NBTI measurements have been carried out at $V_{GS} = 1.15V$ and $127^{\circ}C$.

2.2.2 Physics of NBTI

Although the NBTI effect was first reported in the sixties [Dea67], the exact physical mechanism of NBTI is still not completely clear. It is now well accepted that the overall NBTI degradation is caused by two phenomena: the release/recombination of hydrogen from passivated Si-H dangling bonds (N_{it}) at the gate-silicon-oxide interface and the trapping/de-trapping of holes (N_{ot}) inside the oxide. To make it more clear, Figure 2.8 shows atom constructions at the monocrystalline silicon and the silicon-dioxide interface under the gate. In the figure, the red large circles stand for silicon atoms (Si). The grey small circles are oxygen atoms (O). And the tiny yellow circles represent the hydrogen atoms (H). Under a large negative bias voltage as well as high temperature, the Si-H bonds at the interface are likely to be broken and the released hydrogen ion will diffuse into the gate oxide. The remaining silicon bonds (N_{it}) are dangling as shown in Figure 2.8. In the meantime, there are Si-Si bonds inside the gate oxide which present vacancies for oxygen ions. If holes in the PMOS channel gain sufficient energy to tunnel into the gate-oxide, these oxygen vacancies can trap holes into one side of the Si-Si bond and leave the other side of the Si bond dangling (N_{ot}). The dangling Si bonds from both N_{it} and N_{ot} are responsible for the threshold-voltage shift. As indicated previously, the formation processes of N_{it} and N_{ot} are reversible, which makes the NBTI degradation partly recoverable.

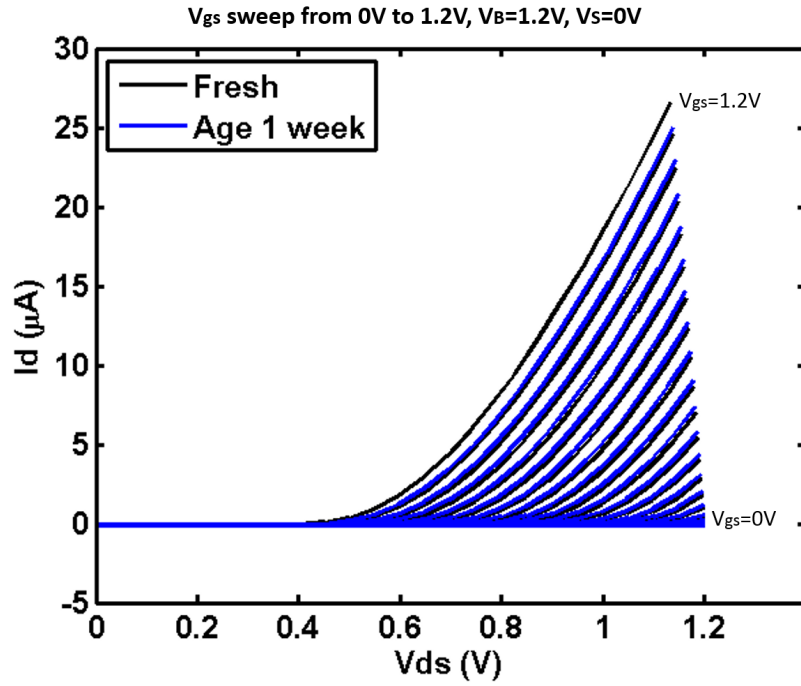


Figure 2.6: The 90nm PMOS transistor drain current decreases due to NBTI. Our NBTI measurements have been carried out at 127°C. The gate source voltage V_{GS} is the parameter.

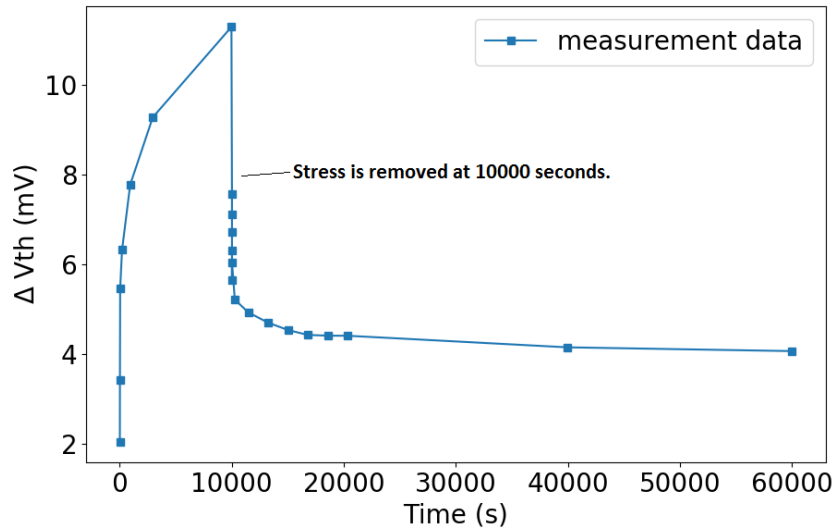


Figure 2.7: The NBTI induced threshold voltage change can recover quite fast after the stress voltage is removed. In the figure, the stress is applied from 0 to 10000 seconds and is removed after 10000 seconds.

Despite the fact that N_{it} and N_{ot} are responsible for NBTI degradation is widely accepted, the modelling of the generation/recombination of N_{it} and N_{ot} is still under debate. Dozens of

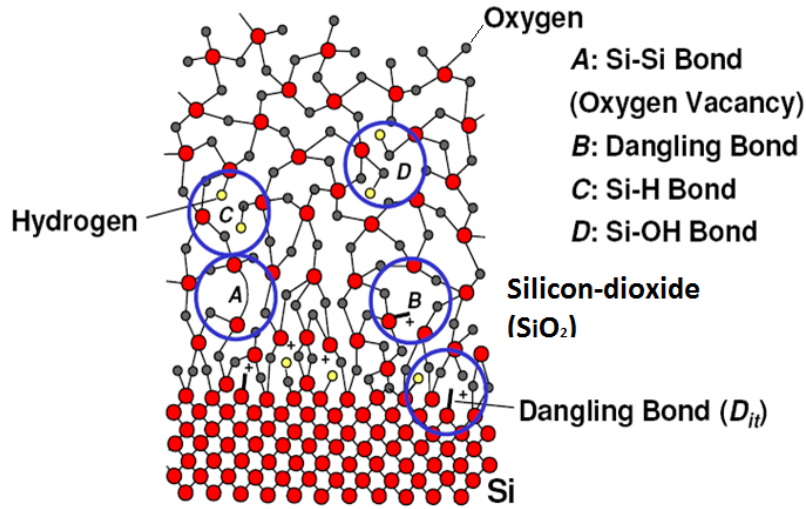


Figure 2.8: The silicon-dioxide interface under the transistor gate [Com09].

NBTI modelling theories have been proposed in literature and tried to explain the mechanisms. Yet none of them have been accepted as the “golden” standard. Among these **NBTI** modelling publications, there are two classes of theories which have emerged as the strongest contenders as compared to the rest in terms of explaining the exact **NBTI** mechanism. They are the **Reaction-Diffusion (RD)** theory and the **Reaction-Limited (RL)** theory.

2.2.3 Reaction-Diffusion Theory

The **RD** theory was first proposed by Jeppson in 1977 [Jep77]. Later on, Alam [Ala05] reviewed many old **NBTI** experiments and proposed new **On-The-Fly (OTF)** measurement techniques which have smaller delays and reduced recovery. It was claimed that the **NBTI** degradation is mainly because of the generation and annealing of interface traps N_{it} , which can be modelled by classical **RD** theory. Based on that explanation, a set of **RD** equations was proposed and it was shown it is possible to model the stress and relaxation of **NBTI** by solving those **RD** equations.

The **RD** theory principle can be explained with the help of Figure 2.9. There are two steps involved during the process of **NBTI**, namely reaction and diffusion. During the reaction phase, some Si-H bonds at the interface are broken under the electrical stress. The generated “Si-” dangling bonds N_{it} remain at the gate silicon-dioxide interface and are responsible for the threshold shift. The H ions will combine into neutral H₂ and diffuse away from the interface into the gate-oxide and eventually into the gate polysilicon. This process is referred to as

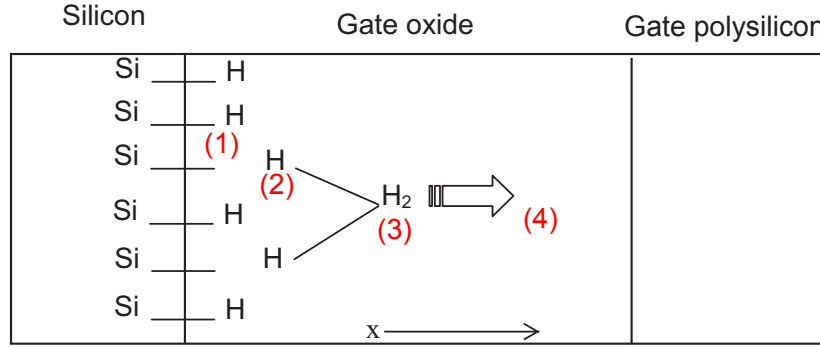


Figure 2.9: The RD theory for NBTI degradation [Ala05]. (1) broken $Si-H$ bond, (2) H ion, (3) recombination to H_2 , (4) diffusion to gate polysilicon.

diffusion. At the moment the stress is removed, the dangling bonds N_{it} can attract H atoms and recombine into Si-H bonds, which is the recovery phenomenon.

In fact, the RD theory is a diffusion-limited theory, being that the reaction is assumed to be much faster than the diffusion and the whole RD process is limited by the neutral H_2 diffusion speed. The RD theory predicts that the long time DC stress degradations are following a power law function $t^{0.16}$ with time t , which has been proven by measurement data. However, the RD theory failed to predict the fast recovery of NBTI. One example has been shown in Figure 2.7. The degradation over 10000 seconds is recovered for about 40% just during the first 10 seconds after removing the stress. In the case of the diffusion-limited nature of the RD theory, it is difficult to explain why 40% of the hydrogen diffuses back to the interface and combines with dangling silicon bonds within this 10 seconds. It would imply that the backward diffusion must be orders of magnitude faster than the forward diffusion, which has not been supported by physical measurements. To overcome this shortcoming, the hole-trapping/de-trapping N_{ot} part is taken into account in the RD framework to explain the fast recovery [Gup12, Mah13]. The RD framework claims NBTI is caused by two uncorrelated contributions. The first contribution is the generation and recovery of interface traps N_{it} , which is modelled by the classic RD theory and response for the long-time degradation. The second contribution is the hole trapping/de-trapping in the gate oxide N_{ot} , which is modelled by a simple empirical formalism [Mah13] which takes care of the response for the short-time fast recovery.

2.2.4 Reaction-limited Theory

The RL is a group of NBTI modelling theories which were proposed by Grassler [Gra07, Gra09b]. The initial model divides NBTI degradation into permanent and recoverable components [Gra07]. Later on, the study was focussed on the detailed behaviour of NBTI recovery and the RD model was improved by addressing the fast-recovery effects. Grassler proposed

that there should be several different traps in terms of their behaviour to attract the diffused H atoms and that these traps can quickly release the H atoms when the stress is removed. In that manner the dangling Si bonds can be combined fast and this explains the fast recovery of NBTI [Gra08a]. The model proposed at that time is also referred to as the “multi-wells” model [Gra08b].

Later it was suggested that NBTI is dominated by two tightly coupled mechanisms, being the interface-state generation N_{it} and hole trapping N_{ot} [Gra09a]. Based on this idea, a “two-stage” model was proposed for NBTI modelling [Gra09b].

Since the reaction processes in his model are much more slower than the diffusion, the NBTI process is dominated by the reaction instead of diffusion. Grassler has classified his models as RL theory [Gra14] to distinguish from RD theories.

The RL theory models the fast recovery very good. However it is more complicated and requires much more model parameters as compared to the RD theory. Sometimes it is even not possible to extract so many parameters based on limited measurement data. Moreover, some scientists claim that the RL theory fails to predict long time DC stress degradation [Mah13].

The research on NBTI is still going on. Now the debate focusses in two parts:

- is the generation of N_{it} and N_{ot} tightly coupled or uncorrelated [Mah13]?
- is the NBTI degradation diffusion limited or reaction limited [Gra14]?

However, any further discussions on the NBTI modelling debate is beyond the goal of this thesis.

2.2.5 NBTI Simulation for Analogue/Mixed-signal Circuits

In order to investigate the reliability of an AMS circuit, the parameter changes of each transistor inside the circuit need to be calculated. This kind of calculation is here referred to as reliability simulation and accurate reliability models are essential. However, one of the key problems for AMS reliability simulation is the lack of accurate reliability models. This is especially true for the NBTI.

Currently there are several NBTI simulation tools used in industry. The most famous one is Cadence RelXpert [Cad11]. It is acquired software which was originally developed by UC Berkeley as Berkeley Reliability Tools (BERT) [Tu93]. The author of BERT is Chenming Hu who is also the leading author of the industry standard compact model for CMOS technologies – the BSIM model. In the beginning, BERT only modelled the HCI effect. After it became RelXpert, Cadence extended it with a similar function to model NBTI as well. RelXpert uses

the simple power-law model to predict **NBTI** degradation. The power-law **NBTI** model is based on fitting the DC stress measurements in the logarithmic time domain and extracting the time-power function ($A \cdot t^n$). The power-law model is not based on any physical meanings but is simply an extraction from measurements and easy to implement in simulation software. In fact, many commercial EDA companies like Synopsys (MOSRA) and Mentor Graphics (Eldo), as well as silicon foundries, such as IBM and TSMC, provide **NBTI** simulation by means of power-law models. However, in theory the power-law model can only handle DC stresses because it cannot model the recovering phenomenon of **NBTI**. More detailed information on RelXpert usage and its AgeMOS model formulas are described in Appendix A.

Verilog-A can also be used as an **NBTI** simulation tool, in which one can construct a dedicated **NBTI** model and subsequently simulate it in Cadence Spectre. NXP Semiconductors uses this kind of method to implement **NBTI** simulation in their PRESTO simulation tools [Kol07]. The advantage of this method is its flexibility. It can adopt almost all kind of **NBTI** models in case one has used Verilog-A. However, despite much effort spent in **NBTI** modelling theories, there is still a big gap between modelling and implementation in SPICE-like environments which are familiar to **AMS** circuit designers. In addition, **NBTI** modelling publications mainly focus on DC stresses and square-wave stresses termed AC stress or dynamic **NBTI** in some publications, which are not typical cases in **AMS** circuits. Currently, many simulation tools apply a simplification by using the *average stress* instead of the real stress to evaluate the **NBTI** degradation. This approach dramatically underestimates the **NBTI** degradation and causes a large error in long-time extrapolation [Mar11].

Another limitation for all reliability simulations including **NBTI**, is the lack of model parameters. Silicon foundries like TSMC, GLOBALFOUNDRIES, IBM and UMC are not willing to share their reliability measurement data and treat this information as a trade secret. Almost all publications on **NBTI** mask their measurements data in arbitrary units (A.U.), which make it nearly impossible to extract **NBTI** parameters from papers.

To solve the above problems, Chapter 3 will explain our **NBTI** modelling, **NBTI** measurements, parameters extraction and **NBTI** simulation for **AMS** circuits in detail.

2.3 Improving the AFE Dependability

This thesis is partly resulting from the large European projects CATRENE **TOETS** [Cat09] and ENIAC **ELESIS** [Eni12]. They were both focussed on improving the dependability of analogue and mixed signal **IPs** in **AFEs** of **SoCs**. In order to carry out our dependability study

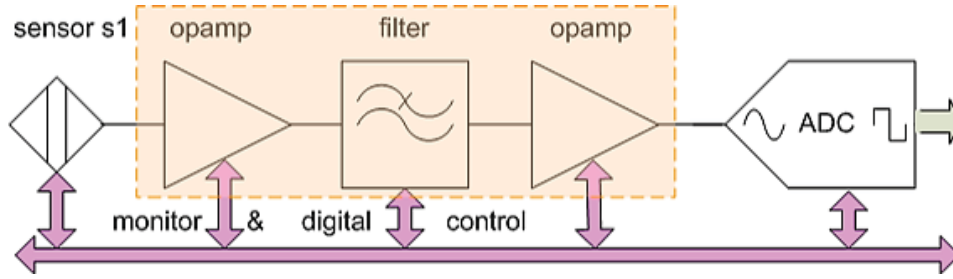


Figure 2.10: Generic setup of a sensor and a programmable AFE [Ker10a]

on analogue/mixed-signal circuits, a target AFE had to be designed as a test vehicle. The major reliability issue, being NBTI, will be simulated using this test vehicle in the thesis and the performance degradation will be determined. After investigating the reliability behaviour, maintainability and availability can be incorporated into solutions which are aimed to improve the dependability of AFEs [Kha14].

2.3.1 The Targeted AFE

The target AFE that has been chosen is a sensor-readout circuit for automotive applications, which is shown in Figure 2.10. The sensor in Figure 2.10 could be a temperature sensor, pressure sensor or magnetic sensor. The AFE following that sensor could be composed of digitally programmable OpAmps, active-filters and ADCs.

To accomplish a dependable AFE, the life time of each IP in the AFE has to be studied and the most sensitive performance parameters for each IP with regard to the reliability have to be quantified by means of NBTI simulations. After determination of the NBTI sensitive parameters, the maintenance strategy will be chosen to reach a high dependability.

2.3.2 Different Approaches to Improve Circuit/IP Dependability

There are two basic approaches for improving the dependability of AMS circuits:

- Design approach — completely change the IP design and make a very robust design of an IP (basically everything in the IP) to make it dependable.
- Embedded Instrument (EI) approach — leave the current IP design untouched but monitor the ageing sensitive parameters in the IP from I/O or an accessible internal node. Control from outside the IP via e.g. embedded programming.

The first approach, the design approach, is by intensive ageing simulation or reliability test to improve the design and achieve a very robust IP. It basically means a complete redesign of the current available IP library and update it to highly dependable IPs. The time and effort costs will be significant and sometimes not affordable for a company which already has a large number of AMS IPs in their design library. In Chapter 4 to Chapter 6, we will discuss this approach.

Figure 2.10 shows the second approach, which is based on monitoring and digital control. A dedicated monitor is build in each IP for detecting the sensitive performance parameter drift with time. After a predetermined amount of drift is detected, the monitor will send an alarm signal and trigger the maintenance operation, which is basically tuning the drifted parameter back to its original value by digital programming and digital control.

Later on, this approach developed to be the EI approach which is to embed some form of test and measurement infrastructure into the silicon to characterize, debug and test the IP. The concept of the EI is different from BIST and other kind of monitors. This is due to the fact that an EI can provide the user with rich and detailed information with respect to the performance of the target IP, not just a *true/false* indication. With accurate information of performance shift, the maintenance no longer needs to be carried out in the analogue domain but can be compensated in the digital domain after the ADC. For example, if the offset shift due to NBTI in an OpAmp is measured by the EI to be 10mV, the acquired ADC data can be modified by adding or subtracting 10mV using digital processing.

The EI approach simplifies the maintenance procedure and makes it even possible to be actuated with software updates. The EI can also be generalized to adapt all kinds of, for example, OpAmp IPs and shared by several IPs. Hence the design effort overheads as well as power and area overheads will be reduced considerably as compared to an approach which makes each IP block dependable by design. The EI approach will be treated in Chapter 4 to 6 also.

2.4 Conclusions

In safety-critical applications, such as automotive, the term dependability is used more frequently than reliability. To improve dependability and its major attribute reliability, it is required to find the dominate ageing effect, which is NBTI in our case. It determines the lifetime of MOSTs in nanometer CMOS technologies. Unfortunately, until now there are still no NBTI models which can perfectly model NBTI degradation under all circumstances. The simulation of NBTI is also not matured. Cadence Relxpert is widely adopted for NBTI simulations, but

it is limited to DC stress conditions. For dynamic stress conditions, customized Verilog-A models are quite often used in industry. In Chapter 3, we will come up with a new model and simulation solution for NBTI for AMS IPs. A targeted AFE is being designed for evaluation. Two different approaches to improve dependability are proposed such as extra design effort and the development of EIs. In Chapter 4 to Chapter 6 their designs and performances will be compared.

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Chapter 3

NBTI Modelling, Measurement and Simulation

Abstract-

In this chapter, [Negative Bias Temperature Instability](#) modelling, measurement, validation and simulation will be discussed. Two original works will be described, which are all dealing with models.

The first one is the [Negative Bias Temperature Instability](#) compact model which is used to simulate [Negative Bias Temperature Instability](#) degradation of [Analogue/Mixed-Signal](#) circuits. The model is based on iteratively solving the [Reaction-Diffusion](#) equations. This model can handle arbitrary stress waveforms and is thus very suitable for analog/mixed-signal ageing simulations. It has been evaluated for [CMOS](#) 140nm technology with square-wave stresses as well as arbitrary wave stresses. The [Negative Bias Temperature Instability](#) model and associated simulation method which are presented in this chapter will be used as a fundamental tool in the remaining chapters to examine the reliability of different [Analogue/Mixed-Signal](#) functional blocks, like [Analogue-to-Digital Converters](#).

The second one is a new closed-form model for the [Metal-Oxide-Semiconductor Field-Effect Transistor](#) drain current. It is provided to facilitate [Metal-Oxide-Semiconductor Field-Effect Transistor](#) threshold-voltage measurements in nanometer [CMOS](#) technologies. The model is valid for all regimes, like the sub-threshold/weak-inversion, moderate-inversion, strong-inversion and the linear regime. The drain current model will be used to build an on-chip V_{th0} measurement [Embedded Instrument](#) and gather a large amount of [Negative Bias Temperature Instability](#) degradation data in a more convenient way as well as to reduce cost.

Parts of this chapter are based on publications of the author: [Wan13], [Wan15a], [Wan15b] and [Wan16].

3.1 Introduction

Modern CMOS technology has entered the nanometer region. In addition to area reduction, speed improvement and power saving, nanometer CMOS unfortunately suffers from several reliability problems, like Negative Bias Temperature Instability, Hot-Carrier Injection, Electro Migration and Time-Dependent Dielectric Breakdown. Research on the exact physical mechanisms of different reliability phenomena has been carried out for more than half a century. In Chapter 2, this research has been summarized and it was shown that Negative Bias Temperature Instability is the most dominant reliability mechanism as well as the most complicated and debatable one.

As a result, this chapter will focus exclusively on Negative Bias Temperature Instability in terms of compact modelling, measurement, validation and simulation.

In highly dependable application areas such as the automotive industry [Ker10], reliability problems need to be considered during the circuit design phase. Accurate ageing simulations are in high demand to assure design success. One of the key problems for AMS ageing simulation is the lack of accurate ageing models. This is especially true for the NBTI, which is probably the most critical ageing mechanism to affect nanometer CMOS technologies during our research.

The dominant degradation due to NBTI is the threshold shift over time in PMOS transistors under high voltage and high temperature stress. Moreover, NBTI degradation can partly recover after the source of the stress is removed, which makes both measurement and modelling very difficult. In fact, it remains difficult until now to accurately measure the NBTI effects [Gra08]. The present measurement limitations prevent insight into the physical cause of NBTI, and hence the modelling theories for NBTI degradation are still under debate [Mah11, Gra09a].

Despite much effort spent in NBTI modelling theories, there is a big gap between modelling and simulation implemented in SPICE-like environments which are familiar to AMS circuit designers. In addition, NBTI modelling publications mainly focus on DC stresses and square-wave stresses termed AC stress or dynamic NBTI in some publications, which are not typical cases in AMS circuits. Currently, many simulation tools apply a simplification by using the *average stress* instead of the real stress to evaluate the NBTI degradation. This approach dramatically underestimates the NBTI degradation and causes a large error in long-time extrapolation [Mar11].

In order to apply NBTI aging simulation to AMS circuits, the NBTI model must:

1. Handle arbitrary stress conditions, such as arbitrary voltage stress waveforms and arbitrary temperature stress waveforms.

2. Be easily implemented in [SPICE](#)-like environments and to embed in existing design flows.
3. Take into account the stochastic effect of ageing and enable the combination of process-variation simulations.
4. Run simulations that are not time-consuming, even for large circuits.

Instead of proposing new [NBTI](#) theories, this chapter tries to reduce the gap between [NBTI](#) theories and [NBTI](#) simulations in [SPICE](#)-like environments. A new compact [NBTI](#) model will be introduced in Section 3.2 which satisfies the above four requirements and is suitable for [AMS NBTI](#) simulations in the Cadence [Analogue Design Environment](#) ([ADE](#)). The new model is based on completely solving the [RD](#) equations [[Ala05](#)] in a smart way, such that it can achieve high accuracy with reduced computational effort.

The proposed [NBTI](#) model in section 3.2 will be validated by [NBTI](#) measurement results. Different from other publications, this chapter fits model simulations with measurements on the up-limit envelope, which will be explained in Section 3.3.2, instead of comparing them with the whole stress-relax cycle. This is because the up-limit envelope of the [NBTI](#) degradation on a large number of stress cycles is the most interesting part in [AMS](#) applications. It can help to determine the design margin. At the same time, by ignoring the exact matching of [NBTI](#) relaxation behaviour it will help to avoid limitations of the [RD](#) model. It will show the strong benefit of the [RD](#) model which needs very few model parameters in modelling arbitrary waveform stresses. The simulations have been validated in [CMOS](#) 140nm technology by Fast-Id measurements for arbitrary voltage stress waveforms. The detailed validation will be provided in section 3.3.

The transistor-level [NBTI](#) simulation in Cadence can be carried out in different ways. Both Cadence RelXpert and Verilog-A based scripts can be employed to simulate [NBTI](#) degradation. However, they all need a transistor-level netlist to carry out transient simulations as a reference. In section 3.4, [NBTI](#) simulations by RelXpert and Verilog-A will be introduced as well as their strengths and weaknesses.

[NBTI](#) measurements are carried out by extracting threshold-voltages of [PMOS](#) transistors. Currently there are several methods to extract threshold-voltages such as [Measurement-Stress-Measurement](#) ([MSM](#)) methods, [On-The-Fly](#) ([OTF](#)) method, Fast-Id/Fast-Vt method and so on, which will be discussed in section 3.5. These methods rely on accurate [MOST](#) transistor drain-current models, and special equipment together with automatic control software. In order

to accelerate degradation and reduce the stress time, a temperature-controlled oven is often used to heat up DUTs at a high temperature like 125°C. If the test is carried out on wafer, a special wafer-probe station is required. In short, NBTI measurements are difficult, expensive and time consuming. In section 3.5, a new MOST transistor drain-current model will be proposed to simplify the NBTI measurements. Based on the proposed MOST transistor model, an EI is designed to extract threshold-voltages on-chip and can thus be used as a low cost NBTI measurement solution as well as an NBTI on-chip monitor for the whole SoC.

The conclusions of this chapter are drawn in section 3.6.

3.2 NBTI Modelling

In Chapter 2, the CMOS ageing mechanisms including existing NBTI modelling and their debates have been discussed in detail. In this section, a newly developed compact NBTI model based on the RD theory will be discussed.

3.2.1 A new compact NBTI model

The proposed new compact NBTI model for AMS ageing simulations is based on the RD theory. The reason is that the AMS circuits are operating under moderately stressed condition and suffer less hole trapping/de-trapping problems as compared to heavily-stressed digital circuits. In addition, for studying the life-time of the circuits, it is more interesting to investigate the long-time degradation instead of instant recovery behaviour. What is more, the RD model is more convenient to handle arbitrary waveform stresses because, in theory, it has no limitation for stress types and requires far fewer model parameters [Wan13] than other models [Wan07, Mar11].

The classic RD equations will be reviewed first. Unlike in other publications, the new compact model is based on iteratively solving the RD equations in a simple way, and will be introduced in the second part of this section.

According to the RD theory, the NBTI degradation can be explained as the generation of dangling bonds in the region close to the Si/SiO₂ interface [Ala05]. There are two steps involved during the process of NBTI, being reaction and diffusion.

During the reaction phase, some Si-H bonds at the Si/SiO₂ interface break under the electrical stress. The generated “Si-” dangling bonds remain at the interface and are responsible for the threshold shift. The H atoms will combine into neutral H₂ and diffuse away from the Si/SiO₂ interface into the gate-oxide and eventually into the gate poly-silicon. This process is referred to as diffusion.

The classic RD equations are expressed in Eq.(3.1) - Eq.(3.3) from [Ala07], where N_{IT} is the number of interface traps at any given instant and N_0 is the initial number of unbroken Si-H bonds.

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H(0, t) N_{IT} \quad (3.1)$$

$$N_{H_2} = k_H N_H^2 \quad (3.2)$$

$$\frac{dN_{H_2}}{dt} = D_{H_2} \frac{d^2 N_{H_2}}{dx^2} \quad (3.3)$$

$N_H(0, t)$ denotes the concentration of hydrogen atoms at the Si/SiO₂ interface at any given instant, k_F is the oxide-field dependent forward dissociation rate, and k_R is the backward combination rate [Ala05]. Equation (3.1) describes the generation rate of interface traps, which is the same as the generation rate of hydrogen atoms. In Eq.(3.2) and Eq.(3.3), N_{H_2} is the concentration of the neutral H₂, k_H is the combination rate of H atoms, D_{H_2} is the H₂ diffusion coefficient, and x is the location perpendicular to the silicon-oxide interface.

The reaction-diffusion equations (3.1) upto (3.3) describe the process of NBTI and could be used to obtain ageing degradations, for example in terms of the threshold-voltage shift. However, they are difficult to solve in a general form. In order to find a solution which is suitable for analogue applications, one needs to simplify the conditions and make some assumptions as discussed below. Based on the research in [Wan07], the trap generation is slow from the initial period of the stress till the end of the product life and the broken Si-H bonds during NBTI are just a very small part of the total Si-H bonds. Hence $dN_{IT}/dt \approx 0$ and $N_{IT} \ll N_0$. Under these realistic assumptions, Eq.(3.1) and Eq.(3.2) can be combined and approximated to:

$$\sqrt{N_{H_2}(0, t)} \cdot N_{IT} \approx \frac{\sqrt{k_H} \cdot k_F}{k_R} N_0 \quad (3.4)$$

The number of interface traps N_{IT} is equal to the total number of H atoms diffused from the Si/SiO₂ interface ($x = 0$) [Ala05]. As a result, the relationship between N_{IT} and N_{H_2} can be expressed as:

$$N_{IT} = 2 \int_0^\infty N_{H_2}(x, t) dx \quad (3.5)$$

In fact, most RD theory-based NBTI models use Eq.(3.3) - Eq.(3.5) to obtain the threshold shift. The difference is that different authors use different approaches to approximate the solution under DC or square-wave stress cases [Jep77, Wan07], or employ complicated solvers to solve the equations in a time-consuming way to accurately evaluate the RD theory [Mah11, Ala05].

Unlike in other papers, we will iteratively solve the equation set Eq.(3.3) - Eq.(3.5) in a simple, fast way. Since in nanometer CMOS technologies, the gate oxide is far thinner than the gate poly-silicon, and the H_2 diffusion is much faster in the gate oxide [Wan07], the number of H_2 in the gate dioxide can be ignored while calculating long stress-time situations. The diffusion coefficient D_{H_2} in the poly-silicon is treated as a constant. Applying the Laplace transform for Eq.(3.3) to solve the differential equation, the solution for N_{H_2} in the Laplace transform [Opp96] can be derived as:

$$\begin{aligned}\mathcal{L}\{N_{H_2}(x,t)\} &= \widetilde{N_{H_2}}(x,s) \\ &= \widetilde{N_{H_2}}(0,s) \cdot \exp\left[-\left(\frac{s}{D_{H_2}}\right)^{\frac{1}{2}} \cdot x\right]\end{aligned}\quad (3.6)$$

In Eq.(3.6), the symbol $\mathcal{L}\{\cdot\}$ and the superscript \sim are referred to as the Laplace transform of corresponding functions. By substitution of Eq.(3.6) into Eq.(3.5), the solution for N_{IT} in the s -domain can be expressed as:

$$\begin{aligned}\widetilde{N_{IT}}(s) &= 2 \cdot \int_0^\infty \widetilde{N_{H_2}}(x,s) dx \\ &= 2 \cdot \widetilde{N_{H_2}}(0,s) \cdot \left(\frac{D_{H_2}}{s}\right)^{\frac{1}{2}}\end{aligned}\quad (3.7)$$

Using Eq.(3.4) and Eq.(3.7) to eliminate N_{H_2} and applying the inverse Laplace transform, one obtains the time-domain equation. The final result can be simplified to an equation with only physical parameters:

$$\mathcal{L}^{-1}\left\{\sqrt{s} \cdot \widetilde{N_{IT}}(s)\right\} \cdot N_{IT}^2(t) = 2\sqrt{D_{H_2}} \left(\frac{\sqrt{k_H} \cdot k_F(t)}{k_R} N_0\right)^2 \quad (3.8)$$

In Eq.(3.8), the symbol $\mathcal{L}^{-1}\{\cdot\}$ denotes the inverse Laplace transform. It can alternatively be written as a convolution form in the time domain:

$$\begin{aligned}\left(\frac{1}{\sqrt{t}} * \frac{dN_{IT}(t)}{dt}\right) \cdot N_{IT}^2(t) &= 2\sqrt{\pi D_{H_2}} \left(\frac{\sqrt{k_H} \cdot k_F(t)}{k_R} N_0\right)^2 \\ &= M(t)\end{aligned}\quad (3.9)$$

The symbol “*” inside the brackets at the left side of Eq.(3.9) represents the convolution operator. At the right side, k_F is proportional to the inversion-hole density, the vertical electrical field and temperature. Parameters k_H , k_R and D_{H_2} are proportional to the temperature only, as

will be shown in Eq.(3.10); E_R and E_D are constant parameters. As a result, the right side of Eq.(3.9) is a function of stress voltage, temperature, oxide thickness and unit gate capacitance. Basically, they are a function of time and can be defined as $M(t)$.

$$\begin{cases} k_F(t) \propto \sqrt{C_{ox}(V_{gs}(t) - V_{th0})} \cdot \exp\left(\frac{E_{ox}}{E_0}\right) \\ k_R \propto \exp\left(-\frac{E_R}{kT}\right) \\ D_{H_2} \propto \exp\left(-\frac{E_D}{kT}\right) \end{cases} \quad (3.10)$$

If the stress voltage and the temperature remain constant with regard to time, e.g. DC stress, $M(t)$ will be a constant and can be written as M . In this situation, Eq.(3.9) will degrade to the well-known closed-form solution for the number of interface traps N_{IT} [Ala05]:

$$N_{IT}(t) = R \cdot t^{\frac{1}{6}} \quad (3.11)$$

In Eq.(3.11), R is a constant and can be expressed as:

$$\begin{aligned} R &= \left[\frac{M}{(\sqrt{\pi})^3} \cdot 3 \cdot \Gamma\left(\frac{2}{3}\right) \cdot \Gamma\left(\frac{5}{6}\right) \right]^{\frac{1}{3}} \\ &= 0.94 \cdot M^{\frac{1}{3}} \end{aligned} \quad (3.12)$$

where the $\Gamma(x)$ is called *gamma* function which has been employed in mathematics books like [Abr64]. The *gamma* function can be expressed as Eq.(3.13).

$$\Gamma(x) = \int_0^{\infty} s^{x-1} e^{-s} ds \quad (3.13)$$

Table 3.1: The new compact NBTI model with *Non-Uniform* Time Step Δt_n [Wan16].

$N_{IT}(n) = \begin{cases} 0, & n = 0 \\ \left(M(1) \sqrt{\Delta t_1} \right)^{\frac{1}{3}}, & n = 1 \\ -\frac{b}{3} + \left[-\frac{b^3}{27} - \frac{d}{2} + \sqrt{\left(\frac{b^3}{27} + \frac{d}{2} \right)^2 - \frac{b^6}{729}} \right]^{\frac{1}{3}} + \left[\frac{b^3}{27} - \frac{d}{2} - \sqrt{\left(\frac{b^3}{27} + \frac{d}{2} \right)^2 - \frac{b^6}{729}} \right]^{\frac{1}{3}}, & n > 1 \end{cases}$	$M(n) = A^2 C_{ox} V_{gs}(n) \exp \left(-\frac{E_a}{2kT(n)} \right) \exp \left(\frac{2E_{ox}}{E_0} \right)$	
	$b = \sum_{i=1}^{n-1} N_{IT}(i) \sqrt{\Delta t_n} \left(\frac{1}{\sqrt{\sum_{x=i}^n \Delta t_x}} - \frac{1}{\sqrt{\sum_{x=i+1}^n \Delta t_x}} \right)$	$d = -M(n) \sqrt{\Delta t_n}$
	$E_{ox} = \frac{V_{gs}(n)}{t_{ox}}$	$\Delta V_{th}(n) = \frac{q \cdot t_{ox}}{\epsilon_{ox}} \cdot N_{IT}(n)$

However, if the stress condition changes over time, it will be difficult to derive a closed-form solution. An alternative way is to modify Eq.(3.9) into a discrete form and find an iterative solution. Moreover, in order to implement the model in Cadence ADE, the compact model needs to effectively handle the Spectre transient simulation results, which adopt non-uniform time steps [Kuf10]. Suppose the timing points are separated non-uniformly by Δt_n seconds. Here, Δt_n is the specified time step between time point t_n and time point t_{n-1} . The digitization in time of Eq.(3.9) can then be written as:

$$\left(\sum_{i=0}^{n-1} \frac{N_{IT}(i+1) - N_{IT}(i)}{\sqrt{t_n - t_i}} \right) \cdot N_{IT}^2(n) = M(n) \quad (3.14)$$

In Eq.(3.14), parameter n is the discrete time index. Rearranging Eq.(3.14) and using the solution of the so-called Cubic equation [Gui30], the iterative solution for N_{IT} can be expressed as in Table 3.1. The parameters b and d in N_{IT} are also given in Table 3.1. The parameter $M(n)$ in Table 3.1 is a function of time, stress voltage, temperature and other relevant process parameters.

The parameters of the equations in Table 3.1 are explained as follows. C_{ox} is the gate capacitance per unit area. Parameter $V_{gs}(n)$ is the stress voltage applied between gate and source, which may change with discrete time index n . The Equivalent Oxide Thickness (EOT) of the gate oxide is denoted as t_{ox} . Constant k is the Boltzmann constant and $T(n)$ is the temperature in degrees Kelvin over the discrete time index n . Parameters A , E_0 and activation energy E_a are model-fitting parameters which need to be extracted from NBTI degradation measurements. The actual threshold shift as function of time due to NBTI can be derived from $N_{IT}(n)$, as shown in Table 3.1. In this formula, q is the charge of a single electron and ϵ_{ox} is the dielectric permittivity of the gate oxide.

Compared to other compact NBTI models, our compact model requires three fitting parameters, A , E_0 and E_a in Table 3.1, which can be extracted from NBTI measurements. This is much less than the seven parameters in [Wan07] and the ten parameters required in [Mar11].

3.3 NBTI Model Validation

Since our new compact model is actually a discrete-form solution of the original RD equations, it makes sense to compare the model results with the reaction-diffusion theoretical results first. Moreover, there are also other compact models based on the RD theory. It is also useful to compare of the results of this model with those from the other RD models described in publications.

The weakness of the RD theory has been argued intensively in recent years, such as the failure to predict the steep recovery of the NBTI degradation and less flexibility in adjusting the time-power parameter. In this section, one solution which is referred to as “fitting the up-limit envelope only” is proposed to improve the model fitness and to avoid the above weaknesses in the RD model.

This model will then be compared with the Fast-Id method threshold-voltage measurement results under arbitrary voltage stresses. Several threshold voltage measurement techniques including the Fast-Id method will be introduced in Section 3.5.

3.3.1 Validation of Our NBTI Model with the Original RD Theory

It is difficult to achieve a closed-form solution for the RD equations except under DC stress, what has been shown in Eq.(3.11) and Eq.(3.12). Our new model was implemented in Matlab and compared with the accurate closed-form solution under the same DC stress. The resulting threshold shifts have been compared as shown in Figure 3.1. The relative errors in percentage are shown in Figure 3.2. The timing points are separated by one second in both figures. Figure 3.2 shows that the maximum error is about 6.7% at the initial timing point. With the number of timing points increasing, the error reduces dramatically and eventually converges to zero. In real applications, this error can be reduced by calibration during the parameter extraction phase, because it can be included in parameter A . Therefore the error introduced by time digitization can be neglected in a practical case.

Figure 3.3 shows the comparison between our model and one of the other RD theory-based models in [Wan07] under the same square-waveform stress. Both models use the same parameter settings and the results match well. From Figure 3.3, the bottom envelopes of the two models are better matched than the top envelope. The reason is the model in [Wan07] uses a simplified approximation while in our model, we did not use a simplified equation and therefore it is much more accurate. Moreover, the model in [Wan07] can only work for square-wave stress and obtain two result points for each stress cycle. Our model can handle arbitrary waveforms and obtain as many results points as required.

3.3.2 Fitting the Up-limit Envelope Only

One of the major weaknesses of the RD model is the slow relaxation [Gra09b, Vel12, Kuf10]. The RD model cannot correctly reflect the actual relaxation part of the NBTI degradation. The relaxation prediction by the RD model is much slower than the measurement results show. The simulated NBTI amplitude is often much smaller than the measured NBTI amplitude. Moreover, there are no model parameters in the RD model to control the relaxation. Therefore,

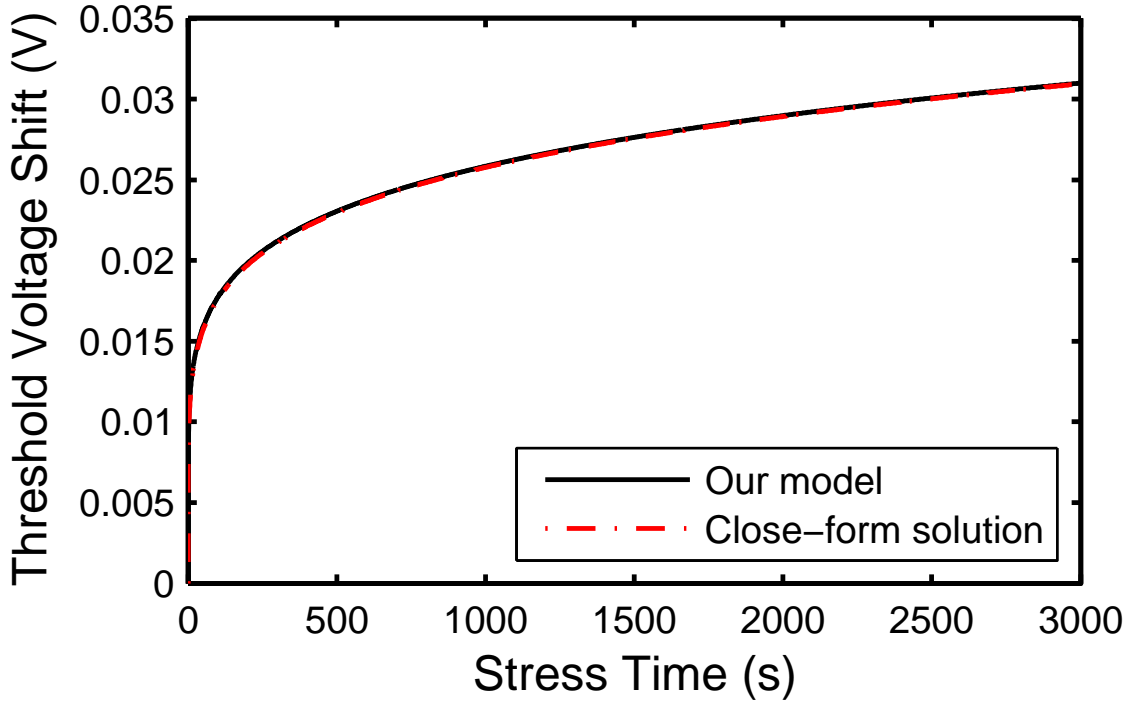


Figure 3.1: Comparison of our model with the closed-form solution of RD equations (DC voltage stressed situation) [Wan16].

in theory, the RD model cannot be improved by tuning the model parameters. To avoid such a problem, this section only fits the RD model simulation result with the *up-limit envelope* of the measurement result.

The meaning of up-limit envelope can be explained with Figure 3.3. The threshold voltage shifts in every stress cycle and one can obtain a maximum value (normally at the end of stress) and a minimum value (normally at the end of relaxation). By drawing a line across every maximum value in each stress cycle, one can obtain the up-limit envelope.

Since the up-limit envelope of the aging is often more interesting than the detailed stress-release degradation in each period, it is often used to determine the design margin. If the RD model, as a mathematical tool, can fit the up-limit envelop well, then it will still be useful for NBTI prediction even though the physical explanation for the NBTI mechanism remains imperfect.

To evaluate the performance of our model, a large number of NBTI degradation measurements have been carried out for single PMOS transistors in 140nm CMOS technology. The detailed information about the measurement set-up, uncertainties, model parameter extraction and silicon measurement results will be discussed in the following subsections.

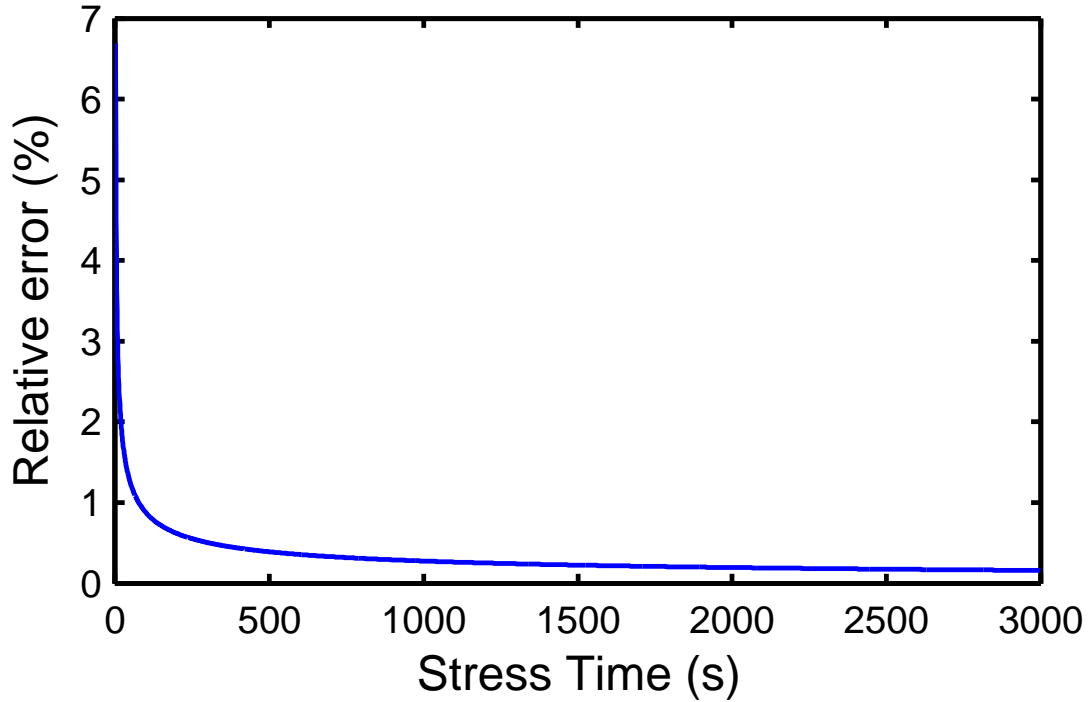


Figure 3.2: Relative error of our model in Figure 3.1 (DC voltage-stressed situation).

3.3.3 Measurement Set-up

NBTI measurements have been carried out on PMOS transistors in a 140nm CMOS technology. The equipment used are the Probe station Summit 12000-Series/Titan Series Temptronic, the HP 4155B Semiconductor Parameter Analyzer, and LabVIEW software (Figure 3.4).

The NBTI degradation is measured using the “Fast-Id” method, which is proposed as a new standard in the JEDEC 14.2 (wafer-level reliability group) proposal [JED04]. This method interrupts stress (typically within 1 ms) and subsequently performs a very fast measurement of the drain current at a gate voltage near the threshold-voltage (the sub-threshold region and partially inverted region). Same drain current has been determined from a similar measurement taken before the stress tests. A small drain-source voltage (0.05V) is continuously applied to simplify the fast switching. The PMOST is in an almost symmetric NBTI configuration. Since the transistor under test is operating far from the maximum of its transconductance, where the transistor is more sensitive to mobility degradation like the OTF method, only the threshold-voltage shift related to the flat-band shift is monitored. This procedure is based on the fact that the sub-threshold slope remains constant after stress. The Fast-Id method is suitable for implementation by a conventional parameter analyzer.

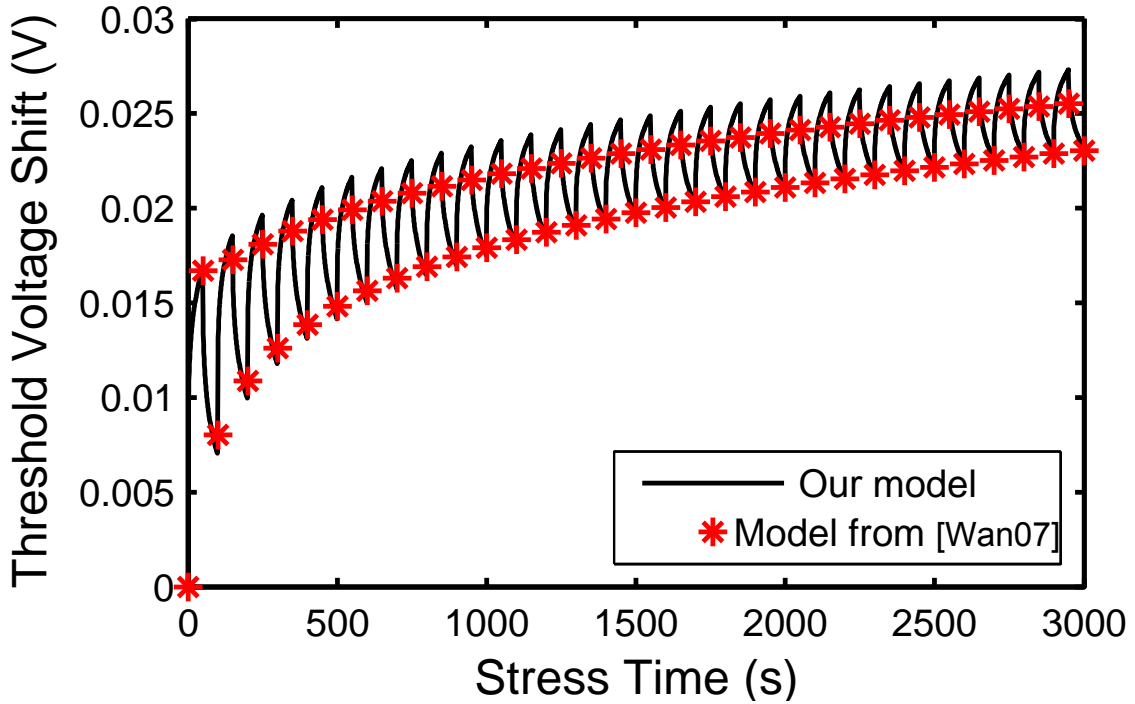


Figure 3.3: Comparison of our model with the RD theory based model in [Wan07] for square-wave voltage stress.

3.3.4 Unavoidable Uncertainties

To reduce undesirable uncertainty, ideally the NBTI degradation can be optionally measured using the same PMOS transistor under various stress conditions. However, this is not possible in real measurements because it is difficult for the PMOS transistor to fully recover from NBTI degradation. Therefore in each measurement, a new PMOS transistor is used. As a result, unavoidable uncertainties from both process variations as well as NBTI degradation variations are introduced into the measurement results.

In addition, although each individual measurement is accurate and trustable, the LabVIEW software-controlled automatic measurement set-up is difficult to repeat for exactly the same stress condition. Since Microsoft Windows cannot produce accurate timing at the millisecond level, the LabVIEW software which is running on it cannot provide accurately repeatable control for NBTI measurements. It is therefore difficult to characterize the stochastic effects of the NBTI degradation by repeating the same stress many times under the current test set-up.

To evaluate the model under the previous stochastic measurement conditions, the stochastic effects of NBTI degradation was taken into account. In this thesis the 3σ method has been

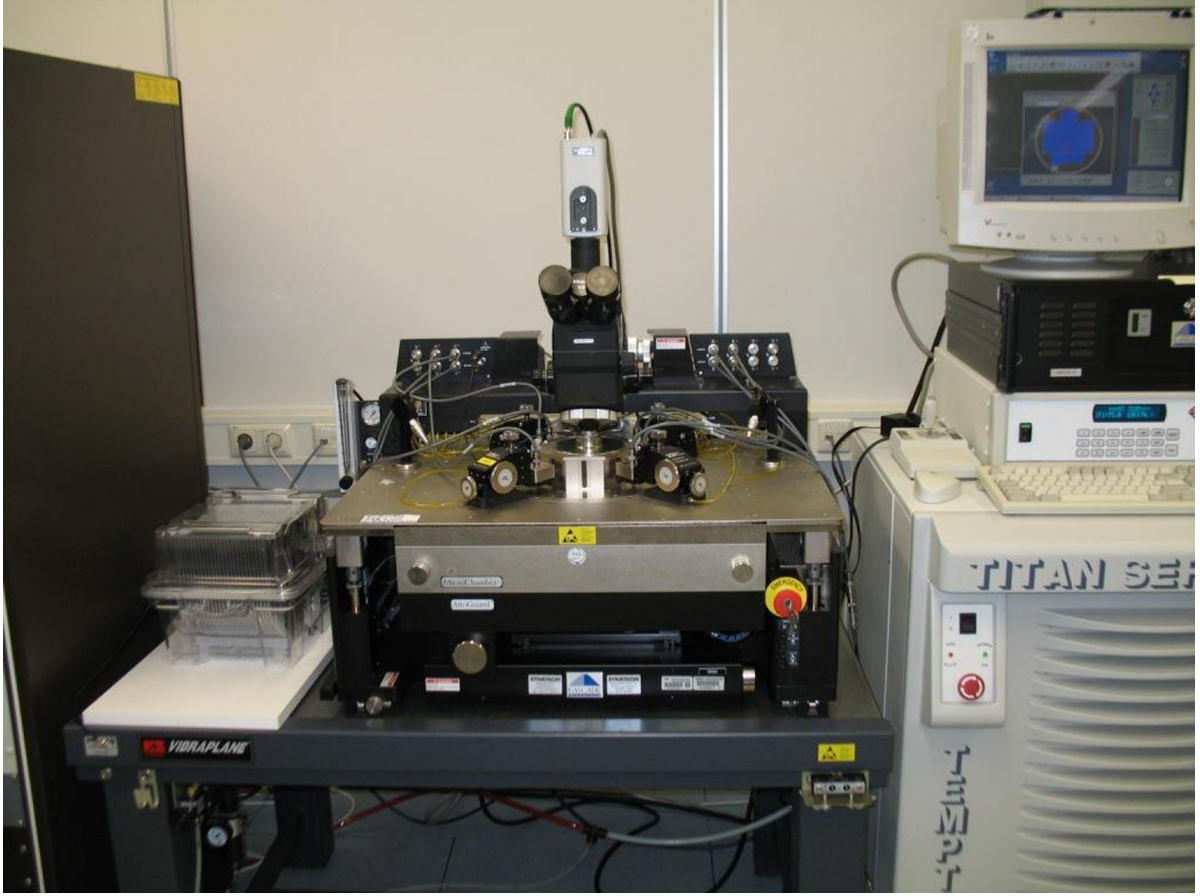


Figure 3.4: Used NBTI measurement equipment: Probe Station Summit 12000-Series/Titan Series Tempronic, and HP 4155B Semiconductor Parameter Analyzer.

used. Assuming a Poisson distribution and randomizing the effect of interface traps under the gate area [Rau07], the variance of NBTI degradation can be calculated as in Eq.(3.15) [Rau07].

$$\begin{aligned} \text{Var}(N_{IT_tot_eff}) &= \text{Mean}(N_{IT_tot_eff}) \\ &= \frac{\text{Mean}(\Delta V_{th}) \cdot \epsilon_{ox} W \cdot L}{2.7q \cdot t_{ox}} \end{aligned} \quad (3.15)$$

W and L represent the transistor gate width and length respectively. The constant number “2.7” is used to take into account both the random number of interface traps and the random spatial distribution of the traps [Rau07]. This is also the reason for the term “effective number of interface traps”, $N_{IT_tot_eff}$. The standard deviation (σ) of the ΔV_{th} is the square-root of its variance.

Table 3.2: Applied stress types in the NBTI measurements.

Stress Type	Sweep Parameters
DC	Stress voltage: 2.5V, 3V, 4V. Stress time: 10^3s , 10^4s , 10^5s .
Square Waves	High voltage: 2.5V, 3V, 3.5V, 4V, 4.5V. Low voltage: 0.5V, 1V, 1.5V, 2V, 2.5V, 3V. Duty-cycle: 2.5%, 5%, 10%, 30%, 50%, 70%, 90%, 95%, 97.5%. Frequency: 0.05Hz, 0.025Hz, 0.01Hz, 0.005Hz, 0.0025Hz, 0.001Hz, 0.0005Hz.
Stairs Waves (6 voltage stairs)	Stair voltage: 0V, 1V, 1.5V, 2V, 2.5V, 3V, 3.5V, 4V. (5 seconds for each stair.) (1.33V, 2.67V, -1V, -4V are used in four extra tests.)

Therefore by this "mean" one obtains the simulated degradation ΔV_{th} and simulated σ . Now up-limit envelopes of the simulated $(\Delta V_{th} + 3 \cdot \sigma)$ and $(\Delta V_{th} - 3 \cdot \sigma)$ are drawn. If the measured up-limit envelope of degradations lie within this range, it is classified as “*Matched*”, which means the model simulation matches the measurement result within 3σ .

3.3.5 Extraction of Model Parameters

In this thesis, all NBTI measurements were carried out at 125°C. Hence, the temperature dependence parameter E_a in the NBTI model (Table 3.1) can be freely selected without any influence on the simulation. Now there are only two model parameters, A and E_0 for the compact RD model to be extracted from silicon measurement results.

The parameters can be extracted by fitting the up-limit envelop of the silicon measurement results. The fitting method is using the Least Squares Method (LSM) between simulation and silicon measurement results. The model parameters are extracted from four silicon measurement results under different square wave stresses.

3.3.6 Model Results versus Silicon Measurement Results

The validation has been carried out using CMOS 140nm technology with three groups of stress waveforms. The stress conditions for three groups are summarized in Table 3.2. The

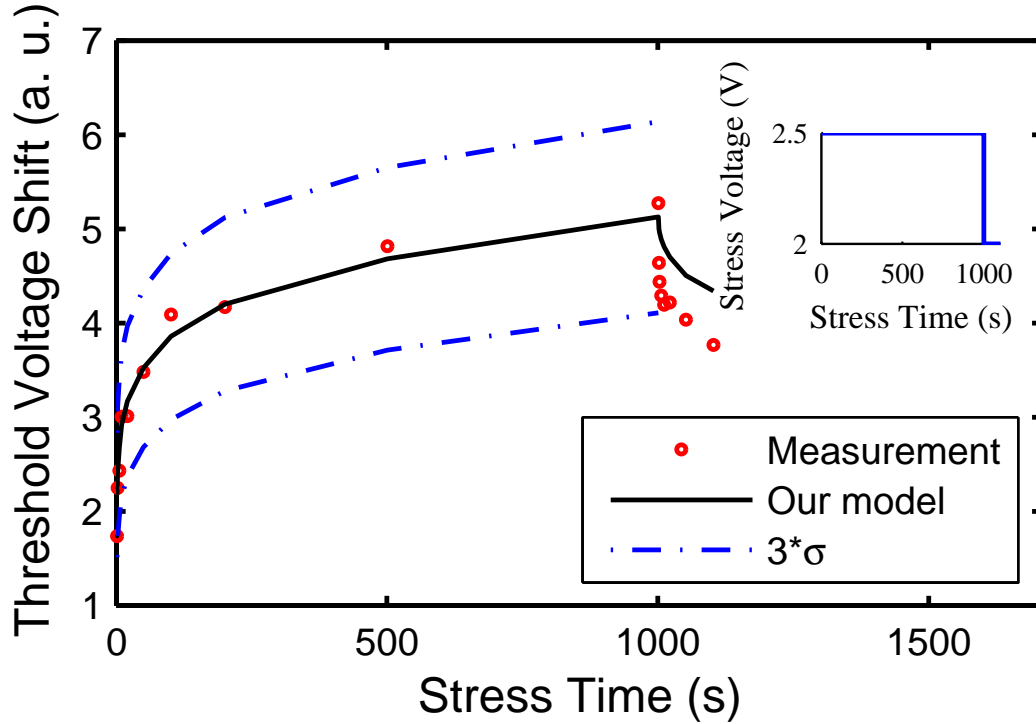


Figure 3.5: Stress at 2.5V DC voltage for 1000 seconds.

temperature for all stress conditions is fixed at 125°C . In total, there are 82 stress conditions. For each stress condition, a new PMOS transistor is adopted. These PMOS transistors have the same size of $8\mu\text{m} \times 160\text{nm}$, and the same gate oxide thickness of 2.9nm . All measurements are input into simulations and compared with their results. The model uses only two extracted model-fitting parameters A and E_0 , which are kept the same under all 82 stress conditions. However, due to the space limitations, only eight of them are described in this section.

The first group is stressed by DC voltages with a small period of relaxation at the end of each measurement. It was found our model cannot fit DC measurements very well. In total, only 70% of the measurements are matched with the simulation. The reason is because of the time-power constant. In our model, the time-power constant will not change with the stress voltage. However, DC measurements show an increasing time-power constant with the stress voltage. This varying time-power constant lets our model fail. In fact, at a low stress voltage (2.5V), the time-power constant is quite stable (around 0.16) and our model can match 11 measurements out of total 12 measurements at 2.5V DC stress. Only one measurement which has a time-power constant of 0.179 can not be matched. Therefore one can say there is 92% accuracy at 2.5V. While at 3.0V and 4.0V DC stress measurements, only 12 measurements out of a total of 21 measurements can be matched by our model. Hence there is 57% accuracy at

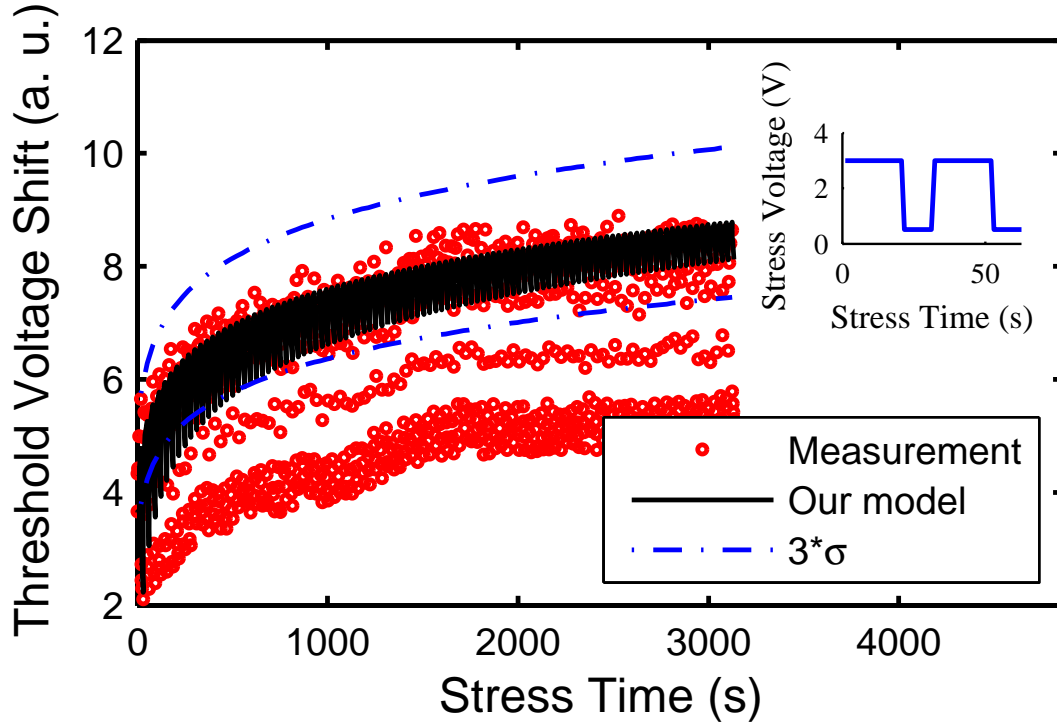


Figure 3.6: Stress by a square-wave: high voltage 3V for 20 seconds, low voltage 0.5V for 10 seconds, duty-cycle 66.7%, 100 cycles (3000 seconds).

3V and 4V. All these measurements which can be matched by our model have a time-power constant of around 0.16. Those measurements which can not be matched by our model all have a time-power constant larger than 0.17. In total, the degradation uncertainties at **DC** stresses are much larger than in the case of **AC** stresses.

Mahapatra et. al [Mah11] claim that in addition to ΔN_{IT} , the **DC** stress causes hole trapping in pre-existing bulk-oxide traps. At relatively higher stress bias, additional hole trapping in newly generated bulk-oxide traps takes place. These hole trappings make the **DC** measurements more uncertain. Figure 3.5 shows the measurement results together with simulation results under 2.5V **DC** stress. The stress continues for about 1000 seconds and at the end of the measurements, a relaxation at 2V for about 100 seconds takes place.

The second group is stressed by square waves, whose duty-cycle, high voltage, low voltage and frequency are being scanned. The scanned parameters are listed in Table 3.2. The simulations match the measurements well in both high-voltage and low-voltage scans, except for two measurements. For the duty-cycle and frequency scans, the simulations can match the measurement well, except for one measurement at a 95% duty-cycle. In the 95% duty cycle,

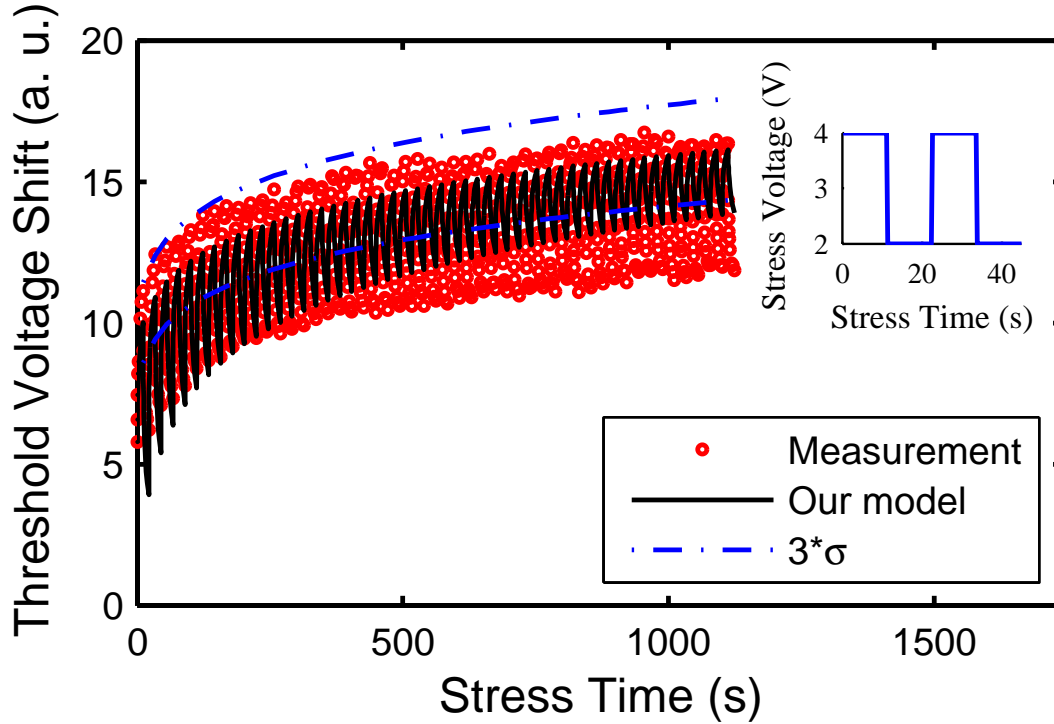


Figure 3.7: Stress by a square-wave: high voltage 4V for 10 seconds, low voltage 2V for 10 seconds, duty-cycle 50%, 50 cycles (1000 seconds).

three measurements are performed. The other two measurements matched with the model simulation.

Two square-wave stress situations are shown in Figures 3.6 and 3.7, in which both simulations match well with the measurements in the up-limit envelopes. Figure 3.6 shows a square-wave stress with high voltage of 3V during 20 seconds, and a low voltage of 0.5V for 10 seconds, duty-cycle 66.7%, and 100 cycles recording. The measured degradation-recovery amplitude is much larger than the simulated one, because our simplified RD equations cannot reflect such fast and deep recovery. Figure 3.7 shows another square-wave stress with a high voltage of 4V for 10 seconds, low voltage of 2V for 10 seconds, duty-cycle 50%, and 50 cycles of recording. Now the measured degradation-recovery amplitude is much closer to the simulation as compared to that shown in Figure 3.6, because the relax voltage is closer to the stress voltage and the recovery is less deep.

The third group employs a stair-waveform of six levels to imitate arbitrary waveform stresses. The stair voltage-levels are also shown in Table 3.2. The reason to use stair-waveforms instead of real arbitrary waveforms is due to the limitation of the instruments. The semiconductor parameter analyzer cannot generate real arbitrary waveforms. Five stair-waveform stresses are

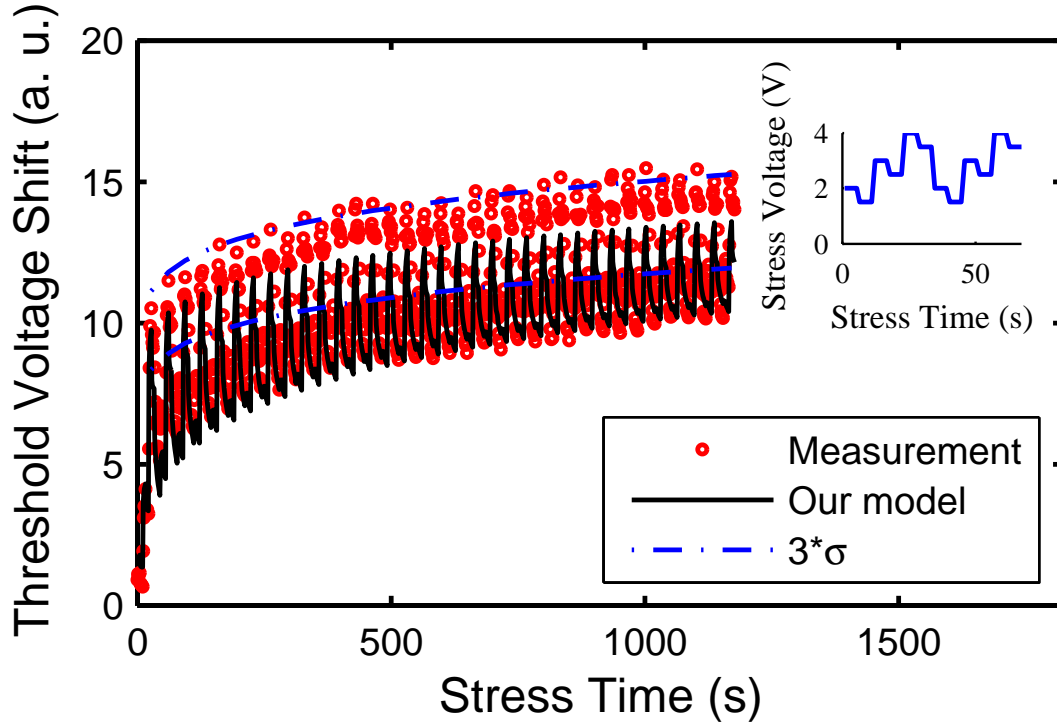


Figure 3.8: Stress by a stair-wave: 2V, 1.5V, 3V, 2.5V, 4V, 3.5V. Each step continues for 5 seconds and is then repeated for 35 cycles (1050 seconds).

shown in Figures 3.8, 3.10, 3.12, 3.14, and 3.16. The more detailed stress-relax behaviour for just a few cycles are depicted in Figures 3.9, 3.11, 3.13, 3.15, and 3.17 respectively. These figures show that measurements lie in the 3σ range of simulations under such complicated waveform stresses. In the Figures 3.8, 3.10, and 3.12, the measured up-limit envelopes are on the edge of simulated 3σ limitations, but the trends follow the edge well. As before, our simplified RD equations cannot reflect fast and deep recovery, but the measurements can. So there is a difference between simulated and measured degradation-recovery amplitude. However, for the Figures 3.8, 3.10 and 3.12, the measured degradation-recovery amplitudes are closer to simulations. This is because the recovery voltage changes in a slow manner in these measurements which make it possible for the simulation to keep up with the change. Figure 3.16 shows a long time, with a large number of cycles of measurement (over 10^4 seconds and 500 cycles) for a stair-waveform stress situation, in which the simulations still match the measurements very well.

The final evaluation results are summarized in Table 3.3. In total, for 82 silicon measurement results, the compact model matches more than 86% of silicon measurements under AC stresses conditions (square-wave and complicated stair-waveform stress). The model can also match 70% of measurement results under DC stress conditions. It is worth emphasizing that the

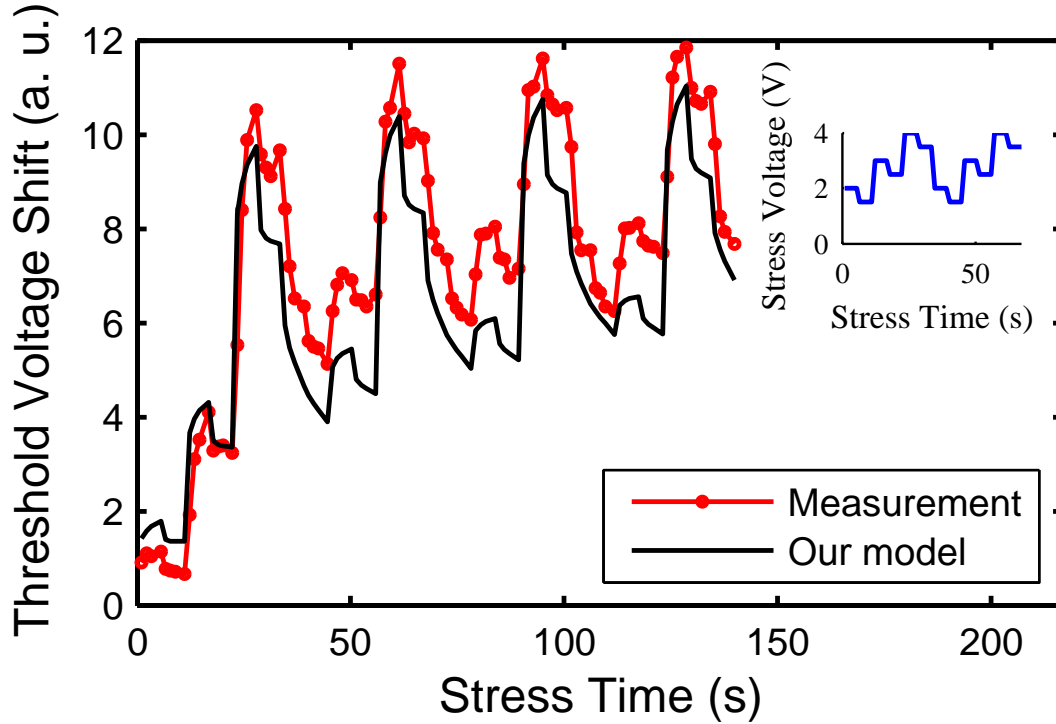


Figure 3.9: A few cycles detail in the beginning of Figure 3.8.

compact model uses only *two* model-fitting parameters which are extracted from 4 square-wave stress measurements and kept unmodified in all 82 measurements to achieve these results.

3.4 NBTI Simulation in Cadence

The NBTI simulation for AMS circuits in the Cadence ADE can be carried out via two approaches, being the RelXpert approach and the Verilog-A approach. They will be explained in the following sections.

Table 3.3: Final evaluation results.

Stress Waveform	Total	Matched	Matched in percentage
DC	33	22	70%
Square Wave	35	32	91%
Complicated Wave	14	12	86%

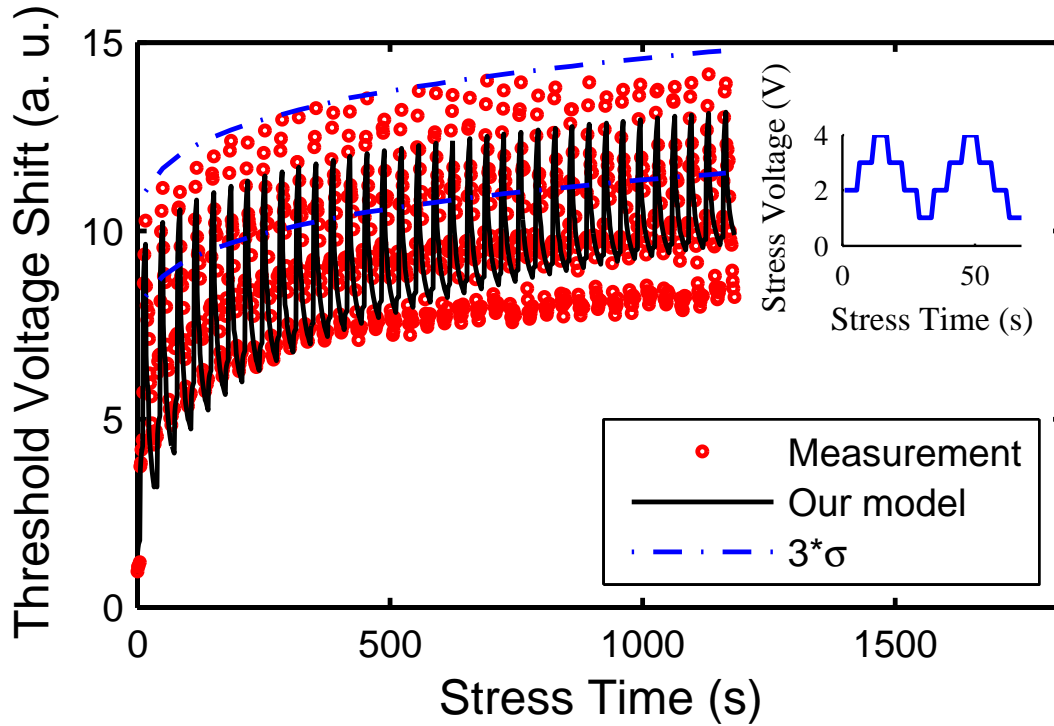


Figure 3.10: Stress by a stair-wave: 2V, 3V, 4V, 3V, 2V, 1V. Each step continues for 5 seconds and is then repeated for 35 cycles (1050 seconds).

3.4.1 Cadence RelXpert Simulation with Power-Model

The first approach is by using the Cadence ageing simulation tools RelXpert, which was originally developed in 1989 by Hu et al. at the University of California, Berkeley [Tu91]. The name of the tool at that time was BERT (Berkeley Reliability Tools). The name was changed later to RelXpert and now it has become the ageing simulation tool of Cadence [Cad11].

RelXpert makes use of the simple power model for the NBTI simulations. Hence in theory, it can only simulate the NBTI degradation for DC voltage stress situations. However, Cadence uses a simple technique to simulate arbitrary voltage stress conditions by integrating the degradation in each time point and average over the whole time range. This approach is similar to the usage of the average stress instead of the real stress, which could significantly under-estimate the NBTI degradation [Mar13].

RelXpert uses its own model to simulate NBTI, which is called AgeMOS model. Refer to Appendix A for the detail of the RelXpert AgeMOS model.

If one wants to modify the supply voltage or temperature in the aged netlist to see what the performance of the circuit after years of stress in normal conditions will be (stress in stress conditions for several years and then again operate under normal conditions), the option “Allow Modify – voltage of aging simulation” in the RelXpert Commands Menu can be used. RelXpert

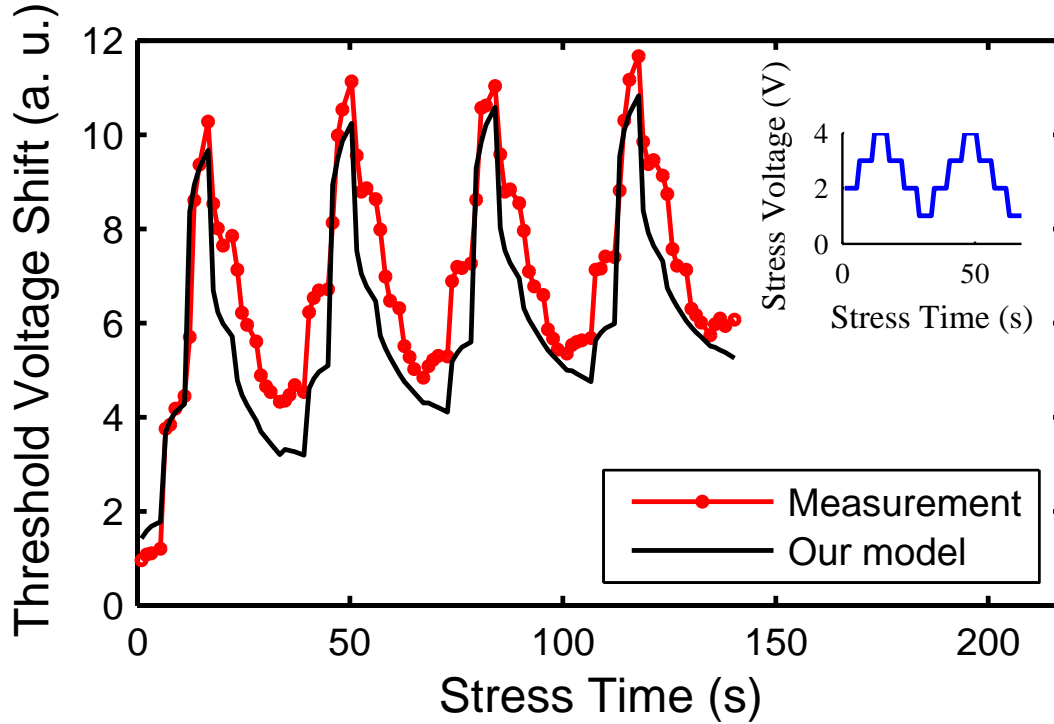


Figure 3.11: A few cycles detail in the beginning of Figure 3.10.

will pop up the netlist before the last run and allows the user to modify the netlist. For detailed simulation information is referred to Virtuoso® RelXpert Reliability Simulator User Guide [Cad11].

3.4.2 Cadence Verilog-A Simulation with our Compact NBTI Model

The second method for NBTI simulations is by using Cadence Verilog-A and a custom-written NBTI modelling script. This method was first used by Kole in the NXP Presto simulator [Kol07].

The compact NBTI model proposed in this chapter can be easily incorporated with transient simulations in SPICE simulators using the same method. However, one issue could be the simulation time. In fact it is impossible to simulate several years of both transient and aging simulations. Therefore the results need to be extrapolated to the required aging time from the short-time detailed simulations. Our new compact model has the capability to incorporate such an extrapolation because the trend of the degradation results is a simple power function of time. Therefore, a simulation strategy has been implemented in Cadence ADE using Verilog-A, which is depicted in Figure 3.18. The Verilog-A code can be found in Appendix B.

The strategy will now be explained using the block numbers in Figure 3.18:

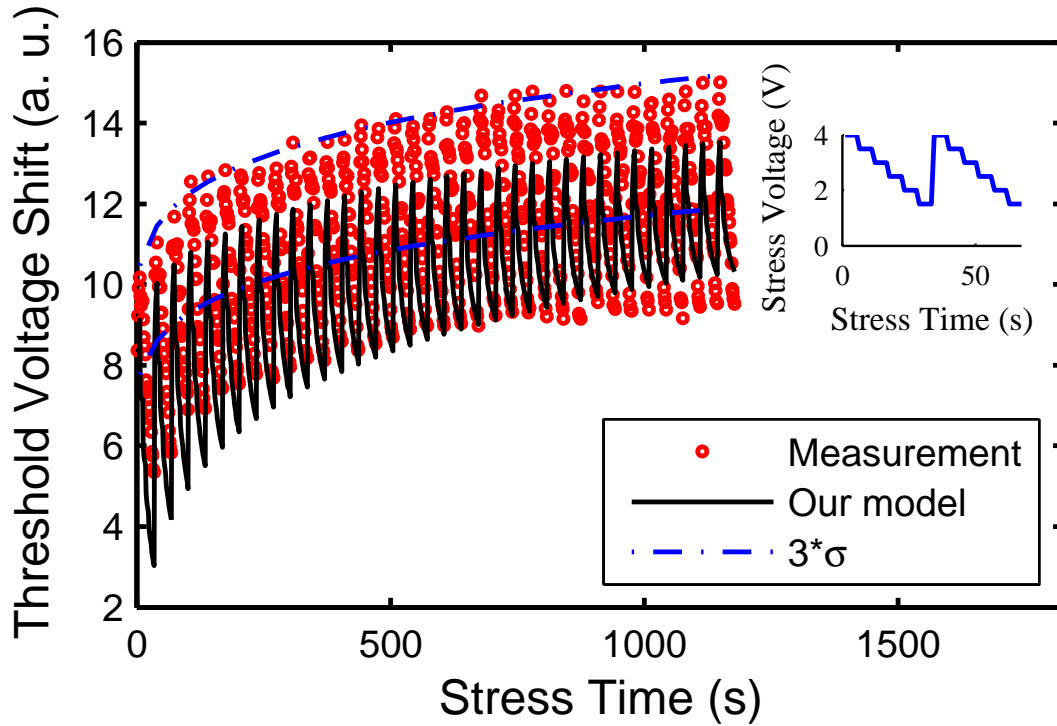


Figure 3.12: Stress by a stair-wave: 4V, 3.5V, 3V, 2.5V, 2V, 1.5V. Each step continues for 5 seconds and is then repeated for 35 cycles (1050 seconds). It can be observed that the simulated top-envelope is lower than the measurement. The measurement is almost out of the 3σ area. It is probably because the average stress voltage is high. As already explained, if the stress voltage is too high, our model will become less accurate.

1. A transient simulation is carried out on a non-aged (fresh) netlist using Cadence Spectre.
2. With the stress voltage waveforms on each **PMOS** transistor obtained from Spectre, the detailed threshold degradation is calculated using our compact model in Table 3.1.
3. Since both the transient simulation and the detailed degradation calculation are carried out over a time span of just a few seconds, rather than years, an extrapolation is required. For each **PMOS** transistor, there are only two parameters in the extrapolation function that one is required to extract from the detailed degradation simulation: A and n , as shown in Figure 3.18. These parameters are fitted using the least-square-error (LSE) method and stored in separate files.
4. The aged netlist is generated by adding a voltage source in series with the gate of each **PMOS** transistor to model the threshold degradations.

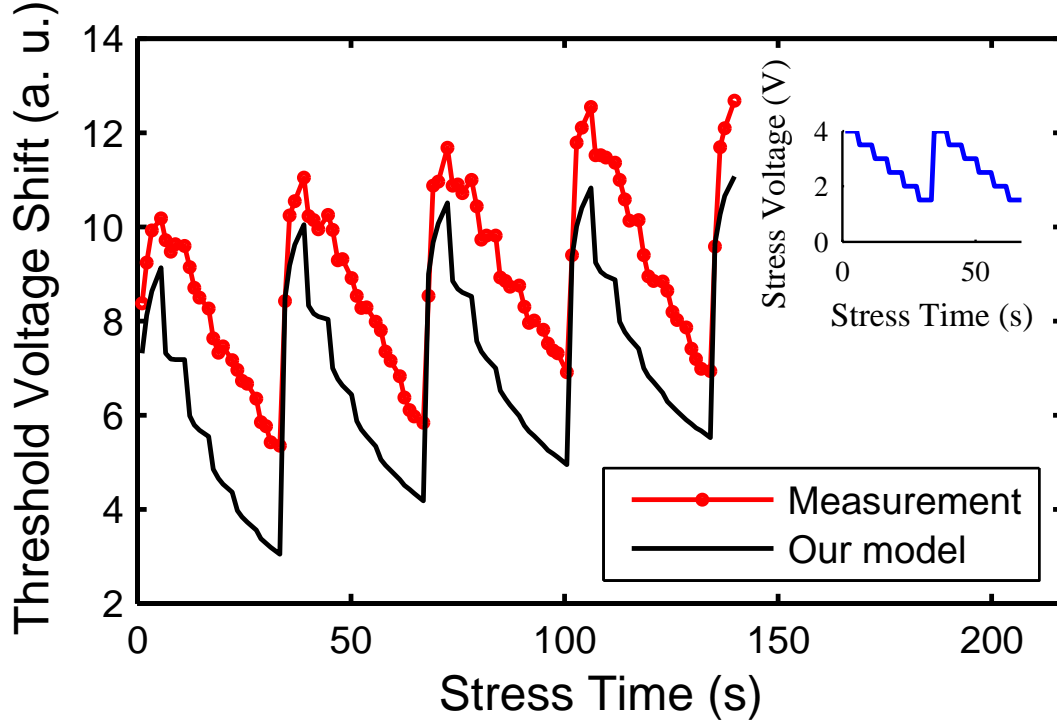


Figure 3.13: A few cycles detail in the beginning of Figure 3.12.

5. The value of each voltage source is calculated by the power function, as shown in Figure 3.18, with the parameters from stored files. Now the aged netlist is ready to be used in any kind of simulation in Spectre with regard to a specified number of aging years.
6. The stochastic effect of NBTI degradation is taken into account by randomizing the effect of interface traps under the gate area assuming a Poisson distribution (Eq.(3.15)).
7. The aged netlist with a stochastic NBTI degradation sample is generated using the same approach as 4), except that the threshold-voltage shift is now calculated from a sampled stochastic number of interface traps which is given by [Rau07]:

$$sample(\Delta V_{th}) = \frac{(2.7) \cdot q \cdot t_{ox} \cdot sample(N_{IT_tot_eff})}{\epsilon_{ox} W \cdot L} \quad (3.16)$$

The $sample(\Delta V_{th})$ and $sample(N_{IT_tot_eff})$ in Eq.(3.16) are the stochastic samples. The whole process is shown in Figure 3.18 and has been implemented using Verilog-A in Cadence ADE. A variable “Quick_sim” is used in ADE to determine the various choices: detailed NBTI simulation to extract power-function fitting parameters, deterministic threshold-aging calculation, or stochastic threshold-aging calculation. The parameter sweep for “Quick_sim” in

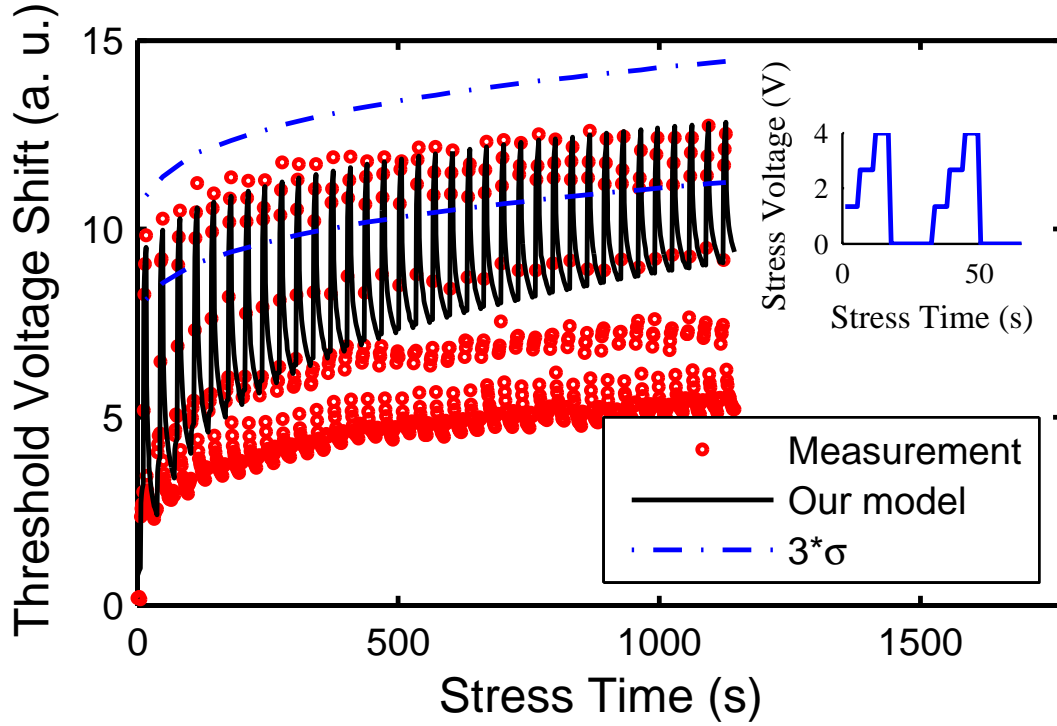


Figure 3.14: Stress by a stair-wave: 1.33V, 2.67V, 4V, 0V, 0V, and 0V. Each step continues for 5 seconds and is then repeated for 35 cycles (1050 seconds). The simulated top-envelope matched the measurement quite good in this case. The bottom envelope is much higher in simulation than in the measurement. It is because the RD theory cannot model the fast recovery well enough which causes the simulation to be always much higher in the bottom envelop than in the measurements. It is also the reason why we use the top-envelope to match the measurement.

ADE can be used to run a batch process, which makes the NBTI aging simulation very easy to combine with normal process variations in Monte-Carlo simulations.

The total simulation time is of the same order of Spectre transient simulation time, which is much faster as compared to that for normal RD solvers, e. g. several minutes for only one PMOS transistor [Kuf10]. Results of an example run on our server with one CPU core are shown in Table 3.4.

Table 3.4: The model simulation time in Cadence ADE vs. reference [Kuf10].

Circuit	# PMOS	Stress	# time steps	Simulation Time
Opamp	11	Sine	55	0.888 seconds (this thesis)
Single PMOS	1	Square	< 100	several minutes [Kuf10]

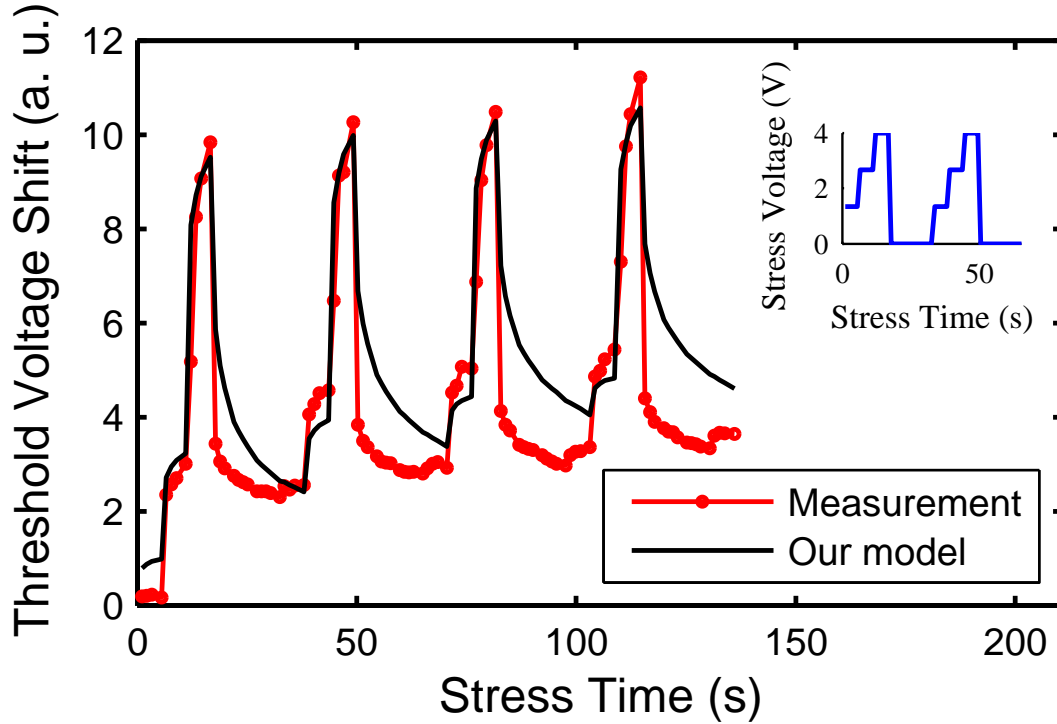


Figure 3.15: A few cycles detail in the beginning of Figure 3.14.

3.5 A New EI for Threshold Voltage Measurements

To validate the NBTI model as well as extracting model parameters, NBTI measurement data from nanometer CMOS chips are an essential requirement. However, this kind of reliability data is sensitive for silicon foundries and it is difficult to obtain by universities and small-to-middle sized companies. As a result NBTI measurements are often required to be performed by oneself and this will be addressed in this section.

Like other reliability tests, NBTI measurements are usually carried out under high temperature and high voltage conditions to accelerate degradations and reduce measurement time. The Device Under Test (DUT) is put into an oven and heated up to a high temperature like 125°C. Also a much higher voltage than the DUT normally experiences is applied. The DUT is kept under such stress conditions for a pre-determined period and then measurements are carried out. This procedure will be repeated until all the required data is collected.

The NBTI degradation is measured by extracting the Metal Oxide Semiconductor (MOS) transistor threshold-voltage, which is the most sensitive parameter in MOSTs in terms of ageing and is also the most difficult part as well as the most important part during NBTI measurements. As a result, this section will emphasize on the threshold-voltage extraction techniques.

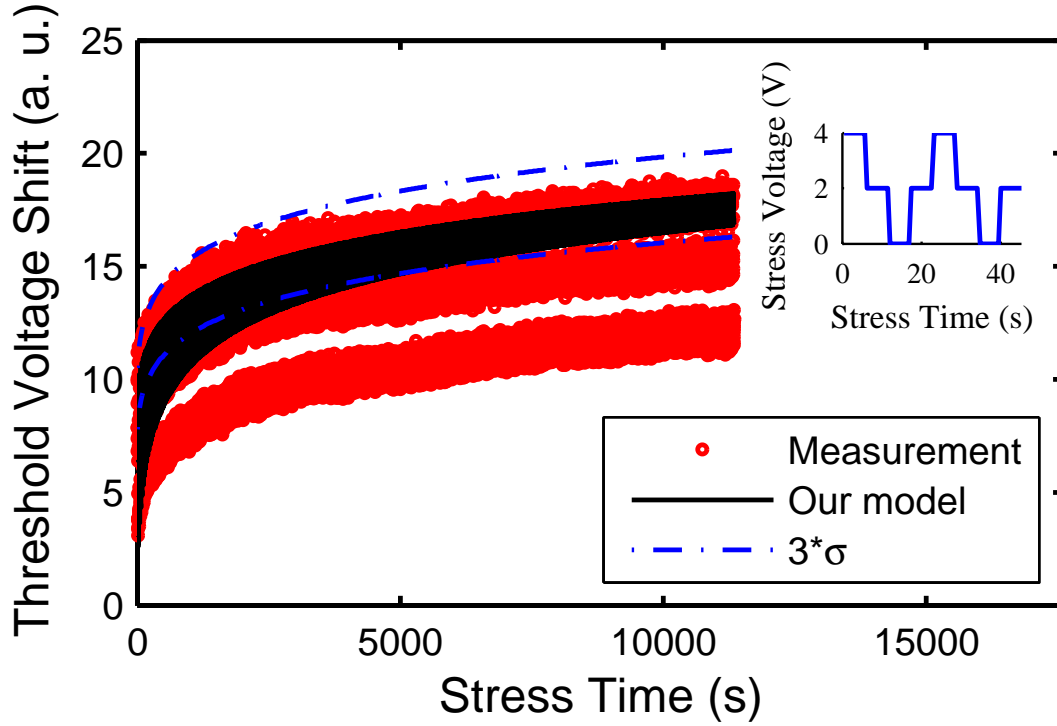


Figure 3.16: Stress by a stair-wave: 4V, 2V, 0V, and 2V. Each step continues for 5 seconds and is then repeated for 500 cycles (10^4 seconds).

3.5.1 MOST Threshold-Voltage Extraction by Traditional Instruments

The NBTI ageing effect tends to increase the absolute value of the threshold-voltage with stress time. Moreover, part of threshold-voltage shift can be quickly recovered after the stress is removed, which is called the “recovery” effect of NBTI [Ala07]. The recovery effect makes the threshold-voltage extraction during NBTI measurements quite difficult. Currently there are several methods to extract the NBTI-induced threshold-voltage shift while reducing the recovery effect. We mention the Measurement-Stress-Measurement (MSM) technique, the On-The-Fly (OTF) method, Fast-Vt approach and Fast-Id method [Rei07].

The MSM method [Rei07] uses the same approach as in characterization of process qualifications. It consists of measuring the drain current of the MOST during a sweep of the gate voltage after each stress cycle. This method allows a long recovery time which is up to the level of seconds. As a result, it only extracts the permanent part of degradation and shows distorted threshold-voltage shift curves. The model available in commercial ageing simulators, such as Cadence RelXpert, is based on parameters extracted with this method.

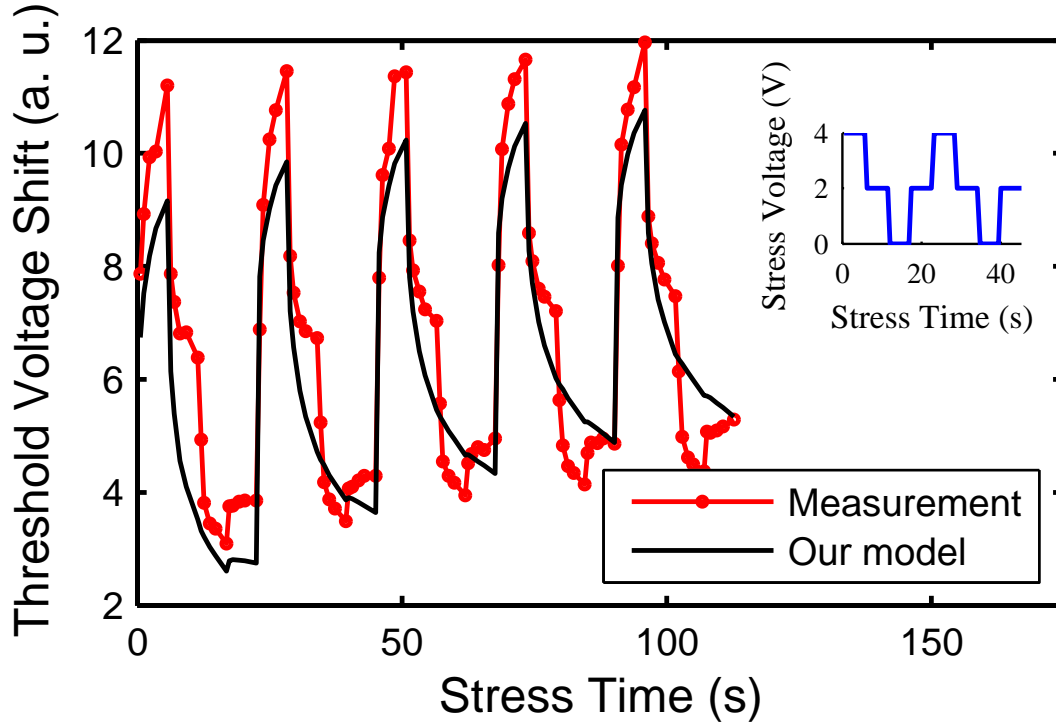


Figure 3.17: A few cycles detail in the beginning of Figure 3.16.

OTF [Rei07] measures the drain current at the stress gate-voltage level without interrupting the stress. It uses a three-parameter equation from a **SPICE** model in the linear regime. As three measurements are required to solve this equation, **OTF** carries out a modulation for the gate voltage around the stress level. The **OTF** method can reduce the **NBTI** recovery effect significantly. However, the simple **SPICE** model it employs to extract the threshold-voltage introduces large errors and a very high accuracy (long integration time) measurement is required. Another problem of **OTF** is that mobility degradation and the threshold-voltage shift are mixed. Both effects are almost indistinguishable in the regime of near stress.

The “Fast-Vt” method and “Fast-Id” method are both proposed by the **JEDEC** 14.2.2 (Device Reliability Working Group) proposal [JED04]. It describes a procedure for wafer level **DC** characterization of **NBTI**. The purpose is to extract the threshold-voltage shift due to unrecoverable damage generated during **NBTI** with customary equipment. The document describes a procedure that consists of a measurement/stress/measurement sequence with measurement delay in the range of 1ms. The threshold-voltage extraction can be performed by two methods, either “Fast-Vt” or “Fast-Id”.

The “Fast-Vt” method interrupts the stress and performs an Id-Vg characterization in the region near the threshold-voltage (sub-threshold region). Then the threshold-voltage can be

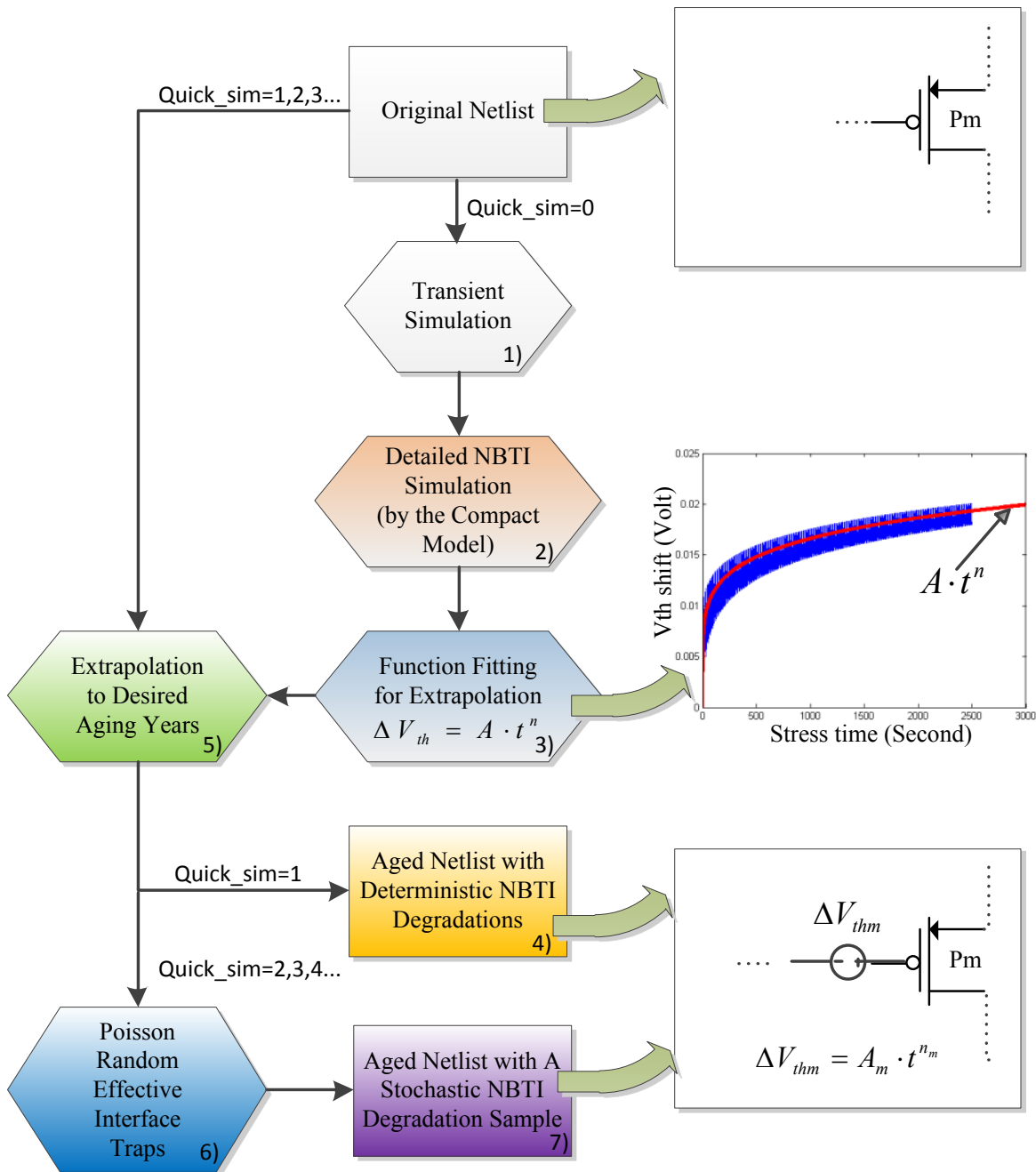


Figure 3.18: NBTI simulation strategy for analog/mixed-signal applications.

extracted using a linear interpolation. However, due to the sweeping and settling time for the gate voltage, the characterization with custom equipment allows a recovery time in the range of 100ms.

The “Fast-Id” method interrupts the stress and performs a fast measurement of the drain current at a gate voltage in the sub-threshold region, in which case the $\log(I_d)$ - V_g characteristic

is linear. This procedure is based on the assumption that the sub-threshold slope remains constant after NBTI degradation, which has been confirmed by measurements. Since the $\log(I_d)$ - V_g curve is linear and the slope of the curve does not change, the threshold-voltage shift is a horizontal shifting along the V_g axis. One measurement is sufficient to extract this threshold-voltage shift. As a result the measurement is fast and the NBTI recovery time can be reduced to around 1ms. In section 3.3.3, more information with regard to the Fast-Id method has been provided. This method has been used to validate our new compact NBTI model.

As described above, none of these methods are perfect and it remains difficult until now to accurately measure NBTI effects [Gra08]. Another problem for NBTI measurements are the cost. Traditionally, threshold voltages are measured with complicated equipment like probe stations and semiconductor parameter analyzers. It increases the cost and limits the time period over which reliability researchers use to observe the threshold-voltage shift. On the other hand, billions of SoCs are produced every year and used in almost all kinds of application areas. Most of them include both ADC and DACs at moderate accuracy (10- to 12-bits) and countless MOST transistors which can be used as DUT. If there is a way to measure the MOST threshold-voltage employing these on-chip ADCs and DACs, the ageing behaviour of these SoCs can not only be monitored continuously, but also measured in rich detail. Besides ageing, threshold-voltage information in SoCs is also of interest to process-variation studies in nanometer CMOS technologies.

In next sections, our new MOST model for the nanometer MOST transistor drain current is proposed, which makes it suitable for extracting the MOST threshold-voltage via on-chip general-purpose ADCs and DACs. Also an embedded instrument for NBTI on-chip measurements is being proposed.

3.5.2 A New MOST Drain-current Model

Since the threshold voltage will change with the body bias, it is worthwhile to define that the threshold voltage studied in this thesis employs a zero body-bias threshold-voltage (V_{th0}). This is the threshold-voltage which is measured at zero source-to-substrate bias. Numerous methods have been published in literature to extract the value of V_{th0} [OC02], and various extractor circuits have also been proposed [Rei06] to automatically measure V_{th0} . They normally measure drain currents at various gate (or both gate and drain) voltages and extract the V_{th0} from these measurement results by employing compact models. Based on the operation regime of the MOST, those methods and circuits can be divided into two groups: measuring in the sub-threshold regime and measuring in the strong-inversion regime.

Measuring in the sub-threshold regime can benefit from the V_{th0} definition and requires less relative accuracy ($< 1\%$) when compared to measuring in the strong-inversion regime ($< 0.1\%$). However, the drain current in the sub-threshold regime is very small, typically in the nA range. The JEDEC standard [JED04] mentions that the measurement system must be able to measure $100pA$ with a resolution of $1pA$ or better, which places a tough requirement on equipment resolution and offset calibration. Therefore it is not suitable for on-chip V_{th0} measurements.

Measuring in the strong-inversion regime takes advantage of the large drain current and low offset influence. However, the definition of the V_{th0} is in the sub-threshold regime and to extrapolate the drain current from the strong-inversion regime down to the sub-threshold regime is difficult even by compact models. It depends very much on the model accuracy. Industry standard compact models like the Berkeley Short-channel IGFET Model (BSIM) 4.6 model [Cha12], Philips Surface Potential (PSP) model [Gil06] and C. C. Enz, F. Krummenacher and E. A. Vittoz (EKV) model [Enz95] all face the problem to satisfy this accuracy issue.

The BSIM 4.6 model is known to be inaccurate in the sub-threshold regime and more than three hundred model parameters make the V_{th0} extraction difficult.

The PSP model is claimed to be accurate in both the strong-inversion regime and the sub-threshold regime [Gil06]. However, besides hundreds of model parameters, the PSP model requires extremely accurate drain current measurements (relative accuracy $< 10^{-5}$) [Rei07] because it actually uses the information from the derivation of the measured drain current. Such extremely accurate measurements are difficult to obtain by on-chip test circuits.

The EKV model is good in the sub-threshold regime, but it loses accuracy in the strong-inversion regime especially for nanometer MOSTs.

Therefore in order to extract V_{th0} on-chip based on the drain current measured in the strong-inversion regime, a new MOST model for the nanometer MOST drain current is required, which is valid for all MOST operational regimes, and is the key to embed the V_{th0} test inside SoCs.

Our new nanometer MOST model for its drain current is expressed in Eq.(3.17) to Eq.(3.21) [Wan15b].

$$I_d = F_{sd} - F_{ds} \quad (3.17)$$

$$F_{sd} = \frac{\beta \cdot \ln^2 \left[1 + \exp \left(\frac{V_p - V_s}{2V_T} \right) \right] \cdot \left(1 + \frac{V_d - V_s}{V_A} \right)}{\left\{ 1 + x \cdot V_d \cdot \ln^\alpha \left[1 + \exp \left(\frac{V_p - V_s}{2V_T} \right) \right] \right\}^{\frac{1}{\alpha}}} \quad (3.18)$$

$$F_{ds} = \frac{\beta \cdot \ln^2 \left[1 + \exp \left(\frac{V_p - V_d}{2V_T} \right) \right] \cdot \left(1 + \frac{V_s - V_d}{V_A} \right)}{\left\{ 1 + x V_s \cdot \ln^\alpha \left[1 + \exp \left(\frac{V_p - V_d}{2V_T} \right) \right] \right\}^{\frac{1}{\alpha}}} \quad (3.19)$$

$$V_p = \frac{V_g - V_{th0}}{n} \quad (3.20)$$

$$V_T = \frac{kT}{q} \quad (3.21)$$

The MOS terminal voltages all refer to the substrate and are expressed as V_d , V_g and V_s . In Eq.(3.17), the model employs a similar idea from the EKV model, which is forward current F_{sd} and backward current F_{ds} . However, unlike the EKV model in which the forward current is independent of V_d and backward current is independent of V_s , in the new model the forward current Eq.(3.18) and backward current Eq.(3.19) are modulated by both V_d and V_s . V_T is the thermal voltage, which is around 26mV at room temperature. Parameters k , T and q are the Boltzmann's constant, temperature in degrees Kelvin and the electrical charge of an electron respectively. Parameter x is for model fitting. V_p is the pinch-off voltage and n is the slope factor, which is linked to the weak-inversion slope. The parameter V_{th0} is the zero body-bias threshold-voltage which is of interest for this thesis. In Eq.(3.18) and Eq.(3.19), β is a fitting parameter for mobility, transistor width-to-length ratio and gate oxide capacitance per unit area, like $\mu C_{ox} W/L$ in the classic square-law model [Gra09c]. Parameters x and α take into account the velocity-saturation effect (of the mobility). Drain-induced barrier lowering (DIBL) and the short-channel effect are taken into account by parameter V_A .

The model is originated from the EKV model and the short-channel effect and velocity-saturation effect were introduced. By keeping the F_{sd} and F_{ds} symmetric and experiment with many fitting formulas, finally the model shown here resulted in the best to fit with measurements. It is hence an experimental model with no strong physical links. The model might be better understood using several extreme cases. Assume V_s is zero and the transistor is operating in the sub-threshold regime while V_d is very small to reduce the DIBL effect (for example 0.05V). This bias condition is normally used for V_{th0} measurement in the sub-threshold regime. In this

situation, V_p is negative. The sub-threshold conditions can then be expressed as Eq.(3.22) to Eq.(3.26).

$$\exp\left(\frac{V_p - V_s}{2V_T}\right) \ll 1 \quad (3.22)$$

$$\exp\left(\frac{V_p - V_d}{2V_T}\right) \ll 1 \quad (3.23)$$

$$x \cdot V_d \cdot \ln^\alpha \left[1 + \exp\left(\frac{V_p - V_s}{2V_T}\right) \right] \ll 1 \quad (3.24)$$

$$x \cdot V_s \cdot \ln^\alpha \left[1 + \exp\left(\frac{V_p - V_d}{2V_T}\right) \right] \ll 1 \quad (3.25)$$

$$\left| \frac{V_s - V_d}{V_A} \right| \ll 1 \quad (3.26)$$

The drain current I_d in sub-threshold as described by Eq.(3.17) can then be simplified to Eq.(3.27) with $V_s = 0$. This is the known expression for the sub-threshold drain current [Gra09c].

$$\begin{aligned} I_d &= \beta \cdot \exp\left(\frac{V_p - V_s}{V_T}\right) - \beta \cdot \exp\left(\frac{V_p - V_d}{V_T}\right) \\ &= \beta \cdot \exp\left(\frac{V_p}{V_T}\right) \cdot \left[\exp\left(-\frac{V_s}{V_T}\right) - \exp\left(-\frac{V_d}{V_T}\right) \right] \\ &\approx \beta \cdot \exp\left(\frac{V_p}{V_T}\right) \cdot \left[1 - \exp\left(-\frac{V_d}{V_T}\right) \right] \end{aligned} \quad (3.27)$$

In the moderate inversion regime, the velocity-saturation effect can be ignored, which means condition in Eq.(3.24) and Eq.(3.25) is still valid. If V_d is larger than the pinch-off voltage V_p , the transistor will work in the saturation regime, and the backward current Eq.(3.19) can be ignored in this case. The left side of Eq.(3.22) will be much larger than 1 and hence dominates. The drain current in this situation can be expressed as shown in Eq.(3.28), which is the classic square-law equation [Gra09c].

$$I_d = \beta \cdot \left(\frac{V_p - V_s}{2V_T} \right)^2 \cdot \left(1 + \frac{V_d - V_s}{V_A} \right) \quad (3.28)$$

If V_d is smaller than pinch-off voltage V_p , the transistor will work in the linear regime. The backward current Eq.(3.19) can not be ignored but equation Eq.(3.26) will remain valid. The drain current in this situation can be expressed as in Eq.(3.29), which is the classic linear-regime equation [Gra09c]:

$$\begin{aligned}
I_d &= \beta \cdot \left(\frac{V_p - V_s}{2V_T} \right)^2 - \beta \cdot \left(\frac{V_p - V_d}{2V_T} \right)^2 \\
&= \frac{\beta}{(2V_T)^2} \cdot \left(V_p \cdot V_d - \frac{1}{2} V_d^2 \right)
\end{aligned} \tag{3.29}$$

In the strong-inversion regime, the velocity-saturation effect will dominate. The backward current can be ignored if V_d is larger than the pinch-off voltage V_p . Both left sides of Eq.(3.22) and Eq.(3.24) will be much larger than 1 and hence dominate. The drain current in Eq.(3.17) can be simplified in this case to Eq.(3.30) and is linearly increasing with V_g instead of following a square-law, which is well known for the velocity-saturation influence. The term $V_d^{-1/\alpha}$ originally comes from the fact that the lateral electric field accelerates the velocity-saturation occurrence. Now it influences the drain-to-source conductance in a way that the drain-to-source conductance will become lower with increasing drain-to-source voltage. This change of drain-to-source conductance in the strong-inversion regime is already known [Gra09c]:

$$I_d = \frac{\beta}{2V_T \cdot x^{1/\alpha}} \cdot V_p \cdot \left(1 + \frac{V_d}{V_A} \right) \cdot V_d^{-1/\alpha} \tag{3.30}$$

For other situations which cannot be simplified, the drain current is required to be calculated by Eq.(3.17) to Eq.(3.21). The entire model only uses 6 parameters, n , β , x , α , V_A and V_{th0} . They are fixed and independent of V_d , V_g and V_s values. Using the measured drain currents in the strong-inversion regime, all 6 model parameters can be extracted by minimizing the error between the model result and the measurement result by using the **LSM** method in Matlab.

3.5.3 Accuracy

In order to validate the new **MOST** model, measurement results from 90nm **NMOS** transistors are shown in Figures 3.19 to 3.21. Moreover, to enable further study on accuracy, simulation results using the **TSMC** 65nm **BSIM4.6** model are provided in Figures 3.22 and 3.23. During the 90nm measurements, the body and source contacts of the **NMOS** transistor were connected to ground. Gate and drain were swept from 0 to 1.2V with 0.05V steps. Figure 3.19 shows the drain current change with drain voltage at different gate-voltage levels. The new **MOST** model fits the measurements well.

To further validate the model, the first-order derivation of the drain current, the drain conductance G_{ds} , of both measurements and model are shown in Figure 3.20. The new model fits the measurement well in most regimes, except the part of the transfer from the linear regime to the strong-inversion regime occurs (at around $V_d = 0.8V$). The measurement results

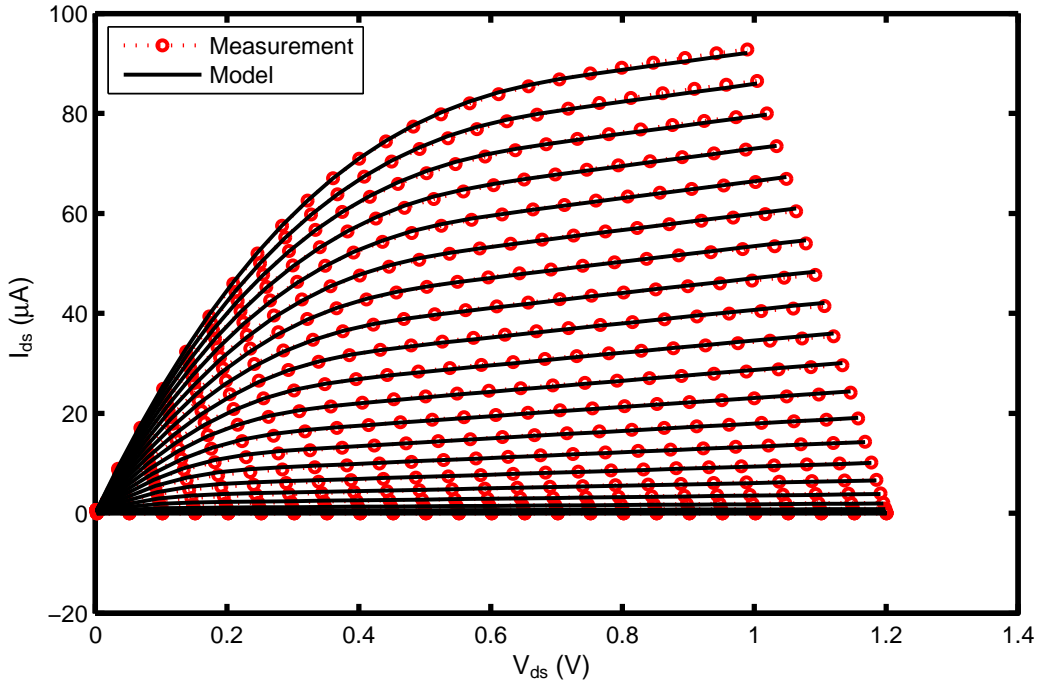


Figure 3.19: Comparison of our new model with the measured drain current of a 90nm NMOS transistor. $V_s = 0$, V_g and V_d are swept from 0 to 1.2V with a step of 0.05V [Wan16].

in Figure 3.19 have been used to extract six model parameters. At the same time, a more accurate measurement has been performed in the sub-threshold regime to check whether the model with parameters extracted from the strong-inversion regime are sufficiently accurate for the sub-threshold regime. For the sub-threshold measurements, the drain current has been measured at least 10 times more accurately in resolution than the measurement in Figure 3.19. Results show that the model with parameters extracted in the strong-inversion fit measurements in the sub-threshold regime well as depicted in Figure 3.21. It should be noted that the noise floor of the sub-threshold current measurement is around $1nA$.

In ageing measurements, the threshold-voltage shift is more important than the actual threshold-voltage. To validate the new model in terms of ageing measurements, simulations have been carried out by comparing this model-extracted V_{th0} with BSIM4.6 model results. The BSIM model parameters originate from the TSMC 65nm Process Design Kit (PDK). The BSIM model has been simulated in Cadence Spectre with a shift in its V_{th0} parameter of $\pm 50mV$. The simulated drain current together with gate and drain voltage have been used to extract the new model parameters. Figure 3.22 compares the extracted V_{th0} between the BSIM4.6 model and our MOST model. The x-axis depicts threshold-voltage shifts from $-50mV$ to $+50mV$ (this is

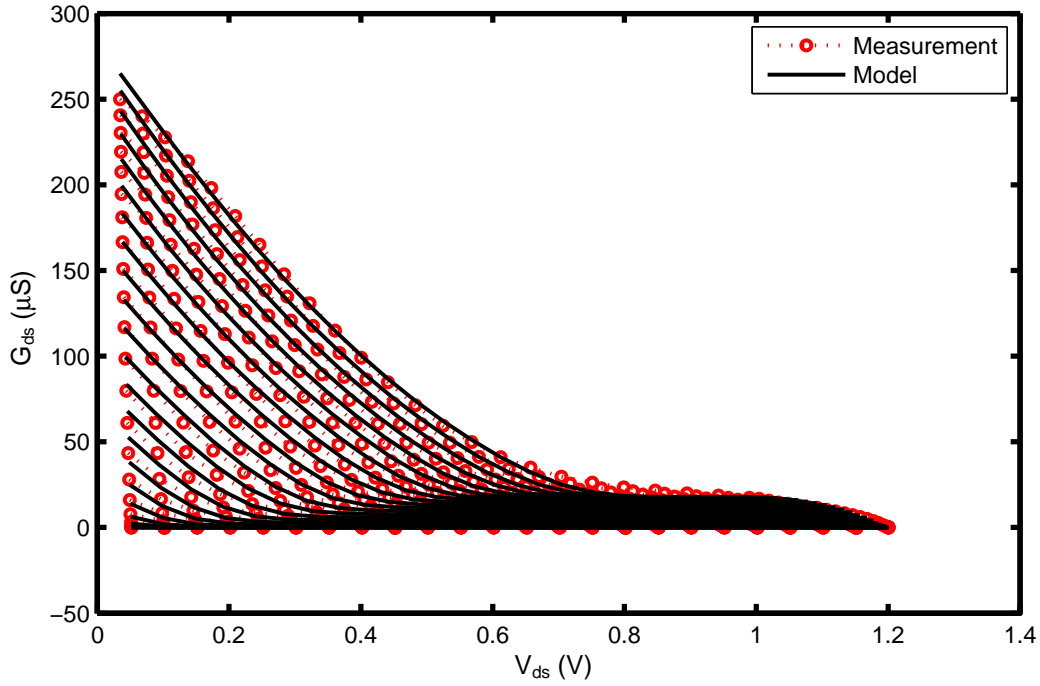


Figure 3.20: Comparison of our new model with the measured drain conductance of the same 90nm NMOS transistor as shown in Figure 3.19.

normally the maximum shift that NBTI can introduce). The y-axis represents the V_{th0} by both the BSIM4.6 model and our model. They are very close and the error is within 1mV.

In order to realize an on-chip V_{th0} test in a SoC without adding extra costs, the drain current needs to be measured by already-existing general purpose ADCs in the SoCs. These general purpose ADCs have normally a 10-bits to 14-bits accuracy. The drain current measurements can not be as accurate as in a semiconductor parameter analyzer. It is therefore important to check the sensitivity of V_{th0} , which is extracted via the new model with respect to the drain current accuracy. Suppose the drain current (whose maximum is below $400\mu A$) is measured by an ADC with a full-scale of 1mA. By changing the accuracy of the ADC from 7-bits to 14-bits, the V_{th0} extracted by the new model is plotted in Figure 3.23. The actual V_{th0} being 443mV is shown as a red solid line for reference. From Figure 3.23, it can be deduced that if less than 1mV V_{th0} error is required, the ADC is required to be at least 10-bits and preferably 12-bits.

3.5.4 Realization of the new EI

The idea to measure the V_{th0} on-chip is shown in Figure 3.24. Two matched MOST transistors, P1, P2 and one load resistor R, are added into a SoC. The transistor P1 will be stressed, while

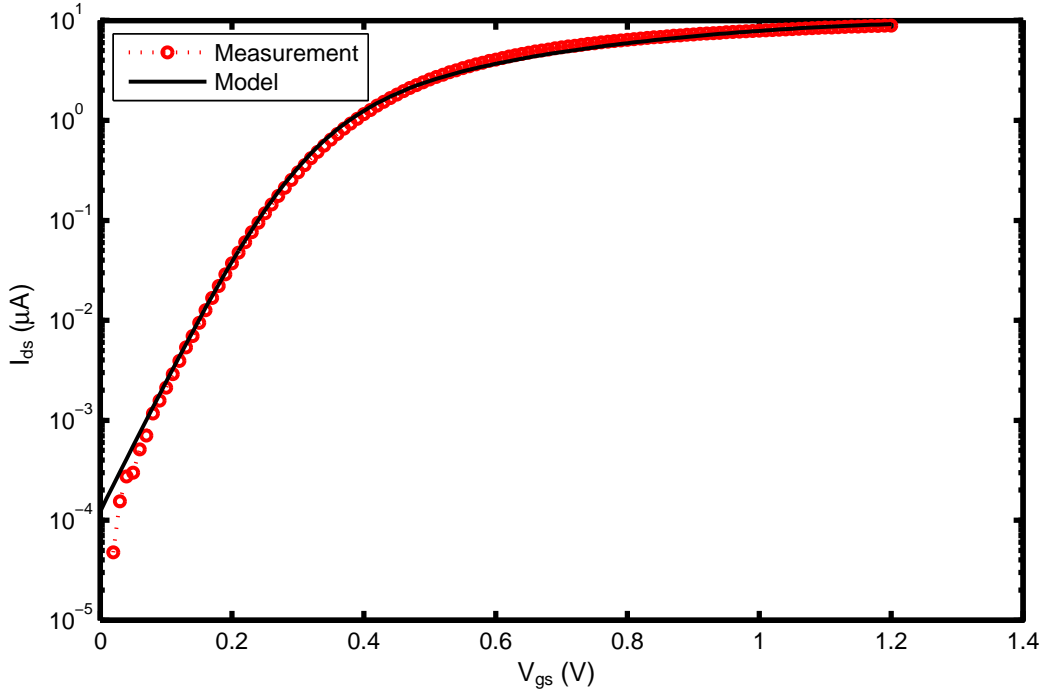


Figure 3.21: Comparison of our new model with the measured drain current I_{ds} in the sub-threshold regime of the same 90nm NMOS transistor in Figure 3.19. Parameters $V_s = 0$, $V_d = 0.05V$, V_{gs} is swept from 0 to 1.2V with a step of 0.01V.

transistor P2 will be unstressed and works as a reference fresh device. A general purpose ADC and DAC in the SoC are applied to sweep each transistor's gate voltage and measure the voltage of the load resistor at the same time. The measurement results are processed by the CPU inside the SoC with the help of our new MOST model. The detailed procedure is depicted in Figure 3.24 and starts from the upper-left sub-figure. The gate of the transistor P1 is connected to the DAC to sweep the voltage from the ground to the power supply. The transistor P2 is turned off by connecting its gate to the supply (PMOS). The voltage at the load resistor R is measured by the ADC at each DAC sweeping step. Now the drain voltage of the P1 can be calculated by the difference of the supply voltage and the ADC measured voltage V_{ADC} . The drain current I_d can be calculated as the ADC measured voltage V_{ADC} divided by the load resistance R . These can be expressed in Eq.(3.31) and Eq.(3.32).

$$I_d = \frac{V_{ADC}}{R} = F_{sd} - F_{ds} \quad (3.31)$$

$$V_{ADC} = R \cdot F_{sd} - R \cdot F_{ds} \quad (3.32)$$

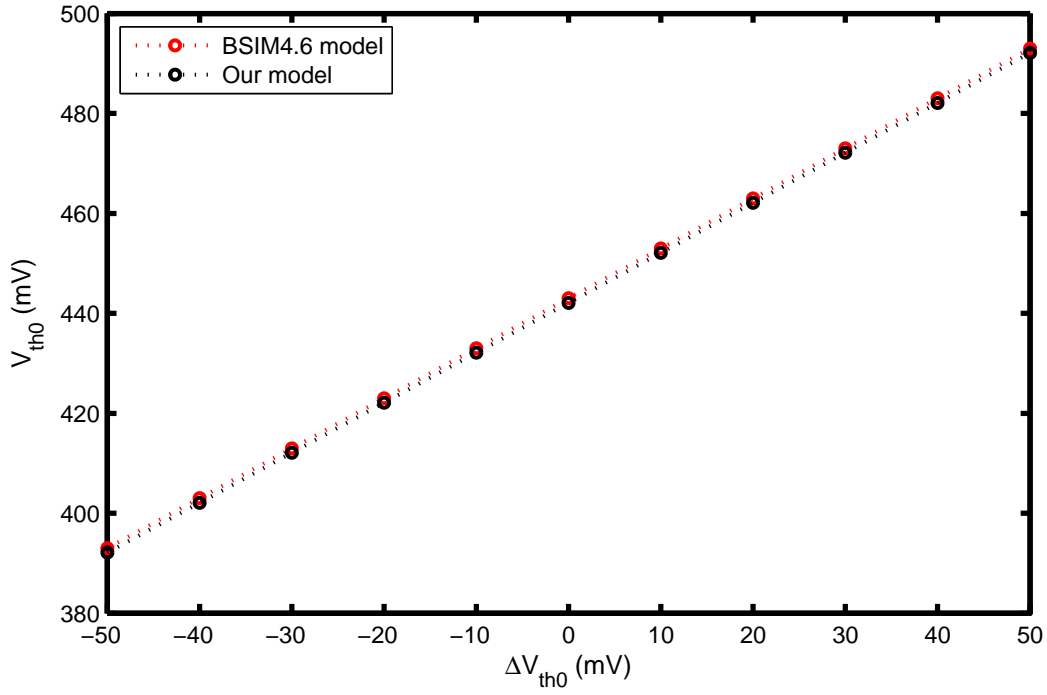


Figure 3.22: Comparison of our new **MOST** model with **BSIM4.6** model from the **TSMC65nm** PDK for the V_{th0} shift. The V_{th0} value in the **BSIM** model is shifted from $-50mV$ to $+50mV$. Originally the V_{th0} value in the **BSIM** model is $443mV$.

Based on the F_{sd} and F_{ds} expressions in Eq.(3.18) and Eq.(3.19), it is interesting to note that the load resistance R can be absorbed into the parameter β as one model-fitting parameter. So the accurate value of R is not required to be known in advance. The six model parameters (including V_{th0}) can then be extracted from Eq.(3.32). Subsequently the V_{th0} of P1 is obtained.

The same procedure can be applied to the transistor P2 in the upper-right sub-figure in Figure 3.24. Now transistor P1 is turned off and the gate of P2 is connected to the **DAC** to be swept. The **ADC** measures the voltage at the same point. The V_{th0} of P2 can be obtained in the same way as for P1. After V_{th0} of both transistors P1 and P2 are measured, the transistor P1 is connected to the stress voltage (for example, to the ground in Figure 3.24c). The transistor P2 is turned off to remove any stress in order to be kept fresh. The stress will be periodically stopped and measurements will be performed for threshold voltages of P1 and P2. In that sense Figure 3.24 shows a loop for its three sub-figures. The V_{th0} values together with the ageing time information can be stored in a local memory and monitored by users as a life-status indication of the **SoC**. This information can also (theoretically after agreement of users) be sent via internet to the manufacturing company as a database for product-reliability studies.

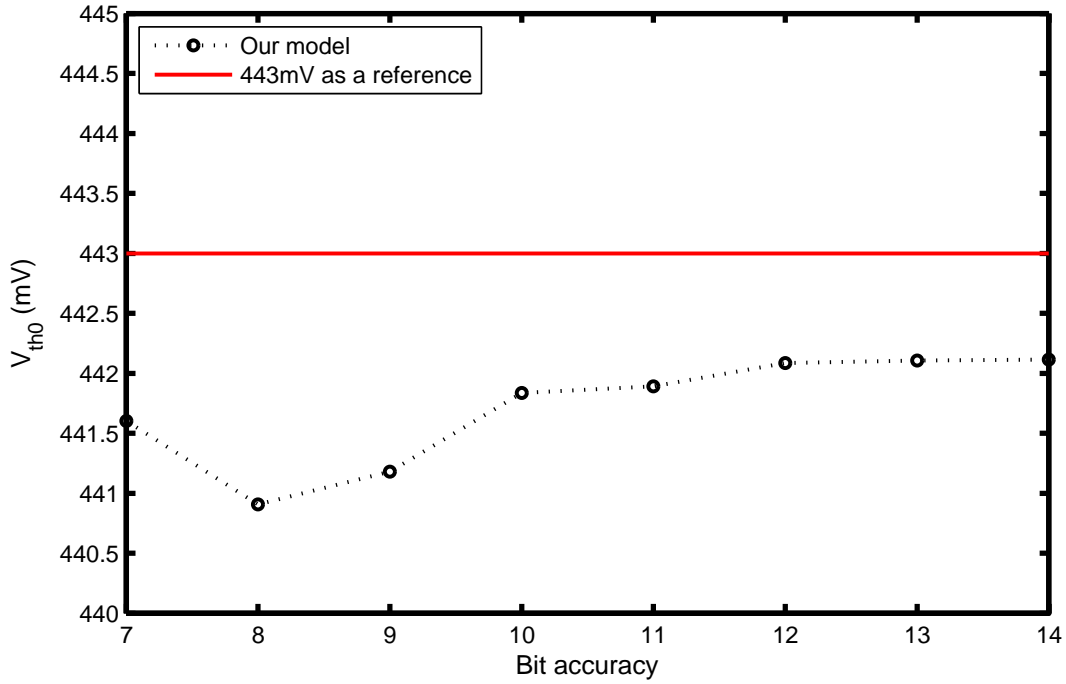


Figure 3.23: Comparison of our new **MOST** model with **BSIM4.6** model from the **TSMC** 65nm PDK for different bit accuracy of the drain current. Original V_{th0} value in **BSIM** model of 443mV is shown as a red solid line for reference.

One problem will be the temperature because it will change the V_{th0} as well, which has a strong influence on ageing. In order to decouple the temperature influence from ageing-induced V_{th0} shift, normally an accurate temperature sensor is required to be incorporated. However, in our opinion the temperature effect can be disconnected without a temperature sensor. This is achieved by using a closely located well-matched **MOST** transistor pair as shown in Figure 3.24. Ageing mechanisms in nanometer **MOST** transistors which change V_{th0} like **NBTI**, **HCI** and **TDD** which are actually changing the surface-state charges in the silicon-dioxide. This can be proven from the definition of the threshold-voltage Eq.(3.33). V_{FB} is the Fermi potential and the parameter ϕ_b is the substrate potential. The body effect parameter is γ and surface-state charges are referred to as Q_{ss} in Eq.(3.33). It is divided by the gate-channel capacitance C_{ox} and then added to the threshold-voltage. No temperature is involved when calculating the threshold-voltage change from the surface-state charges change. As a result, the V_{th0} shift by ageing can be simply measured by the difference in V_{th0} between the reference transistor and the stressed transistor. They are at the same temperature and matched well. Hence the difference in V_{th0} should come from ageing effects (and initial mismatch).

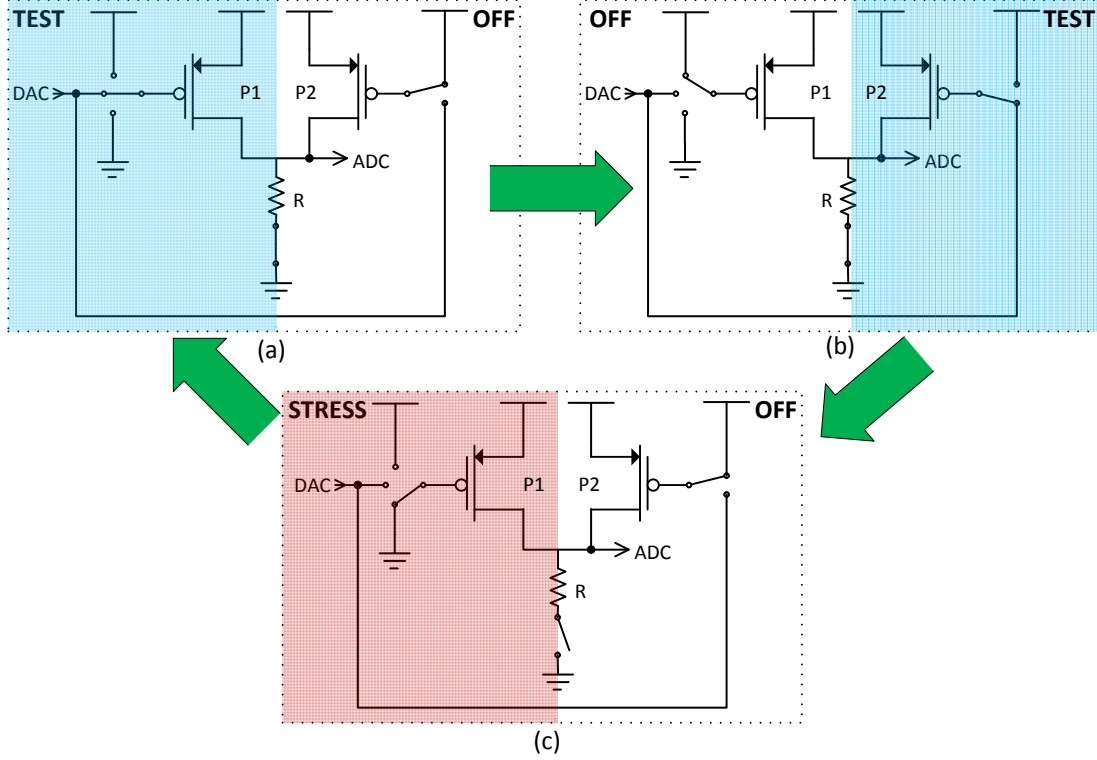


Figure 3.24: Proposed on-chip test scheme for measuring V_{th0} ageing behaviour inside a SoC. (a) measurement of the P1 transistor, (b) measurement of the P2 transistor, (c) no measurements, P1 is under NBTI stress.

$$V_{th0} = V_{FB} + \frac{Q_{ss}}{C_{ox}} + 2\phi_b + \gamma_N \sqrt{2\phi_b} \quad (3.33)$$

Another problem is the ageing of the DAC and ADC. Compared to a DAC, the accuracy of the ADC is more important because the DAC voltage can be measured by the ADC. However, there is not much research on ageing behaviour of an ADC. One publication on this topic [Kha13] claims that the integral nonlinearity (INL) and differential nonlinearity (DNL) of a ADC could increase with ageing, and the offset will increase as well. An offset increase can be calibrated by simple open and short circuits and is thus less of a problem. The increase of INL and DNL is a real problem. It will negatively affect the ADC accuracy. However, our new MOST model can tolerate less accurate measurement results as has been shown in Section 3.5.3. If the ADC accuracy is not lower than 10 bits, the extracted V_{th0} will not be influenced. If the ADC accuracy is less than 10 bits, the accuracy of the extracted V_{th0} will be reduced; the exact effects of INL and DNL changes to the on-chip V_{th0} test is under research.

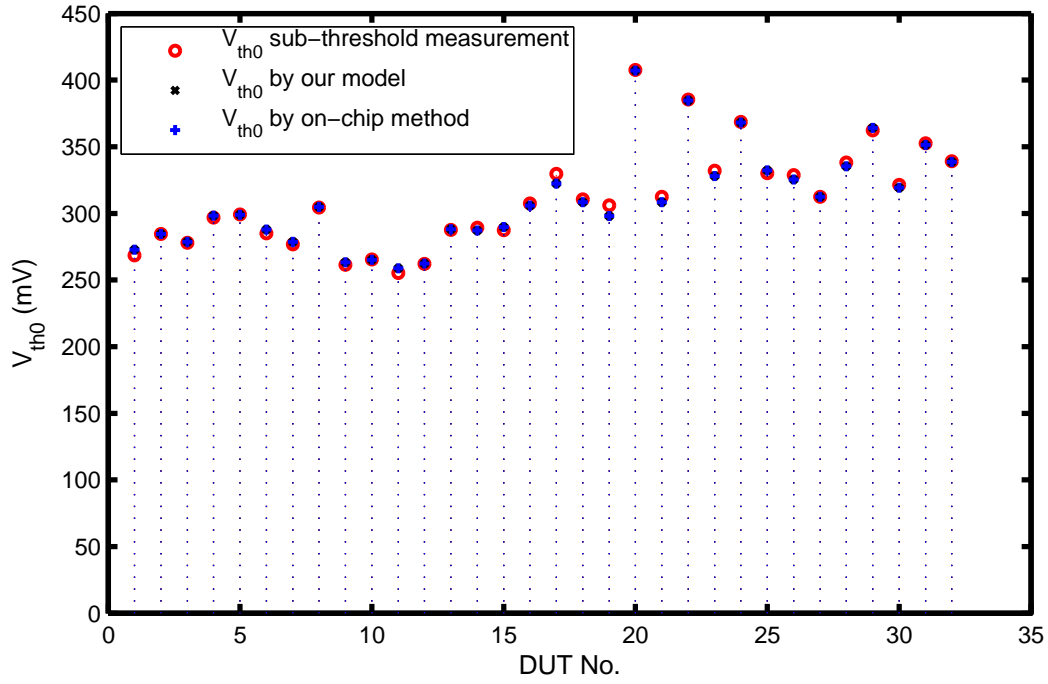


Figure 3.25: Comparison of the fresh V_{th0} between the three methods in the 90nm PMOS DUT transistors. There are 32 PMOS transistors in total. The black stars are overlapped by the blue crosses.

3.5.5 EI Experimental Results

A long-time stress test has been carried out. The aim of the test is to study the ageing behaviour of 90nm MOST transistors, and at the same time, validate the V_{th0} extraction method by our MOST model. The 90nm test chip has been provided by Ridgetop Group Inc. and was put into an oven and heated up to 127°C. The test chip contains 32 PMOS DUT transistors and those transistors are supplied with 1.15V power supply during the stress test. The ProChek System from Ridgetop Group Inc. has been used for performing the measurements [Inc14]. The system contains voltage-controlled resources that allow to sweep the gate and drain voltage of each PMOS transistor as well as measurement resources that allow to measure drain and gate currents concurrently. The stress test had a duration of 12 weeks and is equivalent to around 2000 hours. After each week (167 hours), the stress was stopped and measurements were carried out to check the life status of the DUTs.

In order to reduce the recovery effect, measurements for all DUTs were completed within 1% of the stress time. Measurements included two kind of tests. At first the DUT drain current was measured at a moderate accuracy (0.1μA) with V_g and V_d sweeping from 1.15V down to 0V. The sweeping step was set to be 10mV to gather as many results as possible. Second, the DUT drain current was measured more accurately (around 1nA) in the sub-threshold regime

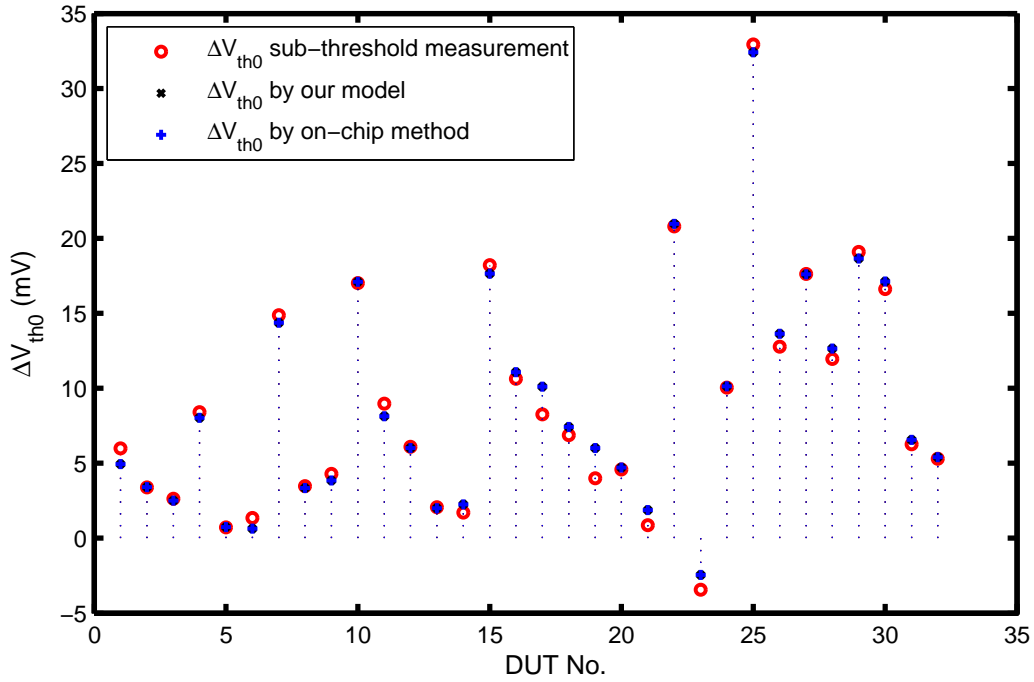


Figure 3.26: After stress for 167 hours, comparing the aged V_{th0} between the three methods in 90nm PMOS DUT transistors. They are the same 32 PMOS transistors as used in Figure 3.25. Again the black stars are overlapped by the blue crosses.

with V_d fixed at 50mV and V_g sweeping from 1.15V down to 0V. For the same DUT transistor, these two kind of tests were carried out at the same time (with only 20ms time difference, 0.000003% of the stress time) to avoid the recovery effect, and make sure that the V_{th0} extracted from both methods should be the same value.

The V_{th0} value has been extracted in three ways. First, all results of the drain current measured in moderate accuracy has been used to fit the new MOST model and extract the V_{th0} . The value of V_{th0} extracted in this way is referred to as “ V_{th0} by our model” and can be used to validate the model accuracy.

Second, one pair of I_d and V_d for each set of V_g sweeping has been measured at moderate accuracy. The selected sub-group results have been used to fit the new MOST model and obtain the V_{th0} . The selection of I_d and V_d is based on $I_d = V_d/R_{load}$, in which R_{load} is the load resistor as shown in Figure 3.24. By this method, the measurement results of the on-chip V_{th0} test method are emulated which has been proposed, and they can validate the on-chip V_{th0} test method under various R_{load} values. The V_{th0} value extracted in this way is referred to as “ V_{th0} by on-chip method”.

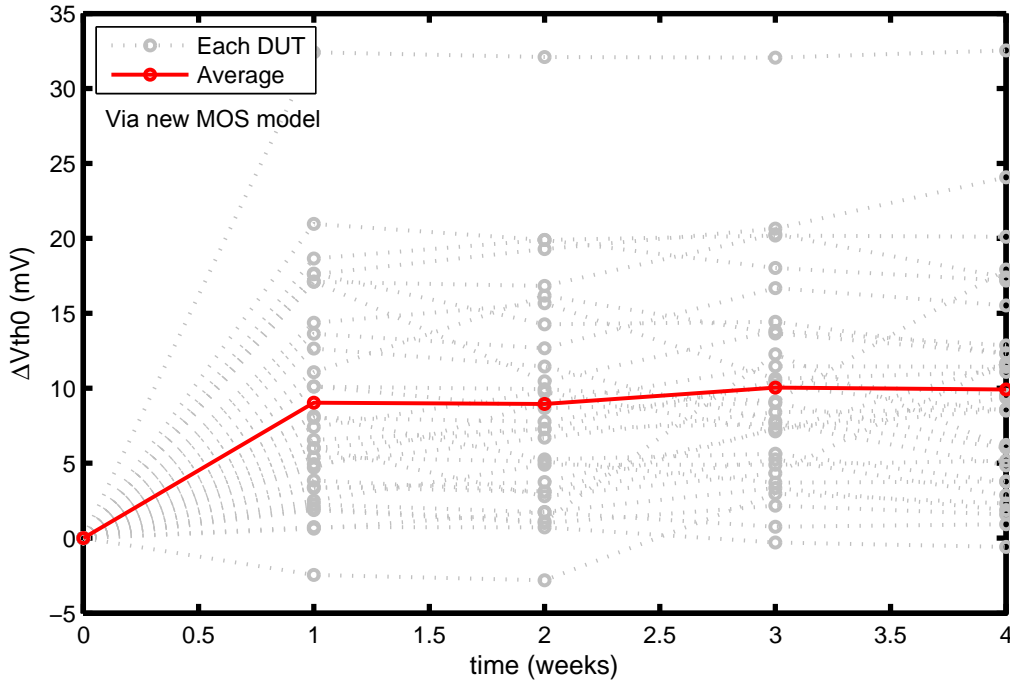


Figure 3.27: The V_{th0} change over time during 4 weeks of stress of 32 PMOS DUTs. Obtained by using the our MOS model.

Finally, from the measured higher accuracy drain current in the sub-threshold regime, the value of V_{th0} has been calculated and named as “ V_{th0} sub-threshold measurement”.

The V_{th0} of 32 PMOS transistors before stress have been plotted in Figure 3.25. The three V_{th0} values, “ V_{th0} sub-threshold measurement”, “ V_{th0} by our model” and “ V_{th0} by on-chip method” are shown in the figure with different colours and symbols. From Figure 3.25, the “ V_{th0} by model” and “ V_{th0} by on-chip method” agree well, because they use the same model. However, the “ V_{th0} by on-chip method” will need much less time as it only requires to sweep the V_g (around 115 times faster in this case) and can be implemented on-chip. The error between “ V_{th0} sub-threshold measurement” and the other two V_{th0} values obtained from the new model changes from DUT to DUT. The mean error is within 1mV while the standard deviation of the error is around 3mV, and the maximum error of these 32 DUTs is around 8mV. The accuracy cannot compare with industry equipment but is sufficient to monitor NBTI-induced threshold shifts.

The change of the threshold-voltage ΔV_{th0} due to ageing is more interesting with regard to reliability studies. Figure 3.26 shows the ΔV_{th0} by the three methods of the same group DUTs after 1 week (167 hours) stress at 127°C and 1.2V power supply. The “ ΔV_{th0} by model” and “ ΔV_{th0} by on-chip method” agree well again. The maximum error between “ ΔV_{th0} sub-threshold

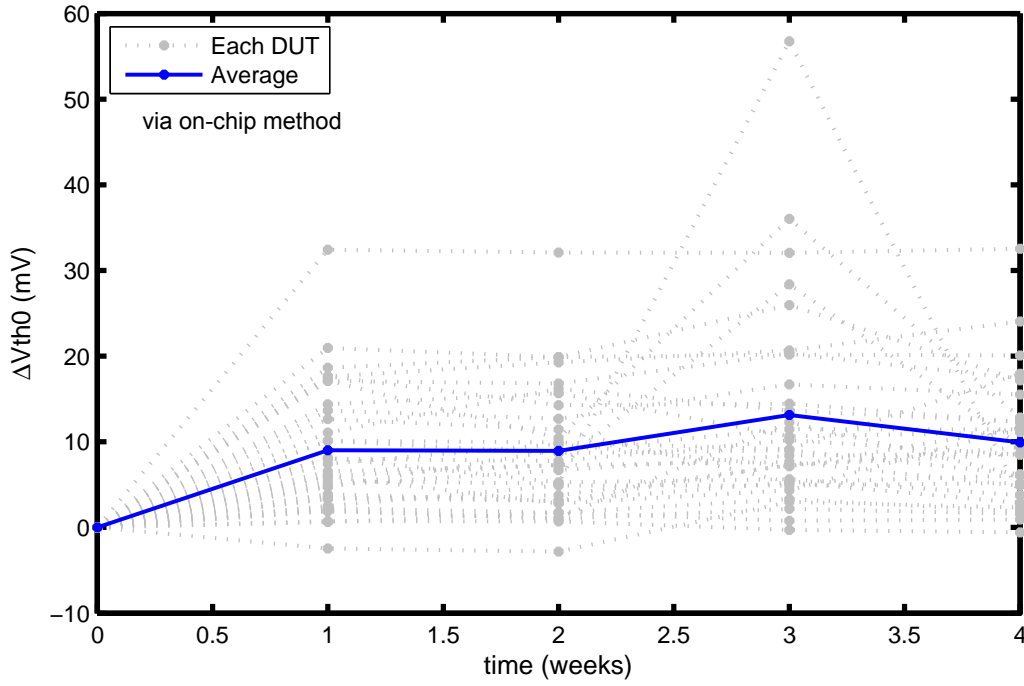


Figure 3.28: The V_{th0} change over time in 4 weeks stress of 32 PMOS DUTs. Obtained by using the on-chip method.

measurement” and the other two ΔV_{th0} methods is around $3mV$. In Figure 3.26, DUT No.23 is interesting because it shows a decrease of V_{th0} after one week stress, which is in contrast with the common understanding that ageing effects only increase the V_{th0} . The measurement results were double checked of both the strong-inversion drain current and the sub-threshold drain current for DUT No.23. There is indeed an increase in the drain current which corresponds to a decrease of V_{th0} . The reason could be a large random behaviour of ageing in nanometer MOST transistors which has been mentioned in other publications [Rei06, Rau07].

Figures 3.27 and 3.28 show the ΔV_{th0} change over time. The gray lines are the ΔV_{th0} value of each DUT. The average ΔV_{th0} of these 32 DUTs from “ V_{th0} by our model” and “ V_{th0} by on-chip method” are shown as a red line (Figure 3.27) and blue line (Figure 3.28) respectively. The average ΔV_{th0} from the “ V_{th0} by on-chip method” agrees well with the one from “ V_{th0} by model” method in the first, second and fourth weeks. However, the “ V_{th0} by on-chip method” has a large error in extracting V_{th0} for 5 DUTs in the third week. After tuning the load resistor R_{load} value, the problem disappeared. The reason for this could be that the “ V_{th0} by on-chip method” has a limitation in terms of the range of the R_{load} value. The new R_{load} value was found to be better suitable to keep the PMOS operating in the saturation region as much as

possible while at the same time, it could provide a larger V_d swing as was previously possible. It is similar to the requirement of the output stage of an OpAmp [Gra09c].

3.6 Conclusions

A new compact **NBTI** model based on iteratively solving the **RD** equations has been presented. This model can handle arbitrary stress waveforms for the up-limit envelope and is thus very suitable for analog/mixed-signal ageing simulations. It has been evaluated for **CMOS** 140nm technology with square-wave stresses as well as arbitrary wave stresses. The latter is of extreme importance in **AMS** simulations. For a total of 82 silicon results, the compact **RD** model can match 86% of **AC** stresses (the square wave stresses and complicated stair-wave stresses), as well as 70% of the **DC** stresses. These results are achieved by using the same 2 model fitting parameters which are extracted from just 4 square-wave stress measurements. The model has been implemented in Cadence **ADE** with Verilog-A, and can simulate both deterministic as well as stochastic **NBTI** aging effects. The simulation speed is about a thousand times faster than for other **RD**-based models, and the speed is at the same level of regular transient simulations.

The new closed-form model for the **MOST** drain current is provided to facilitate **MOST** threshold-voltage measurements in nanometer **CMOS** technologies. The model is valid for all regimes, like the sub-threshold/weak-inversion, moderate-inversion, strong-inversion and the linear regime. Measurements have been carried out in 90nm **CMOS**. Results show that the model agrees with measurements. Threshold-voltage extraction using this new model can tolerate less accurate measurement results in the strong-inversion regime, which can be obtained by already existing general-purpose **ADCs** inside **SoCs**. It will reduce both complexity and cost of ageing measurements. A low overhead on-chip **EI** for ageing-induced threshold-voltage shift measurement has been proposed. Long-time stress tests show that the on-chip V_{th0} test can characterize threshold-voltage shifts with a 3mV accuracy.

In the next three chapters, the focus is on the dependability of **Analogue/Mixed-Signal** circuits. Several fundamental blocks inside **Analogue/mixed-signal Front-Ends**, like operational amplifiers, active filters and **Analogue-to-Digital Converters** will be examined from an ageing point of view. Their performance degradations due to **Negative Bias Temperature Instability** are simulated with Cadence RelXpert while employing the **Negative Bias Temperature Instability** model we proposed in this chapter.

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Chapter 4

Design and Aging Evaluation of Analogue Operational Amplifier IPs

***Abstract-** In this chapter, a target [Operational Amplifier](#) is designed with a new gain-boosting technique to achieve more than 100dB gain in 65nm low-power [CMOS](#) technology. Its performances before and after [Negative Bias Temperature Instability](#) ageing are simulated with the ageing simulation approach presented in Chapter 2. The offset and gain are found to be the most sensitive parameters in terms of [Negative Bias Temperature Instability](#) ageing. Two methods are proposed to improve the dependability of an [Operational Amplifier](#). They are the robust design method and the [Embedded Instrument](#) method. A new [Embedded Instrument](#) for measuring the offset and gain of [Operational Amplifiers](#) is proposed.*

4.1 Introduction

There are not many publications concerning the dependability of [SoCs](#). Most of them are dealing with digital [IPs](#) inside [SoCs](#) and use redundant components together with dynamic routing to improve the dependability. The same method can be applied to [AMS IPs](#). However the area and power cost will be very high. In addition, re-routing of analogue signals may cause additional problems like increased noise and parasitics. The usage of replica circuits as reliability monitor for calibration could be another option [[Ask12](#)]. However, the research on reliability is still progressing and new discoveries, such as the stochastic properties of ageing, pop up frequently [[Rau07](#)]. It indicates that replica circuits will probably not age in the same

Parts of this chapter are based on publications of the author: [[Wan11](#)] and [[Wan14](#)].

way as the target circuit, which make the replica-circuit based reliability monitors less confident to work with as conventional calibration methods.

Our idea for improving the dependability of **AMS IPs** is by making each **IP** digitally observable. By facilitating this, the system can check important performance parameters, like the gain and offset of an **OpAmp**, and detect potential dependability problems in advance. Corresponding maintenance can be chosen to take place at the **IP** level (like the conventional self-calibration method) or at system level [Ker10]. Among different kinds of analogue **IPs**, the **OpAmp** is the most basic one and at the same time also the most important one. As known from Chapters 2 and 3, **NBTI** is the dominant reliability effect in 65nm **CMOS** technology. It can cause increasing thresholds and decreasing mobilities in **PMOSTs**, and hence reduce the gain of an **OpAmp** and increase the offset.

To investigate the reliability problem and therefore improve the dependability, a target **OpAmp** which implements a new gain-boosting method has been designed in 65nm low-power **CMOS** technology. This **OpAmp** is used as our test-vehicle in the Cadence RelXpert software to simulate **NBTI** ageing. Based on the information obtained from RelXpert, there are two ways to improve the dependability of the **OpAmp**. One approach is via more design effort, which uses special design techniques to cancel the performance ageing, for example by adding internal self-calibration circuits to the **OpAmp**. The self-calibration circuit is dedicated to the **OpAmp** design and belongs to the specific **OpAmp IP** block. It cannot be shared between multiple **OpAmps**.

The second method is via **Embedded Instruments (EIs)**, which can measure the performance ageing and send this information to the embedded dependability processor. The performance ageing can be adjusted at the system level by employing compensations [Kha14]. In addition, the **EI** is a independent **IP** and can be shared between multiple **OpAmps**.

This chapter is organized as follows. Section 4.2 introduces the design of the test-vehicle **OpAmp**. A new gain-boosting technique is presented to boost the **DC** gain of the **OpAmp** to 100dB without increasing the power-supply voltage or reducing the unity-gain frequency. The simulated non-aged performance of the test-vehicle **OpAmp** is also shown.

The **NBTI** simulation for the test-vehicle **OpAmp** is discussed in Section 4.3. The resulting performance ageings, especially the gain and offset ageing, are highlighted. The reliability problem discussion for the test-vehicle **OpAmp** can be extended to general **OpAmps**, which is also presented in Section 4.3.

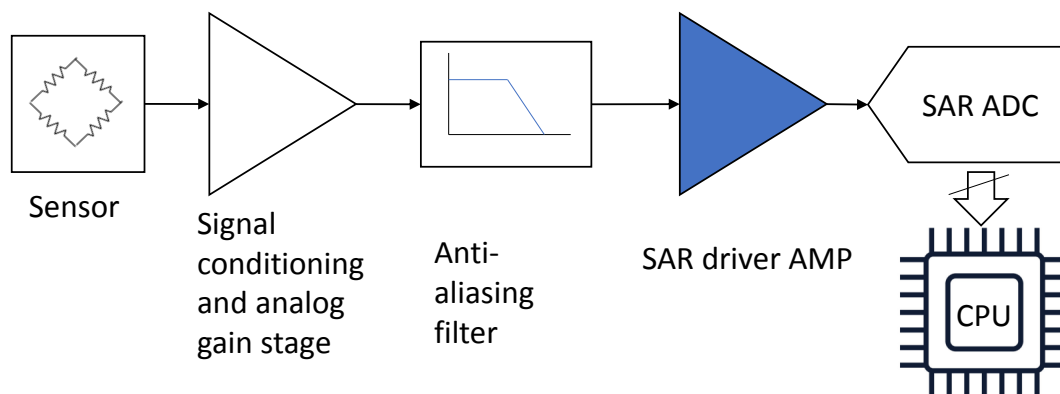


Figure 4.1: Possible AFE employing a SAR ADC.

Two directions can be taken to improve the dependability of the OpAmp. All of them are explained in Sections 4.4 and 4.5. Comparisons between these directions and conclusions are provided in Section 4.6.

4.2 The Test Vehicle OpAmp

Automotive electronics has achieved a big success in recent years. In 2030, 50% of all costs for a car will be spend on electronics [Raj18]. Now more and more sensors are integrated into cars. These sensors capture temperatures, pressures, flows or lights and convert them into the digital domain via AFEs. The AFE normally comprises of a signal conditioning stage, a (programmable) analogue gain stage, an anti-aliasing filter, an ADC driver amplifier, and a 10- to 16-bits ADC.

Figure 4.1 shows the typical signal route for a Successive-Approximation Register (SAR) ADC-based AFE. The signal conditioning stage provides the required sensor-biasing and level-shifting. The purpose of the analogue gain stage in the signal path is to match the voltage output range of the sensor to the input range of the SAR ADC. By using this method, full advantage of the possible number of bits in the ADC can be taken, which is 10- to 16-bits. The anti-aliasing filter follows the analogue gain stage. It is normally a third-to-fifth order analogue filter and removes high frequency noise before the signal reaches the SAR ADC. The driver amplifier buffers the signal. This driver amplifier provides a stable signal to the ADC with ample driving capability. Once the SAR ADC derives a final digital word, the embedded microcontroller or microprocessor further filters the signal or translates that signal to a usable digital value. The SAR ADC is frequently the architecture of choice for medium-resolution applications [Bak12].

The availability of a test-vehicle **OpAmp** design was the first step towards our reliability simulations. However, we have spend an unexpectedly long time in order to find an analogue test-vehicle circuit design in an advanced nanometer **CMOS** technology. Industrial companies prefer to provide the black box version of their design. However, in order to carry out **NBTI** simulations, full details of the schematics at transistor level are required, which are treated as (highly) confidential for industrial companies. This issue forced us finally to give up the search for industrial partners and as a consequence design the test-vehicle circuit ourselves and offer it for free to the analogue design community.

4.2.1 **OpAmp** Challenges in 65nm Low-Power **CMOS** Technology

The test-vehicle **OpAmp** has been targeted for the driver amplifier for the **ADC** range from 10- to 24-bits in automotive (sensor) **AFEs**. The sample rate of the **ADC** can vary from 100K samples-per-second for a 24-bits **ADC**, to 50M samples-per-second for a 10-bits **ADC**. The **OpAmp** to be designed targeted to satisfy both high-accuracy and high-speed requirements.

The **DC** gain (G_{DC}) of the test-vehicle **OpAmp** is determined by the accuracy of the **ADC** used. A general requirement is that the driver **OpAmp** should introduce no more than $LSB/2$ error into the **ADC**. For an **OpAmp** configured into a unit gain driver (a buffer), this can be translated into the **DC** gain requirement for the **OpAmp** by Eq. (4.1), in which N is the number of bits for the **ADC**. Assume the **ADC** to be employed is 24-bits. Then the **DC** gain of the **OpAmp** should be better than 150dB. However, normal 24-bits **ADCs** do not need such high gain **OpAmp** because not all 24 bits are useful. The lowest few bits of the **ADC** are concerned with noise. Nowadays, a 24-bits **ADC** can achieve around 17- to 19-bits **Effective-Number-of-Bits** (**ENOB**), and therefore the **DC** gain requirement of the **OpAmp** can be relaxed to be better than 100dB [Pel13].

$$G_{DC} = 6 * (N + 1) \text{ dB} \quad (4.1)$$

The unity-gain frequency (f_T) of the **OpAmp** is sometimes also referred to as unity-gain bandwidth. It is the frequency where the gain of the **OpAmp** is reduced to one. For a one-pole frequency response **OpAmp**, the unity-gain frequency is equal to the gain–bandwidth product. The frequency f_T is determined by the settling-time requirement of the **ADC**. The most critical settling-time requirement will come from high-speed **ADCs**. For example, a 50MHz 12-bits **ADC** demands the driver **OpAmp** to settle down the signal within its sampling time, which

should be less than a half-clock cycle ($10ns$). The fractional error of the settled-down signal should be less than $LSB/2$. Assuming the OpAmp has a first order step-response, then the required f_T of the OpAmp can be expressed by Eq. (4.2). The parameters N and $t_{sampling}$ in Eq. (4.2) are the number of bits and the sampling time of the ADC. The example 50MHz 12-bits ADC will require a unity-gain frequency of more than 143MHz for the OpAmp.

$$f_T = \frac{\ln(2^{N+1})}{2\pi \cdot t_{sampling}} \quad (4.2)$$

The technology employed for our circuit design is 65nm low-power TSMC CMOS technology. This technology is optimized for low-power digital applications, not for high-performance analogue designs. The transistor intrinsic gain is only about $20dB$ and the intrinsic frequency is around 3GHz [Per12]. This means one gain stage can only achieve $20dB$ gain. To achieve $100dB$ gain, the OpAmp needs at least 5 gain stages. If these 5 gain stages are in series, several Miller or other compensation circuits are required in order to achieve a 60 degrees phase margin to guarantee both stability and fast settling-time [Sto76]. The f_T of the 5-stage OpAmp will be limited to 37MHz as calculated by Eq. (4.3) [DL13]. The parameter n in Eq. (4.3) is the number of series gain stages. The parameter f_{Tn} is the final OpAmp unity-gain frequency in such a configuration. The calculation is approximate and optimistic and can be much worse in a real circuit.

$$f_{Tn} = \frac{f_T}{3^{n-1}} \quad (4.3)$$

One solution to obtain a wider bandwidth is using parallel feed-forward links [Tha03]. However, the main problem for using parallel links is the matching of poles and zeros of gain stages to create a smooth $-20dB/dec$ gain versus frequency dependence without pole-zero doublets [Iva04]. If this is not achieved, the step response of the OpAmp will have a longer settling-time [Kam74].

In this thesis, we use multiple gain-boosting methods to achieve both high gain and high bandwidth for the test-vehicle OpAmp. Gain-boosting techniques are widely used in OpAmp designs [DL13]. Unlike series gain stages, the main benefit for gain-boosting is that it increases the gain of an amplifier without reducing its unity-gain frequency too much. Two classical gain-boosting methods are shown in Figure 4.2, which illustrates the gain-boosting function. The original amplifier shown in Figure 4.2(a) can provide $20dB$ gain with a 65nm NMOST. A cascode NMOST is added in Figure 4.2(b) as one gain-boosting method and the total gain

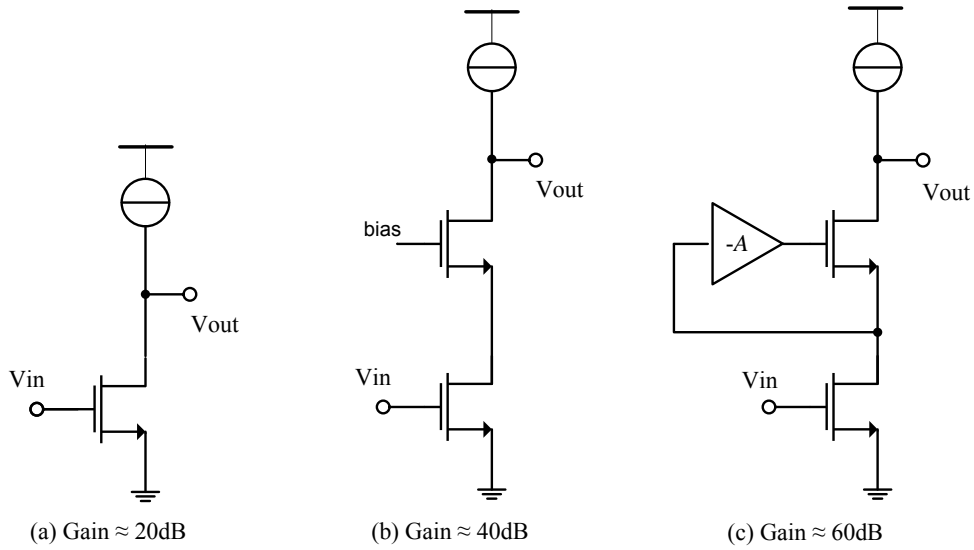


Figure 4.2: The commonly used gain-boosting methods.

of the amplifier will be boosted to 40dB. The active cascode circuit shown in Figure 4.2(c) [Bul91] can be used as another gain-boosting method. The total gain of the amplifier in Figure 4.2(c) can be boosted to $(40 + A)$ dB, in which A is the gain of the loop amplifier in Figure 4.2(c). The loop amplifier is normally implemented by a single gain stage. So the total gain of the gain-boosted amplifier will be around 60dB.

Now we have accomplished 60dB gain by using the two gain-boosting techniques mentioned above. Another 15 ~ 20dB gain can be obtained from a class-AB output stage. There are still 20dB missing to realize an OpAmp with 100dB gain. It could be realized by an additional gain stage which is inserted between the main gain-boosting stage and the class-AB output stage. The resulting OpAmp will have three gain stages with an f_T of about 300MHz. However, the 300MHz bandwidth is a really optimistic estimation. In the real circuit, especially after Process, Voltage and Temperature (PVT) variation check and after layout parasitic extraction, the speed of the circuit can be reduced by half easily. The resulting OpAmp in the three-stage version will marginally satisfy the 143MHz unity-gain frequency requirement. In addition, the extra gain stage and frequency compensation networks which are required by the three-stage OpAmp will increase the complexity of the circuit. The additional gain stage will also increase the power consumption. Additional capacitors inside the frequency compensation networks will occupy more area and thus increase the cost.

Another option which is implemented in this thesis is further boosting of the gain of the first stage. If the first gain stage can be boosted to over $80dB$ gain, the OpAmp will only require two stages. The two-stage OpAmp will achieve a much wider bandwidth (upto 1GHz) as compared to the three-stage OpAmp (300MHz). The frequency compensation in a two-stage OpAmp is also much simpler than a three-stage OpAmp, and hence the power and area consumption can be reduced.

However repeating the same gain-boosting techniques as shown in Figure 4.2 is not a good approach. For example, adding another cascode transistor in Figure 4.2(b) will cause signal-swing problems. Since the power supply in 65nm CMOS is 1.2V, while the threshold voltage for a 65nm MOST is over 400mV, the circuit design needs to obey low-voltage design rules which are described below:

- Limit the stack of transistors between power and ground to less than one gate-source voltage plus two drain-source voltages: $(V_{gs} + 2V_{ds})$.
- Limit the stack of transistors between power and ground to less than four drain-source voltages: $(4V_{ds})$.

Double cascode transistors in Figure 4.2 (b) will result in the circuit shown in Figure 4.3(a), in which the ideal current source is replaced by real transistors and the same gain-boosting has to be used for the current source as well [Gra09]. This configuration stacks six drain-source voltages ($6V_{ds}$) and therefore violates the rule of less than $4V_{ds}$.

Similarly, repeating the same active cascode boosting technique like in Figure 4.3(b) [Bul91] will cause stability problems, and hence require frequency compensations. The overall effect will reduce the bandwidth of the OpAmp to the same amount of bandwidth as the three-stage OpAmp. Therefore, combining different gain-boosting techniques which use single-stage in each gain-boosting loop is the best choice to accomplish both high gain and high bandwidth for the test-vehicle OpAmp. As a result, a new gain-boosting technique which is different from the techniques shown in Figure 4.2(b) and (c) has to be found.

4.2.2 New Gain-boosting Technique for High Gain, High Bandwidth OpAmps

The new gain-boosting method proposed by us is shown in Figure 4.4. The gate voltages of NMOSTs N1 and N2 are both controlled by the input signal V_{in} . The gate voltages of PMOSTs

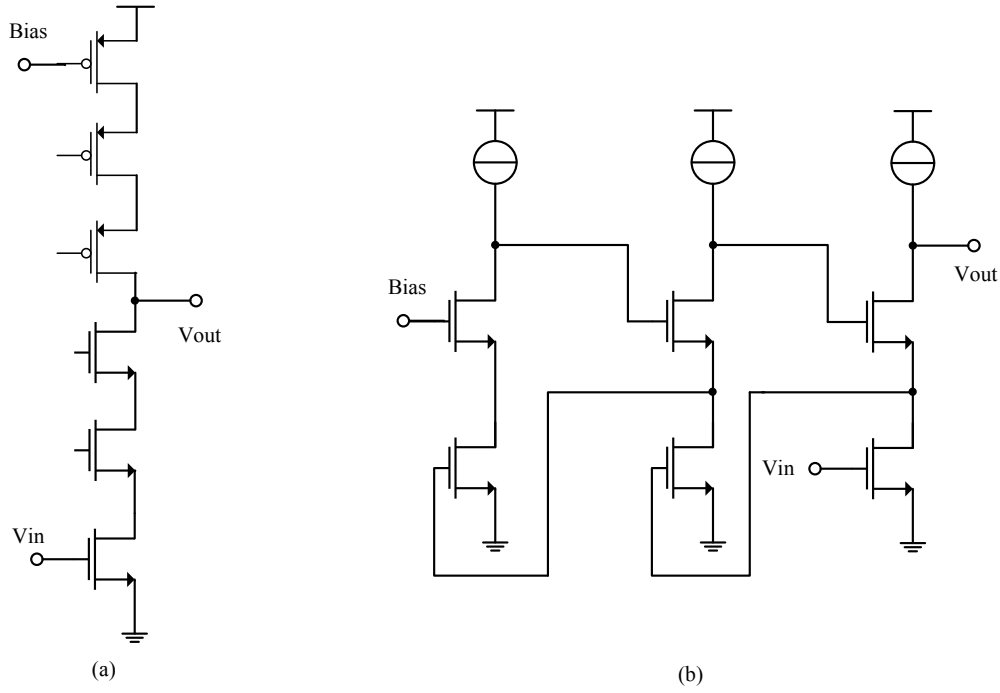


Figure 4.3: The problem and solution of repeating the previous boosting technique.

P1 and P2 are controlled by the gain-boosting feedback amplifier. The configuration seems similar to the current mirror with improved output impedance [Iva04]. However, the theory of operation behind them is totally different.

The gain-boosting operation can be explained as follows. The output impedance can be evaluated by measuring the small-signal current at the output while shifting the output voltage. For example, in Figure 4.4, assume at the DC operation point, no current flows into the output node. The output voltage at this time is V_{out} . Next, shift the output voltage from V_{out} to $V_{out} + \Delta V$. The extra current flow into the output ΔI , together with the output-voltage change ΔV , can be used to evaluate the output impedance R_{out} from Eq. (4.4). The larger the current ΔI , the smaller the output impedance. As can be seen from Eq. (4.5), the gain of the circuit is proportional to the output impedance. The parameter g_m is the transconductance of the NMOST. If one can reduce the current ΔI , the gain G can be boosted.

$$R_{out} = \frac{\Delta V}{\Delta I} \quad (4.4)$$

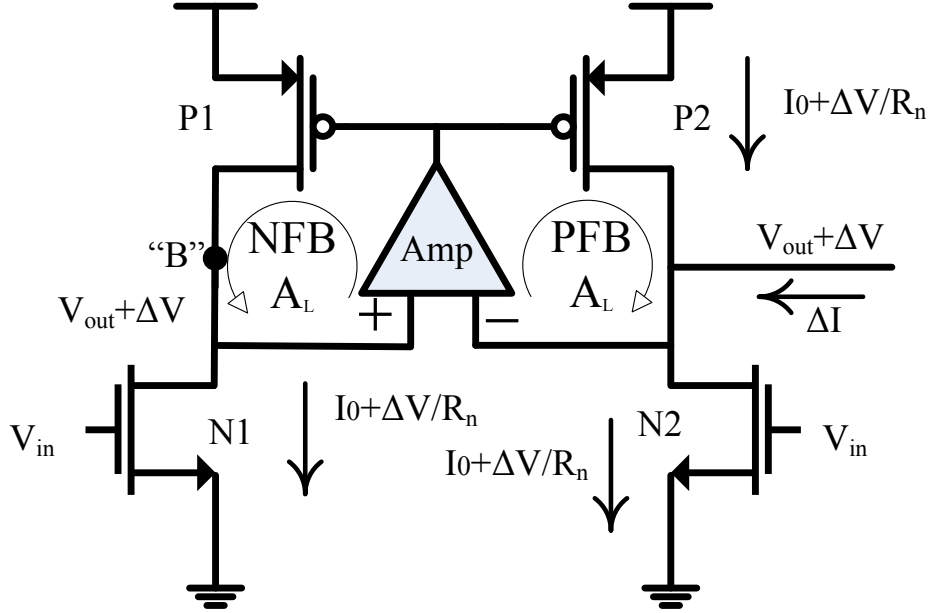


Figure 4.4: Our new gain-boosting method.

$$G = g_m \cdot R_{out} = g_m \cdot \frac{\Delta V}{\Delta I} \quad (4.5)$$

In Figure 4.4, the voltage at node “B” is set to be equal to the output V_{out} by the positive and negative feedback-loop (PFB/NFB). If the output voltage is shifted from V_{out} to $V_{out} + \Delta V$, the voltage at node “B” is also shifted to $V_{out} + \Delta V$. The current of each MOST in this situation is shown in Figure 4.4. The current I_0 is the quiescent current if the output voltage is at its DC operation point V_{out} , which is determined by the input signal. The parameter R_n is the drain-to-source resistance of the NMOSTs. Since the drain voltage of N2 is increased by ΔV , the drain current of N2 will be changed to $I_0 + \frac{\Delta V}{R_n}$. The transistors N1 and N2 are matched, and hence their drain currents are equal because of the same gate and drain voltages. The current mirror and feedback loop copy the drain current of N1 into P2. Therefore the drain current of P2 is the same as the drain current of N1, which is $I_0 + \frac{\Delta V}{R_n}$. Using Kirchhoffs’ current law, the total output current is zero as shown by Eq. (4.6).

$$\Delta I = I_{out} = \left(I_0 + \frac{\Delta V}{R_n}\right) - \left(I_0 + \frac{\Delta V}{R_n}\right) = 0 \quad (4.6)$$

By substitution of Eq. (4.6) into Eq. (4.5), the gain of the circuit in Figure 4.4 would be infinite! However, this is an ideal case which is difficult to achieve due to the finite match of transistors and limited gain of the feedback-loop amplifier.

The voltage amplifier Amp in Figure 4.4 is used to provide feedback. Since the feedback-loop gain cannot be infinite in reality, the voltage at node “B” is close to the output but not exactly equal. There is still some remaining error (V_A) which can be expressed by Eq. (4.7).

$$V_A = V_{out} + \Delta V \cdot \frac{A_L}{1 + A_L} \quad (4.7)$$

A_L is the loop gain as shown in Figure 4.4. The actual output impedance R_{out} and voltage gain G will be:

$$R_{out} = \frac{\Delta V}{\Delta I} = (1 + A_L) \cdot R_n \quad (4.8)$$

$$G = g_m \cdot R_{out} = (1 + A_L) \cdot g_m R_n \quad (4.9)$$

In Eq. (4.9), $g_m R_n$ is the original gain of a NMOST. The new gain is boosted to $(1 + A_L)$ times the original gain, which is similar to other gain-boosting methods.

The new gain-boosting method shown in Figure 4.4 is suitable for differential inputs/single-end output OpAmps since the gates of N1 and N2 can be connected to differential input signals. However, the circuits connected into the two branches of the current mirror have to be matched. For example NMOSTs N1 and N2 in Figure 4.4 have to be of the same size. Otherwise it will degrade into a normal amplifier with a improved current mirror as load. The improved current mirror can only improve the P2 output impedance but provides no improvement for N2. As a result it can not boost the gain.

Ivanov [Iva04] and Kim [Kim10] use a similar current mirror but their circuit cannot boost the gain because of the reason we just described. Kim claims that the Positive-Feedback (PFB) in the current mirror is used to boost the gain [Kim10]. However, that is not correct. The gain in [Kim10] is actually been boosted by the double cascode NMOSTs in the active cascode loop.

Actually due to the special matching requirements, the feedback amplifier in Figure 4.4 is preferably realized with a differential pair. An additional common-mode control circuit is usually required since this differential pair will remove the common-mode output voltage of the original amplifier. This aspect will be shown in the next section.

For a fully differential OpAmp, we have proposed another similar gain-boosting solution which has been published in [Wan11] and will be explained in the next section.

4.2.3 A 100dB Gain, 700MHz Unity-gain Bandwidth OpAmp in 65nm CMOS Technology

The test-vehicle OpAmp has been designed in 65nm low-power digital CMOS technology. The schematic is shown in Figure 4.5. The design applies a constant- g_m rail-to-rail input stage with folding-cascode and a class-AB rail-to-rail output stage which uses folding mesh summation [De 98]. There are three gain-boosting techniques employed in the first stage. They are the folding cascode, the active cascode and the new gain-boosting techniques proposed in the last section.

The folding-cascode circuit uses transistor groups “MN5-MN6-MN7”, “MP8-MP9-MP10”, “MN16-MN17-MN18” and “MP19-MP20-MP21”. Each group has three transistors because of the folding-mesh requirements [De 98].

Active-cascode transistors are used to further increase the gain, which are realized by five transistor groups “MP7-MN4”, “MP13-MN8”, “MN11-MP11”, “MP17-MN15”, “MP23-MN19” and “MN12-MP18”.

After these two gain-boosting stages, the gain of the first stage can accomplish about 70dB amplification. Finally, the new gain-boosting technique is employed by using the amplifiers “Gm_p” and “Gm_n”. The actual circuit of these two amplifiers are shown in Figure 4.6. They use the two Flipped-Voltage-Follower (FVF) differential amplifiers technique to increase their input range [Car05].

While using the new gain-boosting technique, the common-mode voltage of the output has to be controlled. The common-mode control circuits are realized by “MN3-MP3-MP4-MP5-MP7” with current addition. Now the gain can be boosted to more than 85dB. The class-AB output stage provides another 15dB gain. Therefore the total gain of the OpAmp is larger than 100dB.



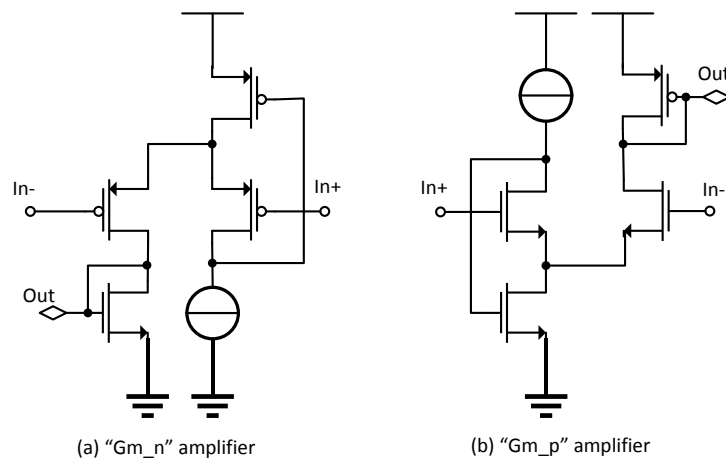


Figure 4.6: The "Gm_p" and "Gm_n" amplifier transistor schemes as used in Figure 4.5

4.2.4 OpAmp Performance Simulation Results without Aging

The simulated open-loop gain and unity-gain frequency of the test-vehicle OpAmp is shown in Figure 4.7. The simulation has been carried out by using Cadence Spectre. The open-loop gain is close to $104dB$ and the unity-gain frequency is around $780MHz$. The average offset of the OpAmp is less than $1mV$ resulting from Monte-Carlo simulations. The current consumption is about $620\mu A$ at $1.2V$ power supply.

4.3 Reliability Issues of the Test Vehicle OpAmp

The dominating ageing effect in $65nm$ is NBTI. By using the Cadence RelXpert software with AgeMOS models, the NBTI effects on the circuit have been examined.

4.3.1 Reliability Simulation Conditions for Test Vehicle OpAmp

Three situations have been simulated with Cadence RelXpert and Spectre simulation tools. All cases followed the same procedure: first simulate the fresh circuit performance at $27^{\circ}C$ using Spectre, and then start ageing at $150^{\circ}C$ for 20 years by RelXpert. Finally, simulate the aged circuit performance at $27^{\circ}C$ with Spectre again.

In the first case, a $1\mu V$ @ $1MHz$ differential input signal with $0.6V$ common mode was applied to the input of the OpAmp, which emulates the normal operational situation in feedback loops. In the second case, a $0.6V$ @ $1MHz$ differential input signal with $0.6V$ common mode

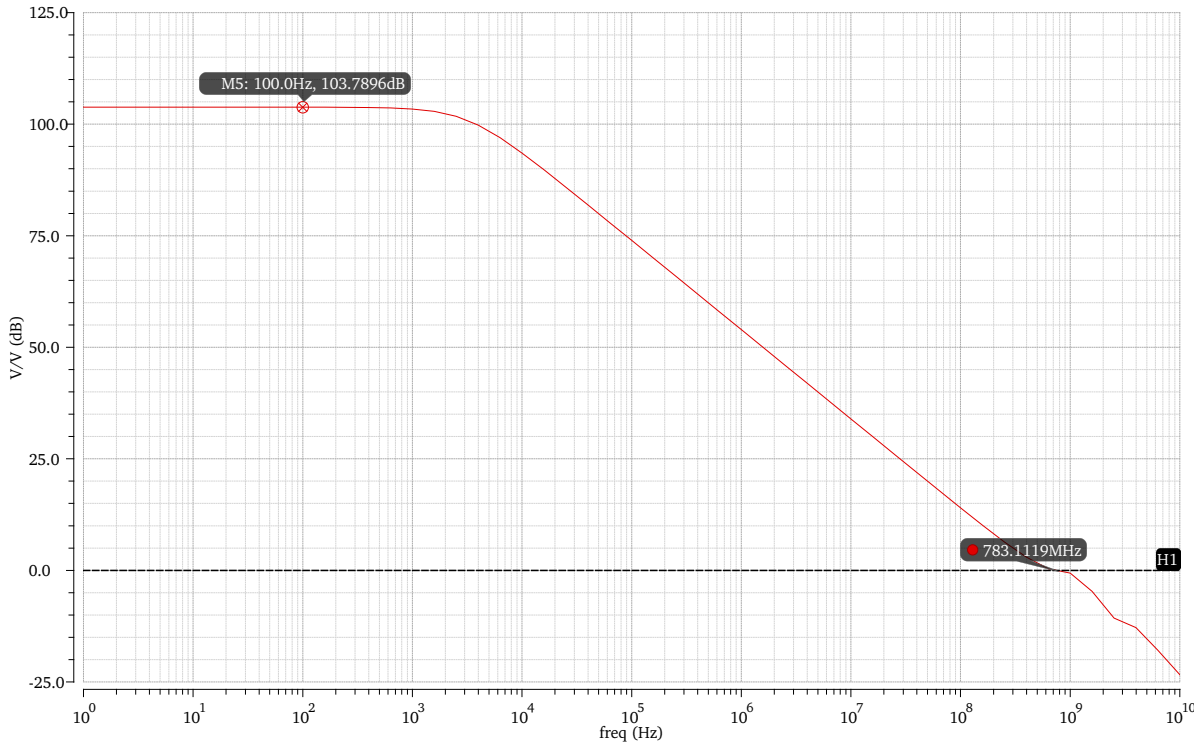


Figure 4.7: The simulated open-loop gain for the test-vehicle **OpAmp** in Cadence Spectre.

Table 4.1: Test vehicle **OpAmp** ageing performance.

Ageing situations	Gain	Unity-gain bandwidth	Offset
Fresh	104dB	783MHz	1mV
Ageing case 1	103dB	783MHz	1mV
Ageing case 2	102dB	783MHz	1mV
Ageing case 3	103dB	783MHz	17mV

(rail-to-rail input) was used as the input, which emulates the overdrive situation. In the third case, a **DC** input with one 1.2V and the other 0V was applied, which represents an extreme ageing situation by V_{dd} stress.

4.3.2 **OpAmp** Performance Degradation with Ageing

The **NBTI** ageing simulation results are shown in Table 4.1. From Table 4.1, it seems the gain and unity-gain frequency are insensitive to **NBTI** ageing under all ageing cases. This could be caused by current bias and matching. Since all bias voltages are generated by current mirrors from the same reference current source, and the AgeMOS model reports the same threshold

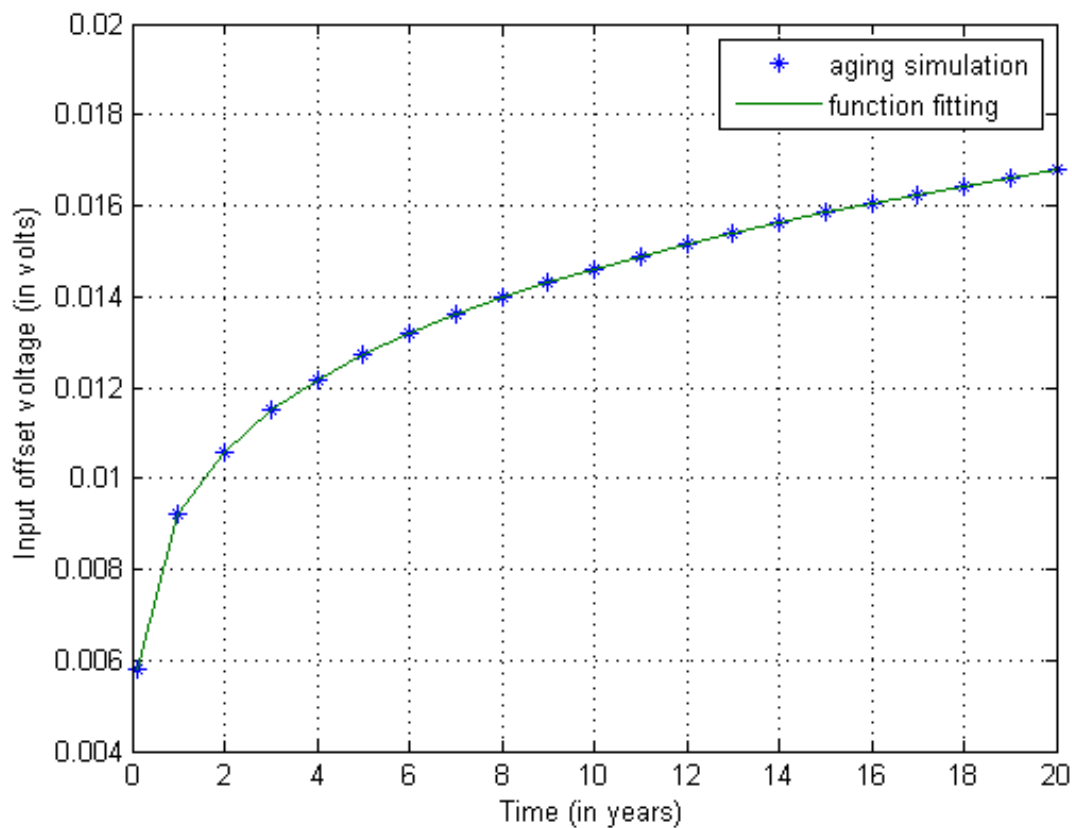


Figure 4.8: The simulation result of input offset for the aging test-vehicle OpAmp in Cadence Spectre.

voltage shift for the same gate-to-source voltage stress, the currents within the OpAmp hardly changed. As a result, the gain and frequency of the OpAmp, which are most sensitive to bias currents, are not changing.

However in the extreme ageing case (case 3), the offset increases from $1mV$ to $17mV$. This ageing is due to the OpAmp stressed in an unbalanced condition. The unsymmetrical operational condition of the two branches in the differential OpAmp makes the ageing also unsymmetrical. In theory, the threshold voltage changes in the two input differential transistors are different. This causes a differential offset voltage shown at the OpAmp input.

A further detailed simulation in ageing case 3 for the offset is shown in Figure 4.8. The offset ageing follows a logarithmic-like behaviour. After the first two years the offset reaches $10mV$. In the remaining 18 years, the offset increases slowly and gradually reaches to about $17mV$ at 20 years.

4.3.3 Reliability Issues for a General OpAmp

For a general OpAmp with differential pairs and tail current sources, the NBTI ageing influences mostly the offset performance. The ageing occurs in the case the OpAmp is operated under unsymmetrical stress. And the most sensitive transistors are the ones in the input differential pairs.

The gain and unity-gain frequency of normal OpAmps are hardly changed by NBTI, because OpAmps usually have tail current sources in their differential input pairs. The tail current source keeps the current of the OpAmp constant and they are usually used in feedback mode.

However, there is one group of OpAmps whose gain and unity-gain frequency are sensitive to NBTI ageing. It is the pseudo-differential OpAmp and is widely used in low-voltage designs. The difference between the pseudo-differential OpAmp and the normal OpAmp is that the pseudo-differential OpAmp has no tail current source for its input differential pair. Instead, the source terminal of the input differential pair transistors are connected to the ground/power supply directly. Therefore the pseudo-differential OpAmp is voltage biased and its gain is sensitive to the increase of the threshold voltage. The gain and unity-gain frequency can be reduced more than 10% by NBTI.

4.4 Highly Dependable OpAmp via Reliability-aware Designs

A highly dependable OpAmp means the OpAmp is able to keep within the accepted performance tolerance under reliability ageing mechanisms like NBTI. It can follow two directions. The first direction is to invest extra design effort to design an OpAmp which is insensitive to ageing. For example, the classical offset removing techniques, like auto-zero and chopper-stabilizer, can be used to remove ageing-induced offset too. A self-calibration method can also be introduced into the OpAmp and the resulting OpAmp can self-calibrate its ageing sensitive parameters like offsets.

The second direction is to employ EIs. The EIs are primarily used during product tests to reduce test costs. If they are there they can also be used as ageing monitors during the life time of the OpAmp as well. In addition, EIs can also be shared by more IPs in a chip and do not need to be changed for each OpAmp design. The EI direction will be discussed in more detail in the next section.

The design tricks for removing offsets, like auto zero and chopper stabilization, can be used to remove ageing-induced offset as well. These techniques have been very well described

in many publications and will not be addressed in this thesis. However, they are normally used in discrete time applications which require a high-frequency clock signal and operate in switching mode. For continuous-time operation, the self-calibration approach is more preferable. Although the self-calibration method also requires to stop the OpAmp and calibrate its offset, the calibration period can be much longer than auto zero and chopper stabilization techniques.

In this section, a self-calibrating OpAmp will be shown based on our previous test-vehicle OpAmp design. It uses a self-calibrating circuit which results in a highly dependable OpAmp.

The new OpAmp configuration is shown in Figure 4.9. It uses a digitally controllable voltage attenuator together with the OpAmp to form a Positive-Feedback system. By controlling the 4-bits voltage attenuator, one can control the positive feedback loop gain [He07]. In the case the loop gain is larger than 1, the whole system becomes unstable and will enter the bi-furcation state [He07]. By checking whether the system enters this bi-furcation state, it can be determined whether the loop gain is larger or smaller than 1. In the case the loop gain is equal to 1, the gain of the OpAmp can be calculated as the reciprocal number of the attenuation.

The offset of the OpAmp can be detected by a trial-and-see scheme, because the bi-furcation state also gives information on whether the offset is saturating the OpAmp or not [He07]. There is an offset compensation current source (DAC) at the input of the OpAmp. By tuning the calibration current source, which is inside the 12-bits offset compensation block, the offset of the OpAmp can be cancelled. The digital logic part in Figure 4.9 is designed to provide controllability at system level and a self-control operation to enable a self-calibrating OpAmp.

Two potential issues have to be solved in order to determine the offset of the OpAmp. The first one is the accuracy of the offset. Since the OpAmp gain can be more than $80dB$, the input offset is preferred to be smaller than $10\mu V$ to avoid saturation. In [He07], a 16-bits DAC is used for offset compensation. In our OpAmp design, a 12-bits offset compensation current source has been designed, which is able to compensate the offset below $40mV$ with a $9\mu V$ minimum step. The second issue is noise. The preferred input noise amplitude should also be smaller than $10\mu V$. In the design, the last stage in the attenuator is designed to have the largest voltage attenuation ratio, which minimizes the OpAmp input noise amplitude.

Another point of attention is that the self-calibration requires switches to be added in series with the OpAmp inputs. This series switches can introduce extra noise into the system. While performing self-calibration, the OpAmp has to be isolated from its connection network. During

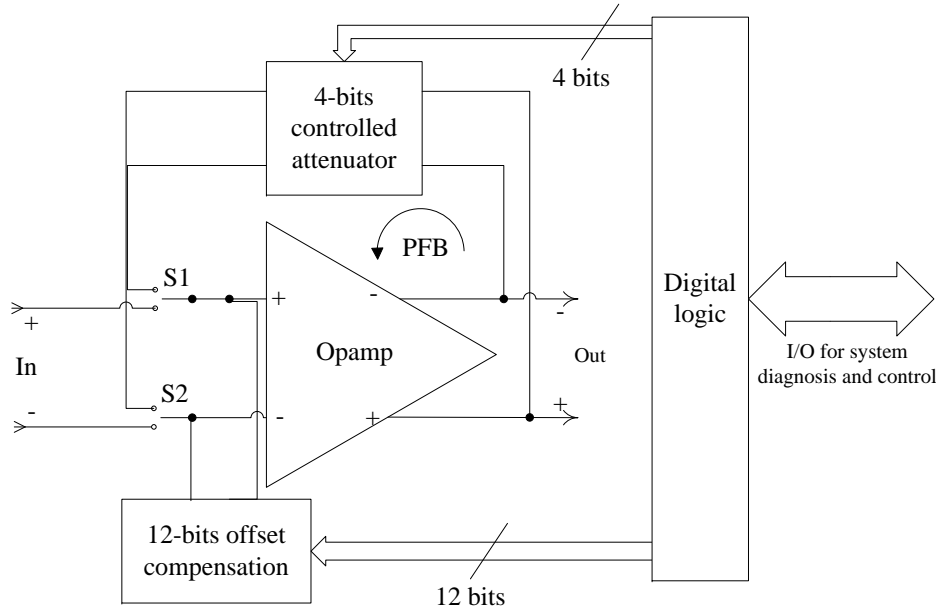


Figure 4.9: The designed self-calibrating OpAmp. PFB is the abbreviation of Positive-Feedback.

the calibration time, the OpAmp is not available for system operation. Simulation results are similar to [He07].

4.5 Highly Dependable OpAmp via Employing Embedded Instruments

An existing solution for on-chip testing is using the EI concept [Ek106]. It provides on-chip test IPs which are connected via standard buses and protocols (IEEE1687) [Ek106]. These on-chip EIs are supposed to measure basic physical parameters like voltages, currents, temperatures, as well as performance parameters of AMS IPs. The embedded instruments are primarily used during final tests. If incorporated, they can be also used as ageing monitors during the life time of a SoC as well.

In this section, an embedded offset and gain instrument for OpAmps is proposed. It can measure the gain and offset of an OpAmp online without isolating it from surrounding feedback networks as well as connected IPs. No accurate stimulation sources are required either. It provides a self-calibration method to remove the resident offsets as well as ageing-induced offsets inside the EI.

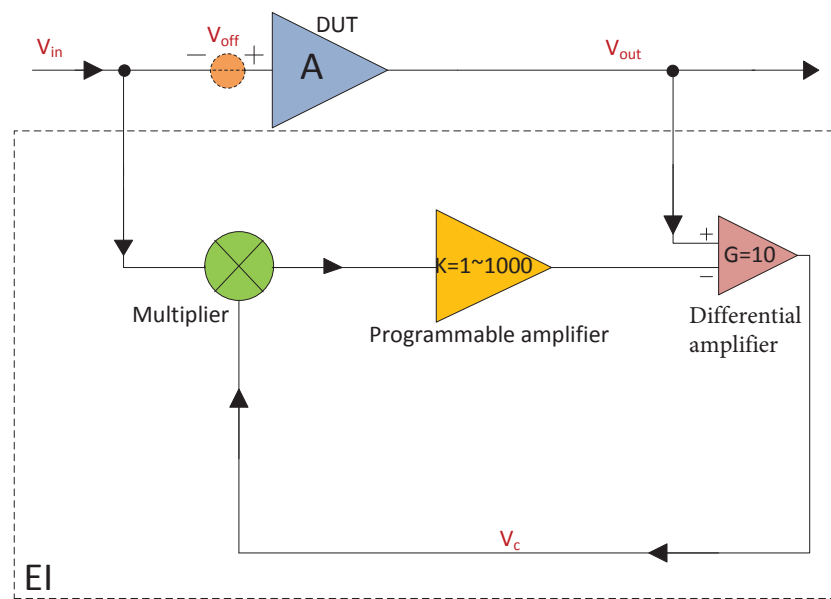


Figure 4.10: Block diagram of the new EI for offset and gain measurements.

4.5.1 Offset Measurements and Self-Calibration Issues

The exact offset value of an OpAmp can be measured by the unity-gain feedback-loop method [Bry11] or calibration-source methods [Arb12]. These methods are either configuring the OpAmp into a unity-gain feedback system, or applying extra stimulation sources to the OpAmp and measuring its output. They are both invasive and require isolating the OpAmp from surrounding feedback networks. Hence a requirement exists to add switches into the original signal paths, which is not preferred by designers considering their noise and mismatch influences. In addition, they will either require an accurate ADC or an accurate stimulation source as the key element, which increases both the complexity and difficulty of the EI design. Self-calibrations to maintain the accuracy of the ADC or the stimulation source add an extra problem as well. To overcome the above issues, a new offset EI theory is proposed.

4.5.2 The New Offset EI Theory

The basic idea is simple. The real output of a Device Under Test (DUT) (Figure 4.10) has an offset. If the ideal output without any offset can be generated, the offset voltage can be measured by comparing these two output signals. This ideal output signal without offset seems difficult to generate. However, with the block diagram shown in Figure 4.10, the goal is achieved in a simple and successful way.

Figure 4.10 shows the DUT OpAmp with an input offset voltage V_{off} . The output of the DUT is compared with a signal from a gain-controlled amplifier. This amplifier has the same

input as the DUT. Its gain is controlled by both the digitally programmed number K and the compared result V_c . The analogue multiplier in Figure 4.10 is introduced to realize such a gain-control mechanism.

From Figure 4.10, V_c can be expressed as Eq. (4.10) and simplified to Eq. (4.11).

$$V_c = (V_{in} + V_{off}) \cdot A \cdot G - V_{in} \cdot V_c \cdot K \cdot G \quad (4.10)$$

$$V_c = \frac{(V_{in} + V_{off}) \cdot A \cdot G}{1 + V_{in} \cdot K \cdot G} \quad (4.11)$$

In Eq. (4.11), V_{in} is the original input signal of the DUT. It means that the DUT can be online while carrying out measurements. V_{off} is the DUT input offset voltage, which is to be measured. The parameter A is the gain of the DUT. G and K are gains of the comparison gain stage and the digitally programmable amplifier in the EI respectively. With different program settings, K can be changed from 1 to 1000. The output signal V_c comes from the comparison-gain stage. All these symbols are shown in Figure 4.10 at their respective locations.

As shown by Eq. (4.11), V_c depends on the input signal V_{in} in most cases. However, there is a special K value for which V_c is independent on the DUT input signal V_{in} . This special K value K_{spc} can be expressed in Eq. (4.12):

$$K_{spc} = \frac{1}{V_{off} \cdot G} \quad (4.12)$$

Substitution of Eq. (4.12) into Eq. (4.11) results for V_c in this situation:

$$V_c|_{K=K_{spc}} = V_{off} \cdot A \cdot G \quad (4.13)$$

So finding this K_{spc} is very important to obtain the offset and gain values. Basically, there is a feedback loop in the EI which includes the multiplier, the programmable amplifier K and the comparator G . The input signal V_{in} controls the loop gain. If the value of $V_{in} \cdot K \cdot G$ approaches -1 , V_c will be driven to either positive infinity or negative infinity (limited by supply rails), depending on which direction the value of $V_{in} \cdot K \cdot G$ approaches -1 . For example, if K is larger than K_{spc} , it can be expressed as Eq. (4.14).

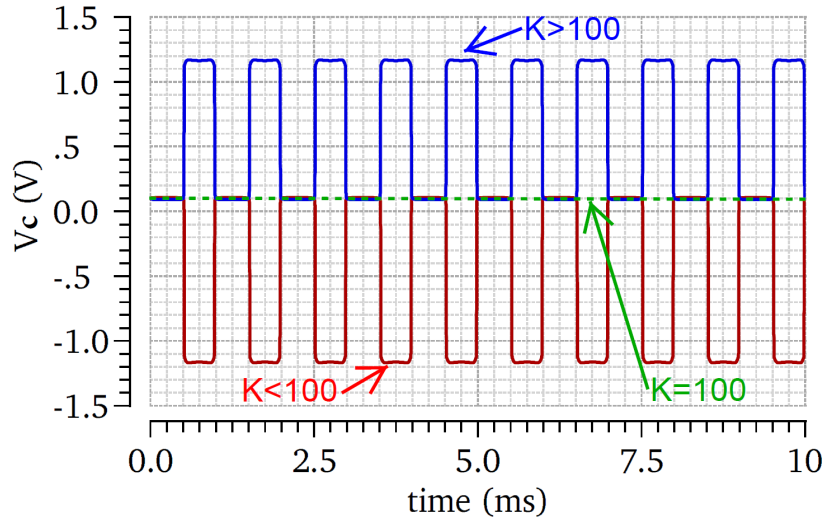


Figure 4.11: The simulation for V_c vs. time for two adjacent programmable K values.

$$K = \frac{1}{(V_{off} - \Delta) \cdot G} \quad (4.14)$$

In Eq. (4.14), Δ is a positive value which is smaller than V_{off} to make sure that the sign of K is not changed. Substitution of Eq. (4.14) into Eq. (4.11) results in:

$$V_c = \frac{(V_{in} + V_{off}) \cdot A \cdot G \cdot (V_{off} - \Delta)}{V_{in} + V_{off} - \Delta} \quad (4.15)$$

In the case V_{in} is approaching:

$$V_{in} = \Delta - V_{off} \quad (4.16)$$

then the denominator of Eq. (4.15) will approach zero while the numerator is still positive. Hence V_c will be driven to positive infinite (limited by the power supply):

$$V_c = \frac{\Delta \cdot A \cdot G \cdot (V_{off} - \Delta)}{0} = +\infty \quad (4.17)$$

Following the same reasoning, it can be concluded that V_c will be driven to negative infinite if K is smaller than K_{spc} . It means that V_c will change dramatically in the case the programmable K value is swept across the K_{spc} value. Figure 4.11 shows this dramatic change in V_c for two adjacent K programmable values if the input is a zero-biased sine wave. The K_{spc} value of 100 shown in Eq. (4.12) is shown in Figure 4.11. It shows that for all K values larger than the K_{spc} , V_c reaches the power-supply top rail (the blue line at 1.2V). While for all K values smaller

than the K_{spc} , V_c reaches the bottom rail (the red line at $-1.2V$ in a full differential system). Now one can find the K_{spc} value with a simple comparator as will be shown in Section 4.5.5. Moreover, it makes a quick binary search possible as well because the V_c result contains the information whether the current K is larger or smaller than the K_{spc} value.

At the moment the value of K_{spc} is found, the offset value V_{off} can be calculated by Eq. (4.12). The G is designed to be 10 in this thesis.

Finally, to obtain the above mentioned dramatic change, the input voltage V_{in} should have an AC component and approach $-V_{off}$ during its variations (like sine wave, square wave and so on). In other words, the input signal of the DUT should have an AC component and the amplitude of the AC component should be larger than its offset. Fortunately, this is the normal case in both functional tests as well as lifetime operations of OpAmps.

4.5.3 Self-Calibration for Resident Offsets

Actually, every component inside the EI has offsets. Moreover, aging effects like NBTI will introduce extra offsets during the lifetime. These offsets are named as resident offsets and can have such a significant influence that it turns the measurement results to be useless. Using an offset minimization technique for each component, such as auto-zero or chopper-stabilization, is possible but too expensive. The same holds for adopting on-chip accurate calibration sources. Here, a simple technique is proposed to accomplish the self-calibration in the digital domain.

Figure 4.12 shows the EI with resident offsets in each component. These offsets can be from non-perfect matching or aging-induced offsets from NBTI. V_{o1} and V_{o3} indicate offsets at the two input ports of the multiplier. V_{o4} stands for the offset at the output of the multiplier in combination with the offset of the programmable amplifier. The offset of the differential amplifier is indicated as V_{o2} . Two “ -1 ” red blocks are inserted into the two inputs paths of the monitor, which indicate phase inversion (multiplying by -1). They are used in the self-calibration procedure and can be easily implemented by switching the sequence of two signal lines in a fully differential system.

If both V_{in} and V_{out} are directly injected into the EI without phase inversion, the expression for K_{spc} in Eq. (4.12) which takes resident offsets into account, can be written as Eq. (4.18).

$$K_{00} = \frac{1}{G \cdot \left(V_{off} - V_{o1} - \frac{V_{o2}}{A} + \frac{V_{o3}}{AG} - \frac{V_{o4}}{A} K_{00} \right)} \quad (4.18)$$

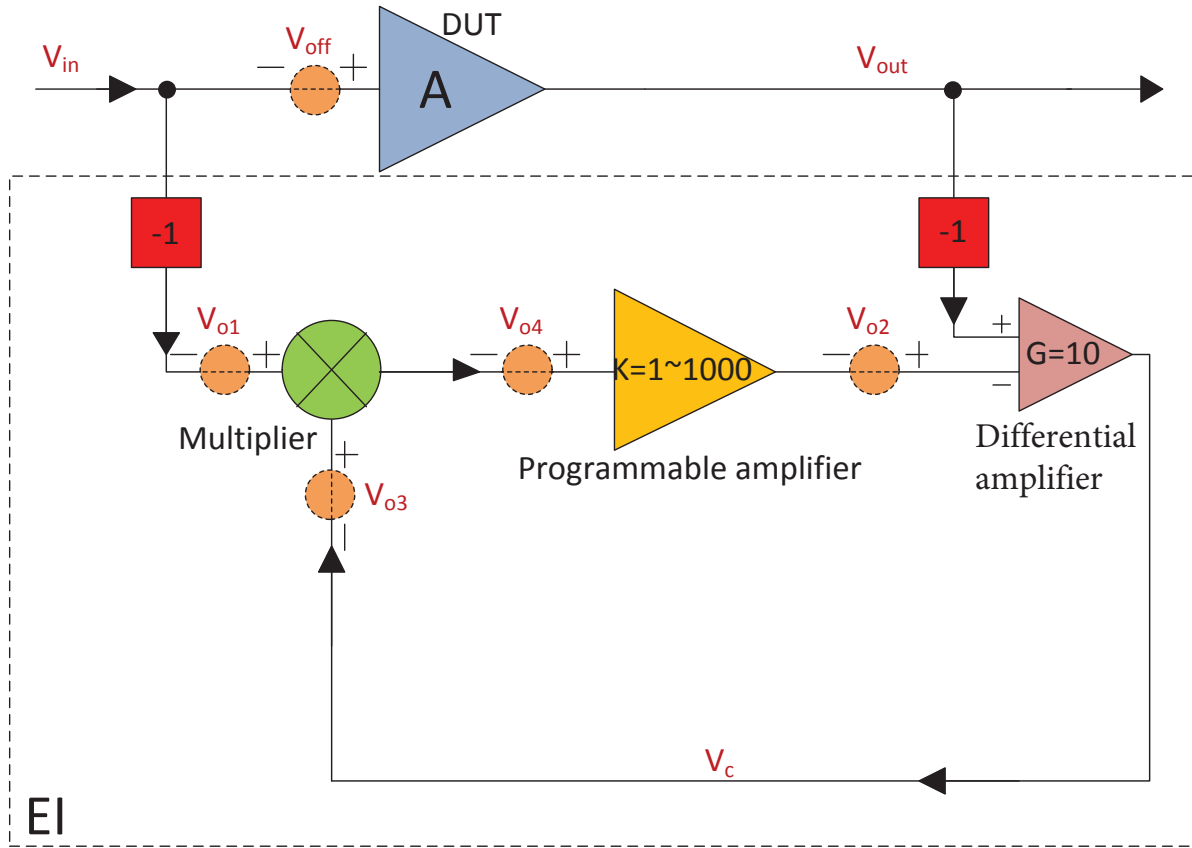


Figure 4.12: Self-calibration for resident offsets inside the EI.

In Eq. (4.18), K_{00} represents the specific K_{spc} value in the case both V_{in} and V_{out} are not inverted. If both V_{in} and V_{out} are inverted, the expression can be derived as Eq. (4.19), in which K_{11} denotes the specific K_{spc} value in the case both V_{in} and V_{out} are inverted.

$$K_{11} = \frac{1}{G \cdot \left(-V_{off} - V_{o1} - \frac{V_{o2}}{A} + \frac{V_{o3}}{A \cdot G} - \frac{V_{o4}}{A} K_{11} \right)} \quad (4.19)$$

In fact, Eq. (4.18) and Eq. (4.19) are both second-order equations of K . Each of them will have two solutions. If these solutions can be written as K_{00a} , K_{00b} , K_{11a} and K_{11b} , their relationships with the DUT gain A and offset V_{off} can be expressed as Eq. (4.20) and Eq. (4.21).

$$A = V_{o4} \cdot G \cdot K_{00a} \cdot K_{00b} = V_{o4} \cdot G \cdot K_{11a} \cdot K_{11b} \quad (4.20)$$

$$V_{off} = \left(\frac{1}{K_{00a}} + \frac{1}{K_{00b}} - \frac{1}{K_{11a}} - \frac{1}{K_{11b}} \right) \cdot \frac{1}{2G} \quad (4.21)$$

In a real circuit, only if V_{o4} is a negative value, the above four solutions K_{00a} , K_{00b} , K_{11a} and K_{11b} are all real numbers and they can be found by scanning the programmable K values as described in Section 4.5.2. As a result, the DUT offset value V_{off} can be obtained by Eq. (4.21).

If V_{o4} has a positive value, those four solutions could be complex numbers and can not be found by just scanning the programmable K values. Extra combinations for phase inversions are required, such as K_{01} , which means only V_{out} is inverted, and K_{10} , which means only V_{in} is inverted. Similar calculations can be made for K_{01} and K_{10} . The DUT offset V_{off} can be obtained by the four solutions for K_{01} and K_{10} as well.

4.5.4 Gain Monitor Theory

The gain A of the DUT is expressed in Eq. (4.20). The only problem to calculate A from Eq. (4.20) is that there is an extra unknown variable V_{o4} . In order to calculate A , one requires another new equation to obtain V_{o4} first. Fortunately, it is not difficult to find such an equation. Just bypass the DUT and connect the second input path of the EI, which used to be connected with V_{out} , to the V_{in} as well. Now it is obvious that the gain of the DUT is equal to one, and Eq. (4.22) can be obtained:

$$V_{o4} = \frac{1}{G \cdot K_{xxa} \cdot K_{xxb}} \quad (4.22)$$

In Eq. (4.22), K_{xxa} and K_{xxb} denote the solutions for K equations in the case of the bypassed DUT configuration. The gain A of the DUT can be calculated by substitution of Eq. (4.22) into Eq. (4.20). The final result for A is presented in Eq. (4.23).

$$A = \frac{K_{00a} \cdot K_{00b}}{K_{xxa} \cdot K_{xxb}} \quad (4.23)$$

4.5.5 System Configuration and Design

In order to verify the proposed theory, a prototype EI has been designed in 65nm low-power CMOS technology. At system level, the selection of G together with the programmable range of K determine the offset/gain measurement range and resolution. In this design, G has been fixed at 10, and K has been programmed as provided by Eq. (4.24).

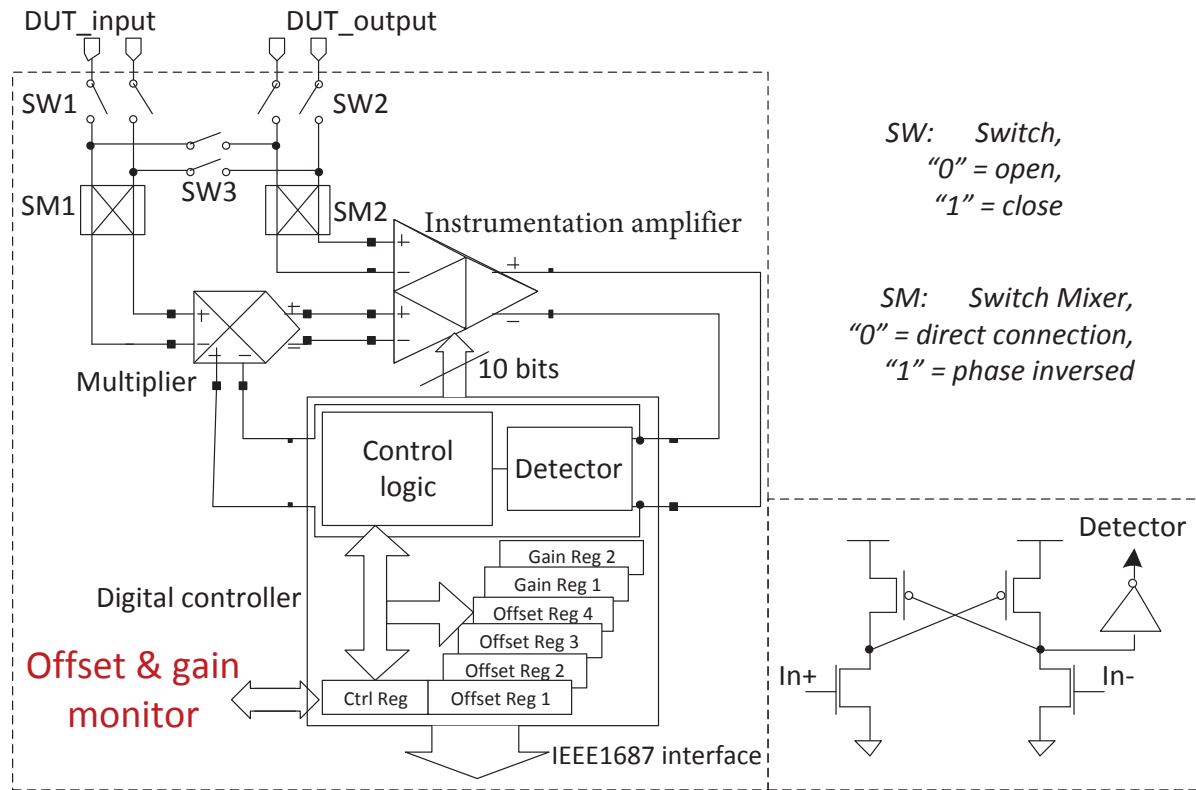


Figure 4.13: System-level architecture of the designed embedded offset and gain embedded instrument as well as the detector used in the EI.

$$K = \frac{1000}{\beta}, \quad \beta = 1 \sim 1000 \quad \text{with stepsize} = 1 \quad (4.24)$$

With these configurations, the theoretical detectable offset range is from $100\mu V$ to $100mV$ with a step-size of $100\mu V$. The detectable gain range is from $0dB$ to $60dB$, which is sufficient for a closed-loop OpAmp (open-loop OpAmp has a much higher gain than $100dB$, but most OpAmps are used in closed-loop in which the overall system gain is less than $60dB$ in most cases). The EI architecture is shown in Figure 4.13. It is a fully differential system. The programmable amplifier is combined with the comparison gain stage. There are 10 bits available to program β from 1 to 1000. The detection circuit for V_c is also depicted in Figure 4.13. It is a voltage-shifter based comparator circuit which is used to determine whether the present K is larger or smaller than K_{spc} . It corresponds to the plot shown in Figure 4.11. The control logic controls the switches $SW1$, $SW2$, and $SW3$, as well as the switch-mixers $SM1$ and $SM2$ which provide the phase inverting/non-inverting function. These are the same kind of switch-mixers employed in chopper-stabilization circuits [God08].

Based on the signal detector and the 10-bits configurations of the programmable amplifier, the digital controller logic will start binary searching for the correct K values for six combinations of switches and switch-mixers. It will find six results and write these K values into registers as from “Offset Reg 1” to “Gain Reg 2” (Figure 4.13). For example, these registers contain four solutions for the offset measurement, such as K_{00a} , K_{00b} , K_{11a} and K_{11b} , and two solutions for the gain measurement, K_{xxa} and K_{xxb} . With the help of Eq. (4.21) and Eq. (4.23), the self-calibrated offset and gain results can be calculated using the CPU inside the SoC. The control register “Ctrl Reg” is used to communicate with the digital world to the system level (Figure 4.13). It controls the EI like “start”, “reset”, “enable”, “error” and “ready”. All these registers are communicating via the IEEE1687 interface.

Multiplier Design

The four-quadrant transconductance multiplier (Figure 4.13) is based on the FVF technology [Car05]. The circuit to realize the four-quadrant transconductance stage is shown in Figure 4.14. The output voltage can be expressed as:

$$V_{outp} - V_{outn} = k(V_{1p} - V_{1n})(V_{2p} - V_{2n})R_{load} \quad (4.25)$$

$$k = \mu C_{ox}W/L \quad (4.26)$$

In Eq. (4.25), k is used instead of $\mu C_{ox}W/L$. The load resistors VR0 and VR1 in Figure 4.14 are both equal to R_{load} . Since k has a temperature dependence via the mobility which we do not want, it is required to cancel the k by the load resistance R_{load} . The circuit in Figure 4.15 realizes the load resistor by a NMOST transistor M9, which is biased in its linear region. The drain-to-source resistance of M9 has a k in its denominator. As a result, the non-stable k in Eq. (4.25) can be cancelled out. Our simulation results for the analogue multiplier are shown in Figure 4.16. It is a DC simulation of Vout while sweeping the inputs V1 with stepping V2. For each line, V2 is fixed at a constant value while V1 is sweeping from -300mV to 300mV. If the multiplier is ideal, the lines should be straight lines and the slopes of the lines are determined by V2. Here due to non-linearity of the circuit, the simulated lines are not straight lines in the case the absolute values of the output voltages are larger than 200mV. Actually, this multiplier is not a rail-to-rail input circuit. Its maximum input range is from 0 to 0.6V. In this version of the design, the rail-to-rail capability is realized by dividing both inputs by two and finally amplify the multiplication result with four.

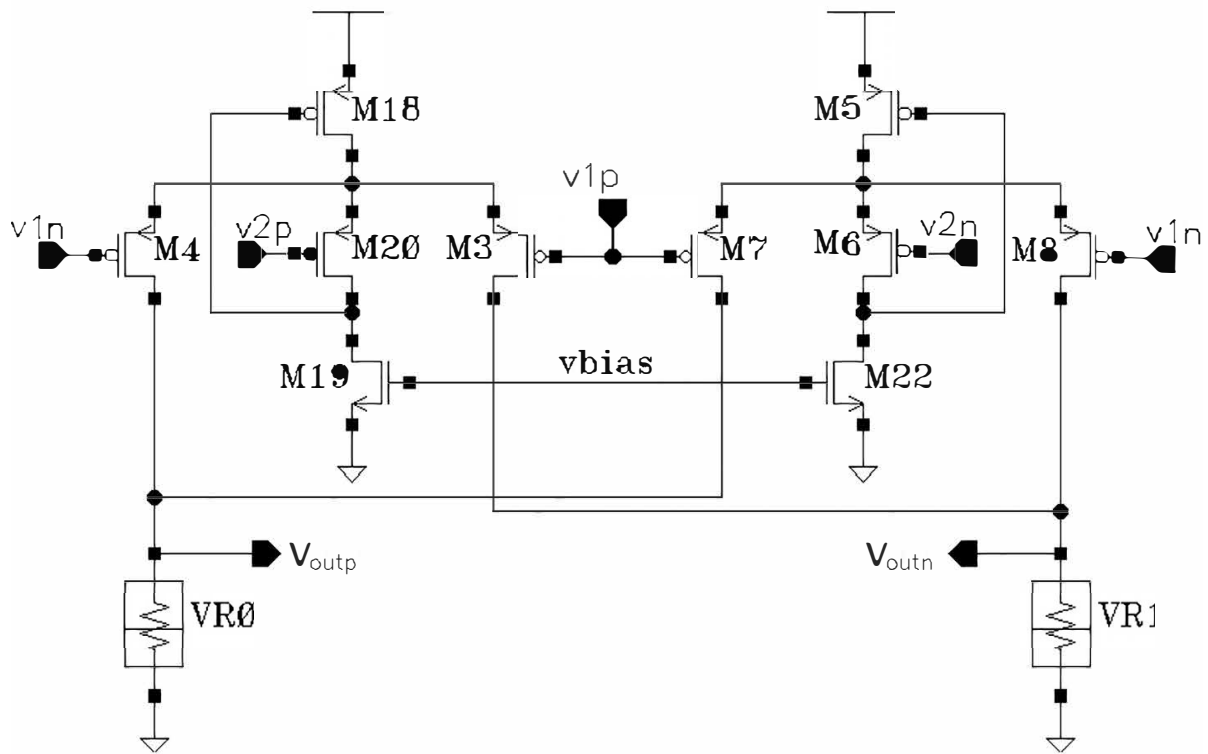


Figure 4.14: The four-quadrant trans-conductance multiplier based on the [Flipped-Voltage-Follower \(FVF\)](#) technology [Car05]. The load resistors VR0 and VR1 are not real resistors but realized as shown in Figure 4.15.

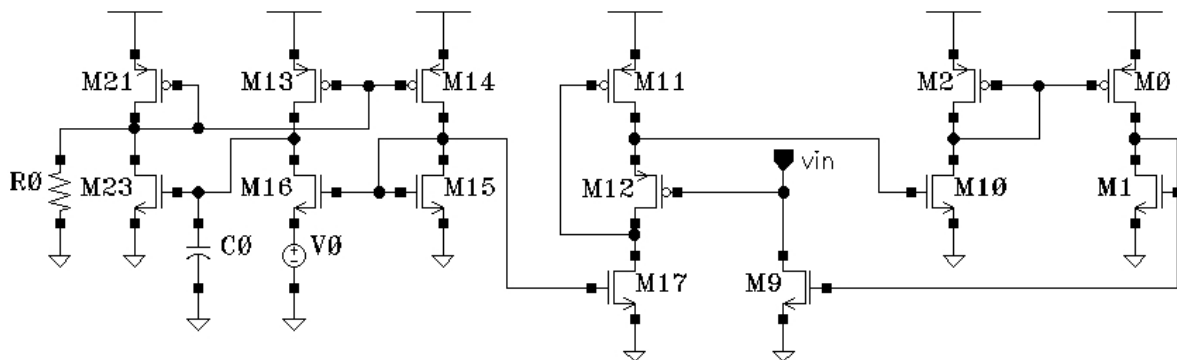


Figure 4.15: The circuit to realize the load resistors (VR0 and VR1). Vin is connected to V_{outp} and V_{outn} in Figure 4.14.

Digital Programmable Amplifier and Comparator Gain Stage

The digital programmable amplifier and the differential amplifier can be combined into one instrumentation amplifier. The configuration is shown in Figure 4.17. The 10-bits digital

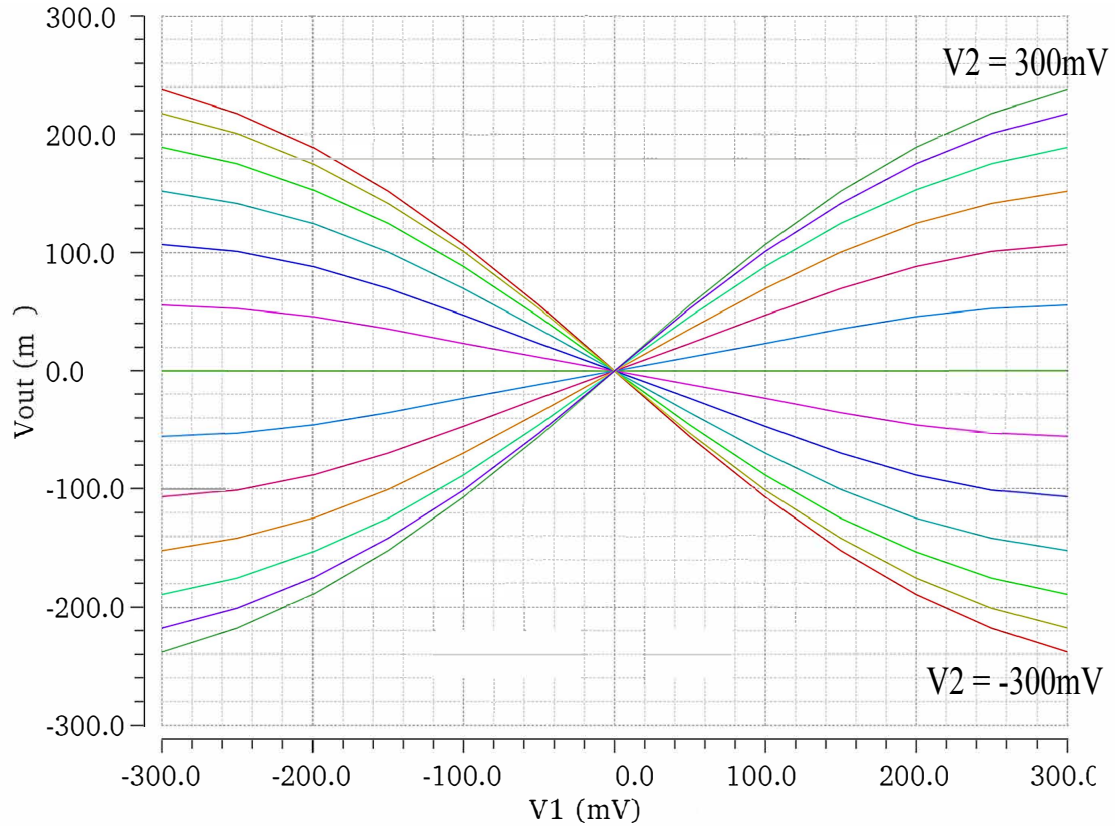


Figure 4.16: Simulation results of the multiplier, V_{out} ($V_{outp}-V_{outn}$) versus V_1 ($V_{1p}-V_{1n}$). Different lines are stepping with different V_2 ($V_{2p}-V_{2n}$) values.

programmability is realized by two “R-2R” resistor ladder networks [Pel13]. The differential amplifier is realized in a subtractive circuit format together with a gain G . In order to reach a 1000 times closed-loop amplification K , the open-loop gain of the OpAmps should be at least $80dB$. In 65nm low-power CMOS technology, the intrinsic gain of a transistor is only $20dB$. Therefore an $80dB$ gain will require 4 gain stages or gain-boosting stages for realization. In addition, transistors stacked between the supply and ground terminals cannot exceed one V_{gs} plus two V_{ds} for 1.2V power supply.

Our OpAmp design applies a constant-gm controlled rail-to-rail input stage, a folding-mesh summation stage and a class-AB rail-to-rail output stage. The fully differential OpAmp used is shown in Figure 4.18. The active cascode gain-boosting technique is employed to further increase the gain, which is realized by three transistor groups M3-M16-M17-M10, M30-M18-M19-M28 and M20-M29-M31. Circuit simulation results in Figure 4.19 show the gain of the OpAmp to be above $80dB$ for all input common-mode voltages.

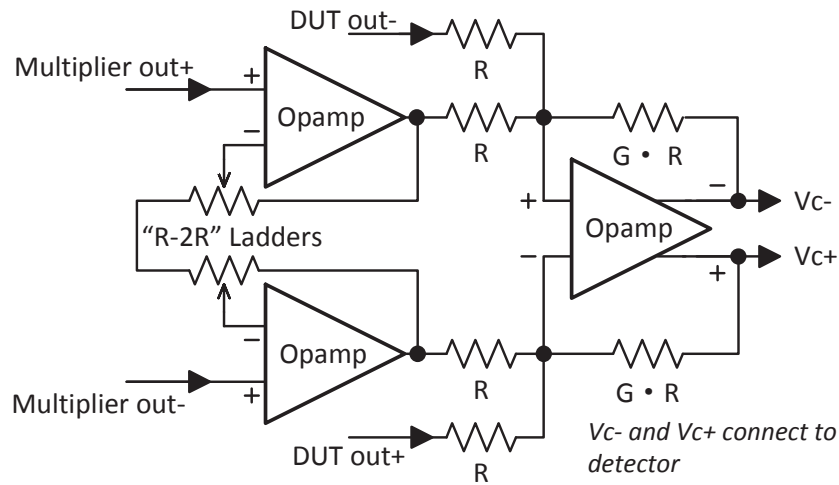


Figure 4.17: Combination of the digital programmable amplifier and the differential amplifier into an instrumentation amplifier. See Figure 4.13.

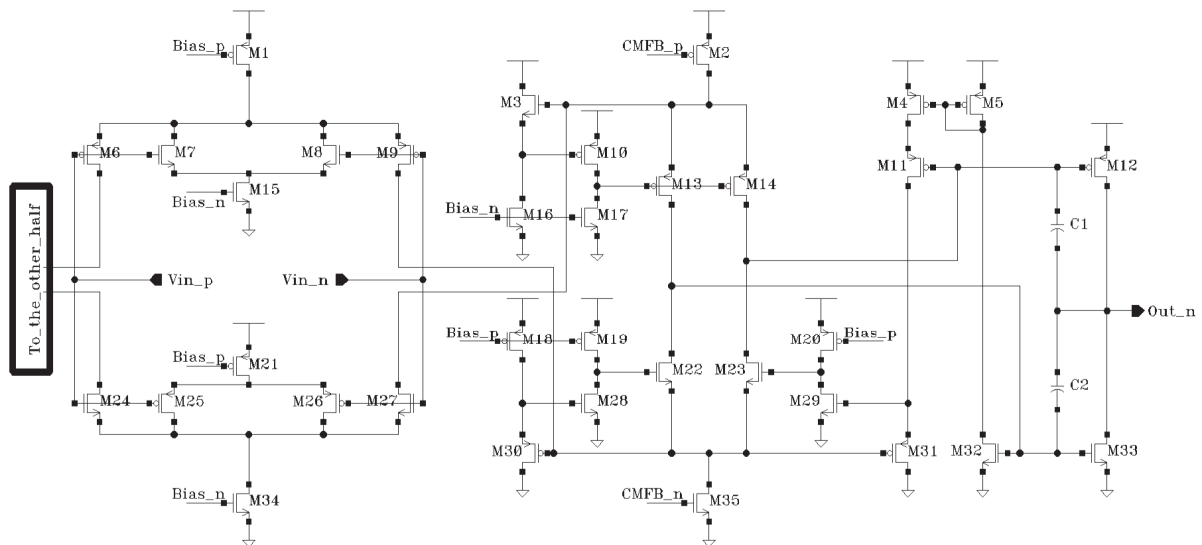


Figure 4.18: A fully differential version OpAmp as used in Figure 4.17 (only half is shown).

4.5.6 Simulation Results

In order to validate the self-calibration technique, five DUTs with different gain and offset combinations have been applied. The results are shown in Table 4.2. For offset simulations, there is an additive error which is less than $0.1mV$, together with a multiplying error which is around 10% of the calculated result. For gain simulations, the error is about $-2.5dB$. The theoretical detectable range is $100\mu V \sim 100mV$ for the offset, and $0 \sim 60dB$ for the gain. However, in this EI, the maximum detectable gain is about $40dB$ and the maximum detectable offset is $70mV$. If the gain and offset are too large, the theoretical signal value of V_c at $K = K_{spc}$,

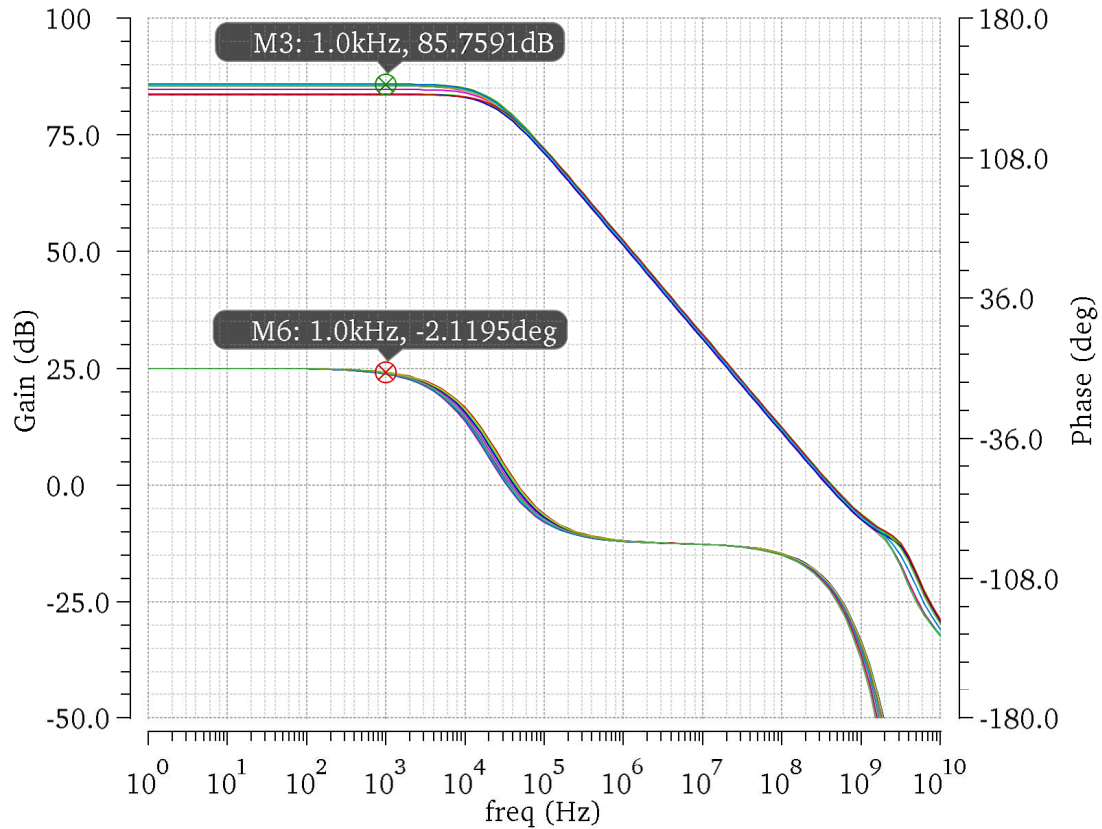


Figure 4.19: The gain and phase of the **OpAmp** with common-mode input voltage varying from 0 to 1.2V.

Table 4.2: **EI** simulation results.

Randomly generated tests						EI results	
V_{off} (mV)	V_{o1} (mV)	V_{o2} (mV)	V_{o3} (mV)	V_{o4} (mV)	Gain (dB)	V_{off} (mV)	Gain (dB)
1	0	0	0	0	34	1.05	not available
1	0.5	-1	10	0.1	34	1.17	32.8
10	-8	4	25	-2	12	11.05	11
0.2	0.5	-1	2	-0.4	40	0.20	37.5
70	25	18	-20	10	0	64.8	-1.8
Maximum Error:						10% \pm 0.1mV	-2.5dB

which is shown in Eq. (4.13), will be above the 1.2V supply limit and will cause the **EI** to saturate.

It is possible to solve this problem by making G programmable instead of fixed at 10. The minimum offset value $100\mu V$ is also not always reachable. This is because the change of V_c is sometimes only detected in case β is smaller than 1. This is not reachable for our designed EI. The actual range for the offset is $200\mu V \sim 70mV$, and $0 \sim 40dB$ for the gain. The testing time for the EI is dependent on the frequency of the input signal. The maximum testing time could be 240 times the input signal period in the case the EI has to step all possible K values and switch combinations. For example, the maximum possible input signal frequency is $30KHz$ due to the EI bandwidth limitation. At this input frequency, the testing time of the EI is $8ms$. The total current consumption is around $3mA$ at $1.2V$ without optimization for low-power operation. The area is around $0.05mm^2$ in a $65nm$ process.

4.6 Conclusions

NBTI simulations require transistor-level schematics which could not be obtained from industrial companies. Therefore, we have designed a test-vehicle OpAmp in $65nm$ CMOS technology ourselves. As part of the OpAmp, a new gain-boosting method has been described which can achieve $104dB$ gain with a unity-gain frequency of $783MHz$. Based on the NBTI simulation results, the most ageing-sensitive parameter in the OpAmp turns out to be the offset.

A new embedded offset and gain instrument for OpAmp IPs has been proposed based on a new measurement theory. The EI does not require to isolate the DUT from their connected feedback networks and other IPs. Neither does it need accurate stimulation sources. This EI can self-calibrate its resident offsets in the digital domain after each measurement. The EI has been designed in a $65nm$ low-power digital TSMC CMOS process and provides an IEEE1687 interface. It can be shared with other analogue OpAmp IPs to reduce the silicon area and shut down in idle situations to save power. The detection range is $200\mu V \sim 70mV$ for the offset and $0dB \sim 40dB$ for the gain.

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Chapter 5

Design and Aging Evaluation of Active Filter IPs

Abstract- *The signals of sensors in e.g. automotive [System-on-Chips](#) contain many electrical disturbances which appear subsequently in the [Analogue/mixed-signal Front-Ends](#). As a result, filters are often used in [Analogue/mixed-signal Front-Ends](#). These filters range from simple first-order RC passive filters to high-order active filters. Active filters have usually better performances as compared to passive filters. Therefore active filters are widely used in [Analogue/mixed-signal Front-Ends](#) of, for instance, automotive mixed-signal [System-on-Chips](#). Due to harsh environments, in some cases degradation of these filters may be encountered during lifetime and hence distorted sensor information could be provided with potential fatal results. In this chapter, the influence of [Negative Bias Temperature Instability](#) ageing in three different types of active filters are investigated. They are an active RC filter, a [Switched-Capacitor](#) filter and an [Operational Transconductance Amplifier-C](#) filter. The bandwidth of the [Operational Transconductance Amplifier-C](#) filter is found to be most sensitive to [Negative Bias Temperature Instability](#) ageing. In order to achieve highly dependable active filters, two approaches are discussed being by extra design effort and by employing an [Embedded Instrument](#). The [Embedded Instrument](#) approach is presented in more detail. Our self-designed [Embedded Instrument](#) will be described which monitors the filter-ageing behaviour. The [Embedded Instrument](#) can be used for instance for flagging problems on a car console or initiate automatic correction.*

Parts of this chapter are based on the author's publication: [\[Wan12\]](#) and [\[Wan15\]](#).

5.1 Introduction

An industrially important area for safety-critical SoC applications is the car-electronics industry. There are currently many electronic systems improving the safety in cars, like Anti-lock Braking System (ABS) and Electric Power Steering system (EPS) [Guo10]. Especially with the introduction of hybrid cars, and future advanced car-control options (e.g. automatic radar-based car-collision prevention), the safety levels of the required electronics have to be extremely high. The conditions (mission profile) under which these SoC electronics have to operate can be very harsh, up to 150°C, including high moisture and vibrations, among others. A lifetime of 20 years for trucks has to be guaranteed. Especially the AFEs in cars are of interest, as the sensors (e.g. angular, temperature, pressure) and associated electronics, are often at close distance to the measured physical quantity.

Filters, including passive filters and active filters, are widely used in AFEs as function blocks to filter out unwanted frequency parts in signals. They are ranging from simple two components first-order RC filters to complex high-order filters with hundreds of transistors and capacitors. Among them, passive filters are normally used in lower-order filter designs, like first-order filters with relatively small components values. The performance of these passive filters are often not that critical. Ageing of passive components like resistors and capacitors on chip is much less than MOS transistors [Pet93]. Therefore, in this chapter, the focus is on active filters which are often used for critical-performance high-order filters.

Active filters are widely used in AFEs as anti-aliasing filter before an ADC, or removing unwanted frequency ranges like low-frequency noise. Incorrect filter-transfer functions, e.g. in terms of amplitude, phase or cut-off frequency, can seriously deteriorate sensor data, and can hence endanger human life. In this chapter, different kinds of active filters are investigated with respect to their ageing behaviour. As EIs are more generic and wider in usage, this path of ageing monitoring in filters during lifetime has been taken.

The organization of this chapter is as following. First, three types of second-order Low-Pass (LP) active filters have been designed in 65nm CMOS technology as test vehicle in Section 5.2. They are an active RC LP filter, a Switched-Capacitor (SC) LP filter and finally an Operational Transconductance Amplifier (OTA)-C LP filter. Their fresh (un-aged) performances have been simulated as reference. Then these three filters are investigated in terms of their ageing behaviour under harsh (automotive) conditions in Section 5.3. Highly dependable active filters can be achieved via two approaches: by extra design effort to reduce the ageing influence or by monitoring the ageing behaviour of the filter over its lifetime with an EI and subsequently compensate for the effect of aging. In Section 5.4, circuit-level simulations of the OTA-C filter show that particular currents are well correlated with its ageing behaviour and are hence

candidates for ageing monitoring. As a result, a current [EI](#) is presented and shown to be suitable for ageing monitoring and communicating to the outside world via the standard IEEE1687 (IJTAG). Finally, some conclusions are being provided in Section [5.5](#).

5.2 Test Vehicle Active Filters

In the process of searching for active filter circuits from our industry partners, we encountered the same situation as mentioned before. Industrial transistor designs of active filters in advanced [CMOS](#) are not available and hence required our own design.

Filters, including passive filters and active filters, are a special area in analogue circuit design. Many analogue circuit designers only use simple first-order RC filters. High-order filters look more like mathematical designs instead of the previous circuit designs. Because of the close relationship between filter designs and mathematical tools, in fact filter design is probably the only analogue implementation which can be synthesised by [Electronic Design Automation \(EDA\)](#) tools similar to digital design. As a result, the circuit design of active filters in this chapter will not be explained in every detail.

If the basic building blocks in a filter are active circuits, it is referred to as an active filter. Active filters can achieve much higher performance with relative small passive component values, and are thus suitable for [IC](#) applications. The loss introduced by active filters is small compared to passive filters. This will be significant in high-order designs. In fact, active filters can provide signal gain instead of loss if this is required. However, most active filters provide a gain of $0dB$ to reduce the possibility of oscillation, especially in high-order active filters. Based on the construction of the basic blocks, active filters can be recognized as active RC filters, [SC](#) filters and [OTA-C](#) filters [[Rau10](#)].

In the next sections, three kinds of second-order Butterworth [LP](#) filters have been designed. They are an active RC [LP](#) filter, a [SC LP](#) filter and an [OTA-C LP](#) filter. All three [LP](#) filters have the same $-3dB$ cut-off frequency being $1kHz$ and aimed for low-frequency sensor applications such as temperature sensors. The [DC](#) gains of the [LP](#) filters are approximately $0dB$.

The three filters have been designed and simulated in Cadence Spectre with a foundry-provided 65nm low-power [CMOS Process Design Kit \(PDK\)](#). The [DC](#) gain of the active RC filter and the [SC](#) filter are close to $0dB$, while the [OTA-C](#) filter [DC](#) gain is around $-2dB$. This is because the [OTA-C](#) filter uses an [OTA](#) instead of an [OpAmp](#) which does not have a driver stage like the class-AB circuit to increase the output current. The simulation results will be shown in the following sections.

5.3 The Ageing of Active Filters

As known from Chapter 2, there are many ageing effects in nanometer CMOS technologies, like HCI, TDDDB, NBTI, and so on. Among them, NBTI is in our thesis the most critical ageing threat. Hence this section will focus on the ageing influence in terms of NBTI in active filters in 65nm low-power CMOS technology. Cadence RelXpert was used to simulate the NBTI degradation (or ageing) in active filters. Only threshold-voltage degradation for the PMOS transistors has been considered. The NBTI model used has been explained in detail in Chapter 3.

The reason to use RelXpert for NBTI simulation here is that we want to verify the worst-case scenario. This means the maximum possible DC stresses to generate maximum degradations. For example, the inputs of the active filters are biased at a DC level close to ground for the worst-case scenario, since the input differential pairs in all active filters are PMOS transistors.

All NBTI ageing simulations have been carried out for a mission profile of 20 years, at 150°C. All circuits were designed with a typical 1.2V power supply.

5.3.1 The Active RC LP Filter and its Ageing Behaviour

As the first filter, an active RC LP filter has been investigated. The circuit diagram is shown in Figure 5.1. It uses the Tow–Thomas universal bi-quad structure [Fle79]. The Vbias in Figure 5.1 is a DC voltage for the input common-mode biasing. The design employs three OpAmps, of which the circuit design is shown in Figure 5.2. The OpAmp employs a PMOST input differential pair with folding-cascode for the first gain stage. A low-voltage class-AB output stage is used to deliver sufficient current to drive the capacitors in the filter. The design is similar to the OpAmps described in Chapter 4. The combination of a folding-cascode circuit and a class-AB output stage provides more than 60dB gain.

The simulated fresh (non-aged) transfer function of the active RC LP filter and aged transfer function are both shown in Figure 5.3. The legend of the amplitude response is at the left y axis (in mdB), and the legend of the phase response is at the right y axis (in degrees).

Figure 5.3 shows that NBTI is not a problem for the ageing of an active RC LP filter, as NBTI has nearly no effect on the designed active RC LP filter. Especially the phase behaviour shows no difference. The explanation for this ageing behaviour is the following. First, the frequency behaviour is mostly determined by the passive RC components. They are insensitive to NBTI ageing. Second, the feedback reduces the sensitivity with respect to the gain of the OpAmps if the loop gain is high. As a result, the gain degradation of the OpAmps does not cause filter-performance degradation. Furthermore, the filter DC gain is low (0 dB), and

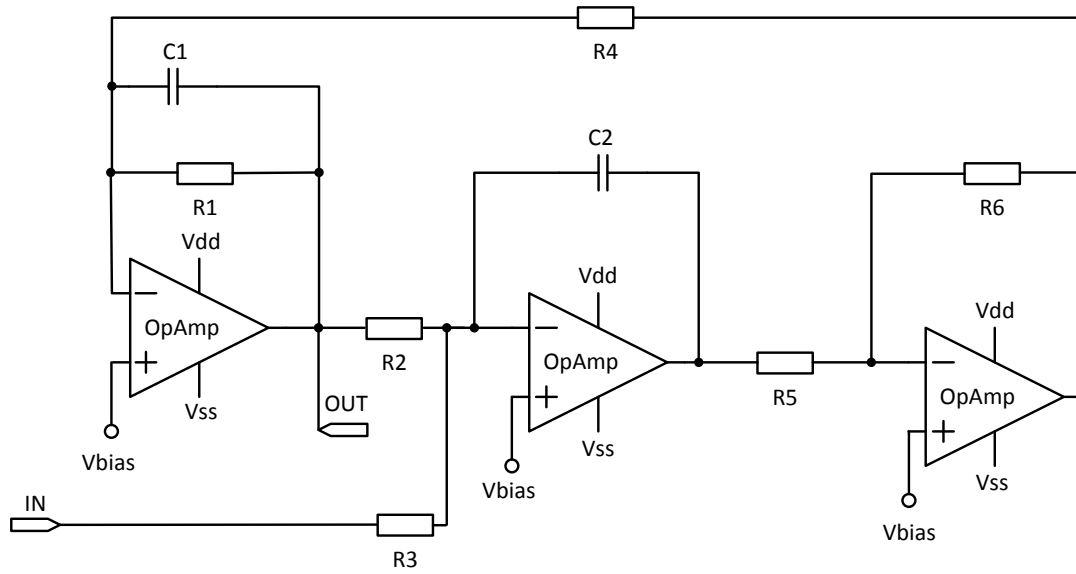


Figure 5.1: Circuit design of a second-order active RC LP filter.

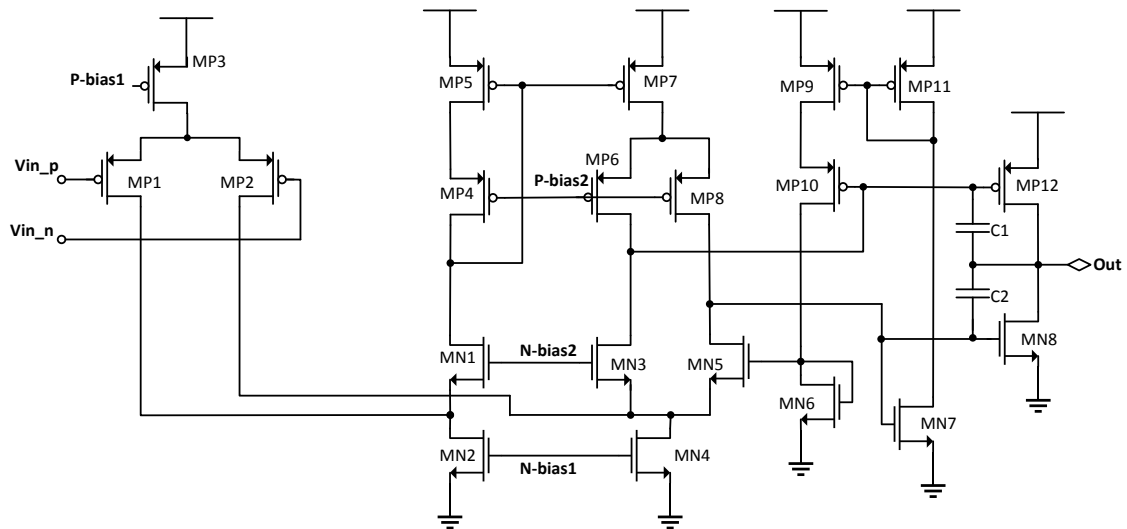


Figure 5.2: Circuit design of the OpAmp used in our filters.

therefore the offset caused by NBTI is not a problem. Hence in this case there is no need for monitoring this filter with respect to its ageing behaviour during life time.

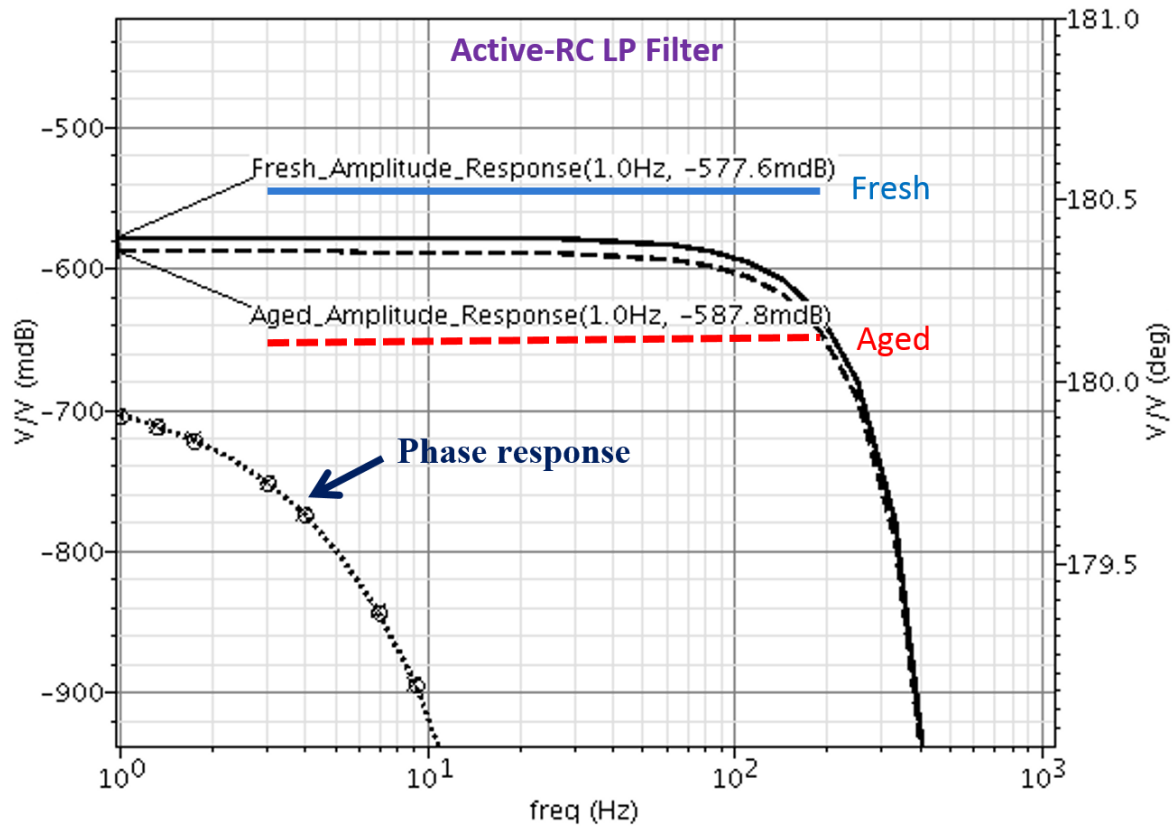


Figure 5.3: Simulated transfer function of the active RC **LP** filter circuit in the case of a fresh and aged circuit after 20 years at 150°C.

5.3.2 The Switched-Capacitor **LP** Filter and its Ageing Behaviour

As the second filter, a **SC** second-order **LP** filter has been investigated. The circuit diagram is shown in Figure 5.4. It employs the Fleischer-Laker approach [Tho71]. The used **OpAmps** are the same as in Figure 5.2, a **PMOST** input differential pair with a class-AB output stage. The class-AB output is necessary for charging the capacitors. The switches are called parasitic-insensitive switches which configure in two clock phases (ϕ_1 , ϕ_2) and as a result cancel the parasitic capacitance charging of the switches. For details of parasitic-insensitive switches, one can refer to [Tho71].

The simulated fresh transfer function of the **SC LP** filter and aged transfer function are both shown in Figure 5.5. The legend of the amplitude response is at the left y axis and the legend of the phase response is at the right y axis.

Figure 5.5 indicates again that **NBTI** has nearly no effect, and hence ageing is also not a problem for the **SC** filter. The design was not optimized in terms of reducing the overshoot,

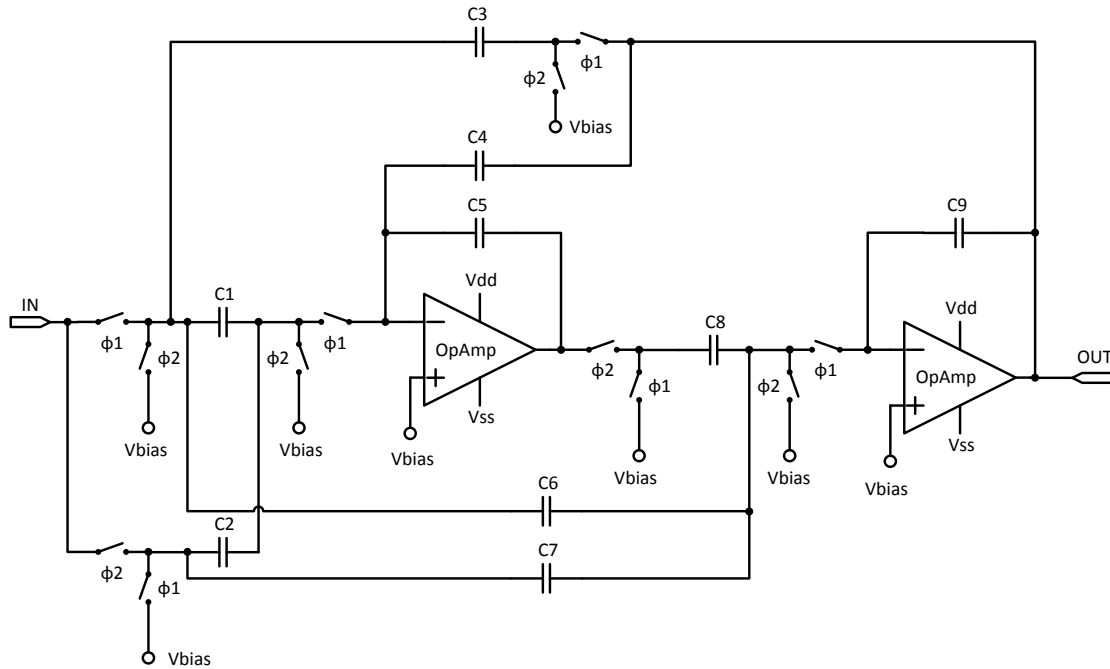


Figure 5.4: Circuit design of the second-order switched-capacitor LP filter. The OpAmp is the same design as shown in Figure 5.2.

but note that in order to visualize the ageing effects, the y axis scale has been made very small. In the case of the phase, the difference is not even visible. Therefore, also in this case there is no need to monitor the ageing behaviour of the filter. The explanation for this dependable behaviour are similar to the active RC filter. The frequency behaviour is determined by the capacitors and the clock period. The feedback reduces the sensitivity of the filter with respect to the gain of the OpAmps.

5.3.3 The OTA-C LP Filter and its Ageing Behaviour

As the last active filter example, an OTA-C LP filter has been investigated. Again, the Tow–Thomas universal bi-quad structure has been used [Fle79]. The design of the filter is shown in Figure 5.6. The circuit design of OTAs used in the filter is shown in Figure 5.7. It uses a PMOST input differential pair with folding-cascode current mirror as the output stage. Different transconductances of the OTA in the filter are marked with g_m in Figure 5.6. These different values of g_m are realized by scaling the size of the transistors while keeping the same circuit structure and bias.

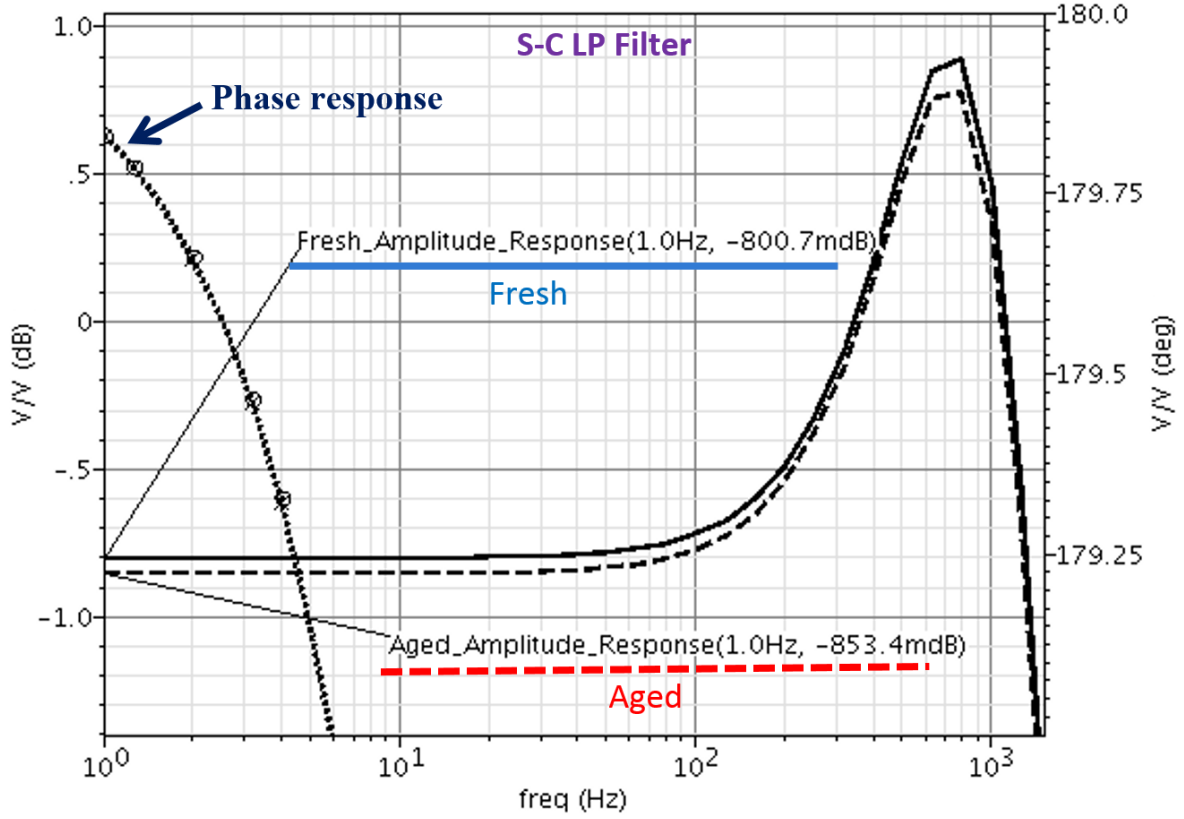


Figure 5.5: Simulated transfer function of the switched-capacitor second-order **LP** filter circuit in the case of fresh and aged circuit after 20 years at 150°C.

The simulated fresh transfer function of the **OTA-C LP** filter and aged transfer function are both shown in Figure 5.8. The legend of the amplitude response (in dB) is at the left y axis and the legend of the phase response (in degrees) is at the right y axis.

Figure 5.8 shows clearly the deviated behaviour after ageing. One can observe, that the filter frequency has changed as is the phase in the case of ageing. The reason can be found by investigating the transfer-function formula of the **OTA-C** filter, which is presented in Eq. (5.1) [Fle79].

$$H(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{g_{m2}g_{m4}}{C_1C_2}}{s^2 + \left(\frac{g_{m3}}{C_2}\right)s + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad (5.1)$$

$$\omega_{-3dB} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (5.2)$$

$$H(0) = \frac{g_{m4}}{g_{m1}} \quad (5.3)$$

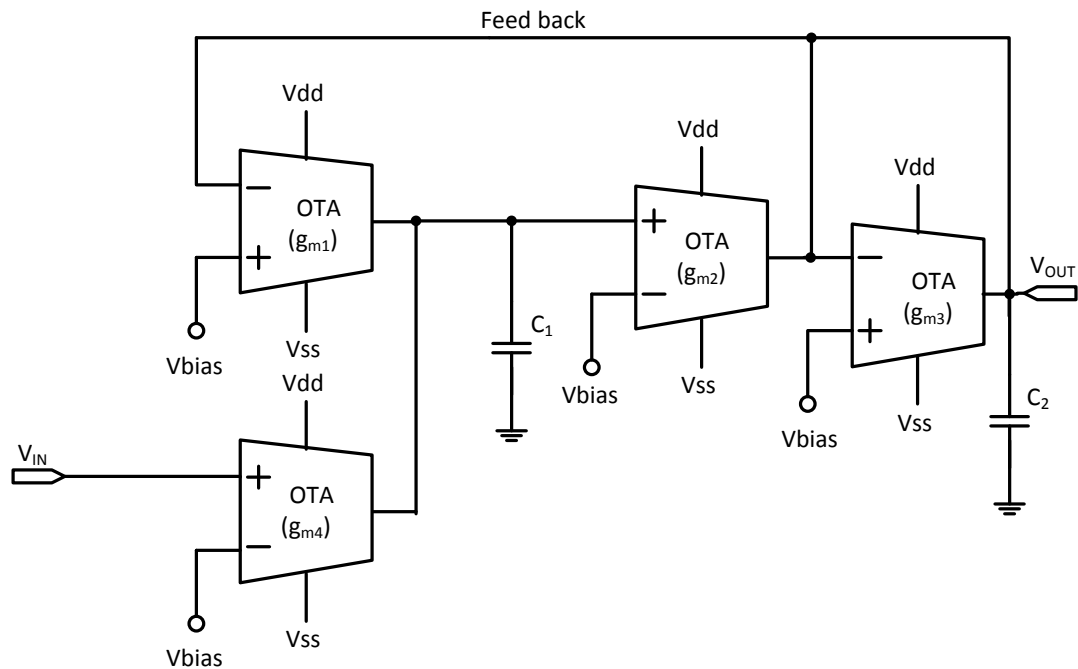


Figure 5.6: Circuit design of a second-order [OTA-C LP](#) filter.

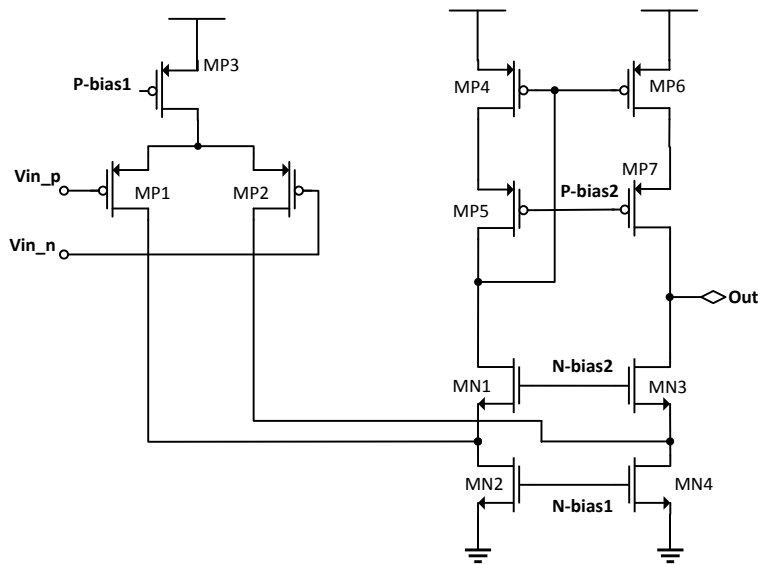


Figure 5.7: Circuit design of the [OTA](#) used in our filters.

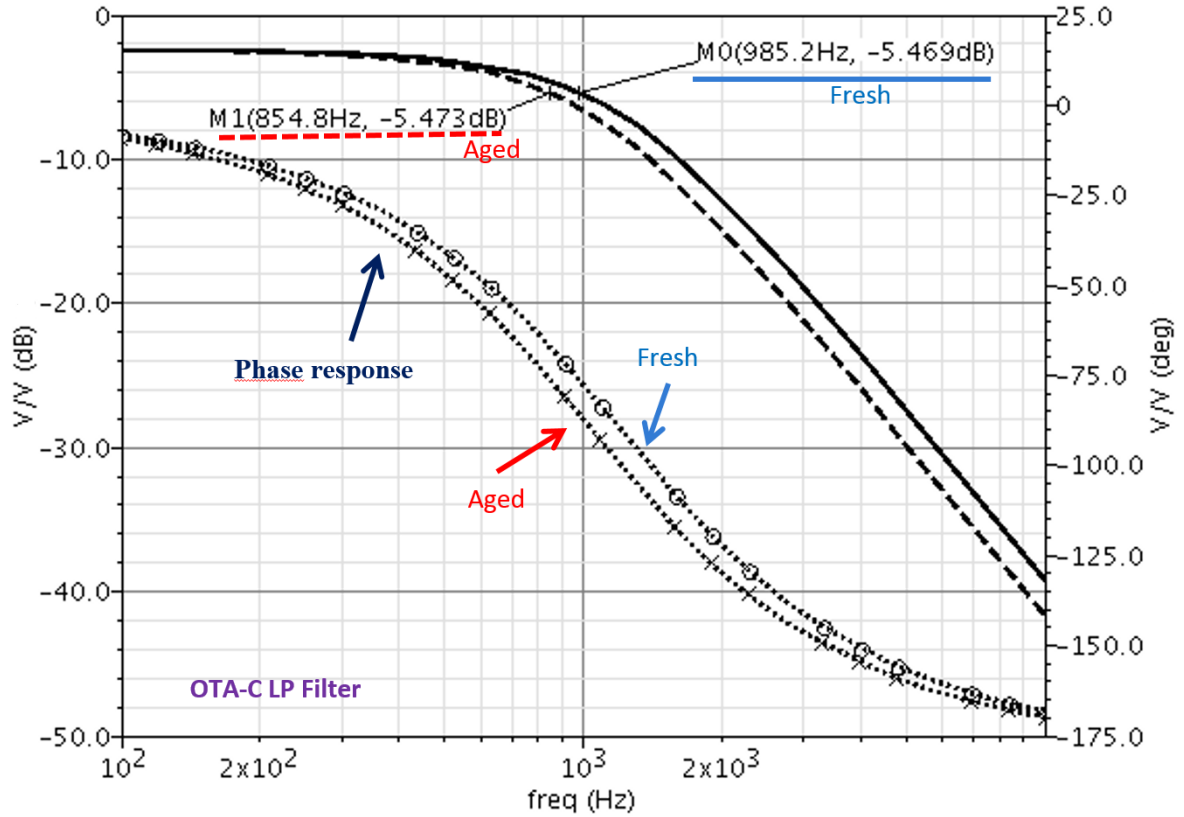


Figure 5.8: Simulated transfer function of the OTA-C second-order LP filter circuit in the case of fresh and aged circuit after 20 years at 150°C.

Where $H(s)$ in Eq. (5.1) is the Laplace transform of the filter transfer function. From the transfer function, the $-3dB$ frequency (ω_{-3dB}) and the DC gain ($H(0)$) of the filter can be expressed as in Eq. (5.2) and Eq. (5.3). They indicate that the $-3dB$ frequency is not only determined by the capacitors, but also by the multiplication of two transconductances g_{m1} and g_{m2} . The DC gain is determined by the ratio of two transconductances g_{m4} and g_{m1} .

One may notice that g_{m3} plays no role for the DC gain and $-3dB$ bandwidth. This is because g_{m3} is controlling the damping factor [Fle79] as seen from the transfer function Eq. (5.1). It determines the overshoot which is close to the $-3dB$ frequency (see the example in Figure 5.5).

The NBTI effect can increase the thresholds of the PMOS transistors in the input differential pair. As a result the drain currents will be degraded and hence the transconductance of the OTA will be reduced after ageing. An interesting result found by these simulations shows that the transconductance degradation for all OTAs in the filter are in close correlation. This is because the stresses for each OTA are proportional and influenced by the overall input signal of the filter. As a result the DC gain of the filter is relatively insensitive to ageing in Eq. (5.3) and

changes less than 0.01dB . The -3dB frequency is more sensitive to the ageing in Eq. (5.2) and has reduced more than 13% (around 130Hz).

5.3.4 Ageing Issues for General Active Filters

General active RC filters and SC filters, whether low pass, high pass, band pass or band stop, will be less sensitive to ageing mechanisms like NBTI when compared to OTA-C filters. This is because the NBTI mainly degrades the performance of the OpAmps inside these filters, which does not determine the key-performance parameters of filters like gain and bandwidth.

The OTA-C filter is more sensitive to NBTI because the transconductance of OTAs are involved in the formulas which determine the gain and bandwidth of OTA-C filters. As a result, OTA-C filters are less reliable. In the case one uses pseudo differential pairs as the building element for an OTA, the designed OTA will be even more sensitive to ageing effects like NBTI. This is because the pseudo differential pairs [Moh03] have a much larger transconductance sensitivity to ageing than normal differential pairs with a tail-current source. As a guideline, using pseudo differential pairs in ageing critical OTA-C filters should be avoided if possible.

5.4 Highly Dependable Active Filters

A highly dependable active filter can be achieved by employing two approaches. Either by extra design efforts or by using EIs to detect ageing. It will depend on the applications and most important, the system-level architecture.

In this section a simple embedded current instrument is presented, basically measuring the differential pair transistor current in the first stage at the DC operational point. The correlation of the currents with ageing of OTA-C filters will be presented. It will be shown that the first mentioned current is a good indication as well as a possible alarm signal that can be used for either correction or flagging in for instance a car console (indicating a particular sensor reading is false).

5.4.1 Highly Dependable Filters Based on Extra Design Effort

Our design guideline would be to avoid using active filters in AFEs. In fact the new trend in AFE design is using delta-sigma high-resolution ADCs to take all signals as well as noise into the digital domain and perform digital filtering. By using this approach, the anti-alias filter before the sigma-delta ADC can be reduced to a first order RC passive filter. In that case no NBTI influence will be introduced at all.

However, in some applications the signal has a wide bandwidth or frequency which cannot be converted into digital data without steep high-order anti-alias filters. In these cases, the active filters are difficult to avoid. Then it is better to use active RC or SC filters instead of OTA-C filters.

OTA-C filters offer improvements in design simplicity, parameter programmability, circuit integrability, and high-frequency capability as compared to OpAmp-based filters, as well as reduced component count and insensitivity to tolerances. If OTA-C filters are required, the designer should design an OTA with a good tail current source which is less sensitive to threshold-voltage changes in bias current mirrors and therefore less sensitive to the NBTI effect.

5.4.2 Highly Dependable Filters using EI

The OTA-C filter could be a candidate for ageing observation via an EI. One option could be to just monitor the output and compare it with a “correct” referenced output, like the method shown in [Hue93]. However, the approach used in [Hue93] cannot monitor the ageing degradation, because the reference circuits have also aged. Another option could be concurrent error detection [Cha93, Str06]. However, the concurrent detection method also faces the same problem. The error detection circuits age as well, which may cause false alarms or missed alarms.

It is also possible to investigate if there is already an internal signal in the OTA-C filter that shows a high correlation with the ageing behaviour, thereby easing the design of an EI. During simulations it was observed that a number of signals in the filter might have that property. It turned out, the current in the differential pair transistors of the OTA based filter (Figure 5.7) is an excellent candidate. This is supported by the correlation graph shown in Figure 5.9. It shows the $-3dB$ frequency versus the differential pair DC current. Each star represents one year of ageing, which indicates that the largest variation in the $-3dB$ frequency is in the first year. This is not surprising because ageing in the first year shows the largest changes according to Chapter 3.

A conclusion one can draw from Figure 5.9 is that a current sensor would be a good candidate for an EI to monitor the ageing of an OTA filter. In fact, there are already some I_{DDQ} monitors which could measure the current flowing in the differential pair [Raj00, Mal95]. However, the I_{DDQ} monitor often requires a high power-supply voltage which is usually harmful for ageing, and the circuits are complex. Following this reasoning in the next section, a much simpler current monitor with a standard supply voltage will be presented.

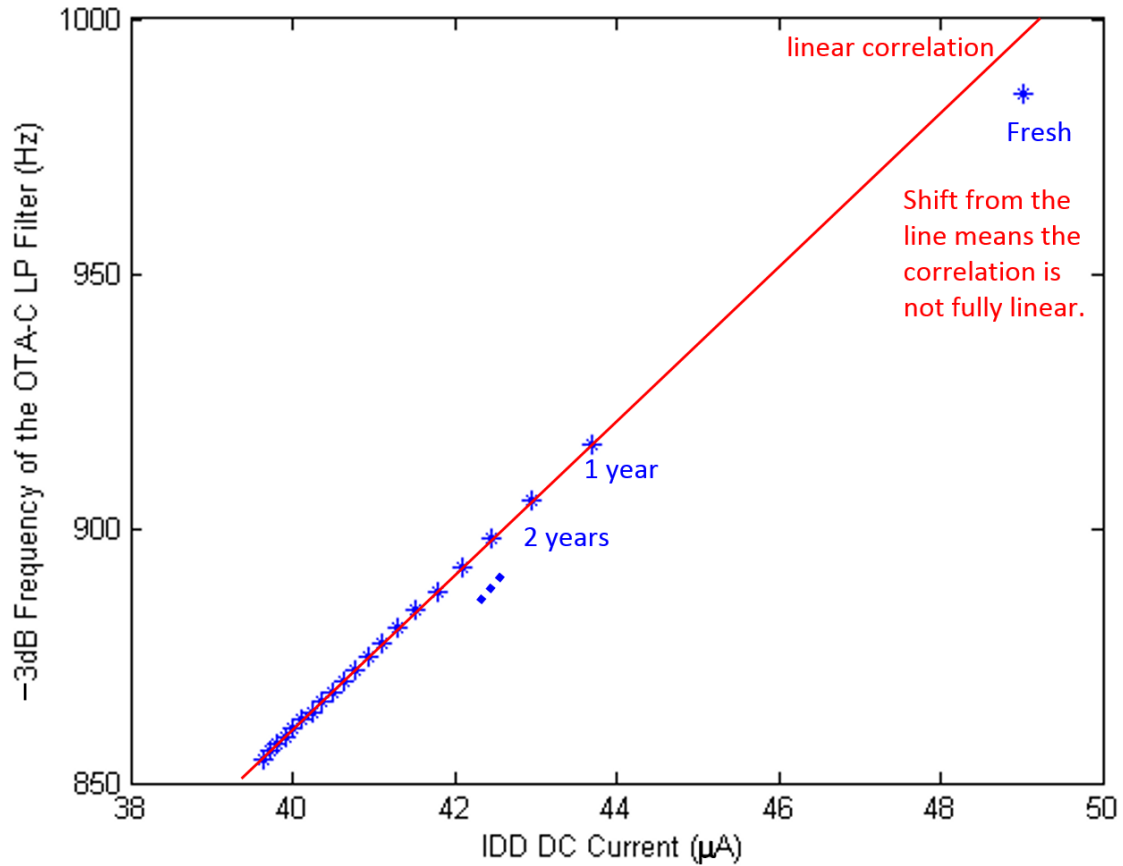


Figure 5.9: Simulated differential pair DC current versus the filter $-3dB$ frequency under NBTI ageing showing the correlation.

A configuration for an embedded current instrument is shown in Figure 5.10. The EI takes the same input as the filter. Hence it will suffer a similar voltage stress as the first OTA stage in the filter. The EI will compare the current it senses with a reference current, and will set the ageing-alarm signal to high if the sensed current exceeds the reference current level. The EI can work both on-line as well as off-line.

Here the reference current is generated by a bandgap-voltage reference divided by a resistor. Both parameters have no NBTI degradations. As a result, the ageing of the reference current can be ignored.

The EI is operating according to the IEEE1687 format, and communicates with the outside world with digital signals. For simplicity, the digital interfacing circuit is not shown here.

The reference current can also be programmed by a programmable current source or a current-steering DAC from the system. It provides the threshold current for the EI. With the ageing proceeding, at some moment the sensed current will reach the threshold and in that case an alarm signal (*Aging_alarm*) will be set. The current EI also works like the comparator in an

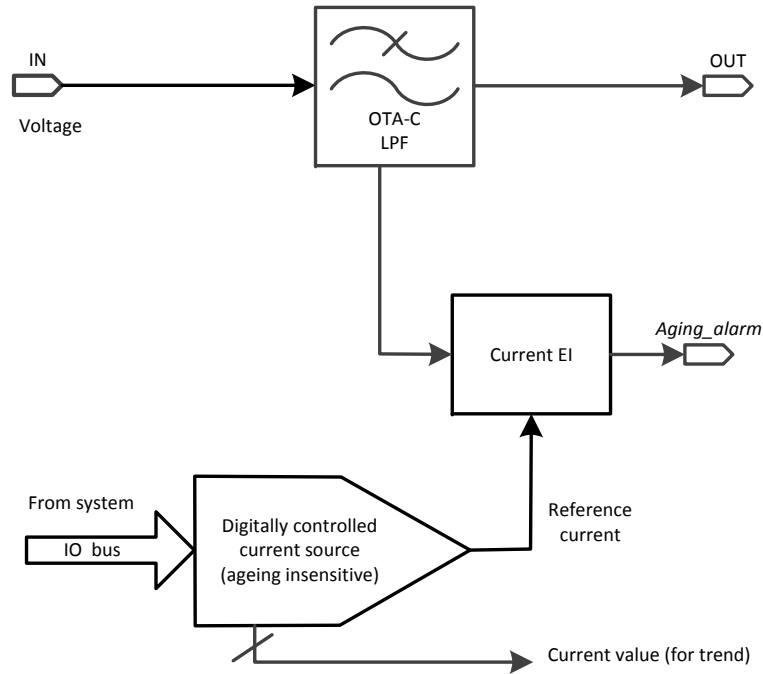


Figure 5.10: Proposed configuration of an **EI** for monitoring the ageing of an **OTA-C** filter.

ADC. Based on the result of the alarm signal, an accurate current value can be obtained which indicates the ageing status.

The detailed circuit design of the current **EI** block in Figure 5.10 is shown in Figure 5.11. It is a simple circuit in 65nm low-power **CMOS** technology. The sense circuit is a differential transistor pair with diode-connected transistor loads which is used to sense a similar common mode current pass through the differential pair transistor in the first stage of the **OTA**. The right current comparator in Figure 5.11 compares the sensed current with the reference current. The *Ageing_alarm* signal is generated to indicate the occurrence of a certain amount of performance degradation due to ageing. The amount of degradation is set by the reference current via the digital control interface. In Figure 5.11, V_{bias} is the same bias voltage as the one in Figure 5.6.

The **NBTI** degradation of the current monitor circuit is considered in the simulations as well. Figure 5.12 shows the reference current setting versus the *Ageing_alarm* pin voltages in the **EI**. For the **OTA** to be monitored, the sensed current will be compared with the reference current. If the sensed current is lower than the reference current, the *Ageing_alarm* voltage

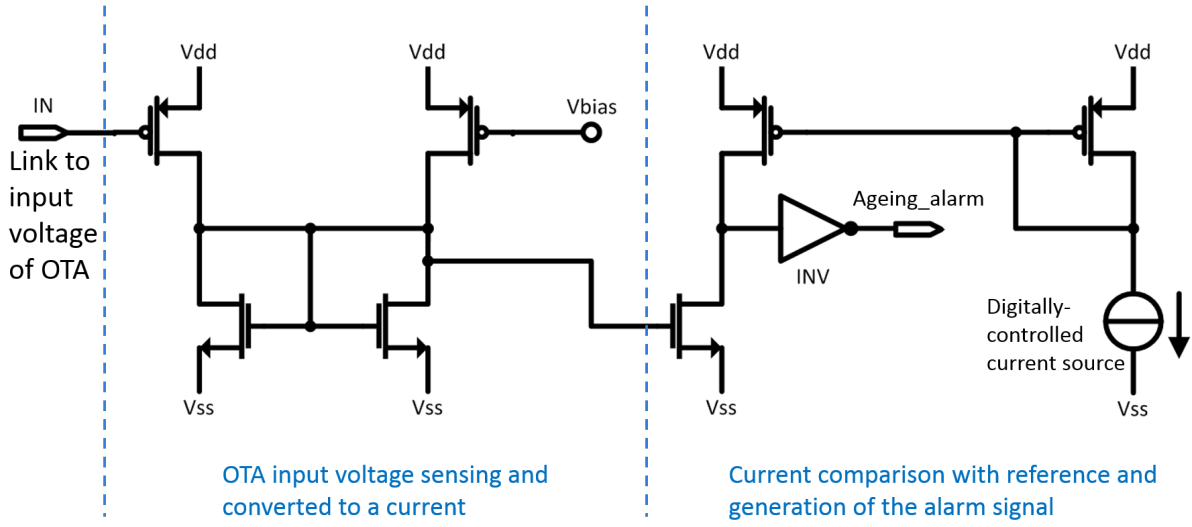


Figure 5.11: Circuit design of the current EI block in Figure 5.10.

will be high. The reference current value can be set from the real measured value from the final test of the product.

Figure 5.13 shows our EI sensed current with the $-3dB$ frequency of the OTA-C filter. It looks similar to Figure 5.9 but now the relationship is between the $-3dB$ frequency and the reference current. Based on Figure 5.13, one can set $5\mu A$ as the reference current value. In the fresh state, the *Ageing_alarm* signal is low. In the case the circuit is aged for around 6 years, the ageing alarm signal will be raised to high, which means 10% degradation of the $-3dB$ frequency has occurred.

Since the EI is required to detect $1\mu A$ current drop, a programmable current source with steps of $0.1\mu A$ has been used. Furthermore, to cover the Process, Voltage and Temperature (PVT) variation, the programmable current source should cover $10\mu A$ in range as indicated from simulations. This means it requires a 6- to 7-bits digital programmable current source or a current-steering DAC. The design can be similar to the one used to monitor offsets in OpAmps [Wan11].

5.4.3 Comparison of the Two Approaches

If one compares the extra design effort approach and EI approach, the EI approach is more general and adds flexibility to the system. However, the EI only provides an indication of a

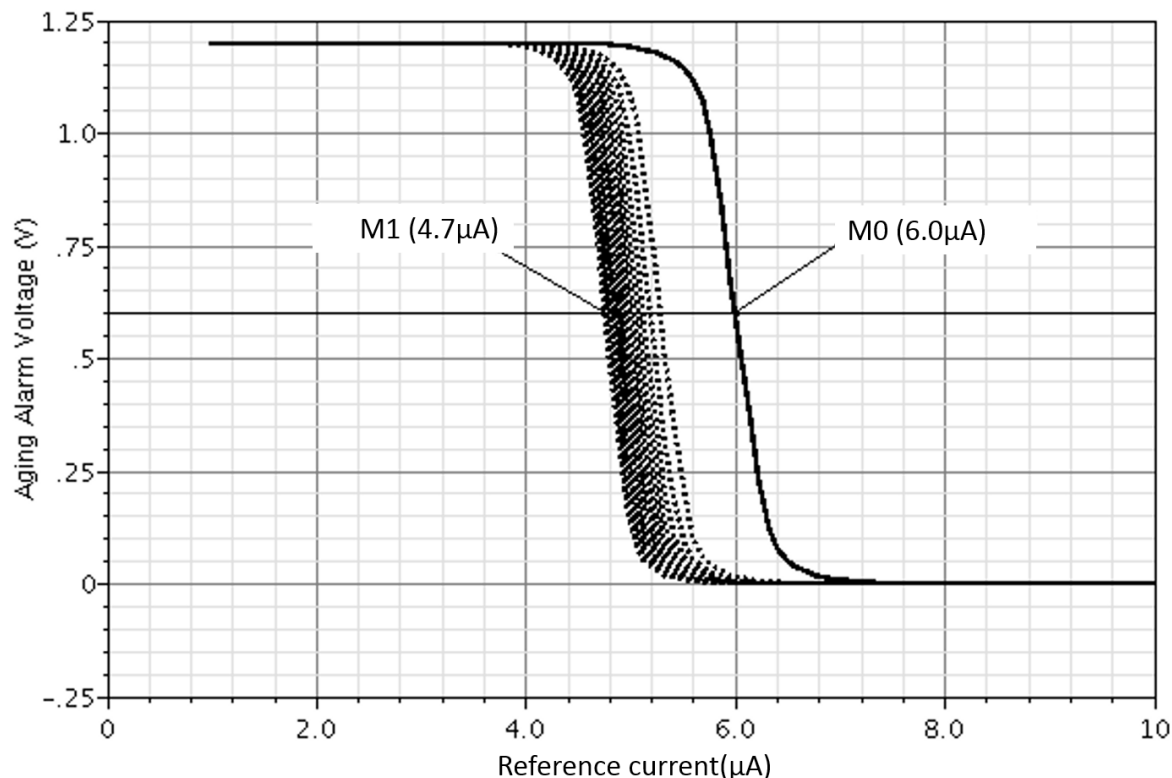


Figure 5.12: Ageing alarm signal versus the reference current. The markers M0 and M1 in Figure 5.12 are the simulated reference current when *Ageing_alarm* voltage is on the threshold (0.6V). It indicates that the OTA differential pair current is reduced by ageing. Thus the transconductance of the OTA is also reduced by ageing which will result in a filter bandwidth reduction as shown in Figure 5.8.

possible ageing problem. The correction action has to be taken by the system to compensate for the $-3dB$ frequency drift.

The design approach normally can achieve the best performance and lowest cost/power consumption. Yet it is highly application dependent and requires a lot of design and verification effort for each individual case.

The best approach is that the ageing is considered at the system level and trade-offs are made with other parameters. A passive filter is the better highly dependable filter as compared to an active filter. Also in modern systems, digital filters are often used which are a good option for highly dependable filters.

5.5 Conclusions

Transistor-level designs of active filters in advanced CMOS are not available from our industry partners. As a result, we had to design all our own active filters. Three types of second-order

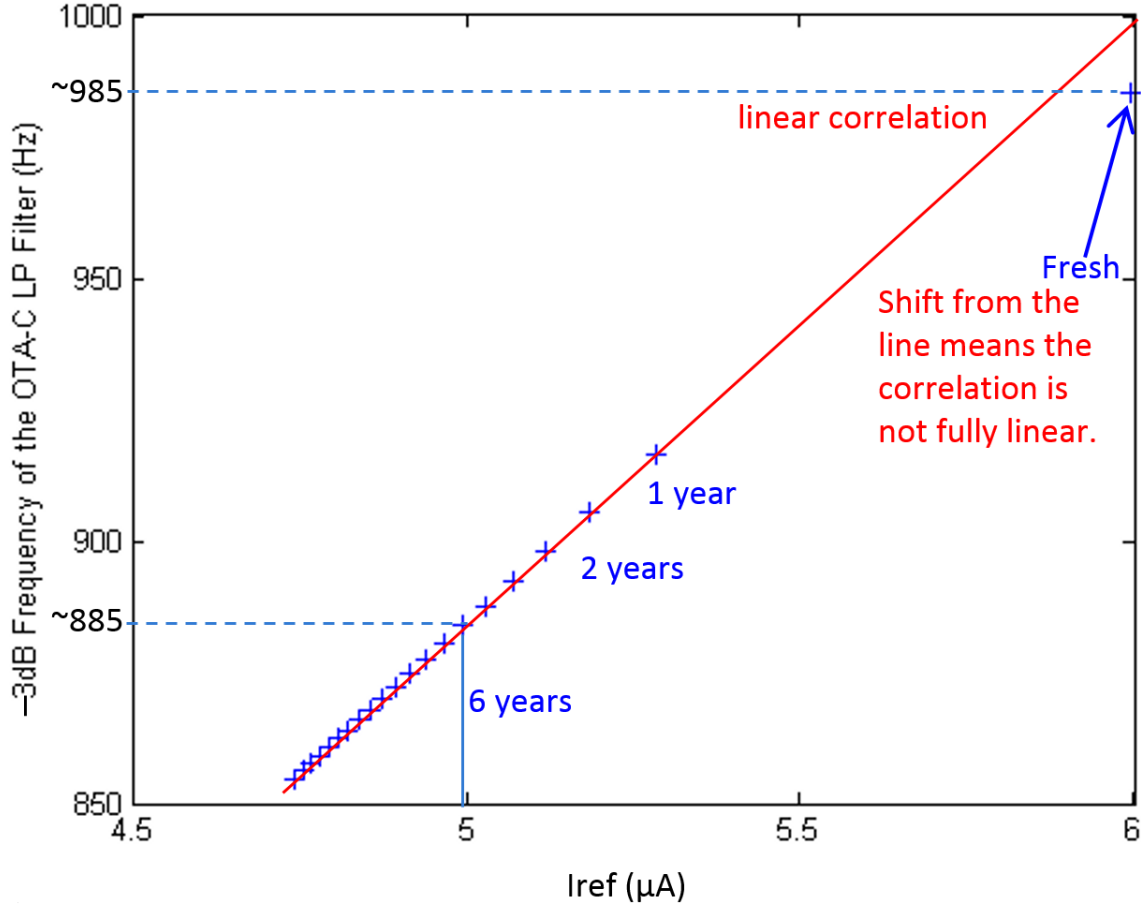


Figure 5.13: Correlation of the reference current setting in the [EI](#) with the filter $-3dB$ bandwidth.

active low-pass filters were designed and simulated for their fresh and aged performances. They are the active RC filter, the [SC](#) filter and the [OTA-C](#) filter. The [OTA-C](#) filter is the most sensitive one to NBTI ageing. Due to the reduction of transconductances in [OTAs](#), the $-3dB$ cut-off frequencies of [OTA-C](#) filters can be degraded by more than 10% and hence endanger sensor readings. This can potentially cause safety-critical issues in a car. By monitoring the filter during lifetime using an [EI](#), either car console flagging or direct corrective actions at system level can be taken. Finally, the design of a current [EI](#) has been presented in the same process as the filter and its capabilities have also been validated by simulations. The current-based [EI](#) is generic in its nature, and can hence also be used for other IPs. In order to use the current [EI](#), system-level operations are required.

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Chapter 6

Design and Aging Evaluation of Analogue-to-Digital Converter IPs

Abstract-

This chapter focuses on the design of a 10-bits [Successive-Approximation Register \(SAR\)](#) [Analogue-to-Digital Converter \(ADC\)](#) in 65nm [CMOS](#) technology and its ageing effect resulting from [Negative Bias Temperature Instability \(NBTI\)](#). The [NBTI](#) degradation of the sub-blocks inside the [SAR ADC](#), like input buffer, bootstrapped switches, dynamic-latch comparator, and asynchronous [SAR](#) logic have been investigated respectively as well as the [NBTI](#) degradation of the whole [ADC](#). It will be shown that [NBTI](#) mainly causes two kinds of degradations for the [SAR ADC](#), timing degradation and offset degradation. Two approaches can be adopted to build highly dependable [SAR ADCs](#): via an extra design effort or the usage of [Embedded Instruments \(EIs\)](#). An [EI](#) for detecting the timing degradation error is proposed and also an [EI](#) for measuring the offset degradation is discussed.

6.1 Introduction

[Analogue-to-Digital Converters](#) are the core blocks in [Analogue/mixed-signal Front-Ends \(AFEs\)](#) of [System-on-Chips \(SoCs\)](#). They convert real-world analogue signals into digital signals with different speeds and accuracies, which can be further processed by digital [Intellectual Property \(IP\)](#) cores. Because of [ADCs](#), almost all [AFEs](#) have more or less the same structure from a system-level point of view.

Parts of this chapter are based on the following publications of the author: [[Wan14a](#)], [[Wan15a](#)] and [[Wan15b](#)].

Depending on the speed and accuracy, several types of ADCs have been developed in the past. For sensor-application related AFEs, SAR ADCs [Pel13] and Delta-Sigma ($\Delta\Sigma$) ADCs [Ste95] are the most popular ADC types.

The SAR ADC represents a majority of the ADC market from 8- to 16-bits resolutions, and tens of kilo-Hertz to hundreds of mega-Hertz sample frequencies. With the interleaving architecture applied, several SAR ADCs can be placed in parallel to further boost the sample speed. The combined ADC can thus operate at as high as 1GHz sample speed. Since the SAR ADC only contains one comparator, the power consumption of the SAR ADC is among the lowest of possible ADC types. The sampling and holding capacitor in the SAR ADC can be shared with the charge-redistribution Digital-to-Analogue Converter (DAC), which makes the SAR ADC simple while the total area is also smaller than other ADC types. The combined features of low-power consumption as well as a small form factor makes SAR ADCs ideal for a wide variety of applications, especially for low-power applications such as portable/battery-powered devices. Therefore in this chapter, the SAR ADCs were targeted for their ageing and reliability.

As discussed in previous chapters, accessing the full design database, especially the transistor-level schematics, is essential to investigate and simulate ageing and reliability. These databases could not be obtained from our cooperating companies and other partner organizations even after significant efforts. The only way to access the full design data of a SAR ADC is to design one ourselves. As a result, the next section will describe our test bench SAR ADC: a 10-bits 50MS/s SAR ADC in 65nm low-power digital CMOS technology which is now available to all academic institutes from us.

This chapter is organized as follows. Section 6.2 will briefly discuss our design of a 10-bits SAR ADC in 65nm as a target vehicle. Section 6.3 will investigate the NBTI ageing of each building block inside the SAR ADC as well as for the whole SAR ADC. Two approaches for designing highly dependable SAR ADCs will be introduced in Section 6.4. Conclusions will be provided in Section 6.5.

6.2 Design of 10-bits 50MS/s SAR ADC in 65nm LP Digital CMOS Technology

Our set-up of a fully differential 10-bits SAR ADC is shown in Figure 6.1. The ADC is composed of input buffers, bootstrapped switches, charge-redistribution capacitor banks, a comparator and asynchronous SAR control logic.

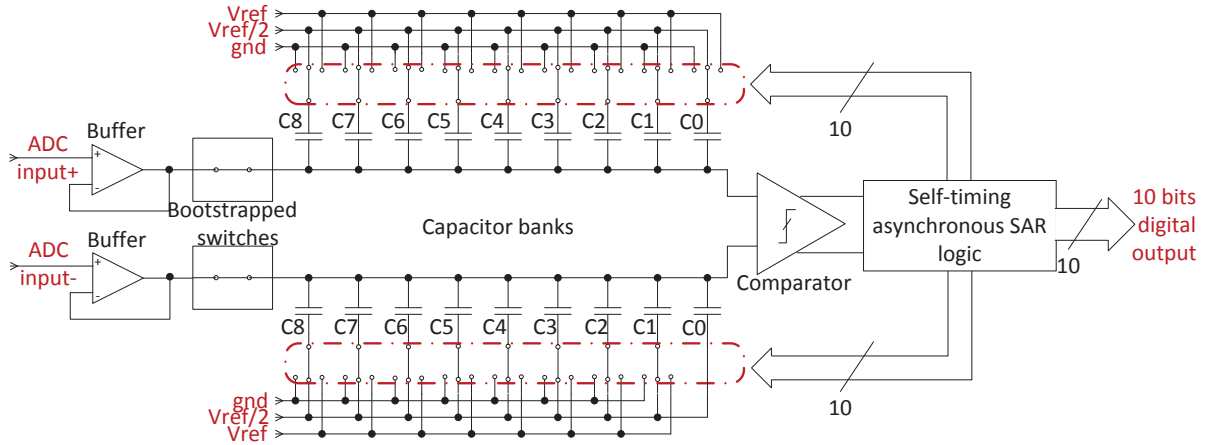


Figure 6.1: The block diagram of our 10-bits fully differential SAR ADC.

Because of the fully differential design, there are two symmetric signal routes before the comparator. In each signal route, there is a symmetrically copied input buffer, bootstrapped switch, charge-redistribution capacitor bank and DAC control blocks which belong to the asynchronous SAR control logic.

The input buffer is providing sufficient charging current and ensures that the charging of capacitor banks can be finished in a limited time frame. The bootstrapped switch is used for sampling and holding the signal. It is a special kind of MOST switch which has a constant “on” resistance regardless the voltage it passes. The charge-redistribution capacitor bank is the core of the SAR ADC. It first stores charges and then puts weights on each bit. The comparator is for comparing the voltages of the two symmetric signal routes which are also the voltages present at the two capacitor banks.

The asynchronous SAR control logic is a digital block in the SAR ADC. It generates asynchronous clock signals and feedback to control the switches inside the charge-redistribution capacitor banks. It also generates the final 10-bits digital output of the ADC. Details can be found in the Appendix C.

The SAR ADC operation principle is briefly described in [Pel13]. During the ADC sampling phase, the bootstrapped switches are closed and the capacitor banks are charged by the differential input signal. The capacitor banks are composed of two arrays, each containing capacitors from C8 (2^8C) to C0 ($1C$). The parameter C is the unit-capacitance value. During the charging of the capacitor banks, all other terminals of these capacitors are connected to $V_{ref}/2$ as shown in Figure 6.1. When the ADC clock signal changes from high to low, the

bootstrapped switches are opened and charges are stored in the capacitor banks. This is the sampling and holding phase.

After the charges are successfully stored in the capacitor banks, the comparator will be activated and starts to compare the two inputs. Based on the comparator result, the **Most Significant Bit (MSB)** is determined. Depending on which input of the comparator is higher (or lower), that input-connected capacitor array will be referred to as the high-voltage side (or low-voltage side). The high-voltage side will switch its largest capacitor terminal, which is C8 in Figure 6.1, from $V_{ref}/2$ to $0V$. This operation will decrease the high-voltage side by a value equal to $V_{ref}/4$. The low-voltage side will switch its C8 terminal from $V_{ref}/2$ to V_{ref} , which will increase the low-voltage side by a value equal to $V_{ref}/4$.

After the C8 capacitor is properly switched, the comparator will compare again and decide on the C7 terminals switching as well as the **(MSB – 1)** bit. The same procedure will be repeated until C0 is switched. In this case, the last comparator operation is performed and the **Least Significant Bit (LSB)** is determined by the comparator result.

It is worth to note that only one C0 can switch its terminal. The C0 at the other side of the capacitor array is fixed at $V_{ref}/2$. This is new as compared to other **SAR ADCs**, in which at both sides C0 capacitors are fixed. By this idea, one can reduce the size of capacitor arrays to half. (The largest capacitor in this design is C8 which is 2^8 times the value of C0. In normal differential **SAR ADCs** designs, the largest capacitor is 2^9 times C0, or even 2^{10} times C0.)

The **SAR** logic, which controls the switching procedure, is clocked by an asynchronous self-generated clock signal. This asynchronous clock signal is generated from a ring oscillator loop which consists of a comparator, delay cells and control logic. After completing the **SAR** procedure, each capacitor array will generate 10-bits data, resulting in two 10-bits data information. The output-processing logic will carry out a subtraction between them and generates the 10-bits digital output of the **ADC**. Refer for details to Appendix C.

The simulated results of the **ADC** will be shown in Section 6.2.6 in the case the capacitors are being switched from C8 to C0.

6.2.1 The Input Buffer

The input buffer is used to supply sufficient current to charge the **SAR ADC** capacitor banks. Sometimes, the input buffer is not included in the **SAR ADC** and in this case the buffer function is combined with instrumentation amplifiers and active filters in the **AFE**. In our design, two unity-gain feedback **OpAmps** are used as input buffers to examine their ageing behaviour.

In order to reduce the **ADC** noise as much as possible, the buffer-induced error should be less than 0.5 **LSB**. The open-loop gain of the **OpAmp** inside the buffer is required to be larger

than 68dB following the discussions in Chapter 4. Leaving some margin for process variation and temperature instability, a two-stage OpAmp was chosen which can reach 80dB gain at room temperature.

Our OpAmp design is the same as shown in Figure 4.18 of Chapter 4. The final differential gain of the OpAmp is more than 80dB for all kinds of input common-mode voltages. The simulation result of the OpAmp has already been shown in Chapter 4 (Figure 4.19). For a detailed discussion of the gain-boosted OpAmp, one can refer to Chapter 4.

6.2.2 The Bootstrapped Switch

A simple pass gate with a NMOST in parallel with a PMOST can be used as a switch. However, the “on” resistance of the pass gate is not constant. The resistance will change with the input voltage level and is proportional to the gate-to-source voltage. If this signal-dependent switch is used as the sampling and hold switch of an ADC, the performance of the ADC will be degraded. As a result, a constant “on” resistance analogue switch is important for ADC applications.

Another kind of switches are called bootstrapped switches [Aks06]. It is more complicated than a pass gate and requires clock signals to function correctly. However the bootstrapped switch can keep a constant “on” resistance regardless of the input signal. The required clock signals are also available in ADCs. Therefore bootstrapped switches are widely used in ADC designs.

A simple bootstrapped switch used in this design is shown in Figure 6.2 [Aks06]. It uses only one NMOST as the switch itself (M4). The rest of the transistors sense the input voltage of M4, add one V_{dd} and then apply it to the gate of M4 when it is in the “on” state. In this way, the gate-to-source voltage of M4 is always one V_{dd} and it keeps the “on” resistance constant.

The control clock signal in Figure 6.2 is clk . When clk is low, M9 and M10 will be conducting and pull the gates of M7, M0 and M4 to ground. The switch M4 is off. In the mean time, the capacitor C0 is charged to V_{dd} via transistor M2q and M8. When clk changes to high, the charge path of the capacitor C0 is removed. The voltage across C0 is stored and added to the gate of M4 via conducting transistor M5. M0 is also conducting at this time. Therefore the overall voltage at the gate of M4 is V_{dd} plus the input voltage. It does not matter how the input voltage is changed. The gate voltage of M4 is always tracking the input and adds one V_{dd} . The simulation of the bootstrapped switch will be shown in Section 6.3.3.

6.2.3 The Capacitor Bank

In Figure 6.1, the capacitor banks are connected to three voltages via switching, being V_{ref} , $V_{ref}/2$ and ground (gnd). In fact, the voltage level $V_{ref}/2$ is not available in the real circuit of

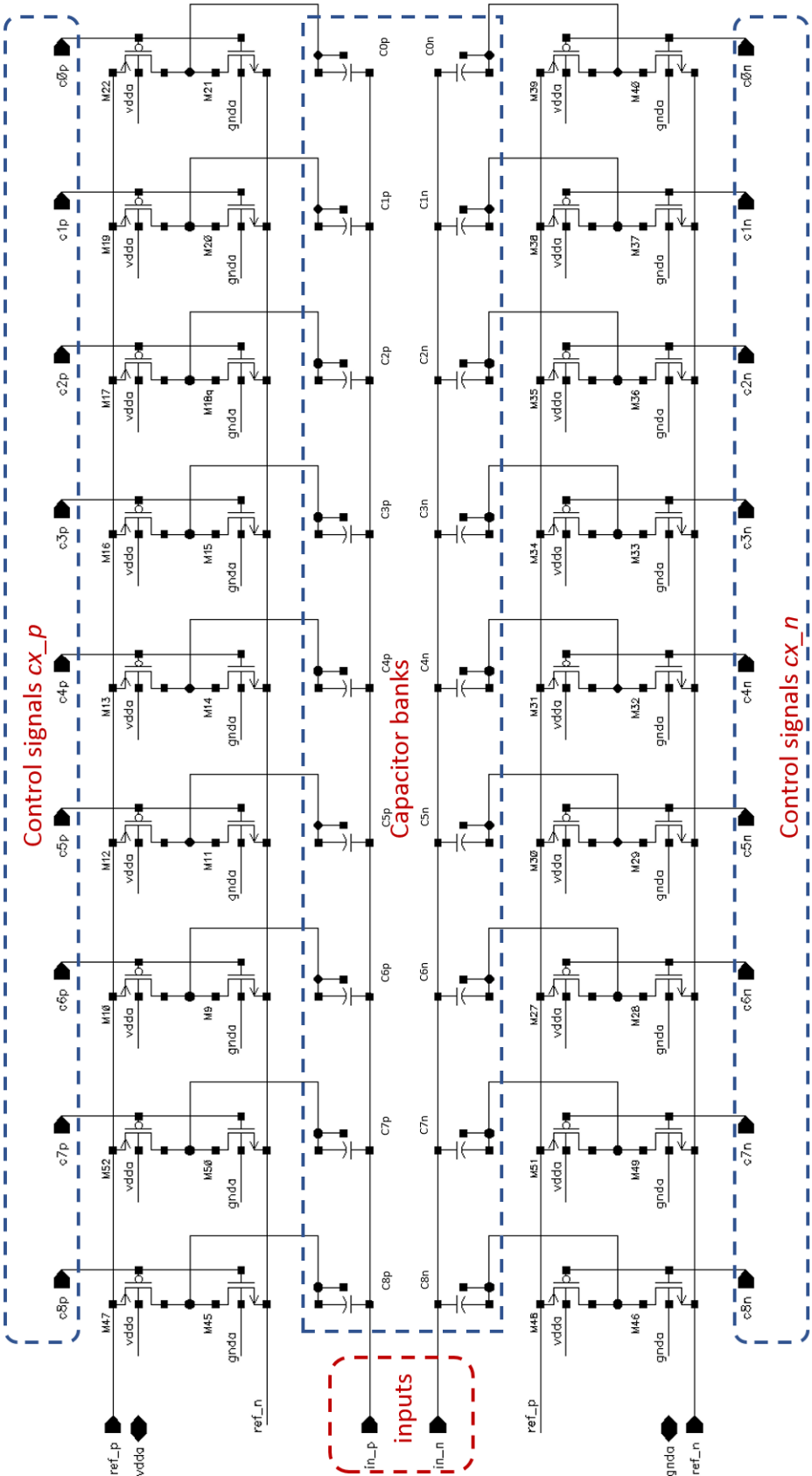


Figure 6.3: The SAR ADC capacitor banks.

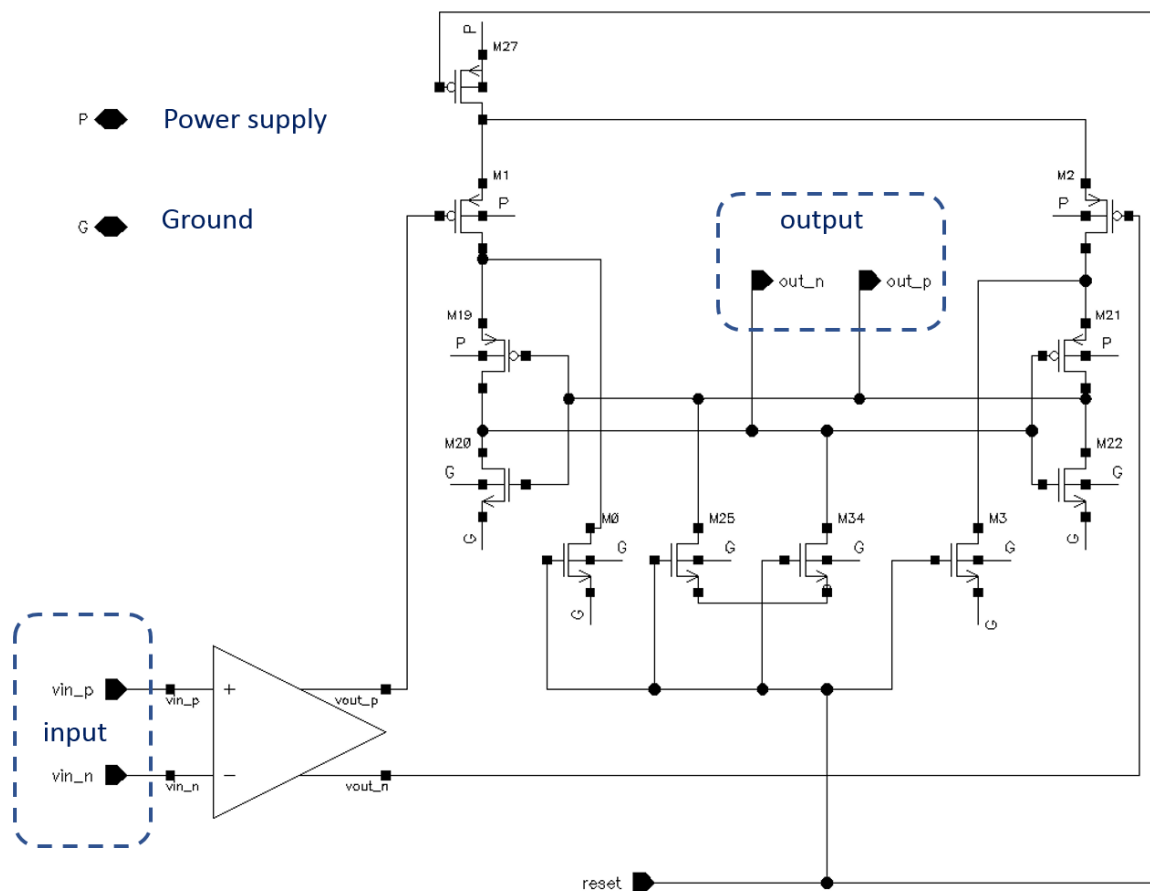


Figure 6.4: The comparator which is composed of a dynamic latch and a pre-amplifier.

6.2.4 The Dynamic-Latch Comparator

The dynamic-latch comparator used in the SAR design is shown in Figure 6.4. PMOS M1 and M2 act as input differential pair. Transistors M19 to M22 combine into a positive feedback loop, or a latch. Transistors M0, M3, M25, M34 and M27 are introduced to clean memory effects inside the circuit. All high-impedance points need to be set/reset to increase the comparison speed and prevent any memory effect from a previous comparison.

The dynamic latch is optimized to have a initial offset of around $8mV$. This offset is still too large and hence a pre-amplifier is added in front of the dynamic latch. The pre-amplifier provides 10 times gain and can therefore suppress the dynamic-latch offset by a factor of 10. The overall initial offset of the comparator is now below $0.8mV$. The LSB of the ADC is around $1.2mV$ and hence the overall offset of the comparator is around $LSB/2$ which is sufficient.

6.2.5 The Asynchronous SAR Logic

The design of the asynchronous SAR logic block is explained in Appendix C. In this section, the function of the self-timing asynchronous ring oscillator is explained in detail, because it is important for understanding the ADC timing issue due to ageing as discussed in Section 6.3.

The self-timing asynchronous ring oscillator is the loop which contains the comparator, two OR gates (OR1 and OR2) and a few delay cells in Figure 6.5. Another OR gate (OR3) can enable or disable this ring oscillator. The DAC control clocks (*Clk1* to *Clk10*) are generated by the D-flipflops on top of Figure 6.5. These DAC control clocks will be the feedback to the capacitor banks to control their switching.

The timing graph of its operation is shown in Figure 6.6. When the *ADC_sampling_clk* is 1, all outputs (*Clk1* to *Clk10*) of the D-flipflops are reset to 0. The output of OR3 is 1 and thus disables the ring oscillator. The comparator is kept in reset mode.

As soon as the *ADC_sampling_clk* falls to 0, the ring oscillator is enabled and as a consequence, the comparator is enabled. The comparator will compare its inputs and generate differential outputs. The *Valid* signal (in Figure 6.5) will be set to 1 as soon as the comparator outputs are available.

The *Valid* signal is also the clock signal of the D-flipflops. As a result, the output of the first D-flipflop, *Clk1*, will be switched from 0 to 1. The *Clk1* is the feedback to the capacitor banks and will start the switching of the MSB capacitor C8. The input voltages of the comparator will be changed due to the switching of the capacitor banks. At the same time, the *Valid* signal is propagated through the ring oscillator loop and resets the comparator. The *Valid* signal will be reset to 0, propagate after some delays, and enables the comparator again. Now a new cycle will start. The *Clk2* will be switched from 0 to 1 and the C7 in the capacitor banks will be switched etc.

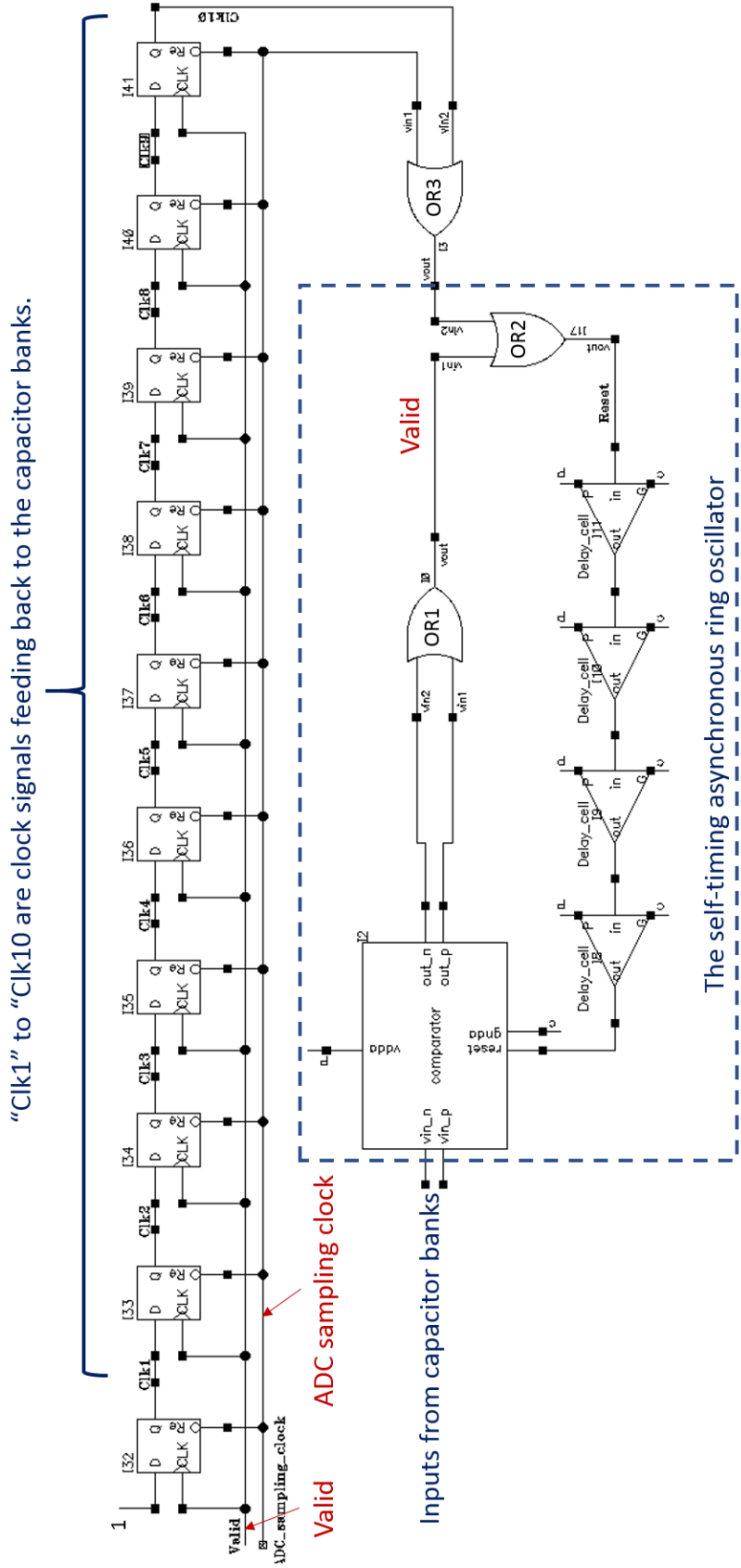


Figure 6.5: The asynchronous SAR logic.

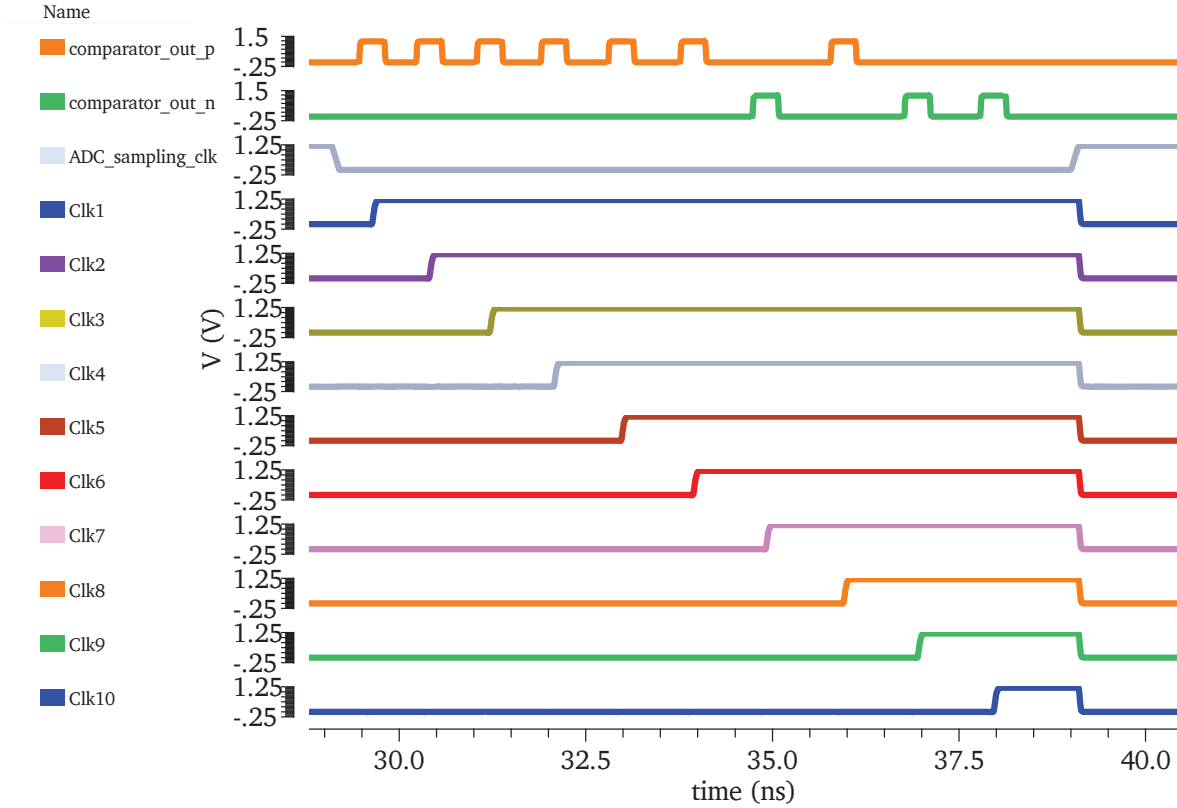


Figure 6.6: The asynchronous SAR logic signals generated by the circuits in Figure 6.5.

The procedure will continue until all DAC control clocks (*Clk1* to *Clk10*) are generated as shown in Figure 6.6. When the signal *Clk10* becomes 1, it will disable the ring oscillator via OR3. The self-timing asynchronous ring oscillator will be stopped.

The self-timing asynchronous ring oscillator can also be stopped/reset by the rising edge of *ADC_sampling_clk*, which is shown in Figure 6.6. Therefore, it has a penitential risk that the rising edge of *ADC_sampling_clk* arrives earlier than the rising edge of *Clk10*. In this case, the SAR ADC will not be able to generate all the bits and hence errors will occur. This is the main speed limitation for SAR ADCs. The designer must make sure that the sampling clock of the ADC is sufficiently slow to allow the asynchronous SAR logic to provide all its bits.

6.2.6 ADC Fresh Performance Simulation Results

The designed SAR ADC operates at a 1.25V power supply and V_{ref} is also 1.25V. This voltage is generated from a bandgap regulator. For a single-ended input, the SAR ADC has a full-scale range of 1.25V, while the LSB equals around 1.22mV. For full differential mode inputs, the SAR ADC can have a full scale range of 2.5V, which results its LSB will equal to 2.44mV. The

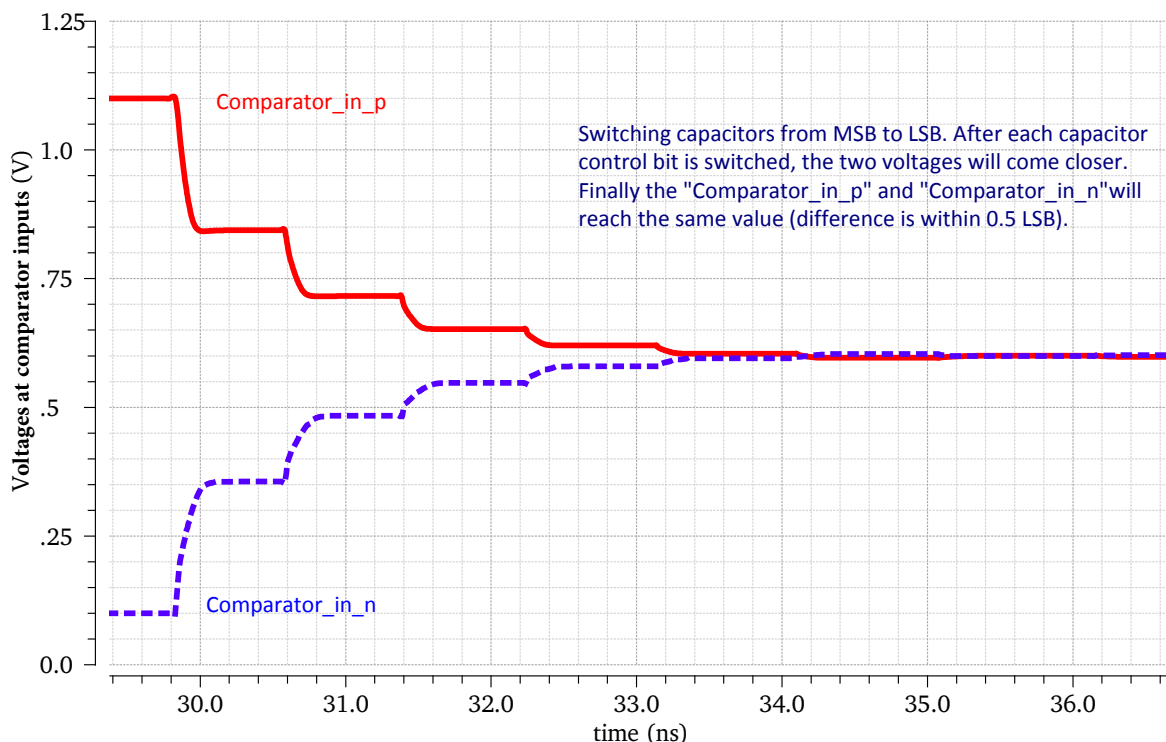


Figure 6.7: The voltage waveforms in the SAR ADC comparator inputs.

ADC accuracy is around 1mV and the SNR is 60dB which fulfils the 10-bits ADC requirements (theoretically, a 10-bits ADC can reach 61.96dB, but practically this number cannot be reached).

The ADC transient simulation for a 1V differential input with 0.6V common-mode voltage is shown in Figure 6.7. At the beginning, the input voltages of the comparator, *Comparator_in_p* and *Comparator_in_n*, are 1.1V and 0.1V respectively. They are the same as the ADC input voltages. The comparator starts to compare its two inputs and obviously the *Comparator_in_p* is larger than *Comparator_in_n*. As a result, after some delays, the SAR logic will provide feedback to switch the MSB of the capacitor banks in a way that the *Comparator_in_p* decreases with $V_{ref}/4$ (-0.25V) and *Comparator_in_n* increases with $V_{ref}/4$ (+0.25V). After the MSB of the capacitor banks is switched, the *Comparator_in_p* becomes 0.85V and *Comparator_in_n* becomes 0.35V as shown in Figure 6.7. A similar action will occur for the (MSB-1) bit. This time, *Comparator_in_p* will decrease with $V_{ref}/8$ (-0.125V) and *Comparator_in_n* will increase with $V_{ref}/8$ (+0.125V). The ADC will continue until all bits of the capacitor banks are switched, and the voltages of *Comparator_in_p* and *Comparator_in_n* will become closer and closer. This is shown at the right-hand side in Figure 6.7.

More simulation results of the fresh ADC will be shown in Section 6.3.

6.3 Reliability Issues for the Aged ADC

Due to its simplicity, low power and small area, SAR ADCs are attractive for today's safety-critical applications like in automotive and health-related products. Recently, much research has been carried out on self-calibrations of SAR ADCs, which are mostly focussed on passive capacitor banks inside SAR ADCs and the INL & DNL performance [Xu12, Um13, Wan14b]. However, about the ageing of a SAR ADC is rarely reported, which is more related to the active circuit parts and is also essential for safety-critical applications.

6.3.1 Reliability Simulations for the Ageing SAR ADC

NBTI is considered as the dominating ageing effect in 65nm CMOS technology. In this section, NBTI simulations have been carried out under a stress condition of 125°C, for a duration of 10 years. The ADC sample frequency is 50MHz and the ADC supply voltage is 1.25V. The NBTI model used is the one developed in Chapter 3 and implemented in Verilog-A.

The input buffer, bootstrapped switches, self-timing asynchronous SAR logic, and the comparator inside the SAR ADC have been simulated to investigate their ageing. The maximum differential input signal of 1V is used as the (stressed) ADC input during the NBTI simulations.

6.3.2 Input Buffer Ageing

The input buffer is used to supply sufficient current to charge the SAR ADC sampling capacitor banks. Sometimes the input buffer is not shown for the SAR ADC in an analogue front-end. Instead, the buffer function is combined with preceding instrumentation amplifiers and active filters. In this thesis, two unity-gain feedback OpAmps are used as input buffers to examine their ageing effects. The buffer design has been discussed in Section 6.2.1. Due to the unity-gain configuration, the two inputs of the OpAmp remain always at the same voltage, and the stress applied on the differential pair transistors is the same. Therefore the threshold degradations caused by NBTI in the OpAmps are well matched and the NBTI-induced offset is small. Moreover, the offset of the OpAmp will be reduced by the OpAmp gain due to the deep feedback. In this design, a 80dB rail-to-rail OpAmp has been used.

However, the two buffers have large differences in their inputs. The common-mode ageing which is expressed by gain degradation is not equal. This unequal gain degradation introduces gain mismatch for the two OpAmps. Figure 6.8 shows the differential voltage output of a buffer before stress (fresh) and after 10 years of ageing. The difference after stabilization is below 1mV. Compared to 0.5 LSB of the 10-bits ADC which is around 1mV, the NBTI ageing effect can be ignored. However, if the ADC resolution is higher than 10-bits, the 1mV error

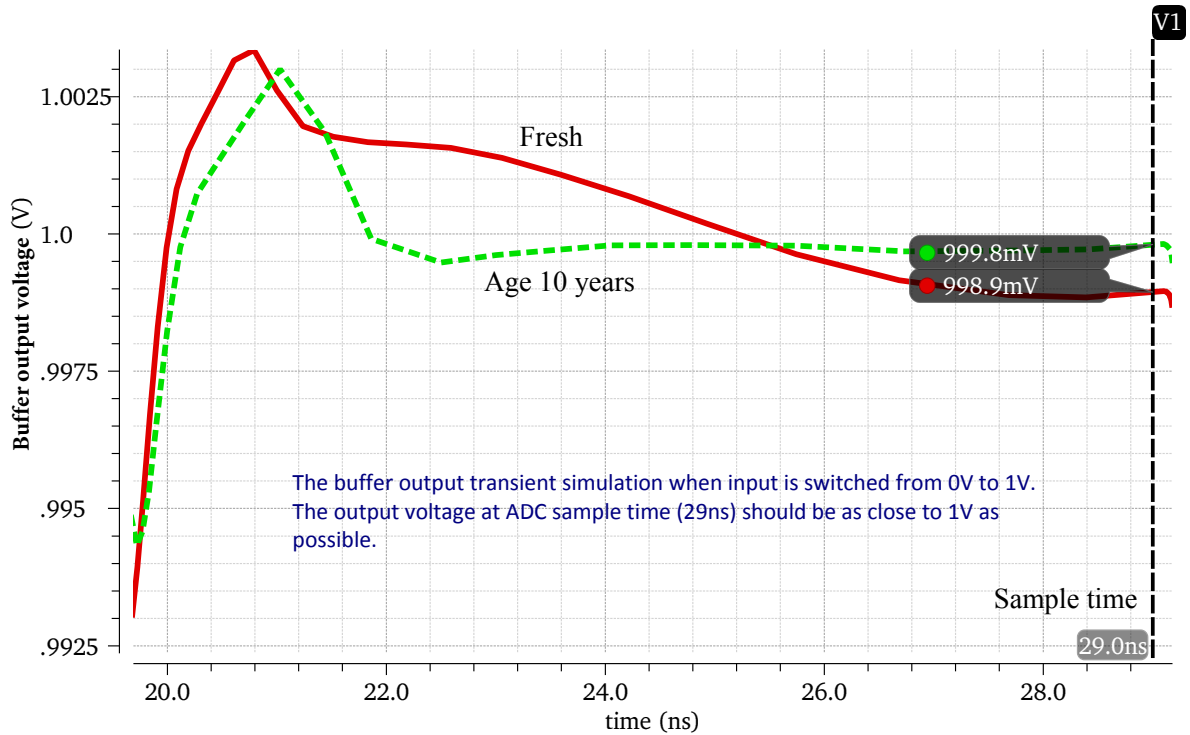


Figure 6.8: The buffer output voltage before and after ageing.

introduced by the input buffer can not be ignored. For a 14-bits [ADC](#), the $1mV$ error will be 8 [LSB](#), which is unacceptable because any errors introduced at the input buffer will be dominant and are difficult to remove by any following self-calibrations inside the [ADC](#).

6.3.3 The Ageing of the Bootstrapped Switches

The bootstrapped switches face the highest possible stress voltage (V_{dd}) applied to its switching transistor [[Abo99](#)]. If this switching transistor is a [PMOST](#), more than $20mV$ threshold voltage increase will be induced by [NBTI](#). This amount of threshold increase will decrease the on-resistance of the [PMOST](#) by more than 10%. The increased on-resistance will prolong the charging time to the sampling capacitor banks and therefore increase the sampling time. If the [SAR ADC](#) does not have sufficient design margin for the sampling time, the [ADC](#) accuracy will be significantly degraded.

Fortunately, most bootstrapped switches use an [NMOST](#) as the switching transistor. A similar bootstrapped switch used in our design has been shown in Figure 6.2. The [NMOST](#) will suffer from [PBTI](#) degradation which is less dominant. Hence [NMOSTs](#) remain unchanged in our [NBTI](#) simulations. The rest of the [PMOS](#) transistors in Figure 6.2 do suffer from [NBTI](#) degradation. These [PMOS](#) transistors act as digital switches and do not influence the gate

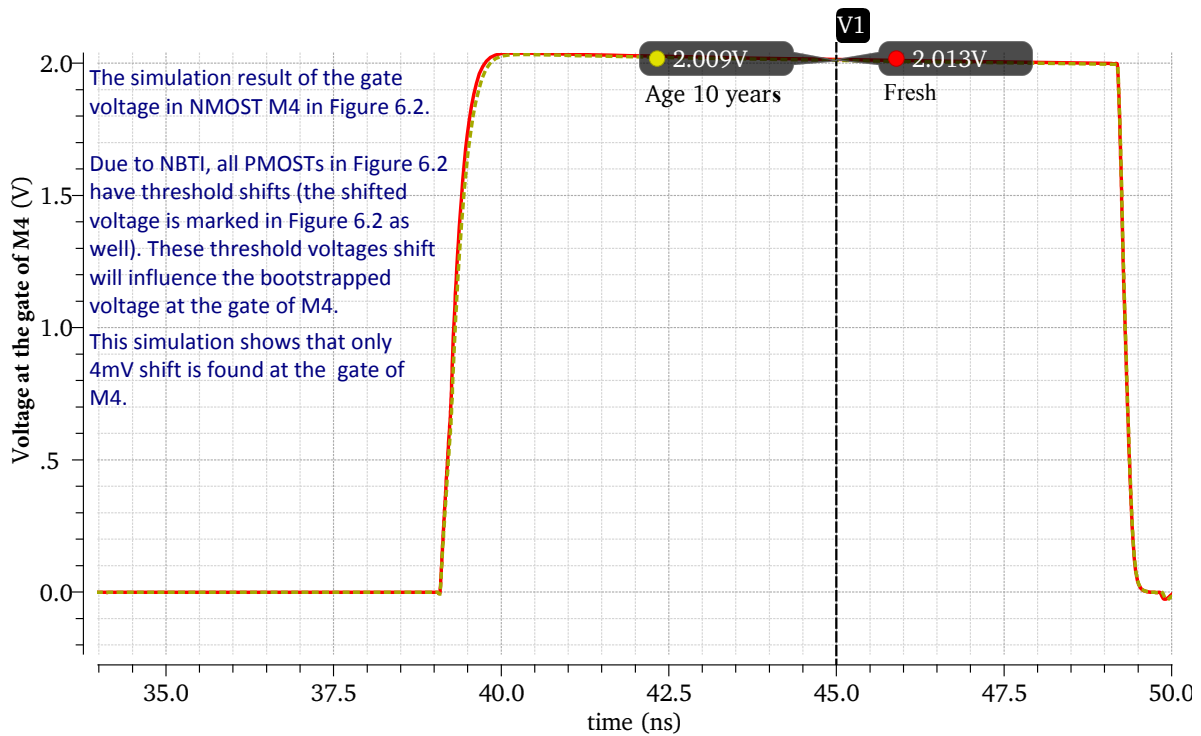


Figure 6.9: The simulated gate voltage on NMOST M4 in the bootstrapped switch which is shown in Figure 6.2 under fresh and aged conditions.

voltage of the bootstrapped switch, which is the NMOS transistor M4 in Figure 6.2. The gate voltage of the M4 is compared in Figure 6.9 in the case of fresh and 10-years of ageing. The change in the M4 gate voltage is 4mV and hence the influence on the M4 on-resistance is less than 1% which can be ignored.

However, with the CMOS technology entering 40nm and beyond, Positive Bias Temperature Instability (PBTI) becomes important for NMOS transistor ageing. Extra PBTI simulations should be carried out while designing bootstrapped switches in 45nm, 32nm and 22nm technologies.

6.3.4 The Ageing of the Capacitor Banks

Capacitors are passive components and not influenced by NBTI. The capacitor switches on the other hand are influenced by NBTI because they are realized by MOSTs. However, our simulations show almost no change in switching speed and “on” resistance. This is similar as the bootstrapped switches in the previous section.

6.3.5 The Ageing of the Dynamic-Latch Comparator

The comparator used in our design is a dynamic latch with a pre-amplifier, which has been presented in Section 6.2.4. The dynamic latch is optimized to have an initial offset of $8mV$. The pre-amplifier provides 10 times gain and can therefore suppress the dynamic-latch offset by ten times. The overall initial offset of the comparator is therefore below $0.8mV$.

The two inputs of the comparator normally have large voltage differences. This voltage difference will stress the input transistor pairs unequally and will introduce different threshold voltage changes. As a consequence, a large ageing-induced offset will occur in the comparator.

From our NBTI simulations, the offset of the dynamic-latch comparator is increased from $0.8mV$ to $5.5mV$ after 10 years, which is a 3 LSB offset error for the 10-bits SAR ADC. The influence can be seen from the overall ageing simulation of the ADC in next section.

If auto-zero offset cancellation [Che13] is used for the pre-amplifier, then the $4mV$ pre-amplifier offset can be removed. The total offset of the comparator will be $1.45mV$ which represents a 1 LSB offset error for the 10-bits SAR ADC.

Some high-speed ADCs only use a dynamic latch as comparator. Self calibrations such as digital tuning and charge-pump techniques [Asg18] are used to cancel the offset of the dynamic latch. Whether these techniques are effective to cancel the ageing-induced offset is dependent on their design. For example, if the calibration technique is designed to cover 2 LSB offset error and the offset induced by ageing is 3 LSB, it will not have sufficient offset-calibration range. The ageing-induced offset will introduce errors to the ADC such as DC offset errors.

6.3.6 The Ageing of the Asynchronous SAR Logic

The self-timing asynchronous SAR logic scheme has been presented in Section 6.2.5. Our ageing simulations show the delay of each stage inside the SAR logic is increasing with time under NBTI stress. After accumulating the delays of all stages, the total time which is required to complete one-period SAR operation is therefore prolonged. For each cycle, the delay increases by around $50ps$, which is a 6% decrease for the asynchronous clock signal frequency. The more bits a SAR ADC has, the more delay is accumulated in the SAR logic. For example, after 10 cycles of the asynchronous clock signal, the total delay induced by ageing has been increased to $0.5ns$. If the ADC has to operate at a high frequency, a $0.5ns$ delay increase in the SAR switching sequence could be critical since the SAR ADC may not complete the comparison of all bits before the next sampling clock cycle arrives. The ageing issues with regard to the SAR logic need to be taken into account at the moment the designers determine the design margins.

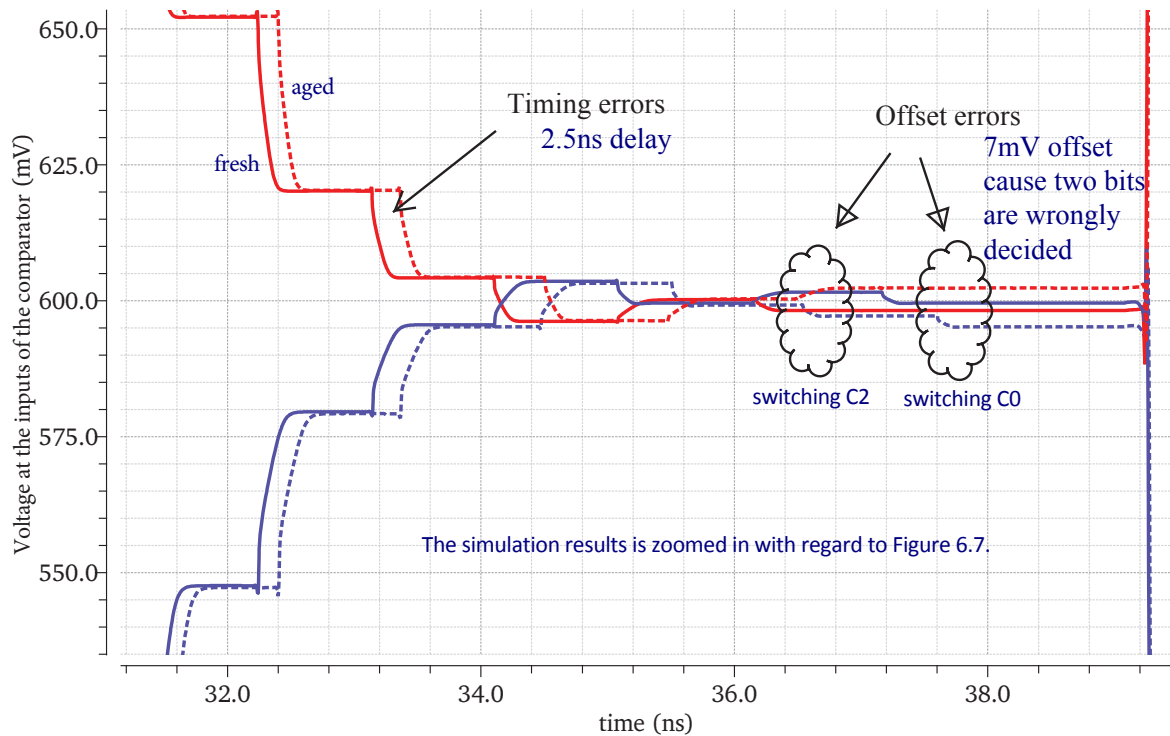


Figure 6.10: The SAR ADC voltage wave forms at the input of the comparator. Fresh simulation results and ageing simulation results are both provided.

6.3.7 The Overall SAR ADC Ageing

The NBTI influence on the overall performance of the ADC can be timing errors and offset errors. Example SAR ADC waveforms are shown in Figure 6.10. The timing error is mainly due to the increased delay from the self-timing asynchronous SAR logic. In each SAR bit switching, the delay is increased by about 50ps. After ten bits switching, the total delay has increased by more than 0.5ns. As a result, the maximum sample frequency of the SAR ADC has to be reduced from 55MHz to about 50MHz. Otherwise the last bit will be lost as explained in Section 6.2.5.

Figure 6.10 also indicates there are two decision errors due to the ageing-induced offset in the comparator. One error occurred while switching capacitor C2, and the other error took place while switching C0.

In the SAR ADC, the capacitor banks are switched in a way that the voltage difference of two inputs of the comparator will become less and less, as shown in Figures 6.7 and 6.10. In Figure 6.10, after switching C2, the voltage difference of the two inputs of the comparator became larger, which means the comparator made a wrong decision due to its offset. The same occurred during the switching of C0.

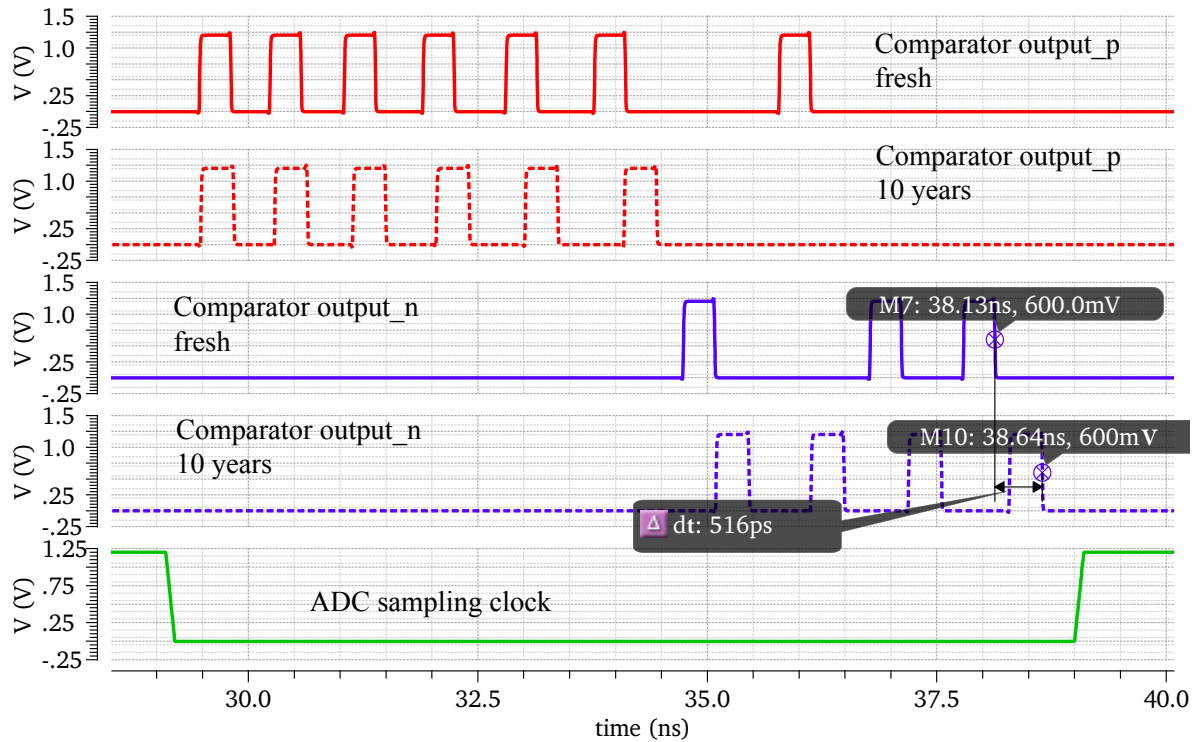


Figure 6.11: The SAR ADC voltage wave forms at the output of the comparator. Fresh simulation results and ageing simulation results are both provided.

The decision error in C2 introduces a 4 LSB error. The decision error in C0 introduces a 1 LSB error. In total they introduce a 5 LSB error at the ADC output.

The same timing errors and offset errors can be seen from the outputs of the comparator as well. In Figure 6.11, the red solid waveform and red dashed waveform are the *output_p* of the comparator before ageing and after ageing. A clear delay can be visible after ageing. Moreover, the dashed waveform is not the same pattern as the solid waveform in the last few cycles. This is because the comparator made wrong decisions due to its offset errors. The same story holds for the *output_n* of the comparator, which is shown in the blue solid waveform and blue dashed waveform in Figure 6.11.

6.3.8 Ageing Issues for SAR ADCs in General

The general SAR ADC can be simplified into the block diagram in Figure 6.12. Except the bandgap reference, all the other blocks will have similar ageing behaviours as has been shown in this chapter. As a result, the comparator and the asynchronous SAR logic are the most ageing sensitive blocks. Adding PBTI into the simulations will not change this conclusion.

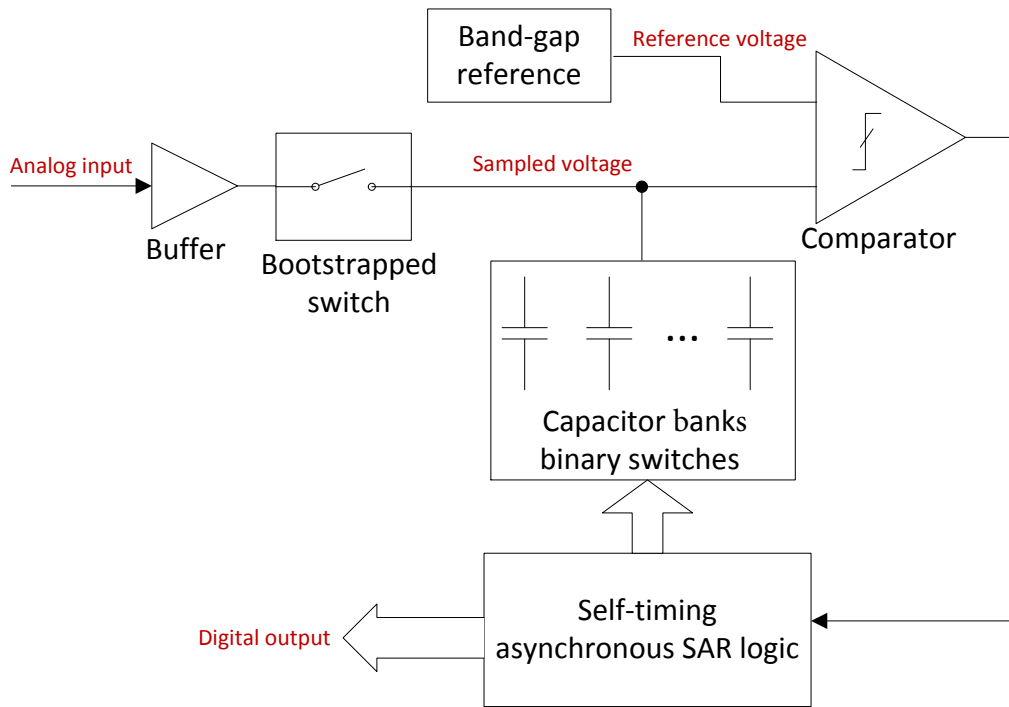


Figure 6.12: The general non-differential SAR ADC block diagram.

The bandgap reference has been simulated for its NBTI ageing performance in other papers [Lat11]. The results show that the bandgap reference has only a very small degradation which can be ignored in most cases.

The currently popular self-calibrated designs for SAR ADCs are focused on capacitor-banks mismatch. It will not solve ageing issues for SAR ADCs, especially for the SAR logic timing problem.

6.4 Highly Dependable ADCs

To prevent ageing-induced timing errors and offset errors, two options are available to designers. The first option is keeping sufficient margins during the design phase for both the maximum clock frequency and comparator-offset cancellation. This option will lead to more complicated designs and reduced performance in terms of frequency, area and power consumption.

Another option is the usage of **Embedded Instruments (EIs)**; they can be generalized and implemented as standard **IPs** and can save considerable design time in the future. Two **EIs** are proposed in the next sections to address both the **SAR ADC** timing and offset error.

6.4.1 Additional Effort During the Design Phase

The self-calibration design approach as discussed in [McN11] could be used to reduce the **NBTI**-induced offsets. However, these self-calibration circuits are not verified for ageing performance. Complicated self-calibration circuits could make the overall ageing of the **ADC** even worse.

A simple way to calibrate the **ADC** offset is to add a shorting circuit (by a switch) between the two input signals in front of the **ADC**. During calibration, the two inputs are shorted and thus become zero. Now the **ADC** output will consist of pure offset and noise. By averaging, the noise can be reduced and the offset can be extracted. This offset value can be stored inside the chip for future calibration.

The weak points for adding a shorting switch between the two (differential) **ADC** inputs are the circuits in front of the **ADC**. They are required to disable their output in order to prevent over-current stress. This will necessitate a proper system-level plan at the beginning of the design.

To avoid frequency degradation, sufficient design margin (at least 10%) seems to be the best option from a design point of view. To carry out burn-in ageing tests during the prototyping phase will be very helpful to determine the correct design margin.

6.4.2 The Usage of **Embedded Instruments**

The idea of an **EI** is to embed some form of test and measurement into silicon to characterize, debug and test chips. In this section, two embedded instruments for **SAR ADCs** focussing on **NBTI**-induced errors are introduced. They are an **EI** for detecting a timing error in the **SAR** logic and an **EI** for determining the **ADC** offset error.

An **EI for ageing-induced timing error detection**

The timing error can be detected by a **EI** as shown in Figure 6.13. The idea of the **EI** is to compare the "finish" signal of the **SAR** logic and the **ADC** sampling signal. If they are overlapping with each other, then an alarm signal will be raised which indicates the **SAR** logic speed is below the **ADC** sampling speed. The system should subsequently reduce the **SAR**

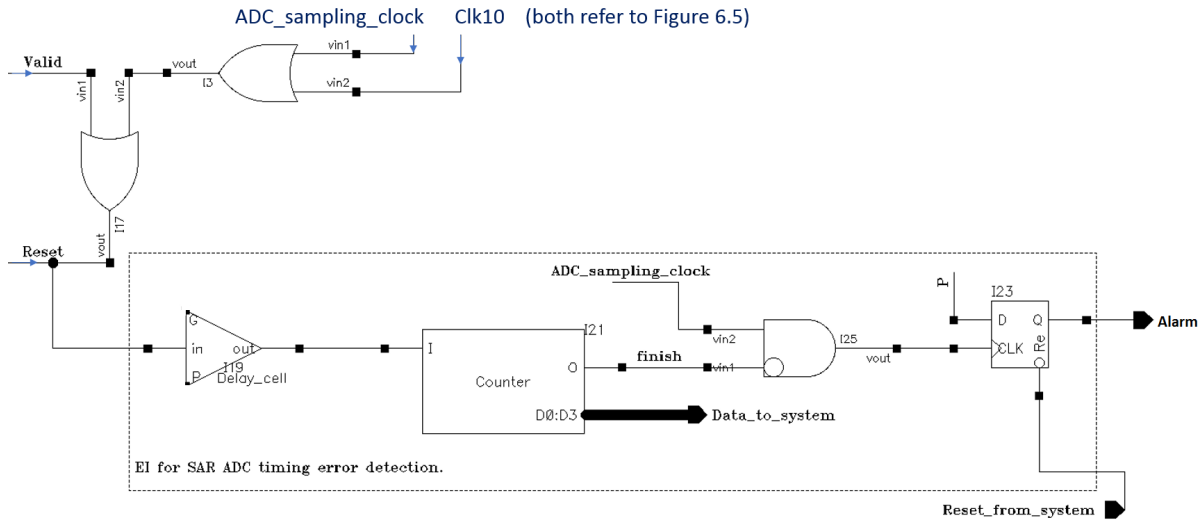


Figure 6.13: The EI for detecting timing errors in the asynchronous SAR logic.

ADC operating frequency, e. g. via a PLL, in order to avoid any data loss. The “finish” signal is generated by a counter, which counts how many asynchronous cycles have been successfully produced. For example, in our 10-bits ADC, the counter should count 10 asynchronous cycles before raising the “finish” signal. The delay cell at the input of the EI is to make sure the high logic level of the cycle has sufficient duration time. The reset D flip-flop stores the alarm signal until it is reset by the system.

If an alarm signal is flagged, the system can read the counter contents and verify how many cycles have been produced. Based on the counter information, the system can decide how to reduce the ADC sampling frequency (designer needs to leave some margin for reducing the frequency). This EI can also be used to detect the maximum operating frequency of the SAR ADC.

An EI for ageing-induced offset error detection

The offset error is caused by the increase of the offset from the comparator. It is more difficult to detect and requires a special EI. Our analogue EI to detect OpAmp offsets has been proposed in [Wan14a]. The same theory but realized in the digital domain instead of analogue circuits can also be used to detect ADC offsets. However, to fully realize this in the digital domain, our method requires two ADCs which will be only possible if the SoC has more than one ADC on-chip.

Figure 6.14 shows the configuration with two ADCs. They are switched to convert the same analogue input. The output digital data is processed using the EI theory as discussed in

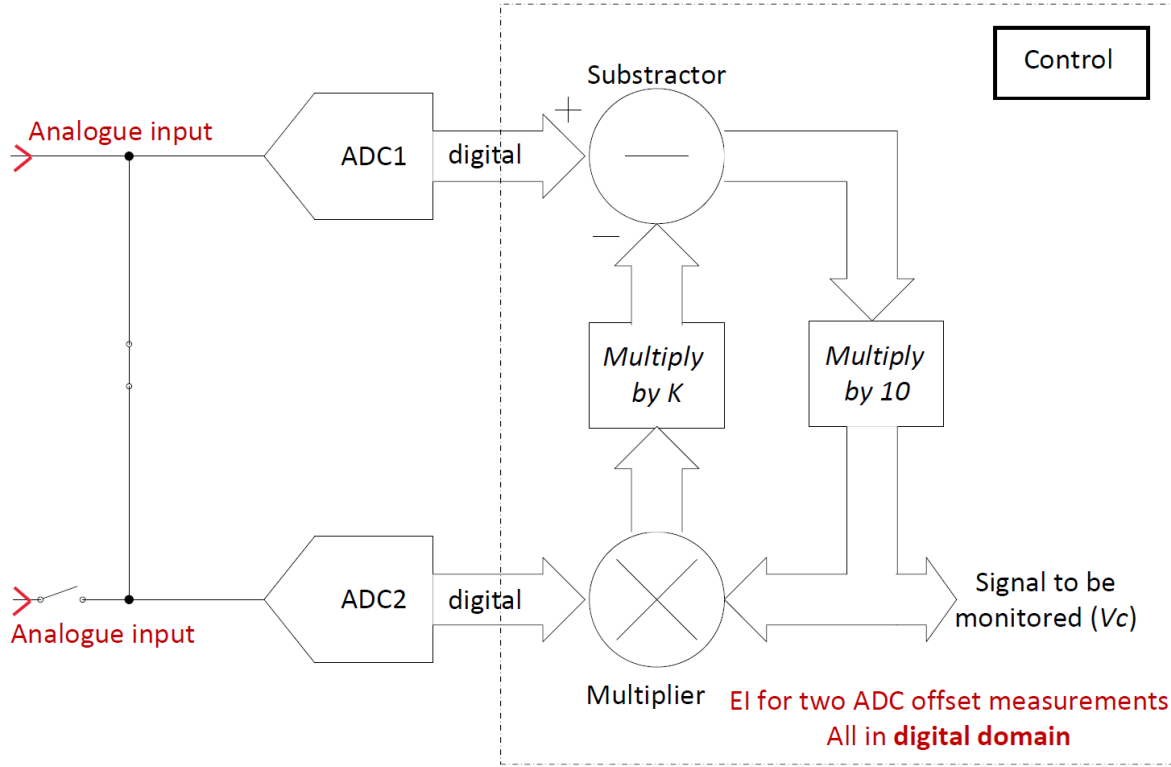


Figure 6.14: Two SAR ADCs are configured for an EI detecting both ADCs' offset errors.

Chapter 4. The multiplier, the programmable gain stage K and fixed 10 times gain stage can all be realized easily in the digital domain without any non-ideal effects. The multiplication is accurate and resident offsets will disappear. The unknown offsets are the offset V_{o1} for ADC1 and the offset V_{o2} for ADC2.

By changing the number K and monitoring the V_c results, it is possible to find a special K value which inverts the phase of V_c . This special K value can be expressed as K_{spec1} as provided in Eq. (6.1).

$$K_{spec1} = \frac{1}{10 \cdot (V_{o1} - V_{o2})} \quad (6.1)$$

After this, one multiplies the ADC1 output data with -1 , and inverts the inputs before the ADC2 (which means exchange the two inputs for a fully differential ADC case) and subsequently the same procedure is repeated. Another special K value can now be found and expressed as K_{spec2} in Eq. (6.2).

$$K_{spec2} = \frac{1}{10 \cdot (-V_{o1} - V_{o2})} \quad (6.2)$$

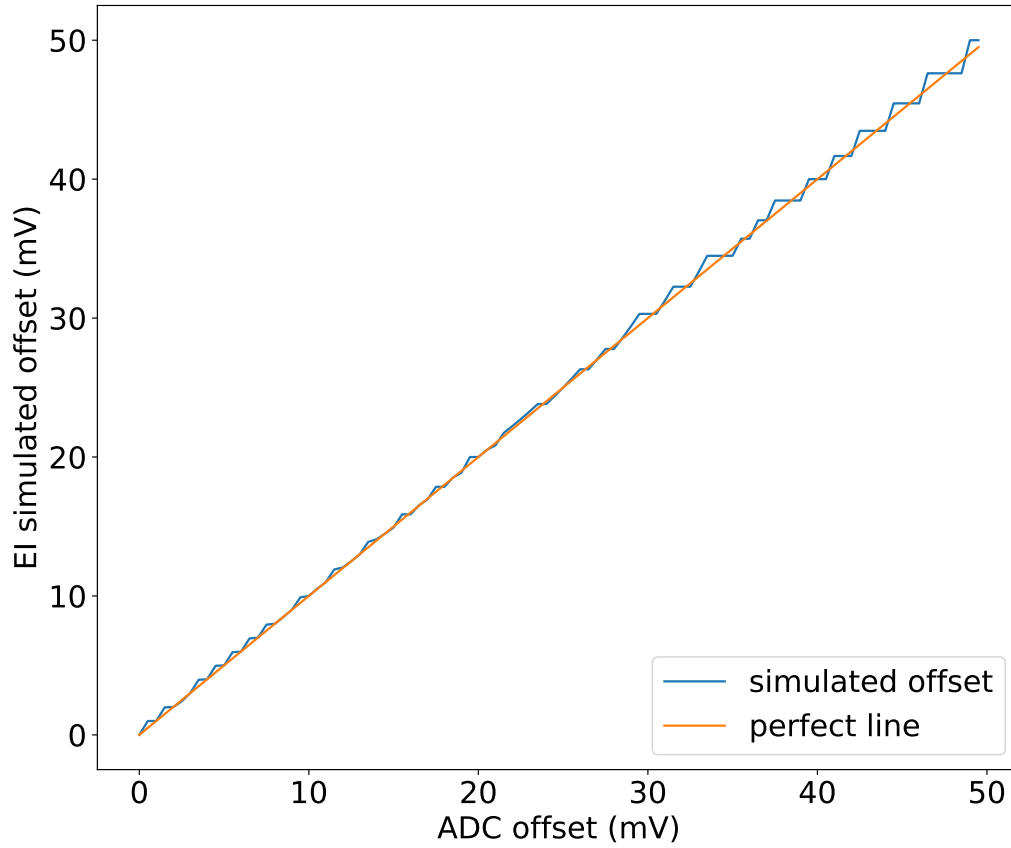


Figure 6.15: Matlab simulation of ADC offset EI.

By combining Eqs. (6.1) and (6.2), both offset voltages for the two ADCs can now be obtained. The theoretical offset error will be less than 1 LSB in this case. The actual error will be influenced by the linearity of the two ADCs and finite step size of K [Wan14a].

A Matlab simulation has been carried out with the proposed ADC offset EI. The parameter K is swept from -100 to 100 with step size of 0.1 . The offset of the ADC is set to be from 0mV to 50mV . The simulation result is shown in Figure 6.15 as the blue line. The orange line is the perfect line in the case of the simulation is exactly equal to the offset of the ADC (ideal case). The maximum error between the blue line and orange line is $1.12 * \text{LSB}$.

After the offsets of both ADCs are known, the system can calibrate the ADC digital output by adding/subtracting the corresponding offset numbers to the ADC output. The offsets of the ADCs, including the ageing-induced offsets will be removed in this way.

6.4.3 Comparison of the Two Approaches

The design-effort approach to improve the ageing behaviour of an ADC can lead to a more complicated design and a reduced performance in frequency, area and power consumption. Yet many companies proceed in this way and rely heavily on all kind of reliability tests like High Temperature Operating Life (HTOL), High Temperature Storage Life (HTSL), Highly Accelerated Temperature/Humidity Stress Test (HAST), Temperature Humidity Bias (THB) and so on [Aut07]. It generates a lot of design costs and a huge amount of test costs.

By using Embedded Instruments, the ADC can test itself during functional test as well as testing during lifetime as ageing monitors. (However, the product-level reliability tests, like HAST and THB are required mainly for package related issues. They cannot be replaced by the kind of EIs proposed in this thesis.) The increased area for the EIs can be reduced by sharing them among several ADCs. The EIs can be generalized in the future as a general library which can be shared in different products. The overall costs will be less as compared to the extra design-effort approach.

After measuring the time error and offset error by EIs, the required counter actions can be taken at the system level as for instance described in [Kha14].

6.5 Conclusions

A 10-bits fully differential SAR ADC target vehicle has been designed by ourselves and verified in 65nm CMOS technology because these databases could not be obtained from our cooperating companies and other partner organizations even after significant efforts. The NBTI ageing effect has been simulated after stressing the ADC at 125°C for 10 years. The NBTI simulations, using our NBTI model, show that after 10 years, the degradation in the input buffer and bootstrapped switches can be ignored. However, the asynchronous SAR logic and the comparator can be a problem with regard to NBTI. The NBTI increases the delay in the asynchronous SAR logic and gives cause to timing errors which can result that the least significant bits of the ADC are faulty. For the comparator, NBTI degradation has induced extra offset and causes a 5 LSB offset error in our ADC. Two embedded instruments have been introduced to detect both timing

errors as well as offset errors of the SAR ADC. After detection, counter actions can avoid the ageing effects.

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Chapter 7

Conclusions, Limitations and Recommendations

***Abstract-** In the final chapter of this thesis, conclusions from our research are provided. Original contributions are summarized and future research is recommended. Own publications are listed at the end.*

7.1 Introduction

In the previous chapters, the [NBTI](#) ageing modelling, ageing simulations and [Embedded Instrument \(EI\)](#) monitoring of [Analogue/Mixed-Signal \(AMS\)](#) circuit blocks inside [Analogue/mixed-signal Front-Ends \(AFEs\)](#) have been discussed. In this chapter, the final conclusions of the research are provided in Section [7.2](#). Subsequently, all original contributions of our research are presented in Section [7.3](#). Due to the limitations in time and resources, there are always items not included in this research and these result in recommendations for future work. The limitations and recommendations are provided in Section [7.4](#). As the last part of this chapter, all papers published by the author are listed.

7.2 Conclusions from this Research

Based on publications, the dominating ageing effect in 65nm [CMOS](#) technology is [NBTI](#). It manifests itself as an increase in the threshold voltage and consequent decrease in the drain current and transconductance of a [PMOST](#). Therefore, an arbitrary-voltage stressed ageing model for analogue circuits has been developed to facilitate ageing simulations on [AMS IPs](#).

From simulation results of AFEs, the offsets of OpAmps can increase, the bandwidth of OTA-C filters can be reduced and the offset errors and timing errors of SAR ADCs can be enlarged.

The AFEs can be made dependable by means of two approaches. The first is by allotting extra design effort which transforms each IP in AFEs to be self-testable and self-repairable. We have demonstrated this approach in the dependable OpAmp. However, it will significantly increase the complexity, power consumption and area of the analogue IP. If there are many different analogue IPs in the SoC, the cost will be very high. Moreover, the more complex the circuit, the more chance of failures will occur in the product, which will again reduce the dependability of the whole chip.

The other technique is to keep the original non-dependable analogue IP untouched and add EIs to monitor the performance of the IP during its life time. The self-repair is not necessarily done at IP level but can be realized at a higher level (software level) based on the parameters collected from the whole AFE. In this way, the EIs can be standardized and shared between different IPs. The repair is handled at the software level which provides much more flexibility than hardware solutions.

Moreover, the EI can not only be used for dependability purposes but can also be used during wafer test and final product test to reduce test complexity and test time.

As a result, regarding the overall solution for dependable AFEs, the EI solutions are recommended for self-test and system-level software trimming based self-repair.

7.3 Contributions

There are a number of original contributions from this thesis. These contributions address the research questions as mentioned in Chapter 1. They are provided and briefly explained below.

7.3.1 A Compact Arbitrary-stressed NBTI Model

In highly dependable application areas such as the automotive industry, accurate ageing simulations are in high demand to assure design success. One of the key problems for AMS ageing simulation, such as NBTI simulation, is the lack of accurate ageing models.

The NBTI degradation can partly recover after the source of the stress is removed, which makes both measurement and modelling very difficult. Despite much effort spent in NBTI

modelling theories, there is a big gap between modelling and simulation implemented in **SPICE**-like environments which are familiar to **AMS** circuit designers. In addition, **NBTI** modelling mainly focuses on **DC** stresses and square-wave stresses termed **AC** stress, which are not typical cases in **AMS** circuits.

In Chapter 3 of this thesis, a new compact **NBTI** model has been presented which can handle arbitrary stresses in analogue circuits. The model is suitable for **AMS NBTI** simulations in the environment of Cadence **ADE**. The new model is based on iteratively solving the **RD** equations in a smart way, such that it can achieve high accuracy with reduced computational effort [Wan13].

It has been evaluated for **CMOS** 140nm technology with square-wave stresses as well as arbitrary wave stresses. For a total of 82 silicon results, the model can match 86% of **AC** stresses as well as 70% of the **DC** stresses. The model has been implemented in Cadence **ADE** with Verilog-A, and can simulate both deterministic as well as stochastic **NBTI** ageing effects. The simulation speed is about a thousand times faster than for other **RD**-based models, and the speed is at the same level of regular transient simulations [Wan16].

The **NBTI** model and associated simulation method have been used as a fundamental tool in the thesis to examine the ageing of different **Analogue/Mixed-Signal** functional blocks.

7.3.2 A Drain Current Model for Nano-meter **MOSTs**

NBTI measurements are carried out by extracting threshold-voltages of **PMOS** transistors. Currently there are several methods to extract threshold-voltages. These methods rely on accurate **MOST** transistor drain-current models, and special equipment together with automatic control software. In the case the test is carried out on wafer, a special wafer-probe station is required. In short, **NBTI** measurements are difficult, expensive and time consuming.

In Chapter 3 of this thesis, a new closed-form model for the **MOST** drain current has been provided to facilitate **MOST** threshold-voltage measurements in nanometer **CMOS** technologies. The model is valid for all regimes, like the sub-threshold/weak-inversion, moderate-inversion, strong-inversion and the linear regime [Wan15b].

Measurements have been carried out in 90nm **CMOS** circuits. Results show that the model agrees with measurements. Threshold-voltage extraction using this new model can tolerate less accurate measurement results in the strong-inversion regime, which can be obtained by already existing general-purpose **ADCs** inside **SoCs**. It will reduce both complexity and cost of ageing measurements.

7.3.3 An Embedded Instrument to Measure MOST's Threshold Voltage

Based on the above MOST drain-current model, an EI has been designed to extract threshold-voltages on-chip and can thus be used as a low cost NBTI measurement solution as well as an NBTI on-chip monitor for the whole SoC (this thesis, Chapter 3).

The EI is based on measuring the MOST drain current under a resistor load in the saturation region, and calculate the threshold voltage by fitting the new drain-current model. The EI was tested in 90nm CMOS technology. Long-time stress tests show that the EI can characterize threshold-voltage shifts with a 3mV accuracy [Wan15a].

7.3.4 A Gain-Boosting Method for OpAmps

The technology employed for our circuit designs is 65nm low-power TSMC CMOS technology. This technology is optimized for low-power digital applications, not for high-performance analogue designs. The transistor intrinsic gain is only about 20dB. To achieve 100dB gain, the OpAmp needs at least 5 gain stages. If these 5 gain stages are in series, several Miller or other compensation circuits are required in order to guarantee both stability and fast settling-time. The unity-gain frequency of the 5-stage OpAmp will be very limited [Wan11].

In Chapter 4 of this thesis, a new gain-boosting method has been proposed to achieve both high gain and high bandwidth for the test-vehicle OpAmp. It applied an active-load like structure and makes use of matching in the two branches of the current mirror.

The designed OpAmp applies a constant- g_m rail-to-rail input stage with folding-cascode and a class-AB rail-to-rail output stage which uses folding-mesh summation. There are three gain-boosting techniques employed in the first stage. They are the folding cascode, the active cascode and the new gain-boosting techniques.

The final test-vehicle OpAmp achieved 104dB gain with a unity-gain frequency of 783MHz [Wan14b].

7.3.5 An Embedded Offset and Gain Instrument for OpAmps

Based on the NBTI simulation results, the most ageing-sensitive parameter in the OpAmp turns out to be the offset.

In Chapter 4 of this thesis, a new embedded offset and gain instrument for OpAmp IPs has been proposed based on a new measurement theory. The EI does not require to isolate the DUT from their connected feedback networks and other IPs. Neither does it need accurate

stimulation sources. This [EI](#) can self-calibrate its resident offsets in the digital domain after each measurement. The [EI](#) has been designed in the 65nm low-power digital [TSMC CMOS](#) process and provides an IEEE1687 interface.

The [EI](#) can be shared with other analogue [OpAmp IPs](#) to reduce the silicon area and shut down in idle situations to save power. The detection range is $200\mu V \sim 70mV$ for the offset and $0dB \sim 40dB$ for the gain [[Wan14a](#)].

7.3.6 An Embedded Instrument to Detect Ageing of [OTA-C](#) Filters

Active filters are widely used in [Analogue/mixed-signal Front-Ends](#) of, for instance, automotive mixed-signal [System-on-Chips](#). Due to harsh environments, in some cases degradation of these filters may be encountered during lifetime and hence distorted sensor information could be provided with potential fatal results.

The [OTA-C](#) filter has been found to be the most sensitive one to NBTI ageing in Chapter 5. Due to the reduction of transconductances in [OTAs](#), the $-3dB$ cut-off frequencies of [OTA-C](#) filters can be degraded by more than 10% and hence endanger sensor readings. This can potentially cause safety-critical issues in a car.

In Chapter 5 of this thesis, the design of a current [EI](#) has been presented in the same process as the filters and its capabilities have also been validated by simulations. The [EI](#) is based on monitoring the current of [OTA](#) input differential pairs and compares it with a threshold. In the case the current is reduced beyond the threshold, it will raise an alarm signal. Either car-console flagging or direct corrective actions at system level can be taken on the basis of this alarm signal.

The current-based [EI](#) is generic in its nature, and can hence also be used for other IPs [[Wan12](#)].

7.3.7 Embedded Instruments to Detect Offset Errors and Timing Errors in [SAR ADCs](#)

The [NBTI](#) ageing of our own-designed 10-bits [SAR ADC](#) in 65nm [CMOS](#) technology has been discussed in Chapter 6. It showed that [NBTI](#) mainly causes two kinds of degradations for the [SAR ADC](#), being timing errors and offset errors.

In Chapter 6, two new [EIs](#) have been designed to detect timing errors as well as offset errors.

The [EI](#) for timing errors has been implemented with pure digital logic. It counts the number of clock cycles that the asynchronous ring oscillator has generated and compares it with the rising edge of the [ADC](#) sampling clock. If the asynchronous ring oscillator becomes so slow that it can not generate all clock cycles before the rising edge of the [ADC](#) sampling clock, an alarm signal will be activated which requests the system to reduce the sampling frequency of the [SAR ADC](#).

The [EI](#) for offset errors implements the same idea as our [EI](#) to detect [OpAmp](#) offsets as discussed in Chapter 4. However this method requires two [ADCs](#) for realization, which will be only possible if the [SoC](#) has more than one [ADC](#) on-chip. As compared to the [OpAmp](#) offset [EI](#), the [ADC](#) offset [EI](#) is much simpler in hardware and only requires two switches. All calculations are carried out in the digital domain instead of the analogue domain. After detection, simple counter actions like subtraction can eliminate the ageing effects [[Wan15c](#)].

7.4 Limitations and Recommendations for Future Research

Due to time and resource limitations, there are currently unavoidable gaps in our research.

First, we have used 65nm [CMOS](#) technology as the basis for all our research. At this moment, it is not the most advanced technology and although not used in this thesis, we have already provided a 40nm [NBTI](#) model for other European projects. However, many automotive semiconductor companies have transferred to 28nm and even 16nm [FinFETs](#). For these more advanced technologies, not only [NBTI](#) but also [PBTI](#) and [Channel Hot-Carrier \(CHC\)](#) need to be taken into account in the case of simulating the circuit-block ageing behaviours.

Second, the [NBTI](#) model we used is based on the [RD](#) theory. Recently the other theory, the two-stage model theory, seems to become increasingly popular. We have not tested the two-stage [NBTI](#) model nor compared it with our model.

Third, the thesis is mainly focussed on how to test or monitor the performance parameters which are sensitive to ageing. The repair part has received less attention. System-level repair methods have been suggested in the PhD thesis of A. Khan [[Kha14](#)].

The last limitation is that we haven't built all [AMS IP](#) blocks into a complete [AFE](#). No tape out and measurements have been performed.

Based on the limitations mentioned above, for future research, it is recommended to focus on the following areas:

- The first area of interest are the **Embedded Instruments**. **EIs** are a clear trend in **SoC** design not only for dependability purposes but also for the sake of testing. It is recommended to build a library of complete solution of **EIs** for **SoC** test as well as dependability.
- Second suggestion is to use the latest semiconductor technologies like **FinFETs** to check their ageing behaviour of **AFEs**, like **NBTI**, **PBTI**, **CHC** and so on. They should be compared with the 65nm results in this thesis.
- Third is to update the latest modelling theory of **NBTI/PBTI**. It should be applied to simulations and compared with the **RD** model which has been used in this thesis.
- The last recommendation is to tape out a complete test-vehicle **AFE**, develop software-based repair mechanisms and perform reliability tests on real silicon to validate our dependability solution for **AFEs** in actual hardware/software.

Reliability and ageing of **ICs** in automotive applications is at this moment in the centre of interest (Semiconductor Engineering, June 17th, 2019 by: Ann Steffora Mutschler; Semiconductor Engineering, February 12th, 2019 by: Ed Sperling and Susan Rambo), and will provide room for many research projects to come.

List of Our Publications

- [Wan11] J. Wan and H. G. Kerkhoff. “Boosted gain programmable Opamp with embedded gain monitor for dependable SoCs”. In *International SoC Design Conference (ISOCC)*, pp. 294–297. 2011.
- [Wan12] J. Wan and H. G. Kerkhoff. “Monitoring active filters under automotive aging scenarios with embedded instrument”. In *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 1096–1101. 2012.
- [Wan13] J. Wan and H. G. Kerkhoff. “An arbitrary stressed NBTI compact model for analog/mixed-signal reliability simulations”. In *International Symposium on Quality Electronic Design (ISQED)*, pp. 31–37. 2013.
- [Wan14a] J. Wan and H. G. Kerkhoff. “An embedded offset and gain instrument for OpAmp IPs”. In *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 1–4. 2014.
- [Wan14b] J. Wan and H. G. Kerkhoff. “The influence of No Fault Found in analogue CMOS circuits”. In *IEEE International Mixed-Signal, Sensors, and Systems Test Workshop (IMS3TW)*, pp. 1–6. 2014.
- [Wan15a] J. Wan and H. G. Kerkhoff. “Embedded instruments for enhancing dependability of analogue and mixed-signal IPs”. In *IEEE International New Circuits and Systems Conference (NEWCAS)*, pp. 1–4. 2015.
- [Wan15b] J. Wan and H. G. Kerkhoff. “New drain current model for nano-meter mos transistors on-chip threshold voltage test”. In *IEEE European Test Symposium (ETS)*, pp. 1–6. 2015.
- [Wan15c] J. Wan and H. G. Kerkhoff. “Reliability of SAR ADCs and associated embedded instrument detection”. In *IEEE International Mixed-Signal, Sensors, and Systems Test Workshop (IMS3TW)*, pp. 1–6. 2015.
- [Wan16] J. Wan, H. G. Kerkhoff, and J. Bisschop. “Simulating NBTI degradation in arbitrary stressed analog/mixed-signal environments”. *IEEE Transactions on Nanotechnology*, volume 15(2), pp. 137–148, 2016.

Appendix A

The RelXpert Algorithm and AgeMOS model in Cadence ADE

RelXpert uses its own model to simulate [NBTI](#), which is called AgeMOS model. Unfortunately, Cadence has not published any details of the AgeMOS model. Here the AgeMOS model is described which was concluded from the following practical exercise.

For [NBTI](#) degradation, there are two parameter sets in the AgeMOS model of RelXpert. One set is called “[NBTI](#) life time parameters”. They are used to calculate the “Age” of the transistor, which is a special value defined in RelXpert and expressed in Eq.(A.1):

$$Age = \left[nba \cdot \exp\left(-\frac{nbea}{kT}\right) \cdot \exp(nbgamma \cdot V_{gs}) \cdot t^{nbn} \right]^{\frac{1}{nbn}} \quad (A.1)$$

The parameters nba , $nbea$, $nbgamma$ and nbn are RelXpert life-time parameters. Among them, nba is the [NBTI](#) scale factor for permanent damage over one year. Parameter $nbea$ is the [NBTI](#) activation energy for permanent damage, while $nbgamma$ is the [NBTI](#) oxide-voltage factor for permanent damage. Finally, nbn is the [NBTI](#) time dependency exponent for permanent damage. Parameter k is the Boltzmann constant and T is the absolute temperature in degrees Kelvin. Furthermore t is the stress time in seconds, V_{gs} the maximum average voltage from the gate-to-source, gate-to-drain and gate-to-body voltage, which is obtained from transient simulations.

The other set of parameters are called “[NBTI](#) AgeMOS parameters”. They are used together with “Age” to calculate the exact aged threshold-voltage. The algorithm of the AgeMOS model in RelXpert is shown in Eq.(A.2) and Eq.(A.3):

$$V_{th0_aged} = (1 + D) \cdot V_{th0_fresh} \quad (A.2)$$

$$D = nd1_vth0 \cdot Age^{nn1_vth0} + nd2_vth0 \cdot Age^{nn2_vth0} + ns_vth0 \cdot \left(nd1_vth0 \cdot Age^{nn1_vth0} \right) \cdot \left(nd2_vth0 \cdot Age^{nn2_vth0} \right) \quad (A.3)$$

The parameters $nd1_vth0$, $nd2_vth0$, $nn1_vth0$, $nn2_vth0$, and ns_vth0 are RelXpert AgeMOS model parameters. The parameter values of $nd1_vth0$ and $nn1_vth0$ in the AgeMOS model can be calculated from Eq.(A.4) and Eq.(A.5).

$$nd1_vth0 = \frac{1}{V_{th0_fresh}} \quad (A.4)$$

$$nn1_vth0 = nbn \quad (A.5)$$

The RelXpert Commands Menu can be set as shown in the Figure A.1.

Set RelXpert Commands

Command File

Simulator User Command Line Option

ENABLE MOS HCI/NBTI MODULE ☒

MOS HCI/NBTI Mode ☐ HCI and NBTI ☐ HCI only ☒ NBTI only

MOS HCI/NBTI Aging Time (s)

Min Age Threshold

Age Method

Domain

Effective Model Calc. ☐

Vth values ☐ calculate ☒ from spice

Lifetime Calc. ☐

Degradation Criterion

Output Options ☐ Sort Devices ☐ Output (Isub/Ids)max
☐ Print Total Isub ☐ Plot Total Isub
☐ Print Total Igate ☐ Plot Total Igate

Allow Modify ☐ voltages for aging simulation

Accuracy

AgeModel Limit ☐

Total Num.

Quantization Method ☒ age ☐ degradation

Id Method

Lifetime Method ☒ calc ☐ table

Lifetime Table File

Output Device Deg. ☐

Vdd value

Specify Spice Path ☐

Spice Path

Dump AgeModel ☐

Figure A.1: The Cadence RelXpert Commands Menu and relevant parameters.

Appendix B

Verilog-A Programme for the New NBTI Model in Cadence ADE

```
// VerilogA for phd_opamp, new_nbti_model, veriloga.
// Made by Jinbo Wan @ Utwente
// Version 1.0
/////////////////////////////////////////////////////////////////
`define DISPLAY_INFOR 1

`include "constants.vams"
`include "disciplines.vams"

module new_nbti_model (d, g, s, b, delta_Vth_detailed,
    ↪ delta_Vth_extraplotted, gnd_nbti);

    inout d, g, s, b, gnd_nbti;
    output delta_Vth_detailed, delta_Vth_extraplotted;
    electrical d, g, s, b, delta_Vth_detailed,delta_Vth_extraplotted,
    ↪ gnd_nbti;

    // Branch diclaration.
    branch (d, g) dg;
    branch (s, g) sg;
    branch (b, d) bd;
    branch (s, b) sb;
    branch (b, g) bg;
```

```

branch (delta_Vth_detailed, gnd_nbti) delta_vth_out;
branch (delta_Vth_extraplotted, gnd_nbti) delta_vth_fitted;

//parameters related to the size of the transistor-----to determine
  ↳ the Vth0.
parameter real Width = 500n from [1.2e-7:0.000900000001];
parameter real Length = 120n from [6e-8:2.000001e-5];

// parameters related to the NBTI measuremnts calibration.
parameter real K_1 = 100*3e4 from [0:inf); //  $C^{(-0.5)} \cdot nm^{(-2.5)}$ 
parameter real E_01 = 0.335 from [0:inf); // V/nm
parameter real E_a = 0.49; // Thermal activation energy

// parameters related to transistor physics.
parameter real EOT = 1.5; // nm
parameter integer time_point_limitation = 20000; // Limit the maximum
  ↳ transient simulation time point.

// Aging requirements.
parameter real years = 10; // Aging years.

parameter integer detail_sim_done = 0;
// 0: The detailed NBTI simulation has NOT been done! Doing the detailed
  ↳ NBTI simulation first and then fitting the power function.
// 1: The detailed NBTI simulation has been done and power function
  ↳ fitting parameter is calculated. The aged netlist will be
  ↳ calculated based on the parameters from "wib_nbti.txt".
// 2--inf : The same as 1 but add Poisson distribution of aging
  ↳ statistic. Taking into account the statistic effect of NBTI. That
  ↳ means even stress at the same conditions, the transistors could
  ↳ ageing differently.

// Variables

```

```

real    Vth0, e_ox, C_ox, C, V_stress, M_stress, d_stress, b_stress,
    ↪ last_time, temp1, temp2, n_fitting, a_fitting, lnx, lny, lnxlny,
    ↪ lnx2;
real    q_c, k_0, e_0, t_ox;
real    delta_Vth[0:time_point_limitation];
real    N_it[0:time_point_limitation];
real    delta_t[0:time_point_limitation];
real    t_abs[0:time_point_limitation];

integer wjb, wjb_i, wjb_x, wjb_n, wjb_file, wjb_file_infor,
    ↪ t_abs_last_zero;

real    a_from_file, n_from_file;
real    delta_vth_from_file, poisson_delta_n, gen_delta_n;

integer poisson_seed;

////////////////////////////////////
// Program start
analog begin

    if (detail_sim_done!=0) begin
        @(initial_step) begin
            poisson_seed = $random*detail_sim_done;
            q_c = 1.6e-19; // C is the unit of charge: Coulomb
            e_0 = 8.854e-21; // F/nm
            t_ox = EOT;
            e_ox = 3.9*e_0;

            wjb_file = $fopen("%I_wjb_NBTI.txt", "r");
            $fscanf(wjb_file, "n_fitting=%g a_fitting=%g",
                ↪ n_from_file, a_from_file);

            delta_vth_from_file = a_from_file*pow(years*365*224*60*60
                ↪ , n_from_file);

```

```

        poisson_delta_n = (1e18)*delta_vth_from_file*e_ox*Width*
        ↪ Length/(q_c*t_ox*2.7);

        if (detail_sim_done==1) gen_delta_n = delta_vth_from_file
        ↪ ;
        else    gen_delta_n = poisson_delta_n==0 ? 0 :
        ↪ $rdist_poisson(poisson_seed, poisson_delta_n)*(q_c*
        ↪ t_ox*2.7)/(e_ox*Width*Length*(1e18));
    end

    V(delta_vth_fitted) <+ gen_delta_n;

    @(final_step("tran")) begin
        `ifdef DISPLAY_INFOR
            $display("Attention!!_The_detailed_NBTI_simulation
            ↪ _is_not_done._If_you_have_changed_the_
            ↪ _schematics,_this_will_give_you_wrong_results
            ↪ _!!\n");
            $display("instance_name=_\"%M\"_\\t\\t_n_fitting=_\"%
            ↪ _g\\t\\t_a_fitting=_\"%g\", n_from_file,
            ↪ a_from_file);
            $display("Deterministic_Vth_shift_is:_\"%g._\\t_
            ↪ Random_Vth_shift_is:_\"%g\\n\",
            ↪ delta_vth_from_file, gen_delta_n);
        `endif
    end
end

else begin

    V(delta_vth_out) <+ 0;
    q_c = 1.6e-19; // C is the unit of charge: Coulomb
    e_0 = 8.854e-21; // F/nm
    k_0 = 8.617e-5; // eV/K
    t_ox = EOT;

```

```

e_ox = 3.9*e_0;
C_ox = e_ox/t_ox;
C = exp(-E_a/(k_0*$temperature));

case (1)
    ((Width>=1.2e-7)&&(Width<=3e-7)&&(Length>=6e-8)&&(Length
    ↪ <=9.999946e-8)) : Vth0 = 0.34168801;
    ((Width<=6e-7)&&(Width>3e-7)&&(Length>=6e-8)&&(Length
    ↪ <=9.999946e-8)) : Vth0 = 0.36316023;
    ((Width>6e-7)&&(Width<=1e-6)&&(Length>=6e-8)&&(Length
    ↪ <=9.999946e-8)) : Vth0 = 0.4183589;
    ((Width<=1e-5)&&(Width>1e-6)&&(Length>=6e-8)&&(Length
    ↪ <=9.999946e-8)) : Vth0 = 0.36983935;
    ((Width>1e-5)&&(Width<=0.000900000001)&&(Length>=6e-8)&&(
    ↪ Length<=9.999946e-8)) : Vth0 = 0.37118957;

    ((Width>=1.2e-7)&&(Width<=3e-7)&&(Length<=2.399996e-7)&&(
    ↪ Length>9.999946e-8)) : Vth0 = 0.42302095;
    ((Width<=6e-7)&&(Width>3e-7)&&(Length<=2.399996e-7)&&(
    ↪ Length>9.999946e-8)) : Vth0 = 0.41517553;
    ((Width>6e-7)&&(Width<=1e-6)&&(Length<=2.399996e-7)&&(
    ↪ Length>9.999946e-8)) : Vth0 = 0.42448966;
    ((Width<=1e-5)&&(Width>1e-6)&&(Length<=2.399996e-7)&&(
    ↪ Length>9.999946e-8)) : Vth0 = 0.43718619;
    ((Width>1e-5)&&(Width<=0.000900000001)&&(Length<=2.399996e
    ↪ -7)&&(Length>9.999946e-8)) : Vth0 = 0.43586814;

    ((Width>=1.2e-7)&&(Width<=3e-7)&&(Length>2.399996e-7)&&(
    ↪ Length<=1.002493e-6)) : Vth0 = 0.40428089;
    ((Width<=6e-7)&&(Width>3e-7)&&(Length>2.399996e-7)&&(
    ↪ Length<=1.002493e-6)) : Vth0 = 0.4015281;
    ((Width>6e-7)&&(Width<=1e-6)&&(Length>2.399996e-7)&&(
    ↪ Length<=1.002493e-6)) : Vth0 = 0.43560449;
    ((Width<=1e-5)&&(Width>1e-6)&&(Length>2.399996e-7)&&(
    ↪ Length<=1.002493e-6)) : Vth0 = 0.3990933;

```

```

((Width>1e-5)&&(Width<=0.000900000001)&&(Length>2.399996e
    ↪ -7)&&(Length<=1.002493e-6)) : Vth0 = 0.40092504;

((Width>=1.2e-7)&&(Width<=3e-7)&&(Length<=1.000249e-5)&&(
    ↪ Length>1.002493e-6)) : Vth0 = 0.39822143;
((Width<=6e-7)&&(Width>3e-7)&&(Length<=1.000249e-5)&&(
    ↪ Length>1.002493e-6)) : Vth0 = 0.39511135;
((Width>6e-7)&&(Width<=1e-6)&&(Length<=1.000249e-5)&&(
    ↪ Length>1.002493e-6)) : Vth0 = 0.39111725;
((Width<=1e-5)&&(Width>1e-6)&&(Length<=1.000249e-5)&&(
    ↪ Length>1.002493e-6)) : Vth0 = 0.40577219;
((Width>1e-5)&&(Width<=0.000900000001)&&(Length<=1.000249e
    ↪ -5)&&(Length>1.002493e-6)) : Vth0 = 0.40465395;

((Width>=1.2e-7)&&(Width<=3e-7)&&(Length>1.000249e-5)&&(
    ↪ Length<=2.000001e-5)) : Vth0 = 0.39886347;
((Width<=6e-7)&&(Width>3e-7)&&(Length>1.000249e-5)&&(
    ↪ Length<=2.000001e-5)) : Vth0 = 0.39586;
((Width>6e-7)&&(Width<=1e-6)&&(Length>1.000249e-5)&&(
    ↪ Length<=2.000001e-5)) : Vth0 = 0.39498798;
((Width<=1e-5)&&(Width>1e-6)&&(Length>1.000249e-5)&&(
    ↪ Length<=2.000001e-5)) : Vth0 = 0.40568103;
((Width>1e-5)&&(Width<=0.000900000001)&&(Length>1.000249e
    ↪ -5)&&(Length<=2.000001e-5)) : Vth0 = 0.40478507;

Width<1.2e-7, Width>0.000900000001, Length<6e-8, Length
    ↪ >2.000001e-5 : $display("Error!_Width_or_Length_
    ↪ of_the_PMOS_out_of_limitation!");
default $display("Error!_Error!_Width_and_Length_are_
    ↪ illegal!");
endcase

```

```

////////////////////////////////////
// Transient simulation-----Normal step:

```

```

if (analysis("tran")) begin

    V_stress = max(max(max(V(sg),V(bg)),V(dg))-Vth0, 0);
    M_stress = pow(K_1,2)*C_ox*V_stress*sqrt(C)*exp(2*(
        ↪ V_stress/t_ox)/E_01)/pow(0.9373,3);
    delta_t[wjb] = $abstime - last_time;
    t_abs[wjb] = $abstime;
    d_stress = - M_stress*sqrt(delta_t[wjb]);

    if (wjb>1) begin

        b_stress = 0;

        for (wjb_i=1; wjb_i<=wjb-1; wjb_i=wjb_i+1) begin

            temp1 = 0;
            temp2 = 0;

            for (wjb_x=wjb_i; wjb_x <=wjb; wjb_x=wjb_x
                ↪ +1) begin
                temp1 = delta_t[wjb_x] + temp1;
            end

            temp2 = temp1 - delta_t[wjb_i];
            b_stress = b_stress + N_it[wjb_i]*sqrt(
                ↪ delta_t[wjb])*(1.0/sqrt(temp1) - 1.0/
                ↪ sqrt(temp2));

        end

        if (d_stress==0) N_it[wjb] = -b_stress;

        else N_it[wjb] = -b_stress/3.0 + pow(-pow(
            ↪ b_stress,3)/27.0 - d_stress/2.0 + sqrt(pow(
            ↪ (pow(b_stress,3)/27.0 + d_stress/2.0),2) -
            ↪ pow(b_stress,6)/729.0) , 1/3.0) + pow(-pow(

```

```

        ↪ b_stress,3)/27.0 - d_stress/2.0 - sqrt(pow(
        ↪ (pow(b_stress,3)/27.0 + d_stress/2.0),2) -
        ↪ pow(b_stress,6)/729.0) , 1/3.0);

    end

    else if (wjb==1) begin

        N_it[1] = pow(M_stress*sqrt(delta_t[1]), 1/3.0);

    end

    delta_Vth[wjb] = q_c*t_ox*N_it[wjb]/e_ox;
    V(delta_vth_out) <+ delta_Vth[wjb];
    wjb = wjb + 1;
    last_time = $abstime;

end

////////////////////////////////////
// Transient simulation-----Final step:
// Least Squares fitting----power function: y=a*t^n
    @(final_step("tran")) begin

        lnx = 0;
        lny = 0;
        lnxlny = 0;
        lnx2 = 0;
        t_abs_last_zero = 0;

        for (wjb_n=1;wjb_n<=wjb-1;wjb_n=wjb_n+1) begin

            if (delta_Vth[wjb_n]!=0) begin
                lny = lny + ln(delta_Vth[wjb_n]);
            end
        end
    end

```



```

        lnx = lnx + ln(t_abs[wjb_n] - t_abs[
            ↪ t_abs_last_zero]);
        lnxlny = lnxlny + ln(delta_Vth[wjb_n]) * ln
            ↪ (t_abs[wjb_n] - t_abs[t_abs_last_zero
            ↪ ]);
        lnx2 = lnx2 + pow(ln(t_abs[wjb_n] - t_abs[
            ↪ t_abs_last_zero]), 2);
    end
    else begin
        t_abs_last_zero = wjb_n;
        lnx = 0;
        lny = 0;
        lnxlny = 0;
        lnx2 = 0;
    end
end

n_fitting = ((wjb-1-t_abs_last_zero)*lnxlny - lnx*lny)/((
    ↪ wjb-1-t_abs_last_zero)*lnx2 - pow(lnx,2));

if (n_fitting==0) a_fitting =0;
else a_fitting = exp((lny - n_fitting*lnx)/(wjb-1-
    ↪ t_abs_last_zero));

//
wjb_file = $fopen("%I_wjb_NBTI.txt");

if (wjb_file !=0 ) begin
    $fwrite(wjb_file, "n_fitting=%g\ta_fitting=%g",
        ↪ n_fitting, a_fitting);
    $display("If_no_error_reported,%M_NBTI_
        ↪ degradation_information_has_been_written_to_
        ↪ file:%M_wjb_NBTI.txt\");
end
else $display("Error!_Can_not_open_file:%M_wjb_NBTI.txt"
    ↪ );

```

```

$fclose(wjb_file);

//
`ifdef DISPLAY_INFOR
    $display("%M---The last zero point in the stress
    ↪ signal is: -%d---", t_abs_last_zero);
    $display("%M---Number of points in the stress
    ↪ signal is: ---%d---", wjb-1);
    $display("%M---n_fitting is
    ↪ :-----%g---",
    ↪ n_fitting);
    $display("%M---a_fitting is
    ↪ :-----%g---",
    ↪ a_fitting);
    $display("%M---Vth0 calcaulted from Width and
    ↪ Length is: ---%g---", Vth0);
`endif
//

wjb_file_infor = $fopen("All_wjb_NBTI.txt");

if (wjb_file_infor!=0 ) begin
    $fwrite(wjb_file_infor, "instance=%Mn_fitting
    ↪ =%ga_fitting=%g\n", n_fitting,
    ↪ a_fitting);
    $display("If no error reported, all PMOS NBTI
    ↪ degradation information has been written to
    ↪ file: \"All_wjb_NBTI.txt\"");
end
else $display("Error! Can not open file: All_wjb_NBTI.txt
    ↪ ");

$fflush(wjb_file_infor);

```

```
// $fclose(wjb_file_infor); // If add this one to close writing file "  
    ↪ All_wjb_NBTI.txt", spectre will report error... Nocloud what  
    ↪ happens.  
  
    end  
  
    end  
  
end  
  
endmodule  
/////////////////////////////////////  
  
'ifdef DISPLAY_INFOR  
'undef DISPLAY_INFOR  
'endif
```


Appendix C

The SAR ADC logic

The SAR ADC logic mentioned in Chapter 6 is further explained in this appendix. The top-level schematics of the SAR ADC is shown in Figure C.1.

The ADC is composed of input buffers, bootstrapped switches, charge-redistribution capacitor banks, a comparator and asynchronous SAR control logic.

The asynchronous SAR control logic is composed of a self-timing asynchronous ring oscillator, and a DAC control-clocks generation; furthermore it incorporates DAC control blocks which control the switching of the capacitor banks, a 10-bits subtractor and a 10-bits output register.

The SAR ADC digital output is processed by a 10-bits subtractor and stored in a 10-bits output register and the ADC results processing block. The reason for using the 10-bits subtractor is that the SAR ADC we designed is not the same as conventional SAR ADCs. After completing the SAR procedure, the two capacitor banks will generate 10-bits data each. Therefore one has two 10-bits data information. The subtractor subtracts the upper 10-bits data from the lower 10-bits data and generates 11-bits information (10 bits plus 1 borrowing). The lowest bit of the 11 bits data is always "1" and therefore disregarded. The remaining 10 bits will be sent to the digital output register of the ADC.

In the case the ADC sampling clock signal changes from low to high, the ADC will transfer its 10-bits digital number to the output and waits for the DSP/CPU read out. At the same time, a new round of sampling and holding is activated.

Each capacitor requires one DAC control block to control its switching and at the same time it outputs digital bits. There are nine capacitors which require switching (C0 to C8). Therefore nine DAC control blocks are required to control these capacitors. One additional DAC control block controls nothing and is just used to output the LSB after all capacitors have been switched.

The circuits inside the DAC control block are shown in Figure C.2. According to the comparator output, the switch-control signal is either set to 1 or reset to 0. However, the actual switch only switches to either high or low in the case the corresponding clock signal arrives. In the case the clock signal is not ready, the switch control signals will keep their previous values. Since one capacitor has been split into two halves, the switch control signal also has two outputs cx_p and cx_n . The two outputs do not have the same logic. It is referred to the cells in front of the two D_buffers of signals cx_p and cx_n in Figure C.2.

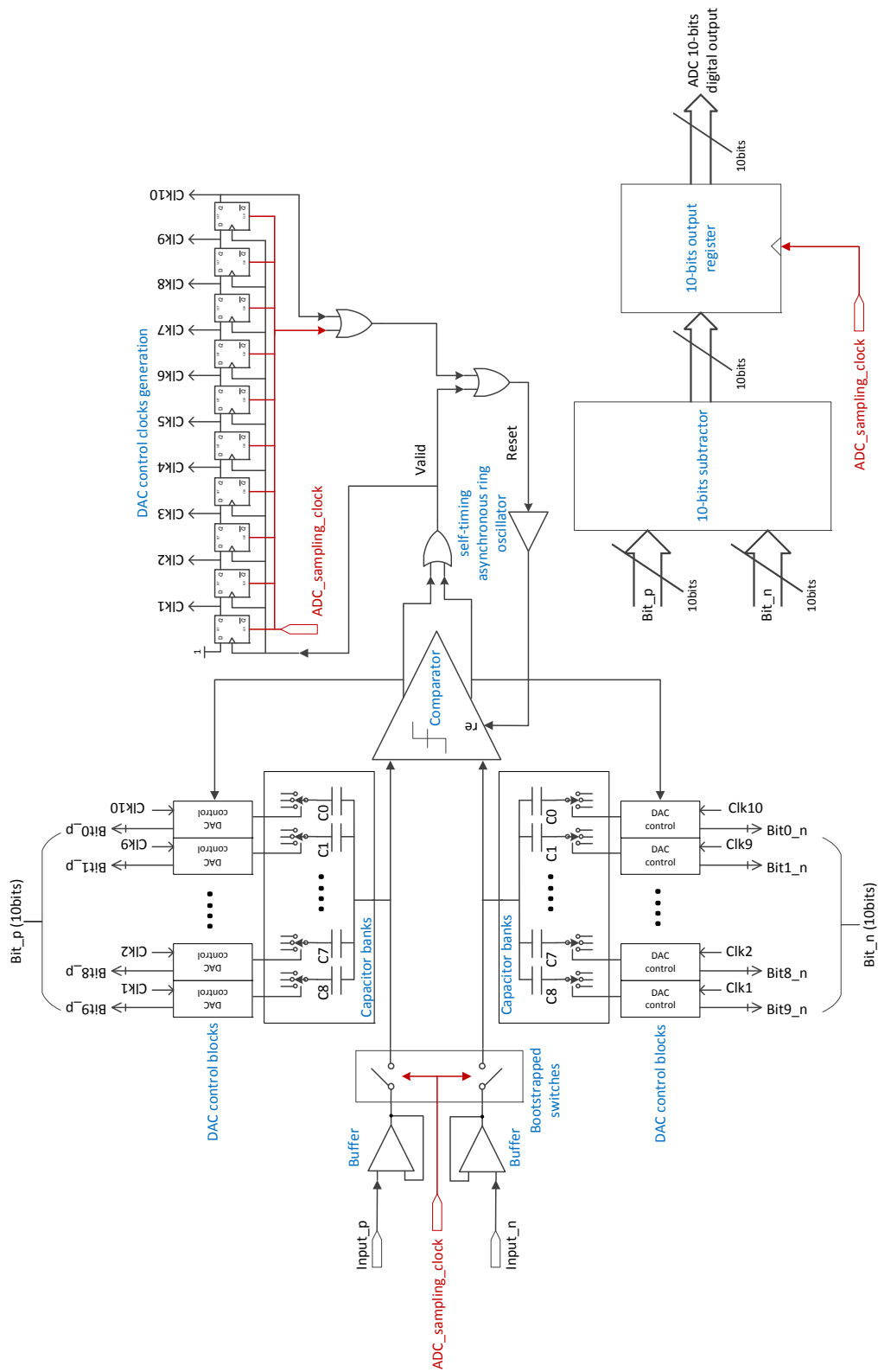


Figure C.1: The top-level schematics of the designed SAR ADC.

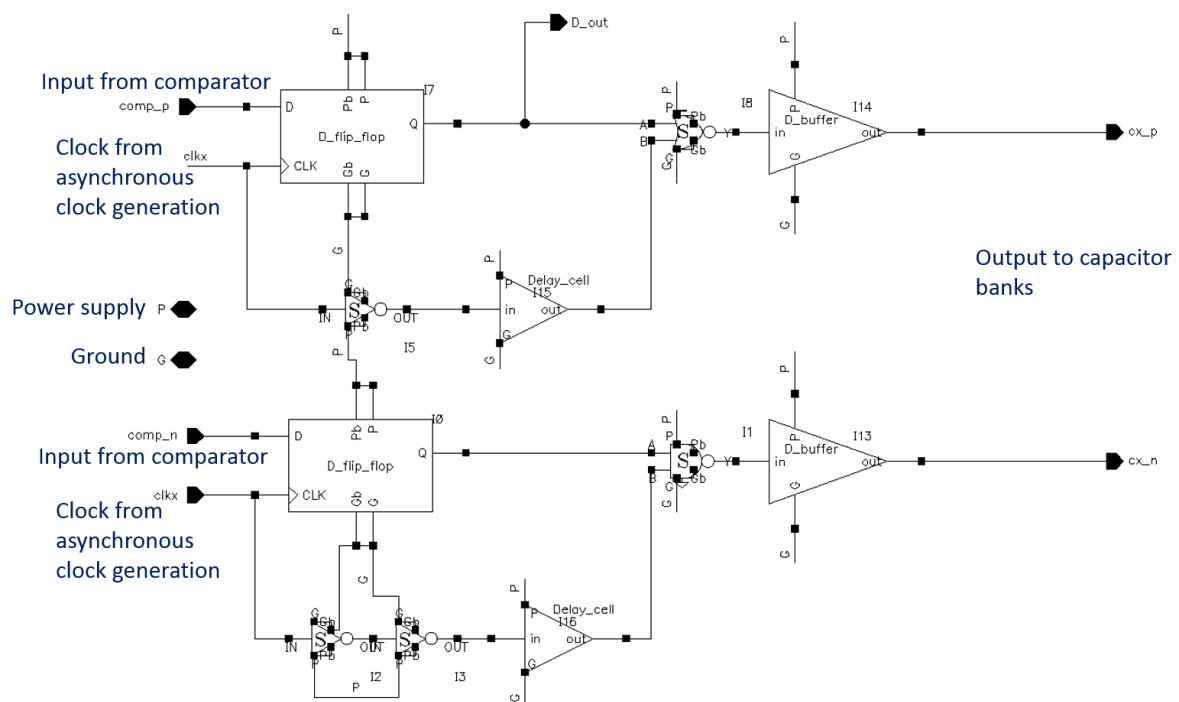


Figure C.2: The DAC control block in detail.