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Influence of Interface Recombination in Light Emission from Lateral Si-based Light Emitting Devices

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The influence of interface recombination on the electroluminescence profile of a lateral $p^+/p/n^+$ light emitting diode fabricated on Silicon On Insulator (SOI) materials has been experimentally investigated. Our device resembles a MOSFET fabricated on SOI (1), except that the source region has opposite doping to the drain. By controlling the voltage bias at the poly gate on top of active emitting region in association with a bias on the silicon substrate under the active region we were able to diminish the non-radiative recombination component at Si/SiO_2 interface and therefore enhance the radiative recombination in the thin film SOI. When the diode is working under constant current condition, we observe an increased light output of ~ 20 % as the gate and/or the substrate are biased negatively. The intensity profile across the device is also strongly influenced. To understand the device thoroughly, the structure has also been simulated showing agreement with experimental results.

Introduction

The need for an efficient and fast light emitter that can be intimately integrated with silicon integrated circuitry is unquestionable. The use of silicon itself as the light emitting material is one of the approaches to the problem. However, the indirect band gap of silicon is the fundamental obstacle that requires a workaround to achieve sufficient efficiency and speed of operation.

SOI materials have vastly increased their role in modern IC industry thanks to its clear advantages over conventional silicon wafers. An SOI substrate consists of a thin single-crystal, defect-free sheet of silicon sitting on top of an insulator. This isolation of the thin silicon sheet (called device layer) from the bulk by the buried oxide (BOX) layer is very appropriate for realizing novel-concept devices. The use of this material for realization of silicon light emitters has been reported to be of importance for the confinement of free carriers in one dimension in order to increase the band-to-band recombination probability (2-3). Moreover, using a vertical electric field to modulate the carrier profile in the active region to favor radiative recombination is an immediate other solution for realizing an efficient lateral diode. The SOI wafers used in this research have a silicon device layer thickness of a few hundred nanometer which can be easily regulated by an electric filed using a MOS gate and/or the handle substrate. Previously reported devices (3-4) are in fact similar lateral P-I-N diodes, however the advantage of having a MOS gate was not available.

The temperature effect in range of 253 - 473 K on electroluminescence from the fabricated lateral diodes also showed very interesting behaviors.

This paper discusses the idea of our approach, then the fabrication of the devices, followed by characterization, observed phenomenon and the explanatory arguments.

Experimental

A. Device Fabrication

The starting material is 100 mm SIMOX SOI substrate, with a silicon layer and buried oxide (BOX) layer of 190 nm and 350 nm thick, respectively. The device layer is p-type silicon of resistivity of 20 Ω cm^{-1}. First a high quality oxide layer of 34 nm was grown in a furnace at 950 ^{o}C, followed immediately by deposition of 50 nm stoichiometric Si_3N_4. Then silicon islands were formed on the substrate by a first mask step to etch away the Si_3N_4 and SiO_2 stack, selective etching in TMAH 10 % solution will etch the silicon layer into islands. Implantation of BF^{+}_{2} and As^{+} with the same doses of 3 x 10^{15} ions/cm^2 was used to respectively to make the p+ and n+ contact regions. The top Si_3N_4 layer was then removed and 300 nm poly-silicon gate was deposited. The poly-silicon layer was doped by Phosphorus ion implantation with a dose of 4 x 10^{15} ions/cm^2 at 65 kV. Dopant activation was processed by furnace anneal at 950 ^{o}C for 50 minutes. Final steps are shaping the poly-silicon layer, dielectric inter-layer deposition, contact hole etching and metallization by sputtering of Ti/W barrier layer and Al (1% Si).

B. Measurement Setup

The measured device is sketched in Figure 1. The length of the active region is varied from 3,5 μm to 25 μm. Compared to a conventional MOSFET fabricated on SOI, the difference is at the source region where silicon has opposite doping to the drain.

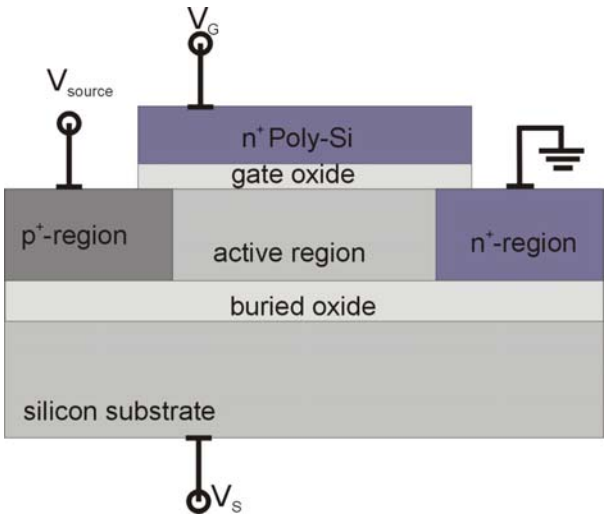

Figure 1. Cross-section of the light-emitting device.

In operation, the drain is grounded, the source is connected to a current source, the gate and the substrate are separately controlled by two voltage sources. To investigate the influence separately, either gate or substrate is grounded. When a current is supplied to the device, photon emission is observed by means of an infrared camera. An image of photon emission over the active region of the device is shown in Fig. 2. This device has

no top polysilicon gate and the active region is a rectangle. The two intense regions at the top and bottom ends are the exposed edges of the device where photons see a larger escaping angle. The right and left edges show the enhanced emission at the p^+/p and p/n^+ junctions. It has been known that the p^+/p always shows stronger intensity compared to the other junction. This is understood by the fact that electrons have higher mobility than holes, thus under a certain injection level, therefore the hole concentration at the p^+/p junction is always higher than that at the p/n^+ junction while the electron concentration difference between the junctions is small. Device simulation supports this explanation.

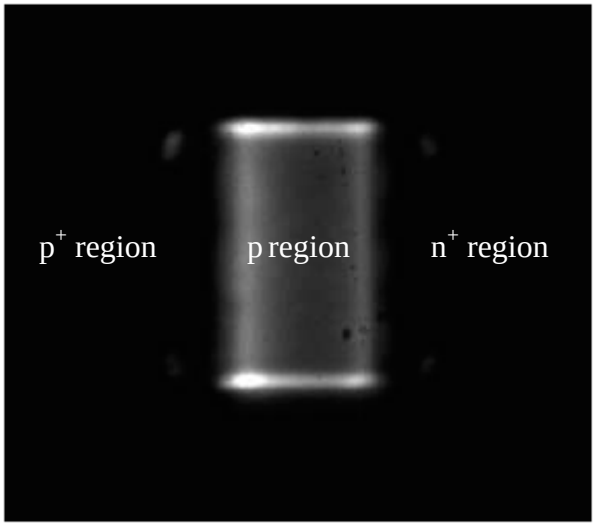

Figure 2. Emission image of the lateral diode without poly-gate on top of the emitting region has been taken by infrared camera via a 20 times magnification microscope.

Results and Discussion

A. Gate Oxide

Due to the difference in device processing compared to the normal CMOS process it was necessary to check the oxide quality. Capacitance-Voltage (C-V) measurements were carried out on MOSFET test structures, the C-V characterizations of n-MOS and p-MOS can be seen in Figure 3. It is interesting to notice the difference of MOS C-V curves on this SOI wafer compared to that on standard substrates (1). From the characteristics, it is concluded that the gate oxide is of good quality (5).

B. Influence of Gate and Substrate Biases

In MOSFETs, the voltage on the gate electrode is to control the conductivity of the channel, which determines the operation of the device. Without the MOS gate the device is two back-to-back diodes and would not let direct electrical currents pass. On the contrary, in our structure the gate will only have supplementary role due to the fact that the p^+pn^+ is a diode with a lowly doped region and would normally allow a forward-biased current. The gate action would mostly modify the interfaces and probably the behavior of the carriers such as mobility. With a standard lateral diode (without the gate)

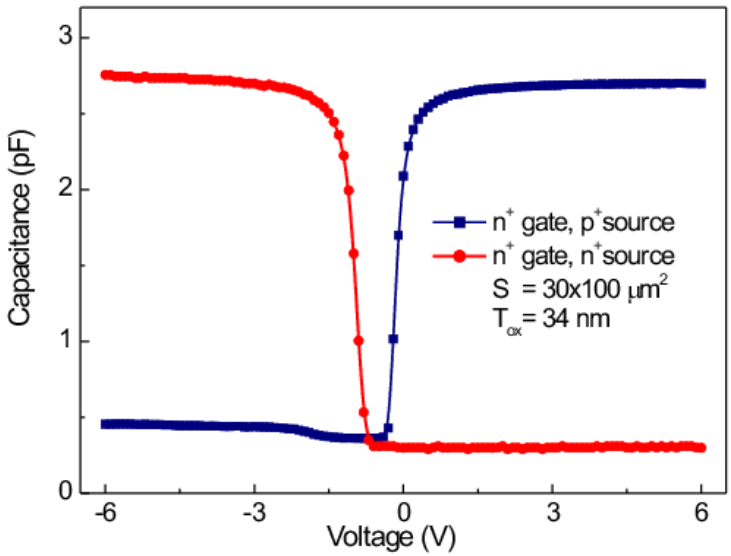

Figure 3. High frequency CV characteristics at 100 kHz of the test MOSFET structures with the same n^+ gate but different source doping: p^+ (rectangular symbol) and n^+ (circle symbol).

the influence of the substrate bias are shown in Figure 4. It is clear that a positive substrate bias reduces the emission intensity, while a negative voltage delivers the opposite effect and that happens mostly at the p/n^+ junction. The intensity at the p^+/p junction stays constant for the whole range of negative substrate biases. The gated lateral diodes we aim to investigate (Figure 1) have similar effect when the gate is biased except that the peak at the p^+/p junction also shows some increase in intensity (see Figure 5). However, the increase of intensity at the p/n^+ interface is still the dominant. Inset in Figure 5 shows the integrated electroluminescence intensity as function of the biased voltages at the gate. We can see the same trend that negative bias will increase the emission intensity.

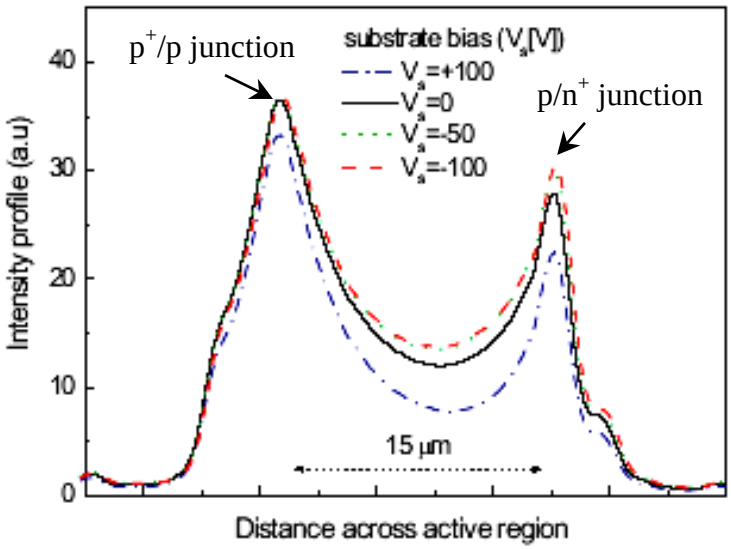

Figure 4. Field influence on the intensity profile across the 15 μm active-region by the substrate biases.

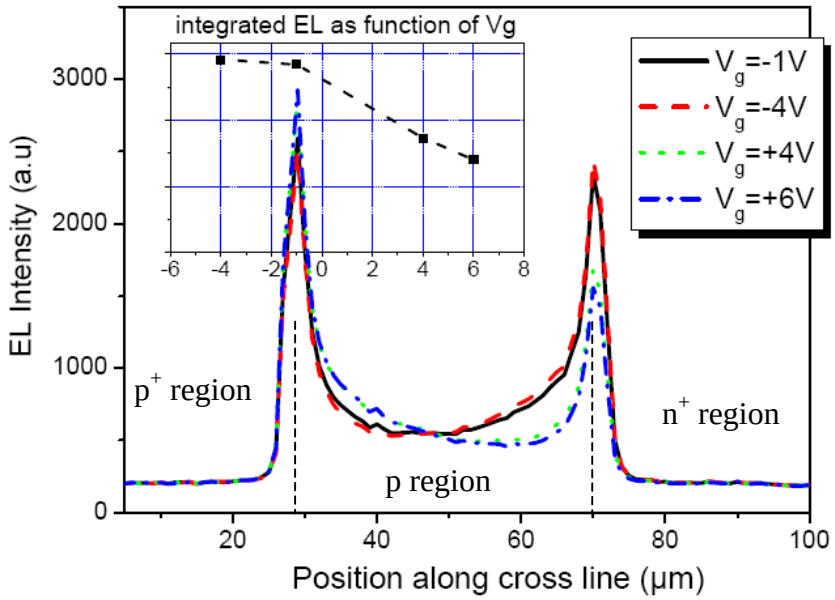

Figure 5. Field influence on the intensity profile across the 40 μm active-region by the poly gate biases. Inset is the integrated EL intensity as function of biased voltage at gate.

The final investigation is when both gate and substrate are simultaneously biased (Figure 6). The same behavior is observed as compared to two previous experiments. However, the difference is that the peak at p/n^+ strongly surpasses the intensity at the other peak. Inset in figure 6 shows that the integrated EL intensity is higher when both gate and substrate are negatively biased. From that we observed an increased light output of 20 % when both electrodes are in negative bias.

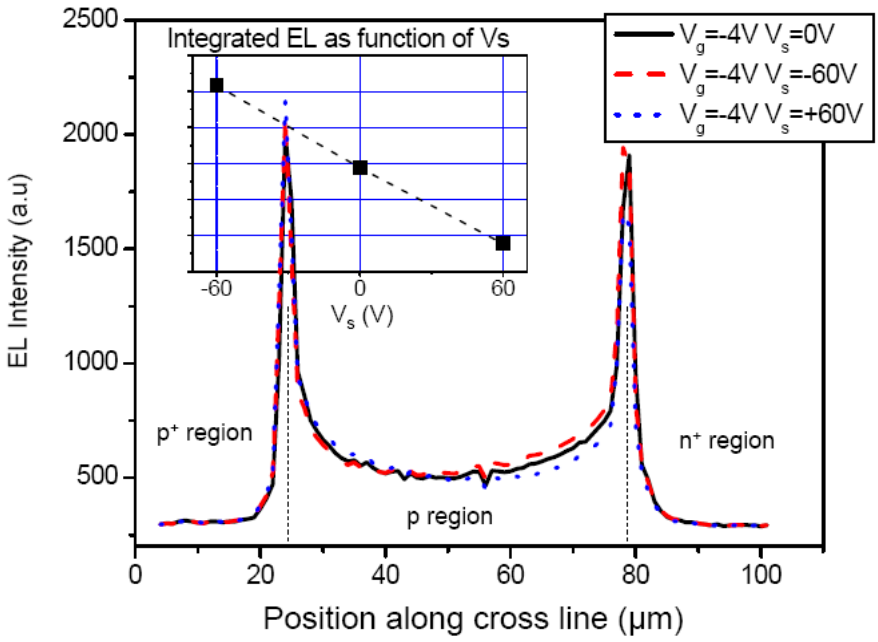

Figure 6. Influence on the intensity profile by both gate and substrate biases simultaneously across the lateral diode with the active region width of 50 μm. The inset is the integrated EL intensity at different substrate bias while the gate was constantly kept at V_s = - 4 V.

C. Simulation and Comparison

To study the trends of the intensity against the applied bias on the gates, we simulate the device structure and its operation. The simulation aims at studying the influence of the electrical field applied on the gate to the change of the total recombination rate. The simulation results are as follows:

- When the gate and substrate are grounded, there are two recombination peaks at the p^+/p and p/n^+ junctions with stronger peak at the former, as previously mentioned.
- When the gate is increasingly biased in the negative direction, both peaks recombination rate increases but at different speeds.

The change of the simulated recombination rate at junctions is collectively displayed in Figure 7. The increase of the simulated total EL intensity when the negative biases ear at the gate and the substrate is shown in the inset. Generally speaking the simulation results show a similar trend as the experimental data. At the p/n^+ junction, the intensity increases for all devices. At the p^+/p the increase of intensity is less prominent compared to the other junction.

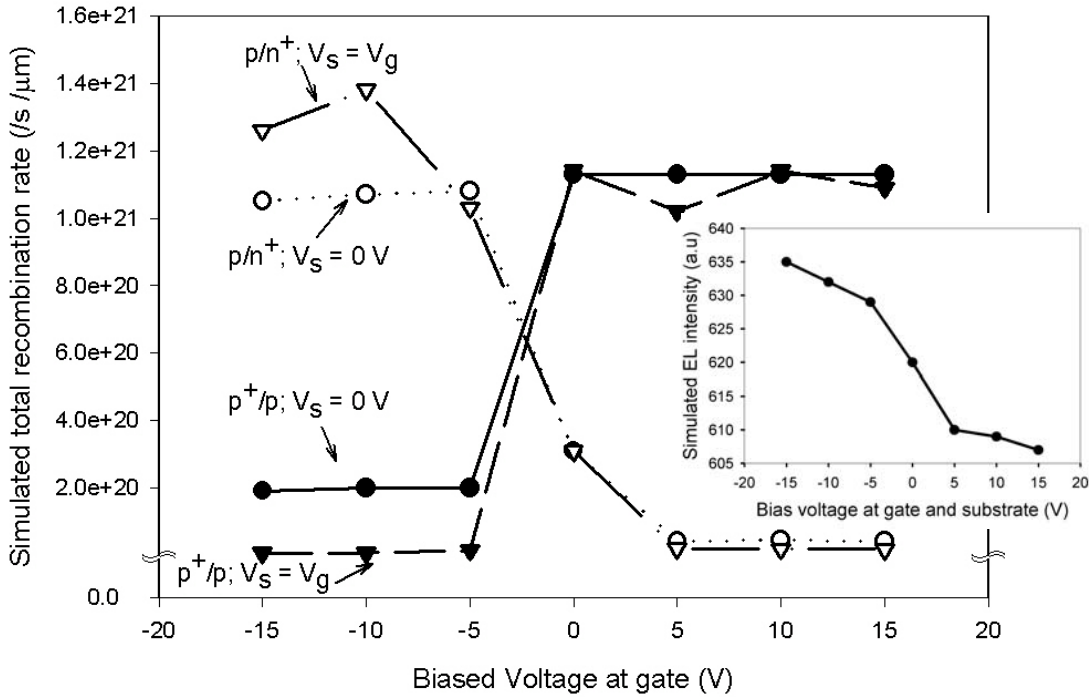

Figure 7. Simulated total recombination rate at the junctions vs. the applied electrical field at both electrodes. Inset is the trend of the simulated total EL intensity as function of the applied voltage at both electrodes.

D. Temperature effect

The temperature dependence of the integrated EL intensity of the fabricated devices is investigated in the range of 253 – 473 K. Figure 8 shows an increase of the total EL intensity with temperature, the device is under a forward-bias current of 2 mA and 5 mA with the gate and substrate grounded. This behavior is in agreement with Ng *et al* (6) and

Kittler *et al* (7), and it indicates that our devices work efficiently in the room temperature range. The explanation for this is that at high temperature phonons are more abundant so radiative recombination (mediated by the absorption of a phonon) can increase with temperature (8).

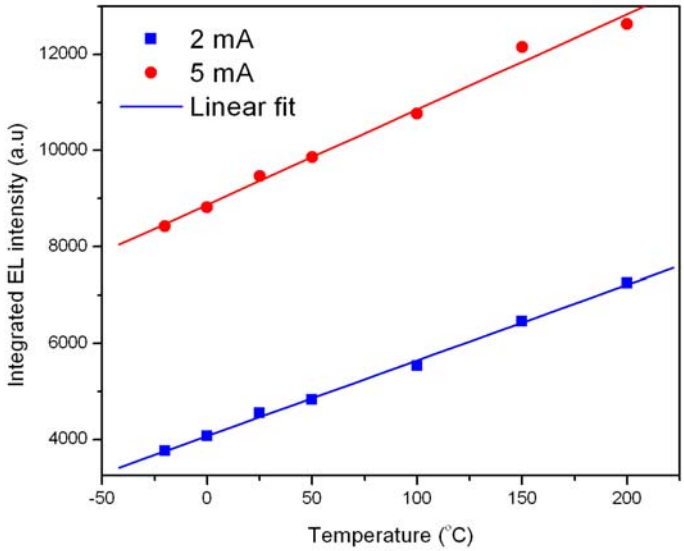

Figure 8. The temperature dependence of the integrated EL intensity of the fabricated devices at 2 mA (rectangular) and 5 mA (circle) forward current.

Conclusions

In conclusions, it is definite that applying an electric field via the gate and/or the substrate influences the light emission properties of the lateral diode fabricated on SOI substrates. It is a gain effect when negative bias is applied. The right combination of gates could introduce the capability to modulate optical processes in the active region of the device. In our current measurement setup it is not yet possible to observe photon emission from the backside of the substrate, thus the optical impact of the polysilicon layer on the emitting profile is still not studied.

Acknowledgments

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