Limits on Thinning of Boron Layers With/Without Metal Contacting in PureB Si (Photo)Diodes

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***Abstract*— A little more than a monolayer-thick pure-boron (PureB) layer was deposited on silicon at 250 °C by chemical vapor deposition (CVD), forming junctions with low saturation current. They displayed the same efficient suppression of electron injection as PureB diodes fabricated with a few nm-thick PureB layer deposited at 400 °C. Assuming high concentrations of acceptor states at the B-to-Si interface, induced by a fixed negative charge in the range from 5×10^{13} cm^{-2} to 5×10^{14} cm^{-2}, would be consistent with the experiments and device simulations that exhibit an efficient suppression of electron injection. Metallization of the B-layers was studied, showing that in many situations, thinning of the layer to monolayer thickness will lead to a significant increase in the electron injection.**

***Index Terms*— Chemical-vapor deposition, electron injection, monolayer, pure boron, photodiodes, silicon, ultrashallow junctions.**

I. Introduction

DEPOSITING as little as 2-nm-thick layers of pure amorphous boron (PureB) by chemical-vapor deposition (CVD) down to 400°C is used today to fabricate the anode region of robust CMOS-compatible photodiode detectors for low-energy electrons [1], [2] and vacuum/near-ultraviolet (VUV, NUV) light [3], [4]. Even with only the boron layer as light-entrance window, these detectors are characterized by low dark currents, high responsivity, and high stability during high-dose irradiation [2]–[5]. All experimental evidence has been consistent with the assumption that B-to-Si interfacial bonds are acceptor states that create a monolayer of fixed negative charge thus attracting holes to the interface [4], [6]. The very high electric field gradient at the surface then repels electrons, enabling the low dark currents and high responsivity. Making the B-layer below 2 nm thin is of interest for obtaining practical signal gains for electrons with energies in the 100 eV range. Moreover, for incorporation of PureB in advanced semiconductor devices, for example source/drain diodes in CMOS or tunneling field-effect transistors [7], [8], the bulk B represents an undesirable extra series resistance and monolayer-like B-coverage may be imperative.

Prior to the PureB research, less commercially used techniques such as molecular beam epitaxy (MBE) [9], [10], and ECR [11] were deployed to deposit monolayers of B on Si. Contrary to the PureB deposition process, the goal was to cap these boron monolayers by a thin layer of crystalline Si to promote hole activation and sheet concentrations higher than 10^{14} cm^{-2} were obtained [9]–[11]. Oxidation of the Si cap was, however, detrimental for the sheet conductance and stability of photodiodes fabricated in this way [12]. It significantly decreased the Si cap thickness and oxide-charge-induced band bending impacted the accumulation of holes at the B-to-Si interface. On the Si surface, boron resides as an adatom decreasing the number of dangling bonds [13], [14], while boron depositions were found to cause band bending at the interface typical of highly doped p$^+$ regions [13], [15], [16]. It is of great interest to find conditions which would preserve such a high concentration of holes at the interface, the structure of which has been shown to have a great influence on the electrical properties [17], [18].

This letter presents answers to two pertinent questions about PureB diodes: will a monolayer B have the same attractive electrical properties as thicker B-layers, and what are the origins of increased electron injection upon metallization of PureB diodes with very thin B-layers? Previous work with such thin layers has shown that metal contacting led to a significant increase of the electron injection, the origin of which is studied here by simulation and experiments with different B-layer deposition conditions. Guidelines are given for when such thin layers could be applied with profit in actual devices.

II. Experimental Devices

Boron depositions at temperatures from 200°C to 350°C were performed by CVD in a commercial PicoSun atomic layer deposition (ALD) system. Native oxide was removed by a HF dip before the deposition, during which the chamber pressure was around 1 mbar. The deposition rate was varied by adjusting the flow rates of the B_2H_6 precursor and Ar carrier gas.

The thickness of the B-layers was evaluated by secondary ion mass spectrometry (SIMS). The layers were deposited in the sheet resistance test structures described in [19] that

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allow contacting via B-implanted p^+-regions instead of metallization. With these structures we could determine the sheet resistance along the B-to-Si interface, R_{SH}, and diode I-V characteristics including the electron current component. To gain more insight into the metallization issues encountered when contacting thin layers, CVD B-layers routinely used for high-quality photodiode fabrication were also examined more closely, including devices reported in [2], [20], [21].

III. Simulations

A model was established where different monolayers of fixed negative charge with concentration N_I were placed at the B-to-Si interface. For the bulk B, the relevant material parameters are either not known or vary considerably depending on the deposition method and literature studies rely on analyzing much thicker layers than we had available [22]–[27]. Here we use the highest reported p-doping of 10^{18} cm^{-3} [28]. For the other parameters, to nevertheless gain some understanding of the influence that metallization can have, the B-layer was set to have the same material parameters as Si.

The simulations were performed using Synopsys Sentaurus Device [29] technology computer-aided design (TCAD) software. The simulated n-type bulk-Si region was set to 500 μm with a constant doping of 10^{15} cm^{-3}. The B-layer thickness, t_{PB}, was varied from 0.2 nm to 10 nm. The N_I was varied from 10^8 cm^{-2} to 5×10^{14} cm^{-2}. The Schottky barrier formed between the B and the metallization is an unknown. Therefore, simulations were performed with a metal work function, ϕ_m, from large values that would form an ohmic contact to the p-type B-layer, to lower values that would give a depletion of the B-surface. At this surface, typical Si electron and hole recombination velocities were assumed, 2.573×10^6 cm/s and 1.93×10^6 cm/s, respectively. The thermionic emission model [30] and Philips unified mobility model [31] were applied, and Fermi-Dirac statistics [32] were assumed for electrons and holes. From the simulated I-V characteristics, the saturation current densities of electrons, I_{Se}, and holes, I_{Sh}, were extracted.

A structure assuming only accumulated holes at the interface with a concentration of N_{hole} is simulated first (Fig. 1a). In Fig. 1b the I_{Se} and I_{Sh} are shown for the case where nonlocal tunneling to the contact was also modeled [29]. We apply a tunneling mass for holes, m_h, of $0.1\times m_0$, while the tunneling mass of electrons, m_e, was varied from $0.1\times m_0$ to $2\times m_0$, with m_0 being the electron rest mass. This case is comparable to the experimental case where the non-metallized B-layer is contacted via implanted p^+-regions. In Fig. 1c the band diagram at the B-to-Si interface is drawn for a diode biasing $V_D = 0$. The potential barrier to electron injection increases with N_{hole}, and I_{Se} decreases by almost a decade for every decade increase of N_{hole}. A dependence on the m_e is seen only for N_{hole} above 1×10^{12} cm^{-2}, at which point the higher electron masses become more and more beneficial for reducing the electron injection.

Simulations were also performed for a structure with the simplified PureB model shown in Fig. 2a where the metal contact to B has $\phi_m = 4.1$ eV, the default Al value. The band alignment and formation of the Al-to-B barrier were chosen

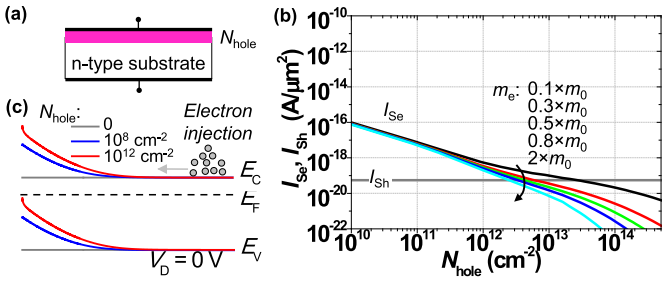

Fig. 1. (a) Cross section of the simulated structure. (b) Electron and hole saturation current densities as a function of N_{hole}. (c) Band diagram for $N_{hole} = 0$ cm^{-2}, 10^8 cm^{-2} and 10^{12} cm^{-2} at $V_D = 0$ V.

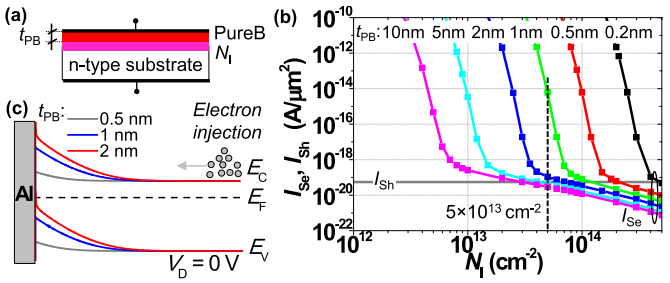

Fig. 2. (a) Cross section of the simulated structure. (b) Electron and hole saturation current densities as a function of N_I extracted for a device with Al/top-layer contact and $t_{PB} = 0.2$ nm, 0.5 nm, 1 nm, 2 nm, 5 nm and 10 nm. (c) Band diagram for $N_I = 5\times10^{13}$ cm^{-2} and $t_{PB} = 0.5$ nm, 1 nm and 2 nm at $V_D = 0$ V.

according to the Schottky contact model [32] while Schottky-barrier height lowering was neglected. Both m_e and m_h were set to $0.1\times m_0$. Due to the Schottky-induced depletion of the B surface, the associated band bending will influence the hole accumulation at the B-to-Si interface. The effect on I_{Se} and I_{Sh} when varying t_{PB} from 0.2 nm to 10 nm and N_I from 10^{12} to 5×10^{14} cm^{-2} are included in Fig. 2b. All the B-layers are so thin that the presence of the metal increases the I_{Se} with respect to the non-depleting case. On the other hand, the expected maximum possible concentration of holes, 6.78×10^{14} cm^{-2} for ⟨100⟩ Si, would be efficient in suppressing the electron injection even for a monolayer B-thickness. For N_I less than 10^{13} cm^{-2}, the effective suppression of I_{Se} is lost even for t_{PB} as thick as 10 nm. For N_I around 5×10^{13} cm^{-2}, 2-nm layers become inefficient. However, in all cases, the effect of any negative fixed interfacial charge is to lower the electron injection (Fig. 2c).

IV. Experimental Results

Only for a B deposition temperature of 250°C with 30 min exposure to B_2H_6, were we successful in achieving monolayer-like thin layers with the desirable electrical characteristics. At 300°C and 350°C, a good interface coverage was impeded by a faster B overgrowth mechanism, while neither sufficient adsorption to the Si nor bulk B growth was realized at 200°C.

As opposed to higher temperature deposition [17], possibly the conditions at 250°C resulted in a preference for the B to adsorb on Si sites rather than B-sites, leading to an almost self-limiting deposition. Something similar was observed for the incorporation of B in Ge in low-temperature delta-doped layer deposition [33]. In all cases it is expected that the presence of H-Si surface bonds plays an important role since

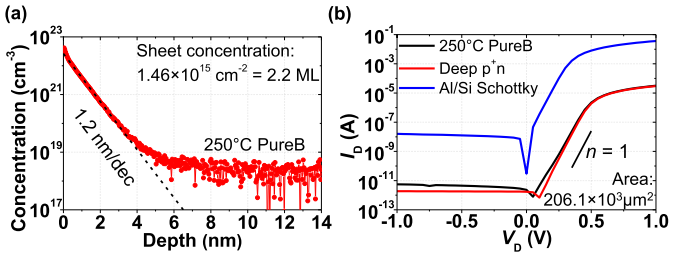

Fig. 3. (a) SIMS profile of ∼1-nm thick PureB layer deposited at 250°C. (b) Measured *I-V* characteristics of a non-metallized PureB diode fabricated with this 250°C layer, a deep B-implanted diode, and an Al-to-Si Schottky diode.

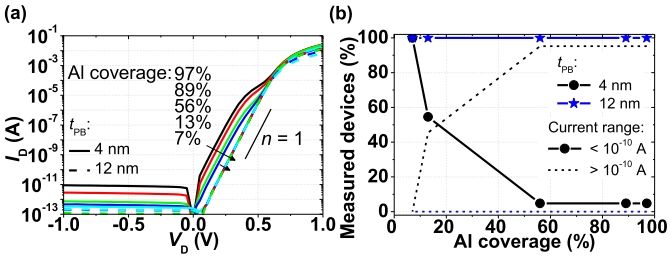

Fig. 4. (a) Measured *I-V* characteristics of rectangular test structures for a PureB layer deposited at 700°C to thicknesses of 4 nm and 12 nm with aluminum coverage indicated in the figure. (b) Distribution of currents at $V_D = 0.2$ V for $t_{PB} = 4$ nm and 12 nm for varied Al coverage.

at higher deposition temperatures they are known to impede the chemisorption of B [34]. The interaction between B and B_xH_y molecules, and the Si surface at temperatures as low as 250°C is at present unknown.

In Fig. 3a, the SIMS profile of the 250°C PureB layer is seen to have a 1.2 nm/dec slope which is the resolution limit of SIMS. The integrated B concentration is 1.46×10^{15} cm^{-2}, 2 times the amount needed for a complete monolayer. The *I-V* characteristics of non-metallized 250°C PureB diodes are shown in Fig. 3b together with those of a comparable deep p^+n diode. Apart from a very small non-ideal leakage current in the PureB device, the two curves are almost identical. The sheet resistance along the B-to-Si interface was 45 kΩ/□, and the $I_{Se} \sim 7 \times 10^{-20}$ A/μm^2. Both values are very close to those of 400°C B-layers [17]. From the simulations shown in Fig. 1b, the N_{hole} necessary for achieving such a value would be $\approx 2 \times 10^{12}$ cm^{-2} to 2×10^{13} cm^{-2} for m_e between $2 \times m_0$ and $0.1 \times m_0$.

In metallized diodes with a few nm-thick 700°C PureB deposition $I_{Se} << I_{Sh}$, so it could only been determined that $I_{Se} < 10^{-20}$ A/μm^2 [17]. Much higher values are regularly seen for very thin B-layers. In [20] it was shown that a 5×10^{13} cm^{-2} B-coverage gave 3 decades lower I_{Se} than Al-to-Si Schottky diodes, and 2.5 decades higher than the full coverage needed to reach the lowest $I_D \cong I_{Sh}$ values. Other experiments show that even a very small fault in B-coverage may significantly increase the I_{Se}. This is best illustrated by the experimental results compiled in Fig. 4a. Here *I-V* characteristics are shown of a series of 700°C PureB diodes [21] that have B-layer thickness from 4 nm to 12 nm and different areas of metal coverage. With 12-nm layers all diodes had ideally low I_D. As shown in Fig. 4b, as the thickness was decreased and the metal area increased, the number of defected devices increased, being characterized by an increase in I_D of at least 1 decade, plausibly representing a single defect where the Al either comes close to or touches the Si. Above 0.4 V the extra high currents roll off, presumably due to high-injection effects from the very high current density through the small areas without (sufficient) B-coverage. The results are consistent with the presence of a few process-related defects, probably particles and associated native oxide residues after the pre-deposition cleaning step.

For diodes with B-layers grown at temperatures below 500°C it has been shown that the B-layer becomes less and less compact as the deposition temperature decreases [4]. This increases the probability of weak spots for the Al to penetrate and attempts to fully metallize 4-nm-thick 400°C layers like the ones used for electron detectors in [2] led to *I-V* characteristics with current levels within a decade of the Al-to-Si Schottky characteristics. Likewise, putting Al-metallization on 250°C diodes results in high Schottky-like characteristics corresponding to an almost complete loss of the extra electron suppression otherwise provided by the B-layer. This is most likely due to many weak spots where the Al actually touches the Si.

V. Conclusions

The simulations of PureB diodes with an interfacial layer of fixed negative charge support that for charge densities above about 5×10^{13} cm^{-2} such a layer can be responsible for the low saturation current reliably reproduced in PureB diodes fabricated with B-deposition temperatures from 400°C to 700°C. The experimental diode made here with a 250°C B-deposition thickness of ∼1 nm is a verification that only the interfacial B-to-Si bonding and not the bulk boron layer is of importance. When a metal layer is added, the simulations confirm earlier experimental observations that proximity of the metal to the interface may lead to a significant increase in the electron injection into the PureB. The presence of small imperfections in the PureB coverage contacted by metal can increase the forward current by a decade or more. This explains earlier experimental results that have shown that with deposition temperatures below 400°C, where the B-layer is more loosely bonded, layers thicker than 4 nm are needed for successful metallization with Al. When the PureB-induced interfacial hole layer is contacted without metal coverage, the low electron injection is maintained as long there is enough fixed negative interfacial charge.

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