Theory and Implementation of a Load-Mismatch Protective Class-E PA System

Jeroen Ponte, *Student Member, IEEE,* Ali Ghahremani, *Member, IEEE,* Maikel Huiskamp, *Student Member, IEEE* Anne-Johan Annema, *Member, IEEE* and Bram Nauta, *Fellow, IEEE*

***Abstract*—Highly efficient switch-mode class-E Power Amplifiers (PAs) are sensitive to load impedance variations. For Voltage Standing Wave Ratios (VSWRs) up to 10:1, the peak switch voltage and average switch current can increase by a factor 1.7 and 2.5, respectively, relative to those under nominal load conditions, imposing serious reliability risks. This work describes a technique to self-protect class-E PAs to decrease their sensitivity to load variations, relying on tuning of the switch-tank relative-resonance frequency, implemented by an on-chip Switched-Capacitor Bank (SCB). To validate the technique, load-pull measurements are conducted on a class-E PA implemented in a standard 65 nm CMOS technology, employing an off-chip matching network, augmented with a fully automated self-protective control loop. Under nominal conditions, the PA provides 17.8 dBm at 1.4 GHz into 50 Ω from a 1.2 V supply with 67% efficiency. The proposed self-protective PA can reduce its peak switch voltage below the technology- and switch design-related limit for any load with a VSWR up to 19:1, while not considerably impacting output power and efficiency, which see a maximum degradation of 1.6 dB and 6%, respectively. Furthermore, a class-E PA designed to safely handle 2.5× the nominal average switch current can reliably operate for VSWRs up to 19:1 when protected with our technique.**

***Index Terms*—CMOS integrated circuits, load mismatch, VSWR, power amplifiers (PAs), class-E PA, self-healing, self-protecting.**

I. Introduction

EFFICIENCY is an important Power Amplifier (PA) parameter in modern battery-powered systems. Consequently, Switch-Mode PAs (SMPAs) compare favorably to linear PAs due to their exceptionally high efficiency. The class-E PA topology is one such SMPA, employing a resonant waveform-shaping network to achieve the Zero-Voltage Switching (ZVS) and Zero-Slope Switching (ZSS) conditions necessary to achieve high (ideally 100%) efficiency [1–5]. A schematic representation of a class-E PA and its switch voltage and current waveforms under ZVS and ZSS conditions are shown in Figure 1a and b, respectively [6]. On the downside, class-E PAs are sensitive to load mismatch conditions: the resulting de-tuning of their resonant networks causes unwanted effects such as high switch currents and high peak switch voltages, which can result in PA degradation or even instantaneous destruction [7–10].

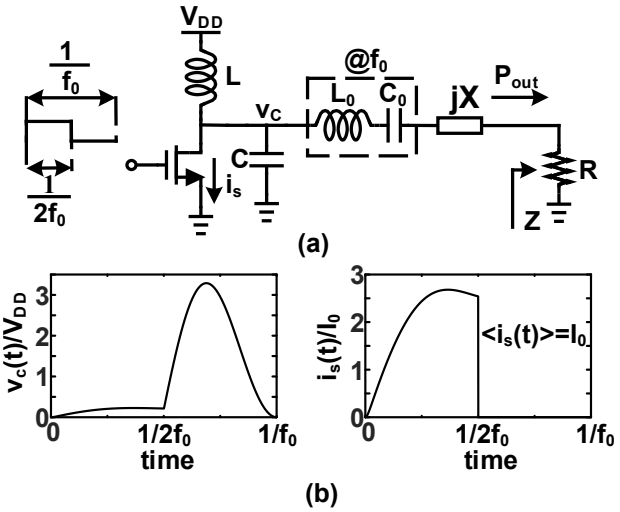

Fig. 1: (a) Schematic representation of a single-ended class-E PA (b) Switch voltage and current waveforms for a class-E PA designed for ZVS and ZSS with $q = 1.412$, $d = 1$ and $m = 0.05$, operating under nominal conditions [6].

Antenna impedances are a strong function of their EM environment, with Voltage Standing Wave Ratios (VSWRs) reaching up to 10:1 [11–13]. Under such load mismatch conditions, class-E PA reliability is degraded by several phenomena. Firstly, an increase in PA dissipation due to non-ZVS conditions can cause PA degeneration through thermal (over-)stress. Additionally, the associated increase in average switch current may damage the switch through electromigration [14, 15] or hot carrier degradation [1, 16]. Lastly, and most importantly, extreme switch voltage excursions exceeding the switch transistor breakdown voltage limit can cause instantaneous and permanent failure as a consequence of gate-oxide breakdown [17, 18].

There is prior published work concerning the protection of PAs under load mismatch conditions. Karoui et al. [19] report a self-protecting class-A PA that utilizes an analog control loop to automatically keep output stage current below a set limit. Applying this type of self-protecting system to class-E PAs results in waveform corruption and a reduction in efficiency. Scuderi et al. [20] demonstrated a class-C-E PA utilizing bias variations and variable gain control to decrease PA gain in order to reduce active device voltage stress under load mismatch. This technique is not easily applied to switched-mode PAs (e.g. class-E PAs) because their gain cannot be readily

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Jeroen Ponte, Maikel Huiskamp, Anne-Johan Annema and Bram Nauta are with the Department of Electrical Engineering, Mathematics and Computer Science, University of Twente, 7500 AE Enschede, The Netherlands (e-mail: j.ponte@student.utwente.nl; a.j.annema@utwente.nl).
Ali Ghahremani is with Dialog semiconductor, Den Bosch, The Netherlands.

tuned. Bowers et al. [21] presented a self-healing class-AB PA system, in which PA bias-point control is combined with active load tuning to achieve improved operating performance under load mismatch conditions. Their load-tuning technique could be adapted for use in a self-protective system, at the cost of reduced efficiency and increased complexity. A technique aimed specifically at class-E PAs was demonstrated by Wei et al. [22]. In it, the peak switch voltage is sensed and kept constant by varying the gate drive level and thereby varying the switch on-resistance R_{ON}. Unfortunately, the reduction in switch drive and associated increase in switch transistor R_{ON} degrades PA switching performance, and hence significantly degrades output power and efficiency. Another option is the application of isolators/circulators to isolate the PA from reflections due to load mismatch. However, at frequencies up to tens of GHz, their bulky nature renders them impractical for use in integrated circuits, while reflected power is absorbed in a termination resistor, significantly impacting efficiency under load mismatch conditions.

We previously proposed and demonstrated a new technique for protecting a class-E PA under load mismatch [6] with low impact on output power and efficiency. With the technique in [6], the (relative) resonance frequency (q) of the class-E PA switch tank is tuned in such a way that switch transistor (over-)stress due to load impedance variations is minimized. In this work, we present the theoretical foundation for this technique, which is backed up by simulation results and more measurement results. It was shown in [7] that changing the relative resonance frequency of the switch tank and changing the switch duty cycle have approximately opposing effects on class-E PA behavior. The use of this duty cycle tuning as a complementary method to switch tank tuning is also described.

This paper is organized as following. Section II reviews the reliability concerns relevant to class-E PAs. In section III, the theoretical effects of load mismatch on class-E PAs are presented in load-pull contours. The consequences of the observed variations in PA behavior are discussed. Section IV presents a discussion of second-order effects that were not taken into account in the theoretical treatise in Section III, focusing on the resulting differences in PA behavior. Section V shows the effects of load mismatch on class-E PAs by utilizing load-pull contours obtained from simulation results. Based on these contours, a Safe Operating Areas (SOA) is drawn to indicate where the PA is at risk of degradation or destruction. Section VI deals with the effects of changing the relative resonance parameter, q, and duty cycle, d, on PA behavior. This shows that a proper selection of the q parameter can move the SOA to enclose almost any load impedance, while variation in the d parameter allows for limited SOA tuning. Section VII presents measurements performed on a class-E PA system, both for non-tuned and tuned cases, demonstrating the validity of the shown theory and simulations. Section VIII shows the implementation of a self-protecting system for the class-E PA, leveraging the results from section V. Measurement results are shown and compared to the experimental and theoretical data. Finally, in section IX, conclusions drawn from the work are summarized.

II. Reliability concerns in class-E PAs

A. Gate-oxide breakdown

When a high voltage exceeding the specified breakdown limits is applied to a MOS transistor, gate-oxide breakdown can occur, typically breaking bonds in the transistor gate-oxide [23, 24]. Although gate-oxide breakdown can manifest in several ways, this work mainly focuses on hard breakdown, wherein a highly conductive path is formed in the gate-oxide [23, 24]. This conductive path significantly reduces the off-resistance of a MOS transistor, heavily compromising its performance [1].

B. Hot carrier degradation

When a high lateral field is present in an MOS transistor, at drain-source voltages exceeding the material bandgap, carriers can gain significant kinetic energy [25, 26]. Such carriers, denoted as "hot carriers", can amass enough energy to produce impact ionization upon collision with the crystal lattice. This process can generate surface defects, leading to reduced carrier mobility in the channel and the trapping of charges in the gate oxide, shifting the local threshold voltage [25, 26]. These effects manifest as an increase in on-resistance and switch turn-on voltage, degrading the performance of SMPAs. For significant hot carrier degradation to occur, both a high drain-source voltage and substantial drain current must be present, which only occur under severe load-mismatch conditions in SMPAs that are designed for ZVS [1].

III. Class-E PAs under (non-)nominal conditions

A. Class-E PA basics

Class-E PAs in single-ended form consist of a (transistor-based) switch and two resonant (LC) tanks. A schematic representation of a single-ended class-E PA is shown in Figure 1a. The switch tank, $L-C$, is dimensioned to shape the switch node voltage $v_{\mathrm{c}}(t)$ to achieve ZVS and ZSS conditions, as represented in Figure 1b. The second tank at the output, L_0-C_0, is a band-pass filter designed to pass energy to the load only at the fundamental frequency, f_0. The relative duty cycle parameter, d [1], describes the duty cycle of the switch drive voltage as

$$S \triangleq \begin{cases} \text{ON}, & 0 < \ 2\pi f_0 t < d\pi, \\ \text{OFF}, & d\pi < \ 2\pi f_0 t < 2\pi. \end{cases} \tag{1}$$

Typically, the PA switch is driven by a square wave with $d=1$ (50% duty cycle). The level of violation of ZVS and ZSS, respectively, are indicated by α and β as in [1]

$$v_c\left(\frac{1}{f_0}\right) = \alpha V_{\mathrm{DD}}, \qquad \frac{dv_c}{dt}\left(\frac{1}{f_0}\right) = 2\pi\beta f_0 V_{\mathrm{DD}}, \tag{2}$$

where V_{DD} is the PA supply voltage.

Acar [1, 27–29] formulated relationships between class-E PA behavioral parameters and component parameters using the so-called K-design set, shown in Table I.

TABLE I: K-design set

$K_{\mathrm{L}} = \frac{2\pi L f_0}{R}$	$K_{\mathrm{C}} = 2\pi f_0 R C$	$K_{\mathrm{X}} = \frac{X}{R}$	$K_{\mathrm{P}} = \frac{R P_{\mathrm{out}}}{V_{\mathrm{DD}}^2}$

The K-design set parameters depend on α, β, the relative resonance frequency q, and the technology-dependent relative switch-on resistance, m, which is a function solely of the operating frequency, f_0, and the technology-specific switch transistor time constant $R_{\mathrm{ON}}C$, where R_{ON} is the switch on-resistance and C is the parasitic switch capacitance. The q and m parameters are defined as

$$q = \frac{1}{2\pi f_0 \sqrt{LC}}, \tag{3}$$

$$m = 2\pi f_0 R_{\mathrm{ON}} C. \tag{4}$$

Load-pull contours for various amplifier metrics can be derived for a class-E PA designed for specific q, d and α and β [7]. To perform load-pull analyses, the PA load Z, is varied over a range of mismatch conditions. The resulting contours are shown in Smith charts normalized to the nominal load, $Z = R_{\mathrm{nom}}$. For each load condition, PA metrics such as switch voltage, switch current, efficiency and output power can be derived. A full mathematical derivation of the load-pull analysis was presented in [7] and will not be repeated here. The load-pull contours show the peak switch voltage normalized to V_{DD}, efficiency and the average switch current and output power normalized to those under nominal load and design conditions ($Z = R_{\mathrm{nom}}$, VSWR=1:1, $q = q_{\mathrm{nom}}$ and $d = d_{\mathrm{nom}}$). For high PA output power, the q parameter is set to 1.4 [1]. The m parameter for a typical $65\,\mathrm{nm}$ CMOS in the low GHz range is approximately 0.05. The d parameter is set to 1 (50% duty cycle). The supply voltage is chosen as $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$ to comply with typically available CMOS supply voltages.

B. Effects of load mismatch on class-E PA behavior

To perform a load-pull study on the class-E PA, the K-design set parameters as well as the performance (output power and efficiency) and reliability related parameters (maximum switch voltage and average switch current) are derived as a function of the fixed parameters q, d and m and the load-dependent parameters α and β. Under nominal load conditions

$$K_{L_{\mathrm{nom}}} = K_{L(q,d,m,\alpha=0,\beta=0)} = \frac{2\pi f_0 L}{R}, \tag{5}$$

$$K_{X_{\mathrm{nom}}} = K_{X(q,d,m,\alpha=0,\beta=0)} = \frac{X}{R}. \tag{6}$$

Under load mismatch conditions, the load impedance Z deviates from the nominal load R, giving

$$Z = kR + jk'R. \tag{7}$$

where $k > 0$ and k' are real numbers. Under nominal load conditions, $k = 1$ and $k' = 0$. Under non-nominal load conditions, ZVS and/or ZSS conditions are violated and the K-design set K_L and K_X can be written as

$$K_{L(q,d,m,\alpha,\beta)} = \frac{2\pi f_0 L}{\Re\{Z\}} = \frac{2\pi f_0 L}{kR}, \tag{8}$$

$$K_{X(q,d,m,\alpha,\beta)} = \frac{X + \Im\{Z\}}{\Re\{Z\}} = \frac{X + k'R}{kR}, \tag{9}$$

which can be related to the nominal K-design set values by

$$K_L(q,d,m,\alpha,\beta) = \frac{K_{L_{\mathrm{nom}}}}{k}, \tag{10}$$

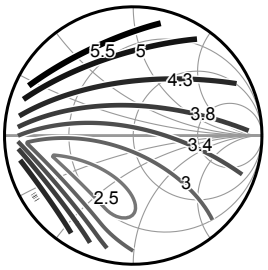
$$K_X(q,d,m,\alpha,\beta) = \frac{K_{X_{\mathrm{nom}}}}{k} + \frac{k'}{k}. \tag{11}$$

For any mismatch (k, k'), the switching parameters α and β can be found from (10) and (11) using a numerical solver. Once the load-dependent switching parameters α and β are obtained, the maximum switch voltage normalized to V_{DD}, average switch current normalized to that under nominal condition, output power normalized to that under nominal condition and efficiency follow.

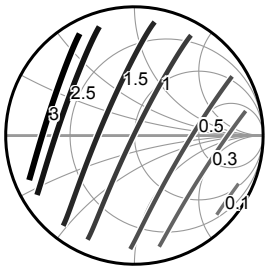
Using this theory, developed in [7], a theoretical load pull analysis is performed on a class-E PA with parameters $q = 1.4$, $d = 1$, $m = 0.05$, $\alpha = 0$, $\beta = 0$. This design will henceforth be referred to as the nominal design. The resulting load-pull contours are shown in Figure 2. Inspection of the peak switch voltage load-pull contours reveals extreme behavior towards the upper left of the Smith chart, with peak switch voltages over $5.5 \times V_{\mathrm{DD}}$. Likewise, the average switch current contours show an increasing trend towards the left side of the Smith chart, reaching over $3 \times I_{\mathrm{nom}}$. These extreme peak switch voltages and average switch currents are accompanied by an increase in output power and a reduction in drain efficiency. When the load conditions shift towards the lower right of the Smith chart, high efficiency operation is maintained, but output power is degraded severely, reaching near-zero values. Because of the rapidly destructive nature of over-voltage-stress related oxide breakdown, relative to the gradual degrading effects of over-current, excessive switch peak voltage and the reduction thereof are the primary focus of this work.

IV. Second-order Effects

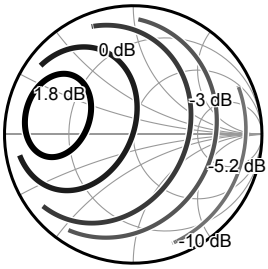
To obtain analytical results, the theory in [7] relies on an idealized switch model that has a finite R_{ON}, infinite R_{OFF} and instantaneous switching behavior. In practice, several second-order effects influence PA behavior. One such effect plays a role for highly negative switch voltages (highly negative α), which occur toward the upper left of the Smith chart in the theoretical load-pull contours [7]. In practice, these negative voltages are clamped due to reverse conduction of the switch transistor. This clamping leads to a reduction in switch voltage as compared to the theory due to the energy loss associated with this clamping action. Secondly, the m parameter varies under load mismatch due to the voltage-dependent switch transistor R_{ON}. This effect reduces the extreme switch currents. Another effect is the loss due to finite feed inductor Q, reducing PA efficiency. Additionally, losses in the matching network, output filter and interconnects reduce the impact of load mismatch on the PA, reducing extreme behavior. Lastly,



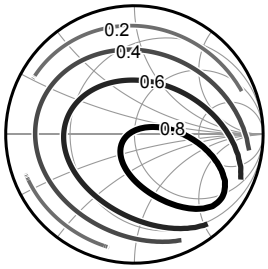
(a) Peak switch voltage normalized to the PA supply voltage V_{DD}



(b) Average switch current normalized to that under nominal conditions



(c) Output power normalized to that under nominal conditions



(d) Drain efficiency

Fig. 2: Theoretical class-E PA load-pull contours for $q = 1.4$, $d = 1$, $m = 0.05$, $\alpha_{\mathrm{nom}} = 0$ and $\beta_{\mathrm{nom}} = 0$

the finite loaded Q of the output filter can result in significant transmission of energy at harmonic overtones, impacting PA performance. The main influence of the second order effects on the simulated and measured contours are warping and scaling with respect to the theoretical contours. A detailed discussion of these second-order effects and their impact on PA behavior is outside the scope of this paper, but can be found in [7].

V. Simulation Results

As intermediate step between theoretical results and measurement results, load-pull simulations are performed on a class-E PA design using Cadence Spectre. The demonstrator PA is designed for $q = 1.4$, $d = 1$, $\alpha = 0$ and $\beta = 0$, $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$, $f_0 = 1.4\,\mathrm{GHz}$ and $P_{\mathrm{out}} = 17.5\,\mathrm{dBm}$. The switch consists of a $1.2\,\mathrm{V}$ thin-oxide MOS transistor (W/L = $0.84\,\mathrm{mm}/60\,\mathrm{nm}$) cascoded by a $2.5\,\mathrm{V}$ thick-oxide MOS transistor (W/L = $1.65\,\mathrm{mm}/280\,\mathrm{nm}$) with its gate biased to $1.8\,\mathrm{V}$ [30]. The PA component values shown in Table II were derived using the K-design set [1].

TABLE II: PA parameters

L	C	X	R	P_{out}
$1.8\,\mathrm{nH}$	$3.4\,\mathrm{pF}$	$\mathrm{j}0\,\Omega$	$25\,\Omega$	$17.5\,\mathrm{dBm}$

The schematic of the PA is shown in Figure 3. The matching network is lossless, the feed inductor has a quality factor $Q \approx 25$ and the loaded quality of the series filter is $Q_{\mathrm{L}} \approx 5$.

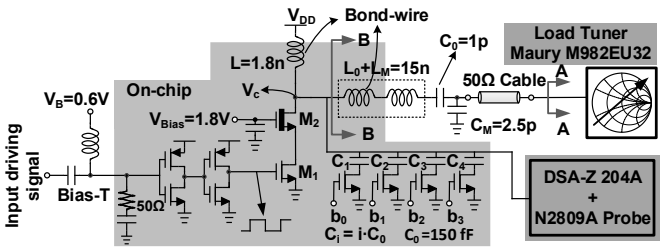


Fig. 3: Schematic representation of the class-E PA. On-chip components are shown in the light-grey area, measurement-related information is contained in dark-grey areas. Modified from [6]. The chip micrograph and PCB setup of this PA, as used for the measurements in Section VI are shown in Figure 4.

A dead-zone of $\Delta V_{\mathrm{c}} = 0.2\,\mathrm{V}$ was added to the algorithm to decrease noise sensitivity. At startup, the algorithm fully enables the SCB to ensure a safe starting condition for the PA. It then checks the peak switch voltage, $V_{\mathrm{c,\,max}}$, lowering the SCB state while $V_{\mathrm{c,\,max}} < V_{\mathrm{c,\,nom}}$ and $C_{\mathrm{bank}} > 0\,\mathrm{fF}$, where $V_{\mathrm{c,\,nom}}$ is

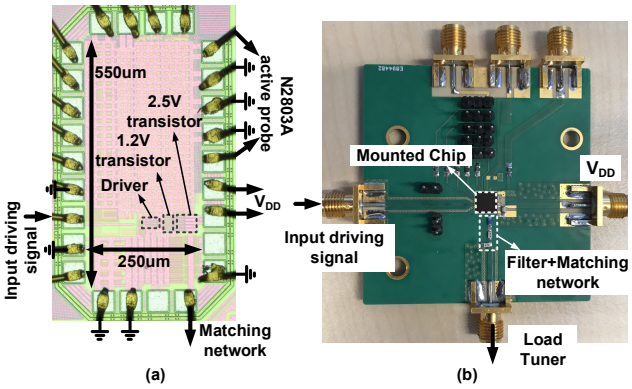
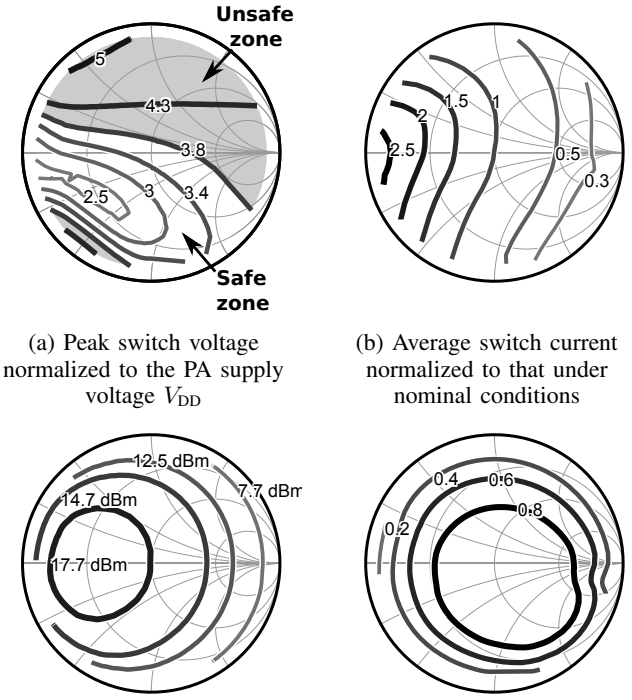


Fig. 4: (a) Chip photomicrograph showing external connections and on-chip components [6] (b) PCB showing external connections and filtering + matching network [6]

The design of the switch allows a maximum switch voltage of $4.6\,\mathrm{V}$, or $3.8 \times V_{\mathrm{DD}}$ ($1.8\,\mathrm{V} + 1.1 \times 2.5\,\mathrm{V}$, including a 10% voltage margin). The focus of this work is on preventing oxide-breakdown due to high peak switch voltages and the reduction/prevention of hot-carrier degradation that may occur when ZVS conditions are severely violated.

Simulated contours for this PA are shown in Figure 5; the contours are scaled and warped version of the theoretical contours in Figure 2 due to the second-order effects discussed in Section IV. Excluding the region of the load-pull plot in Figure 5a where the switch voltage exceeds $3.8 \times V_{\mathrm{DD}}$ yields a Safe Operating Area (SOA). Figure 5b shows that a PA which has its switch designed to handle an average switch current slightly over $2.5\times$ that under nominal conditions sees no average switch current-related SOA reduction from the effects of load mismatch. The switch used in simulation and measurements meets this criterium.

Figure 6 shows switch voltage waveforms for some load-mismatch conditions. The switch (oxide) breakdown limit ($3.8 \times V_{\mathrm{DD}}$) is indicated by a dashed line. A violation of



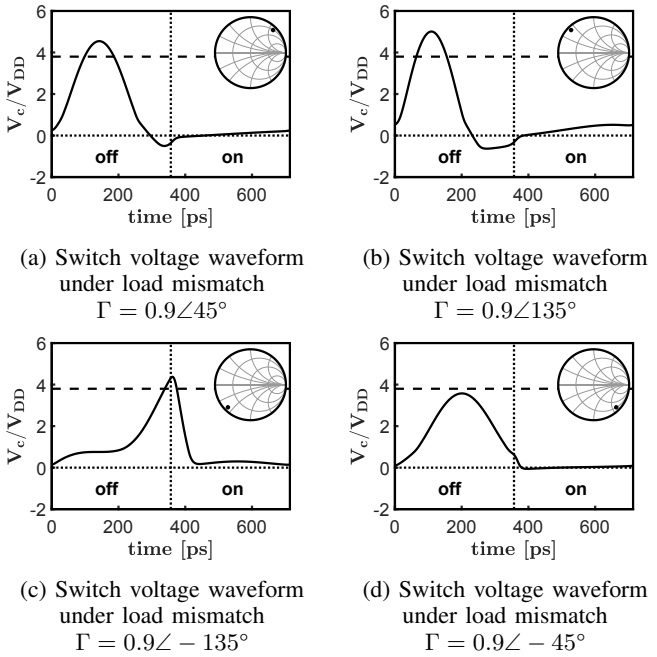
(a) Peak switch voltage normalized to the PA supply voltage V_{DD}

(b) Average switch current normalized to that under nominal conditions

(c) Output power

(d) Drain efficiency

Fig. 5: Simulated class-E PA load-pull contours for $q = 1.4$ and $d = 1$



(a) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle 45°$

(b) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle 135°$

(c) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle -135°$

(d) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle -45°$

Fig. 6: Simulated nominal PA switch voltage waveforms for several load mismatch conditions. The switching moment is indicated by the vertical dotted line.

the breakdown limits can be observed for three of the four shown load conditions. The switch voltage waveform shown in Figure 6c exhibits high switch voltages at the switching moment, indicating the possibility of Channel Hot Carrier (CHC) degradation for load mismatches in the lower left region of the Smith chart.

VI. Effects of the q and d parameters on PA behavior

In [31], the theoretical effects of varying the class-E PA q and d parameters were presented. The theory shows that, among other things, peak switch voltages occurring under load mismatch can be reduced by decreasing the q parameter or by increasing the d parameter. This behavior is illustrated using the theoretical load-pull analyses in the next subsections.

A. Effects of the q parameter on PA load-pull contours

Figure 7 shows the effects of changing the q from the original value of 1.4 to 1.15. Apparent is the receding of extreme peak switch voltage behavior, resulting in an increased SOA. Interestingly, the average switch current, output power and efficiency contours are virtually unaffected aside from a counter-clockwise rotation. The rotation of the efficiency contours is of special interest, as it implies that an increase in the effective high-efficiency operating area can be achieved by appropriate tuning of the q parameter.

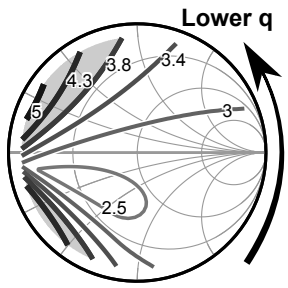
The extension of the SOA by reduction of the q parameter opens the door to a self-protecting class-E PA system, as was demonstrated in [6]. Increasing the q parameter leads to a reduction of the SOA, and is thus not of interest for this work. In addition, a reduction of the q parameter would require a reduction of the switch tank capacitance, requiring down-scaling of the switch transistor. This necessarily leads to a higher switch R_{ON} and thus degraded PA performance [7].

B. Effects of the d parameter on PA load-pull contours

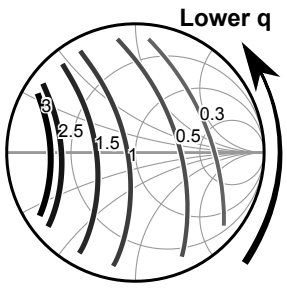
In addition to showing the effects of the q parameter, the work in [31] also showed that the d parameter can be used to influence PA behavior. This is illustrated using theoretical load-pull contours for a significantly increased d parameter.

Figure 8 shows the contours resulting from a change of the d parameter from 1 to 0.6. The resultant contours display a clockwise rotation with respect to the nominal load-pull contours. Notably, the (unshaded) SOA now covers the area in the lower left of the Smith chart that was not safe in the nominal case for $q = 1.4$ and $d = 1$.

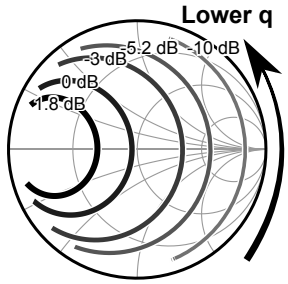
The change in PA behavior due to a change in the d parameter is shown to be complementary to a similar change in the q parameter. As decreasing q advances the SOA towards the upper left of the Smith chart, a complementary change (increase) in d thus similarly extends the SOA. The results show that the unsafe area in the upper left of the Smith chart is the main region limiting PA SOA, which is decreased by both a decrease in q and an increase in d. This suggests a combination of the two approaches would permit a larger increase in SOA than either alone. Fortunately, the reverse switch conduction discussed in section III effectively implements an increase in switch on-time, thereby virtually increasing the d parameter, which results in an extra counter-clockwise contour rotation for the associated load impedances. In this way, d tuning is automatically implemented for load conditions in the main



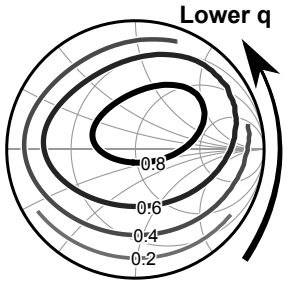
(a) Peak switch voltage normalized to V_{DD}



(b) Average switch current normalized to that under nominal conditions

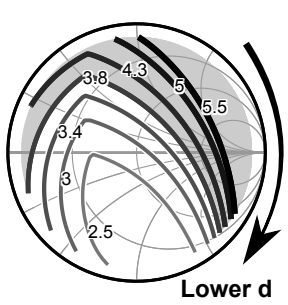


(c) Output power normalized to that under nominal conditions

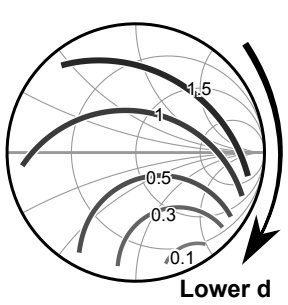


(d) Drain efficiency

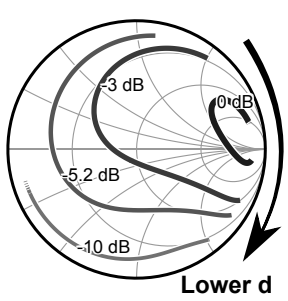
Fig. 7: Theoretical load-pull contours for $q = 1.15$ and $d = 1$. Contour rotation due to reduction of the relative resonance frequency is illustrated.



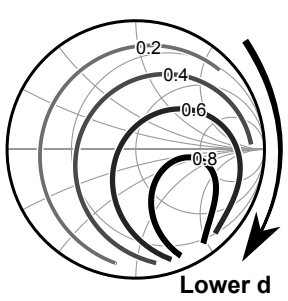
(a) Peak switch voltage normalized to V_{DD}



(b) Average switch current normalized to that under nominal conditions



(c) Output power normalized to that under nominal conditions



(d) Drain efficiency

Fig. 8: Theoretical load-pull contours for $q = 1.4$ and $d = 0.6$. Contour rotation due to reduction of the switch duty cycle is illustrated.

unsafe area on the Smith chart. This automatic d tuning is the reason the SOA in Figure 5 is larger than predicted by the theory in Figure 2. The effect of reverse switch conditions can be seen in the clamping behavior exhibited in e.g. Figure 6b.

VII. Measurements

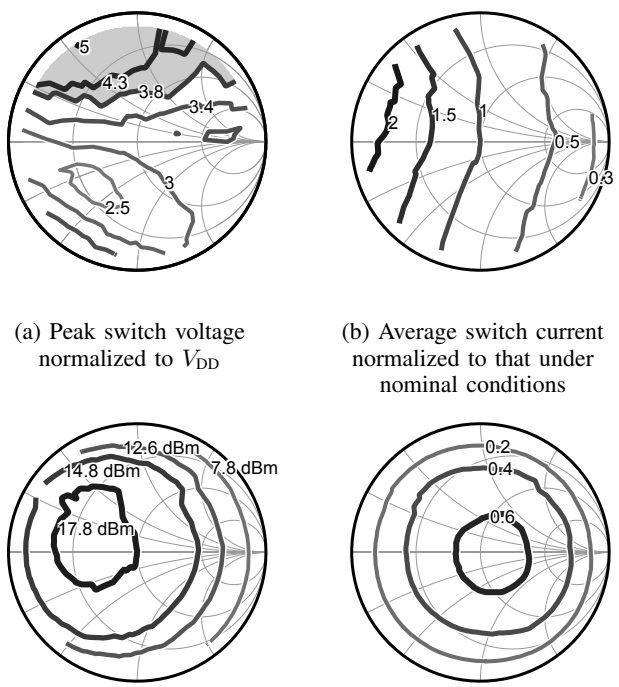
A class-E PA chip was developed in $65\,\mathrm{nm}$ for the work in [31]; some (component) values of this PA are shown in Table II. The design and implementation of the class-E PA are shown in Figure 3 and Figure 4, respectively. The square-wave drive signal is produced on-chip by a cascaded pair of inverters. The first inverter input is biased using a bias-T to allow tuning of the switch drive signal duty cycle. The default switch tank capacitor is formed by the parasitic switch transistor capacitances.

In Section VI, the effects of varying the class-E PA q and d parameters were described. It was shown that the PA SOA can be rotated on the Smith chart by tuning either the relative (switch tank) resonance frequency, the switch duty cycle, or both. Because tuning the switch tank inductance is impractical, an increase in the q parameter is achieved by variably increasing the switch tank capacitance. This variable capacitance is implemented by a Switched-Capacitor Bank (SCB) with 4 control bits, utilizing $2.5\,\mathrm{V}$ thick-oxide switch transistors. These switch transistors are dimensioned to limit their maximum voltage stress to below $3\,\mathrm{V}$. The residual capacitance the SCB presents to the switch node when it is in the off-state is compensated for by reducing the main switch size, lowering efficiency by less than 2% under nominal load conditions. The SCB switched capacitor bank utilizes four switches, switching $150\,\mathrm{fF}$, $300\,\mathrm{fF}$, $450\,\mathrm{fF}$ and $600\,\mathrm{fF}$, respectively, for a total capacitance $C_{\mathrm{SCB}} = 1500\,\mathrm{fF}$. This additional capacitance allows tuning of the q parameter from approximately $q = 1.4$ to $q = 1.15$ for a fully-disabled and fully-enabled SCB, respectively.

To verify the theory and simulations, a measurement setup was built using a Maury load tuner to detune the load and an $80\,\mathrm{GSa/s}$ oscilloscope with an Agilent active probe to capture the switch voltage waveform $V_{\mathrm{c}}(t)$, as depicted in Figure 3. Additionally, the output power and power supply voltage and current are recorded. The load is pulled over the entire VSWR 19:1 range available from the Maury load tuner, in 196 steps, scanning at $|\Gamma| = \{0, 0.1, 0.3, 0.5, 0.7, 0.9\}$. In order to prevent destruction of the class-E PA under test, the supply voltage V_{DD} is scaled down to keep the peak switch voltage below the switch breakdown limit. The data is scaled back to the nominal $V_{\mathrm{DD}} = 1.2\,V$, which does not compromise data accuracy. Phase shifts due to the matching network and interconnects were de-embedded.

Figure 9 shows the load-pull contours obtained for the PA with $q = 1.4$ and $d = 1$. A good match with the simulation results in Figure 5 can be observed.

In Figure 10, measured switch voltage waveforms normalized to V_{DD} are shown for the same load-mismatch conditions as used for the simulated results in Figure 6, showing good correspondence between measurement and simulation.



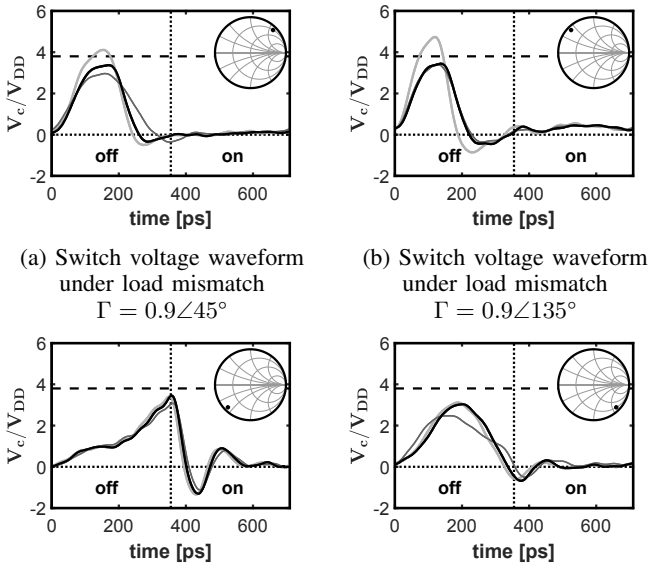
(a) Peak switch voltage normalized to V_{DD}

(b) Average switch current normalized to that under nominal conditions

(c) Output power

(d) Drain efficiency

Fig. 9: Measured load-pull data of the PA optimized for operation for the nominal load (center of the Smith chart); the frequency of operation is $1.4\,\mathrm{GHz}$.



(a) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle 45°$

(b) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle 135°$

(c) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle -135°$

(d) Switch voltage waveform under load mismatch $\Gamma = 0.9\angle -45°$

Fig. 10: Measured PA switch voltage waveforms for $q = 1.4$ (thick light grey) $q = 1.15$ (thin medium grey) and with the self-protecting loop enabled (thick black) for several load mismatch conditions. The switching moment is indicated by the vertical dotted line.

VIII. Self-healing system

Using the q-tuning technique previously discussed and demonstrated, a demonstrator self-healing PA system was constructed. For this, the setup used to gather the measurement data in Section VI is complemented by a control loop implementing the algorithm shown in Figure 12. The oscilloscope continuously monitors the switch voltage waveform $V_{\mathrm{c}}(t)$ and extracts its peak value, which is input to the self-protecting algorithm. In our demonstrator setup, this computationally light algorithm was executed on the measurement data processing PC.

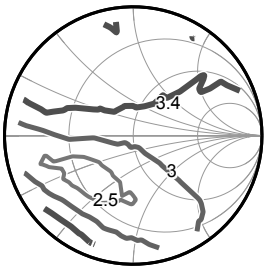
A dead-zone of $\Delta V_{\mathrm{c}} = 0.2\,\mathrm{V}$ was added to the algorithm to decrease noise sensitivity. At startup, the algorithm fully enables the SCB to ensure a safe starting condition for the PA. It then checks the peak switch voltage $V_{\mathrm{c,\,max}}$, lowering the SCB state while $V_{\mathrm{c,\,max}} < V_{\mathrm{c,\,nom}}$ and $C_{\mathrm{bank}} > 0\,\mathrm{fF}$, where $V_{\mathrm{c,\,nom}}$ is the peak switch voltage under nominal conditions. If the peak switch voltage increases above $V_{\mathrm{c,\,nom}} + \Delta V = 4.2\,\mathrm{V}$, the SCB state is incremented until the peak switch voltage drops below this level or the SCB is at the maximum state. If, in the latter case, the switch voltage is above the $4.6\,\mathrm{V}$ switch transistor breakdown limit, the algorithm reports that it cannot heal the PA. The algorithm runs continuously to ensure safe PA operation.

Figure 11 shows the measured load-pull contours for the self-healing class-E PA system, operating at $1.4\,\mathrm{GHz}$. Note that the unshaded SOA covers the entire VSWR 19:1 range, proving experimentally that our self-protecting class-E PA system is reliable under load mismatch conditions exceeding those presented by antenna loads. As predicted by both theory and simulation, efficiency and output power are not significantly effected by the self-healing system, with a worst case degradation in output power of $-1.6\,\mathrm{dB}$ and a worst case absolute efficiency decrease of 6%.

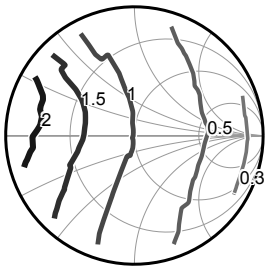
Because the self-protecting system requires only information about the peak switch voltage, only needs to track (low-frequency) load-impedance variations and involves the checking of simple conditions, the computational power and hence the power consumption of an on-chip implementation would be negligibly small relative to PA power consumption.

IX. Conclusion

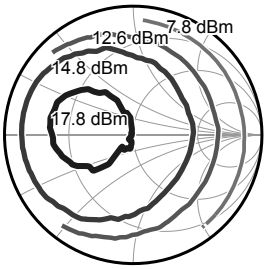
Class-E PAs may encounter severe and destructive reliability degradation under load mismatch conditions when not including significant design margins, especially for (over-)voltage. This work showed, both experimentally and theoretically, the effects of such load mismatch conditions on a number of relevant PA parameters. It was shown that high peak switch voltages present the main danger to reliability. The effects of the relative resonance frequency of the tank, q, and the switch duty cycle, d, on class-E PA behavior were demonstrated, showing that while either can be used to increase the Safe Operating Area (SOA), the q parameter has a stronger influence. A tuning technique for reducing the peak switch voltage under load mismatch conditions based on tuning the q parameter was implemented alongside a class-E PA on a $65\,\mathrm{nm}$ CMOS chip by means of a switched capacitor bank. It was shown that in addition to the implemented controllable q tuning, virtual switch duty cycle tuning occurs under load



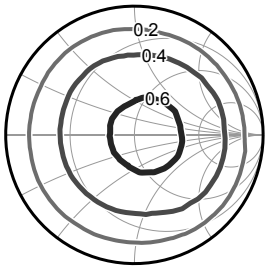
(a) Peak switch voltage normalized to V_{DD}



(b) Average switch current normalized to the nominal case



(c) Output power



(d) Drain efficiency

Fig. 11: Measured load-pull data of the self-healing system

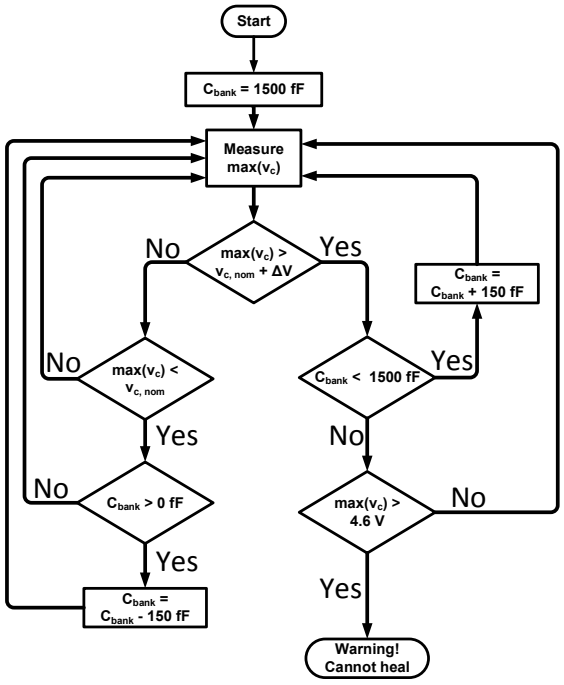


Fig. 12: Demonstrator algorithm flow chart. Modified from [6]. The algorithm starts by ensuring PA safety by fully enabling the SCB. It then measures the peak switch voltage, based on which it increments or decrements the SCB state to attempt to return the PA back to nominal operation conditions. If the SCB is at the maximum state and the switch breakdown voltage limit is exceeded, an error is reported to the user.

conditions with large negative switch voltages. Using the proposed tuning technique, a class-E PA was augmented with a self-protecting system utilizing a simple tuning algorithm to automatically tune the PA by varying the SCB capacitance to obtain reliable operation under previously disastrous load mismatch conditions. Our tuning technique extends the SOA of the class-E PA up to VSWRs of 19:1. This demonstrates that our self-protecting class-E PA system can operate reliably with a large safety margin under the typical VSWR 10:1 load-mismatch conditions presented by an antenna. The self-protecting system has a low impact on output power and efficiency, with these metrics seeing a worst-case degradation of $-1.6\,\mathrm{dB}$ and 6%, respectively.

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Jeroen Ponte received the B.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2018. He is currently pursuing the M.Sc. degree in electrical engineering at the University of Twente.

Ali Ghahremani (S'17) received the B.Sc. and M.Sc. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree at the Integrated Circuit Design Group, University of Twente, Enschede, The Netherlands.

His current research interests include high-speed and low-power CMOS analog circuits and power amplifiers for RF applications.

Dr. Ghahremani was ranked third in the 2009 Iranian Student Scientific Olympiad on Electrical Engineering, Honored by Ministry of Science.

Maikel Huiskamp received the B.Sc and M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2012 and 2015, respectively. He is currently pursuing the Ph.D. degree with the Integrated Circuit Design Group, University of Twente, The Netherlands.

His current research interests include sampling systems and efficient power amplifiers for RF applications.

Anne-Johan Annema (M'00) received the M.Sc. degree in electrical engineering and Ph.D. degree from the University of Twente, Enschede, The Netherlands, in 1990 and 1994, respectively.

In 1995, he joined the Semiconductor Device Architecture Department, Philips Research, Eindhoven, The Netherlands, where he was involved in a number of physics-electronics-related ranging from low-power low-voltage circuits, fundamental limits on analog circuits related to process technologies, and high voltage in baseline CMOS to feasibility research of future CMOS processes for analog circuits. Since 2000, he has been with the Integrated Circuit Design Group, Department of Electrical Engineering, University of Twente where he is associate professor and program director. He is also a part-time Consultant in industry and a co-founder of ChipDesignWorks, Twente. His current research interests include physics, analog, and mixed-signal electronics, RF power and deep submicrometer technologies and their joint feasibility aspects.

Bram Nauta (M'91-SM'03-F'08) was born in Hengelo, The Netherlands, in 1964. He received the M.Sc. degree (*cum laude*) in electrical engineering and the Ph.D. degree in analog CMOS filters for very high frequencies from the University of Twente, Enschede, The Netherlands, in 1987 and 1991, respectively.

In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven The Netherlands. In 1998, he joined the University of Twente, where he has been a Chair of the EE Department since 2016, and currently a Distinguished Professor and heading the IC Design Group. His current research interests include high-speed analog CMOS circuits, software defined radio, cognitive radio, and beamforming.

Dr. Nauta is a member of the Royal Netherlands Academy of Arts and Sciences. He was a co-recipient of the ISSCC 2002 and 2009 Van Vessem Outstanding Paper Award and the Simon Stevin Meester Award (500.000), in 2014, the largest Dutch National Prize for achievements in technical sciences. He is currently the President of the IEEE Solid-State Circuits Society for 2018 to 2019 term. He served as the Editor-in-Chief of the IEEE Journal of Solid-State Circuits (JSSC) from 2007 to 2010 and the 2013 Program Chair of the International Solid State Circuits Conference.

Also, he served as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 1997 to 1999, and the IEEE JSSC from 2001 to 2006. He was in the Technical Program Committee of the Symposium on VLSI Circuits from 2009 to 2013 and is in the Steering Committee and Programme Committee of the European Solid State Circuit Conference. He served as a Distinguished Lecturer of the IEEE.