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Incorporation of in-plane interconnects to reflow bonding for electrical functionality

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Abstract
Incorporation of in-plane electrical interconnects to reflow bonding is studied to provide electrical functionality to lab-on-a-chip or microfluidic devices. Reflow bonding is the packaging technology, in which glass tubes are joined to silicon substrates at elevated temperatures. The tubes are used to interface the silicon-based fluidic devices and are directly compatible with standard Swagelok® connectors. After the bonding, the electrically conductive lines will allow probing into the volume confined by the tube, where the fluidic device operates. Therefore methods for fabricating electrical interconnects that survive the bonding procedure at elevated temperature and do not alter the properties of the bond interface are investigated.

1. Introduction

Borosilicate glass (Duran®) tubes have been recently presented as fluidic interconnects to wafer-level microfluidic devices, where reflow bonding is the joining technology. This technology is referred to as 'MEMS-on-tube assembly' [1] or 'MEMS within a Swagelok' [2]. It was shown that the connections can be operated at high pressures and are inherently hermetic. However, integrated microfluidic devices incorporate a lot of functionality, which usually require electrical interconnects for sensing and actuation. Typical applications are valves, pumps and flow sensors [3], integrated devices for chemical and biological analysis, optical sensing elements, cooling of electronics [4] and manipulation of fluids through electrowetting or electrophoresis [5]. Therefore, in this paper, the incorporation of in-plane electrical interconnects to reflow bonding is investigated. The electrical lines start outside the tube and run through the bond interface allowing access to the volume encapsulated by the tube. The wires should be able to survive the bonding process and preserve the bond quality, i.e. they should stay conductive and should not produce any direct leak paths or cause reduction in the package strength.

2. Fabrication

Two types of in-plane electrical interconnects are fabricated for integration to reflow bonding of the glass tubes. The first design is to fabricate boron-doped lines in an n-type silicon substrate and the second one is to deposit metallic lines. The mask consists of two sets of nine different structures with varying parameters. An example is shown in figure 1 labelling the structural parameters. The length of the metallic lines, L, is 10 mm and always kept the same. The line widths, w, of 100, 200 and 500 μm are tested with separations, r, of 200, 500 and 1000 μm. The glass tubes are bonded to one set of the lines as described earlier [1], while the second set acts as a reference. After microfabrication, the sheet resistance is measured using the four-probe (i.e. four terminal) method as shown in the 3D view in figure 1.

2.1. Doped lines

Schematics of the fabrication of heavily boron-doped lines are displayed in figure 2(a). The selected substrate wafers are lightly n-type doped, ⟨1 0 0⟩ oriented, single-side polished (SSP) wafers of 380 micron thickness. The first step is to grow 2 μm thick silicon oxide by wet thermal oxidation in a

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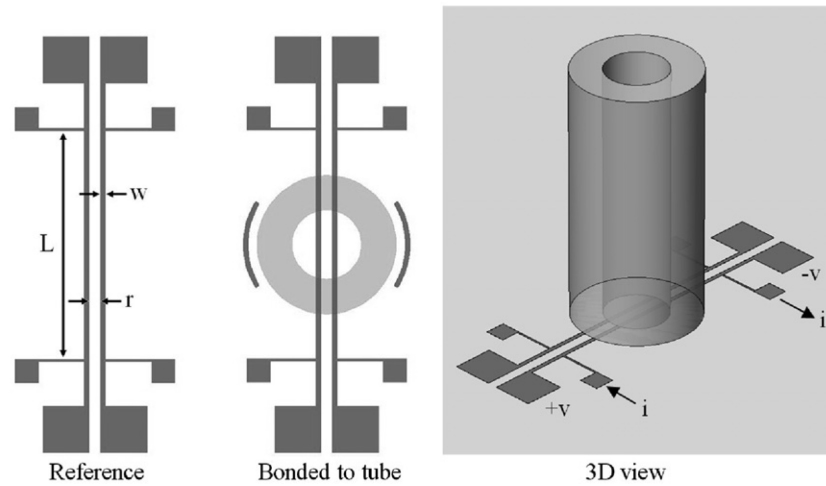


Figure 1. Top view and 3D view with the four-point contacts to measure the resistivity.

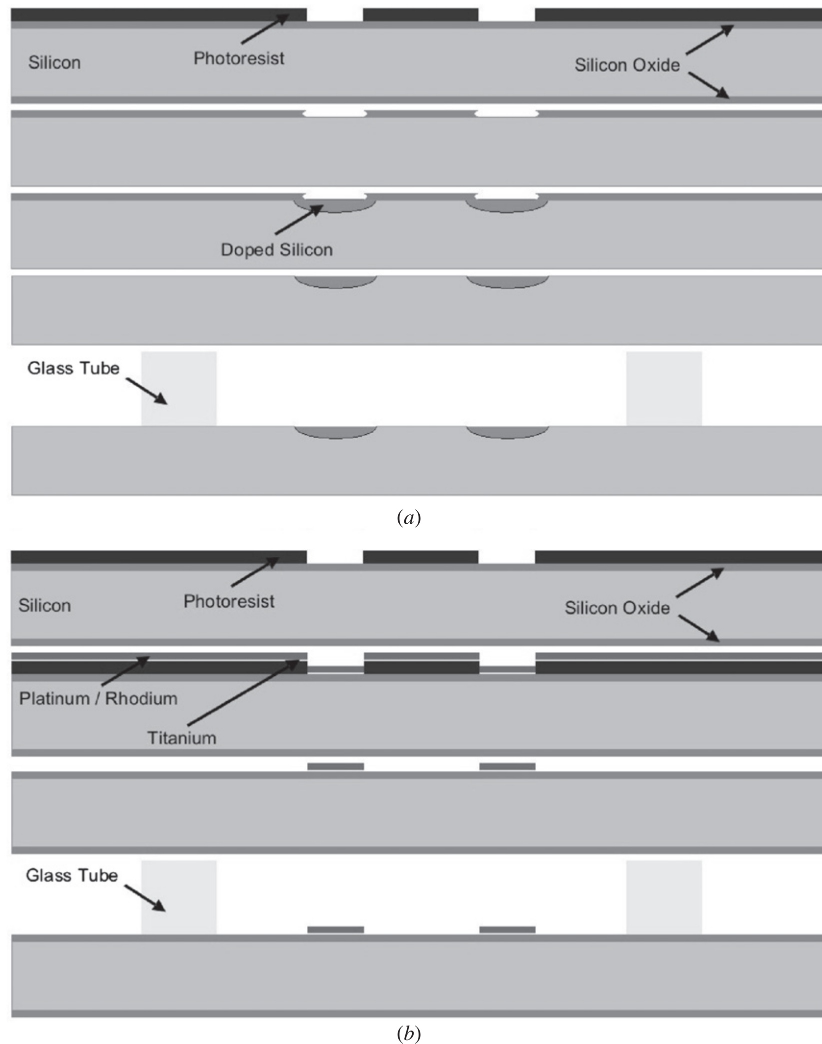


Figure 2. Schematics of the fabrication of (*a*) boron-doped and (*b*) metallic lines.

tube oven. Secondly, this oxide layer is patterned in buffered hydrofluoric acid (BHF) using a hard baked photosensitive resist mask. After removing the resist in 100% nitric acid (HNO_3), the p^+-doping can be performed in a tube oven.

Boron nitride wafers were used as solid sources and placed in the wafer boat to face the silicon wafers. During the high temperature diffusion, the boron evaporates in the form of boron trioxide from the solid source and is transferred directly

to the surface of the silicon wafer [6]. This process is constant-source diffusion as the dopant concentration is held constant at the surface during the diffusion process and is referred as solid source doping (SSD). After the doping, wells of p^+-type are created in the junction with the n-type substrate. SSD was performed at 1000, 1050 and 1100 °C for 60 min.

After the doping, there was a boron-containing residue on the doped regions. Therefore, the following post-doping cleaning was performed. The samples were initially dipped in 50% HF for 2 min. The wet thermal oxide mask was completely removed but the doped regions were not hydrophobic. Therefore the wafers were briefly oxidized at 800 °C for 30 min and etched for another 2 min in 50% HF. After this procedure, the whole silicon surface was clean and hydrophobic. The step heights between the protected and the boron-doped regions were measured by the Dektak profiler to be approximately 30, 50 and 100 nm for the wafers treated for 60 min at 1000, 1050 and 1100 °C, respectively.

2.2. Metallic lines

The schematics of the fabrication of metallic lines are displayed in figure 2(*b*). The selected substrate wafers are ⟨1 0 0⟩ oriented, single-side polished (SSP) wafers of 525 μm thickness. The first step is to grow 310 nm thick silicon oxide by dry thermal oxidation in a tube oven. This oxide layer will act as a diffusion barrier between the metals and the silicon substrate to prevent formation of silicide [7]. After the standard lithography of the oxidized wafers, the metallic lines are sputtered in argon plasma. Before starting sputtering, the deposition chamber is pumped below 2×10^{-6} mbar and the deposition pressure is set to 6.6×10^{-3} mbar regulating the argon flow. In all of the samples, 10 nm thick titanium is deposited on the SiO_2/Si stack as the adhesion layer (or the bond layer) as it is known to react directly with silicon oxide [7]. The second metallic layer is the functional layer and it is chosen to be either platinum or rhodium due to their high melting temperature and resistance to oxidation. The thickness of the platinum layer was about 310 nm and the thickness of the rhodium layer was about 270 nm. In the last step, the resist mask is lifted off to release the metallic interconnects. For effective removal of the resist layer, the wafers were put in acetone and isopropanol at 50 °C in an ultrasonic bath for half an hour each and left to dry in open air.

3. Results and discussion

After the fabrication, the electrical resistance of the structures was measured. Subsequently, the tube bonding was performed [1] and the resistance was measured again to test the performance of the integrated wires after the reflow bonding. Then, the hermeticity of every bonded tube was tested by a helium leak detector. The bond surface between the glass tube and the silicon was sprayed with helium gas to search for immediate leaks. The last step of characterization was to measure the burst pressures of the bonded tubes to check if the in-plane electrical interconnects caused any reduction in the strength of the package and change in the fracture behaviour of the silicon substrate.

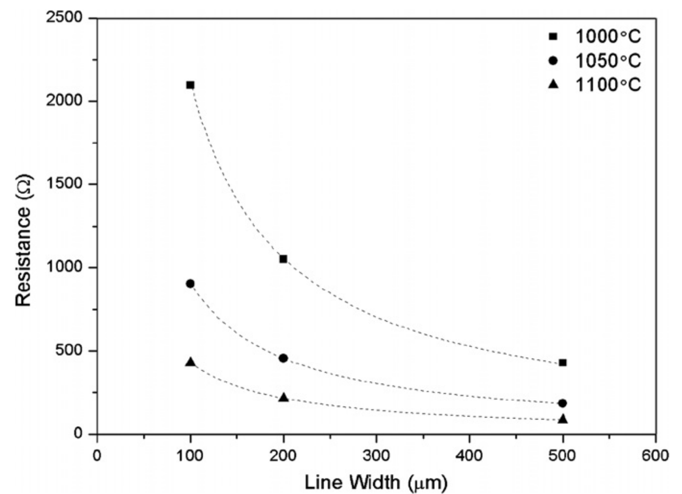


Figure 3. Electrical resistances of 10 mm long boron-doped lines with respect to the line widths at different temperatures.

Table 1. Sheet resistances and junction depths of boron-doped lines at different temperatures.

	60 min at 1000 °C	60 min at 1050 °C	60 min at 1100 °C
Sheet resistance (Ω/□)	21.1	9.1	4.3
Junction depth (μm)	0.9	1.7	2.8
Average resistivity ($\mu\Omega$ m)	19	15.5	12

The effects of the structural parameters and the design approaches will be discussed in light of these test results. If all the results are positive and the connections survive the bonding process without altering the bond quality, the integration can be called successful.

3.1. Electrical resistivity

The electrical resistances of the fabricated structures were measured with the four-point-probe method either by obtaining current–voltage curves between ±0.5 V or simply by multimeter measurements. The electrode configuration is shown in figure 1, where the connections on the side were used to apply current and the connections on the ends were used to measure the voltage drop. The electrical resistances of the doped lines were measured in the dark to minimize photocurrents. The junction depths of the diffused layers were measured by the groove-and-stain method [6]. The resistance of 10 mm long doped lines before the bonding with respect to the line width is plotted in figure 3 and the sheet resistances, the junction depths and the average resistivity values of these samples are presented in table 1. The deviation of the measurements was less than 5% of the value shown for each measurement. The accuracy was limited by the uniformity of the process, rather than the measurement equipment. The real resistance values can be calculated by multiplying the sheet resistance by the 2D aspect ratio of the structure, i.e. the ratio of the length of the structure to its width, and the average

resistivity is found by multiplying the sheet resistance with the junction depth.

The SSD process is constant-source diffusion because the surface dopant concentration remains the same during the high-temperature diffusion and is determined by the solid-solubility limit of boron in silicon [6]. For temperatures higher than 1000 °C, the solid-solubility limit of boron is higher than 10^{20} atoms cm^{-3} [8–10]. During diffusion of high dopant levels, the impurity concentration is higher than the intrinsic-carrier concentration of silicon and the diffusion coefficient of boron becomes dependent on its local concentration. Therefore, the dopant concentration profile deviates from complementary error function curves and extra measures have to be taken to calculate the junction depth. This effect has been studied in detail by Fair [11] and formulated as follows:

$$x_j = 2.45\left(\frac{N_0 D_i t}{n_i}\right)^{0.5} \tag{3.1}$$

$$N_0 = 9.25 \times 10^{22} \exp\left(-\frac{0.73}{kT}\right) \tag{3.2}$$

$$D_i = 3.17 \exp\left(-\frac{3.59}{kT}\right) \tag{3.3}$$

$$n_i = \left(1.5 \times 10^{33} T^3 \exp\left(-\frac{1.21}{kT}\right)\right)^{0.5} \tag{3.4}$$

where x_j is the junction depth [11] in cm, N_0 is the surface concentration and the solid-solubility limit of boron in silicon [8] in cm^{-3}, D_i is the intrinsic diffusion coefficient of boron in silicon [11] in $cm^2\ s^{-1}$, t is the high-temperature diffusion time in seconds, n_i is the intrinsic-carrier concentration of silicon [12] in cm^{-3}, k is the Boltzmann constant in eV K^{-1} and T is the diffusion temperature in K. If the values of equations (3.2)–(3.4) are substituted in equation (3.1) for temperatures of 1000, 1050 and 1100 °C and time of 60 min, the corresponding junction depths can be calculated as 0.84, 1.55 and 2.72 μm. These values are quite close to the experimental measurements displayed in table 1, especially considering that the diffusion coefficient of boron will be changing more than a factor of 10 during the diffusion process between 1000 and 1100 °C [13].

The electrical resistance of the doped lines was measured after the reflow bonding for 30 h at 700 °C. The bonding was performed in air environment and therefore the silicon wafers were oxidized about 20–30 nm [14]. Such an oxide layer was thick enough to insulate the test probes from the diffused layer and alter the resistance measurements. Therefore, the wafers were dipped in dilute HF solution after the tube bonding in order to remove the surface oxide layer before the actual resistance measurements. The measurement results after the tube bonding showed that the resistance values increased about 3% on average. However, the accuracy of the doping process was only 5%, and therefore, it can be stated that the increase in the electrical resistance of the doped lines after the bonding was within the error range, i.e. less than 5%.

The metallic lines were deposited on silicon dioxide to form $Pt/Ti/SiO_2/Si$ and $Rh/Ti/SiO_2/Si$ stacks. Titanium was used as the adhesion layer as it is known to react with silicon oxide to form continuous and smooth coverage [7]. The thickness of the titanium layer was about 10 nm. The thicknesses of the functional layers were about 310 and 270 nm for platinum and rhodium, respectively. The electrical resistance of 10 mm long metallic lines before the bonding with respect to the line width is plotted in figure 4. The sheet resistances of these samples are presented in table 2. The deviation of the measurements was less than 2% of the mentioned value. Again, the accuracy was limited by the uniformity of the process, rather than the measurement equipment. The sheet resistance of the rhodium stack was slightly less than the platinum stack, while both of them were about one tenth of the lowest sheet resistance of the boron-doped lines.

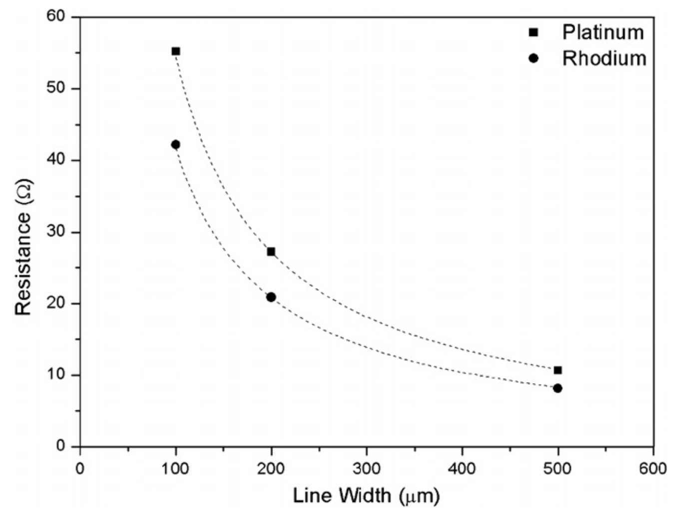


Figure 4. Electrical resistances of 10 mm long metallic lines with respect to the line widths.

Table 2. Sheet resistances of metallic lines as deposited.

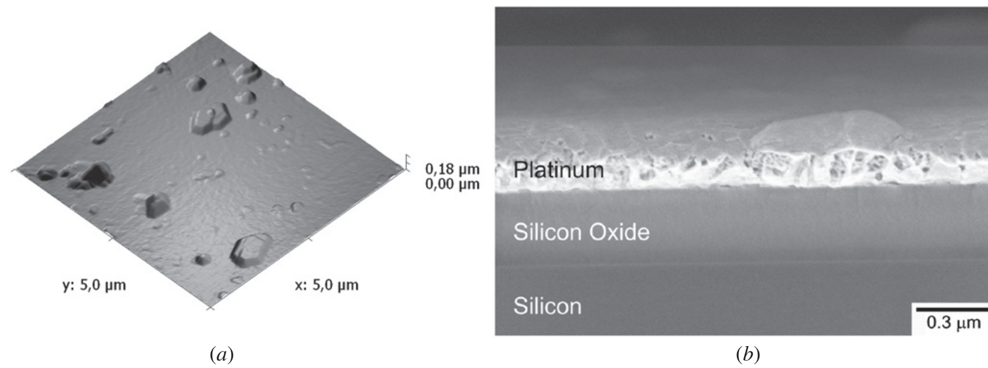
	Platinum	Rhodium
Sheet resistance (Ω/□)	0.54	0.42
Layer thickness (μm)	0.31	0.27

Table 3. Sheet resistances of metallic lines after the tube bonding.

	Platinum	Rhodium
Sheet resistance (Ω/□)	0.47	7000–8000 (without tubes) 1000–2000 (with tubes)

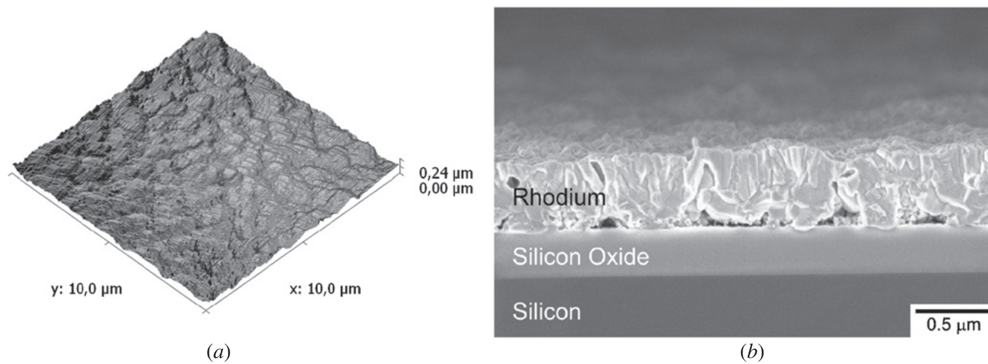
The electrical resistance of the metallic lines was measured again after the reflow bonding that was performed for 30 h at 700 °C. The bonding was performed in air environment and therefore oxygen was present in the environment during high-temperature annealing. The sheet resistivity of each stack is presented in table 3.

The platinum lines stayed conductive and their resistance has slightly decreased, presumably due to healing of defects and grain growth [15]. An atomic force micrograph (AFM) of the surface of the platinum layer after the bonding is displayed in figure 5(*a*). The grain growth and hillock formation in



(*a*) (*b*)

Figure 5. Platinum layer annealed for 30 h at 700 °C in air environment after tube bonding. (*a*) AFM surface image and (*b*) SEM cross-section.



(*a*) (*b*)

Figure 6. Rhodium layer annealed for 30 h at 700 °C in air environment after tube bonding. (*a*) AFM surface image and (*b*) SEM cross-section.

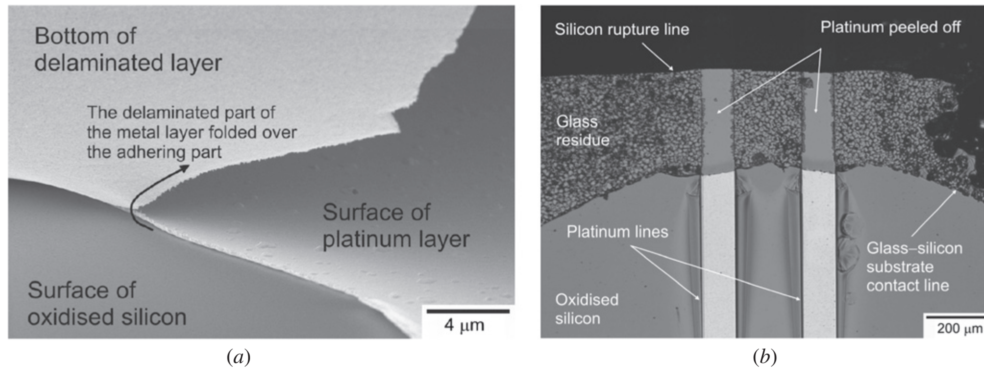
the platinum layer are clearly visible in the topography. The scanning electron micrograph (SEM) of the cross-sectional view of the stack in figure 5(*b*) indicates the porosity of the large grains.

When Olowolafe *et al* [16] and Kreider *et al* [17] investigated the post-deposition annealing (PDA) of the $Pt/Ti/SiO_2/Si$ stack at high temperature, they observed that the platinum layer on the surface remained unreacted even if oxygen was present in the annealing environment. In agreement with their results, energy dispersive x-ray (EDX) analysis in the SEM confirmed that the platinum layer was not oxidized. Relevantly, the base thickness of the platinum layer is observed to remain constant after the annealing at 700 °C in air environment.

The rhodium lines lost their conductivity and their resistance strongly increased. In the presence of oxygen, rhodium starts to oxidize above 600 °C [18]. Above 700 °C, the oxide layers grow on the surface in the form of Rh_2O_3 which is a stable product up to 1000 °C [18]. Although the lines on which the tubes were bonded showed a lower resistivity, their sheet resistance values were higher than 1000 Ω/□. An AFM of the surface of the rhodium layer after the bonding is displayed in figure 6(*a*) with a SEM of the cross-sectional view of the stack in figure 6(*b*). EDX confirmed that the rhodium layer was oxidized. The base layer thickness of the rhodium layer was measured to be 580 nm, which is higher than twice its initial thickness. The reason is ascribed to the incorporation of oxygen into the rhodium lattice during oxidation. Furthermore, due to this tendency to strain, compressive stresses will develop at the interface to cause local delamination of the layer.

3.2. Hermeticity

The hermeticity of every bonded tube was tested by a Leybold UL 500 helium leak detector. The open side of the tubes was connected to the detector through a flange and pumped down to the background pressure of 0.5 Pa. The bond between the glass tube and the silicon was sprayed with helium gas. If there was an apparent leak, helium molecules could migrate through direct paths and the detector would read a signal as long as it is above 10^{-9} Pa m^3 s^{-1}. The maximum signal was obtained by continuously spraying helium onto the leaky region and the leak rates were recorded. As a result of the described leak test, all of the tubes bonded to the boron-doped electrical interconnects were found to be hermetic. In other words, the helium leak detector did not read any signal and the doped lines did not cause any instant leak above 10^{-9} Pa m^3 s^{-1}. However, all of the tubes bonded to the metallic electrical interconnects were found to be leaking. The maximum level of flux was measured to be about 10^{-6} Pa m^3 s^{-1} for the $Pt/Ti/SiO_2/Si$ stack and 3×10^{-6} Pa m^3 s^{-1} for the $Rh/Ti/SiO_2/Si$ stack. No correlation between the structural parameters of the lines and the leak values could be found.



(*a*) (*b*)

Figure 7. (*a*) Oblique view of the platinum layer, which is peeled off the silicon substrate after annealing for 30 h at 700 °C in air environment. (*b*) Top view of the edge of a fractured silicon plate containing platinum lines after the tube bonding and burst pressure test, where the lines at the interface are stripped off the silicon piece during the fracture of the pressurized assembly.

Table 4. Burst pressures of ⟨1 0 0⟩ single-side polished silicon wafers of 380 μm thickness, containing boron-doped lines at different temperatures, after the tube bonding.

	1000 °C; 60 min	1050 °C; 60 min	1100 °C; 60 min
Burst pressures (MPa)	5.71 ± 0.16	5.71 ± 0.18	5.66 ± 0.1

Table 5. Burst pressures of ⟨1 0 0⟩ single-side polished silicon wafers of 525 μm thickness, containing different types of metallic lines, after the tube bonding.

	Platinum	Rhodium
Burst pressures (MPa)	7.53 ± 0.53	6.79 ± 0.74

3.3. Bond strength

The electrical interconnects running through the bond interface might reduce the maximum pressure to which the assembly can be subjected and cause change in the fracture behaviour of the silicon material. Therefore, the burst pressure of every bonded tube was tested to measure the effect of in-plane electrical interconnects on the strength of the package. As explained in another paper [1], the bonded glass tubes were connected to a water compressor setup and pressurized until the failure of the assembly to record the burst pressure values and establish the mechanism of failure.

The burst pressures of the silicon–glass assembly containing the boron-doped electrical interconnects were measured and the results are shown in table 4. All of the pressurized samples were found to fracture in the silicon plate. The values are similar to those obtained by testing non-processed 380 μm thick silicon wafers [1]. The step between the protected and the doped regions was completely filled by the softened glass and the fracture mechanism of the silicon substrates with boron-doped lines was the same as non-processed substrates. Therefore, the doped lines can be said to cause no reduction in the strength of the bonds or the mechanism failure of the assembly.

The burst pressures of the silicon–glass assembly containing the metallic electrical interconnects were measured and the results are shown in table 5. All of the pressurized samples were found to fracture in the silicon plate. The burst pressures of the samples containing platinum lines are similar to those obtained by testing non-processed 525 μm thick silicon wafers [1] and the burst pressures of the samples containing rhodium lines are more scattered and slightly lower than non-processed wafers.

During the post-deposition annealing of the Pt/Ti/SiO_2/Si stack, the thin titanium layer at the interface can oxidize [16]. The oxidation of the titanium bond layer can lead to coalescence of the platinum layer and loss of adhesion was observed with surface roughening in the platinum layer [17]. In agreement with the literature, the platinum layer peeled off from the underlying substrate. A SEM of a partly stripped platinum layer is shown in figure 7(*a*) from an oblique view. This is the edge of the sample, the cross section of which was presented in figure 5(*b*). Another example is displayed in figure 7(*b*), which is the surface of a ruptured silicon piece containing platinum lines. The crack initiated in the glass tube near its inner rim before propagating into the silicon and the neighbouring platinum layers at the interface stayed on the fracture surface of the glass tube. The loss of adhesion of the platinum layer after the annealing was the reason for the apparent leaks discussed in the previous section.

During the post-deposition annealing of the Rh/Ti/SiO_2/Si stack, the rhodium layer was oxidized [18] and thickened from 270 to 580 nm. Just as with the platinum lines, the rhodium lines lost their adhesion to the underlying oxidized silicon substrates. In addition, the rhodium lines at the glass tube–substrate wafer interface were cracked. The oxidation and the cracking behaviour of these lines are thought to have altered the electrical resistance measurements and the stiction problem after the annealing is the reason for the apparent leaks discussed in the previous section.

4. Conclusions

The incorporation of electrical interconnects to reflow bonding is required for probing the volume encapsulated by the tube and is therefore investigated. Two types of electrical lines were

tested for integrability with tube bonding. The first design was to fabricate boron-doped lines in an n-type substrate. The sheet resistances between 5 and 20 Ω/□ were obtained after doping. The conductivity of the lines did not change after the reflow bonding. The doped lines did not cause any leakage or reduction in the strength of the tube–silicon assembly.

The second design was to deposit metallic lines. Platinum or rhodium metallic lines were deposited on oxidized silicon using a titanium adhesion layer to form a $Pt/Ti/SiO_2/Si$ or a $Rh/Ti/SiO_2/Si$ stack. The sheet resistance of both types of metal were about 0.5 Ω/□ after deposition. After the reflow bonding, the resistivity of platinum lines slightly reduced while the rhodium lines lost their conductivity. Both types of metallic interconnects caused direct leak paths through the bond interface. Although the presence of these metallic lines did not considerably affect the strength of the glass tube–silicon joint, both types of metals lost adhesion to the underlying silicon substrate after the post-deposition annealing for the reflow bonding.

In the light of these results, it was concluded that the doping process is easily integrable to the reflow bonding, as they survive the bonding process and preserve the bond quality.

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References

[1] Moğulkoç B, Jansen H V, Berenschot J W, ter Brake H J M, Knowles K M and Elwenspoek M C 2009 Characterization of MEMS-on-tube assembly: reflow bonding of borosilicate glass (Duran®) tubes to silicon substrates *J. Micromech. Microeng.* **19** 085027

[2] Unnikrishnan S, Jansen H V, Berenschot J W, Moğulkoç B and Elwenspoek M C 2009 MEMS within a Swagelok: a new platform for microfluidic devices *Lab Chip* **9** 1966–9

[3] Gravesen P, Branebjerg J and Jensen O S 1993 Microfluidics—a review *J. Micromech. Microeng.* **3** 168–82

[4] Erickson D and Li D 2004 Integrated microfluidic devices *Anal. Chim. Acta* **507** 11–26

[5] Squires T M and Quake S R 2005 Microfluidics: fluid physics at the nanoliter scale *Rev. Mod. Phys.* **77** 977–1026

[6] Jaeger R C 1993 *Introduction to Microelectronic Fabrication: Modular Series on Solid State Devices* vol 5 ed G W Neudeck and R F Pierret (Reading, MA: Addison-Wesley) pp 49–83

[7] Liehr M, LeGoues F K, Rubloff G W and Ho P S 1985 Chemical reactions at Pt/oxide/Si and Ti/oxide/Si interfaces *J. Vac. Sci. Technol.* A **3** 983–6

[8] Armigliato A, Nobili D, Ostoja P, Servidori M and Solmi S 1977 Solubility and precipitation of boron in silicon and supersaturation resulting by thermal predeposition *Proc. 3rd Int. Symp. on Silicon Materials Science and Technology Semiconductor Silicon* ed H R Huff and E Sirtl pp 638–47

[9] Vick G L and Whittle K M 1969 Solid solubility and diffusion coefficients of boron in silicon *J. Electrochem. Soc.* **116** 1142–4

[10] Fair R B 1977 Recent advances in implantation and diffusion modelling for the design and process control of bipolar ICs *Proc. 3rd Int. Symp. on Silicon Materials Science and Technology Semiconductor Silicon* ed H R Huff and E Sirtl pp 968–87

[11] Fair R B 1975 Boron diffusion in silicon—concentration and orientation dependence, background effects, and profile estimation *J. Electrochem. Soc.* **122** 800–5

[12] Morin F J and Maita J P 1954 Electrical properties of silicon containing arsenic and boron *Phys. Rev.* **96** 28–35

[13] Matsumoto S, Ishikawa Y, Shirai Y, Sekine S and Niimi T 1980 Concentration dependence of the diffusion coefficient of boron in silicon *Japan. J. Appl. Phys.* **19** 217–8

[14] Deal B E and Grove A S 1965 General relationship for the thermal oxidation of silicon *J. Appl. Phys.* **36** 3770–8

[15] Lee D-S, Park D-Y, Woo H-J, Kim S-H, Ha J and Yoon E 2001 Preferred orientation controlled giant grain growth of platinum thin films on SiO_2/Si substrates *Japan. J. Appl. Phys.* **40** L1–3

[16] Olowolafe J O, Jones R E Jr, Campbell A C, Hegde R I, Mogab C J and Gregory R B 1993 Effects of anneal ambients and Pt thickness on Pt/Ti and Pt/Ti/TiN interfacial reactions *J. Appl. Phys.* **73** 1764–72

[17] Kreider K G and Gillen G 2000 High temperature materials for thin-film thermocouples on silicon wafers *Thin Solid Films* **376** 32–7

[18] Carol L A and Mann G S 1990 High-temperature oxidation of rhodium *Oxid. Met.* **34** 1–12