Clock Switching: a New Design for current Testability (DcT) Method for Dynamic Logic Circuits

Richard Rosing[1], Andrew M.D. Richardson[1], Yassine Eben Aimine[1], Hans G. Kerkhoff[2] & Antonio J. Acosta[3]

[1] Microelectronics Research Group, Lancaster University, Lancaster LA1 4YR, United Kingdom
[2] MESA Research Institute, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands
[3] Centro Nacional de Microelectronica, Edif. CICA, Avd de Reina Mercedes s/n, Sevillia, Spain.

Abstract

Using an I_{ddq} test methodology on circuits with dynamic logic tends to be problematic, mainly due to charge leakage related problems. A new Design for current Testability (DcT) method has been developed, which overcomes these problems by switching the circuit into a static mode during test. The method referred to as clock switching is applicable to both Domino logic and True Single-Phase Clock circuits. This paper shows that this technique can lead to higher levels of I_{ddq} testability and a reduced test vector set for the detection of bridging faults.

1. Introduction

Quiescent power supply current (I_{ddq}) testing of CMOS integrated circuits has been proven to be a technique that can significantly improve reliability [1,2,3,4]. I_{ddq} testing is very suitable for detecting Gate Oxide Shorts and bridges with a resistance higher than the critical resistance [5,6,7].

Dynamic logic circuits are used when high speed, minimal transistor functions are required. The clock frequencies are often in the order of hundreds of MHz for these circuits. Since Industrial I_{ddq} testers perform measurements at much lower frequencies (between 10kHz and 100kHz), charge leakage related problems can occur [8]. This charge leakage is caused by the subthreshold current of transistors, leakage current and charge redistribution.

In section 2 these problems will be reviewed. In section 3 the DcT technique, clock switching, is introduced and in section 4 the technique is demonstrated on a shift and rotate function implemented using a True Single-Phase Clock methodology.

In [9] and [10] it is shown that opens in dynamic CMOS circuits are easier to detect than opens in static CMOS. In this paper the detection of bridging faults is considered.

2. Problems with I_{ddq} testing of dynamic logic circuits

The Domino logic circuit [11] of figure 1, consisting of two cascaded two-input AND gates, will be used as an example to explain charge leakage mechanisms that can occur in dynamic logic circuits.

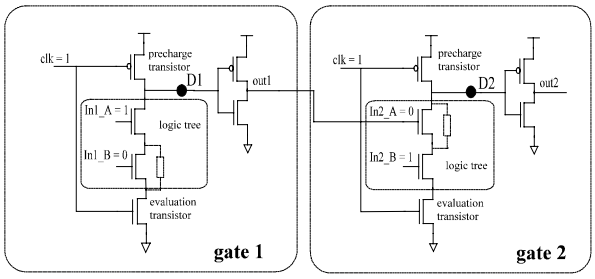


Figure 1. Domino logic example circuit

The nodes indicated by D1 and D2 are the dynamic nodes of the circuit. These nodes are precharged to a logic 1 when the clock signal is a logic 0. They are conditionally evaluated when the clock signal is a logic 1. If the dynamic nodes are electrically isolated during an evaluation period, as is the case for both dynamic nodes in figure 1, they must maintain their charge until the next

precharge period. If the amount of charge on these nodes becomes too low two problems can occur [8]:

- The output of a gate may switch incorrectly from a logic 0 to a logic 1 before any measurements are made. Controllability is now reduced, since a logic 1 can not be applied to a cascaded gate during testing.
- If the voltage on a dynamic node drops below the threshold voltage of the PMOS transistor in the cascaded inverter, an excessive current will be drawn from the positive to the negative voltage supply through the inverter, regardless of a fault being present. Functional circuits will thus be classified as faulty. The observability of faults is therefore reduced.

Another problem that can occur when performing I_{ddq} testing on dynamic logic circuits is that drain-source shorts in the logic tree can't be detected. Since the precharge and evaluation transistors are never open at the same time, a potential current path from the positive voltage supply through a drain-source short in the logic tree to the negative voltage supply is prevented. In figure 1 both gates contain a drain-source short. The test vectors are set up in a way that normally would enable detection of these shorts. However, they are undetectable since the precharge transistor is turned off.

Two possible solutions for the charge leakage related problems are:

- Compensation for charge leakage during test mode.
- Conversion of the circuit into a different configuration during testing, where charge leakage related problems do not occur.

In [8] the first of these solutions is applied to domino logic. The application of this method depends however on the configuration of the circuit and is therefore not general applicable to all dynamic logic circuits.

An attempt to solve charge leakage related problems using the second solution was proposed in [12] using a "Clock separation" method on Zipper-logic dynamic circuits. The observability of faults was increased by modifying the clock driver, so that the precharge transistor and the evaluation transistor are open at the same time during test mode. However, the controllability decreases if this method is used. Furthermore, this idea will be hard to apply to other kind of dynamic logic circuits, which use a different clock driver.

Since all dynamic circuits contain precharge blocks, the problems associated to the application of I_{ddq} measurements to domino logic will also occur with other dynamic logic circuits.

3. Clock switching applied to domino logic

3.1. Clock switching - the basics

Using the principle of clock separation, a new DcT method, "*clock switching*", has been developed. Both a high controllability and observability are achieved using this method. The technique involves converting the circuit into a static configuration during testing, avoiding charge leakage related problems. The principle is illustrated on the domino logic example in figure 2.

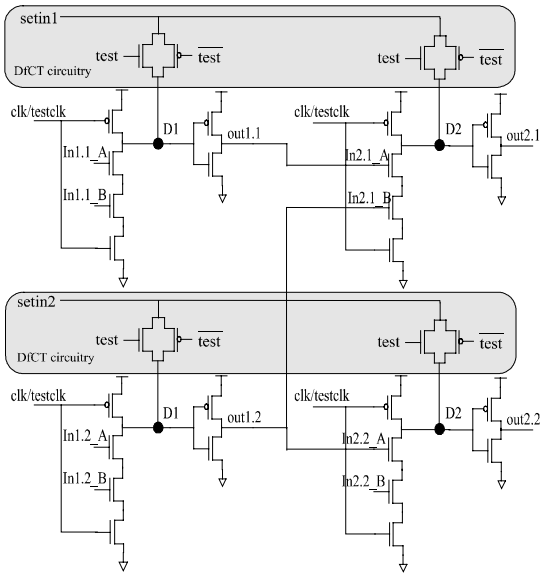


Figure 2. "*Clock switching*" applied to Domino logic

The additional DcT circuitry is indicated by the shaded areas in the circuit. It consists of one transmission gate per Domino logic gate.

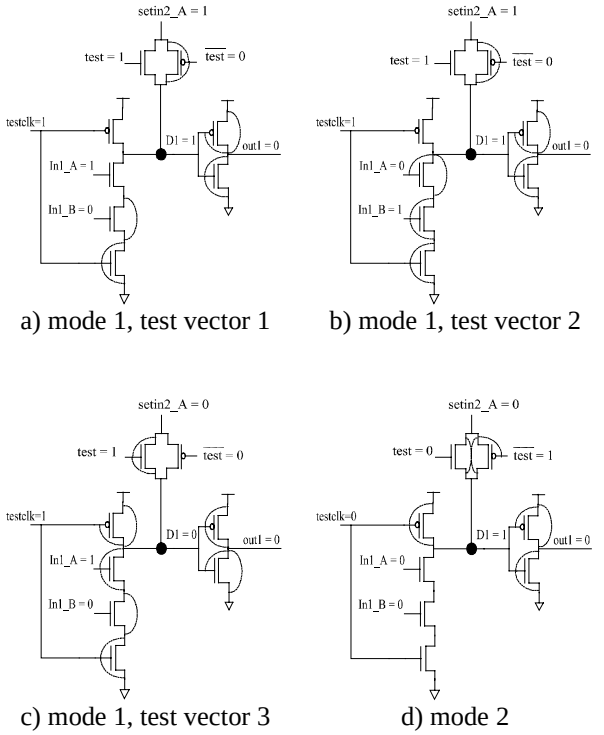
During normal operation of the circuit the clock signal is applied to the clock lines and the transmission gates are turned off. During test mode the transmission gates are turned on (test=1) and a test signal, testclk, is applied to the clock lines.

There are two modes of testing:

1. The testclk signal is a logic 1. One condition has to be met during this mode: a current path through the logic tree has to be avoided. This prevents an excessive current being drawn, in the fault free condition, when the setin-signal is a logic 1. The dynamic nodes are only connected to a setin-signal during this mode. These signals are used to set the output of a gate and thus the input of a cascaded gate to a desired value. Two different setin-signals are used to enable the application of different values to the two inputs of gate 2.1. This means that test vectors do not have to

propagate through previous circuitry. This is the reason that the same setin-signals can be used for gates in the same row. The detection of bridges during this test mode is schematically shown in figure 3.a, b and c. The detection of a bridging fault is indicated by a dotted line at the position of the fault. During this mode source-drain bridges of transistors inside the logic tree of a gate can be detected. This occurs when the setin signal is a logic 1 and if only one transistor in the logic tree is closed.

2. The testclk signal is a logic 0. All clocked PMOS transistors are now turned on. The detection of bridges during this mode is shown in figure 3.d. The test-signal is now switched to a logic 0 to enable detection of source-drain bridges in the transistors of the transmission gates. All setin-signals are now set to a logic 0. Except for the detection of these two bridging faults this mode is used to detect a number of other bridging faults that are not detected in the other mode.



a) mode 1, test vector 1 b) mode 1, test vector 2

c) mode 1, test vector 3 d) mode 2

Figure 3. Detection of faults in the Domino logic circuit

3.2. Evaluation of the effects of the DcT circuitry

The effects of adding the DcT circuitry to domino logic circuitry will only be roughly estimated. A better estimation, based on simulation, will be given for the effects of application of the clock switching technique to a True Single-Phase Clock circuit.

With regard to the area overhead, only two transistors are added per gate (forming the transmission gate). The area overhead in a typical domino logic circuit with a large number of typically wide transistors will be minimal if the DcT transistors are chosen minimum size. This is possible since these transistors operate at a low frequency due to I_{ddq} test rates. One extra pin is necessary to apply the test signal to the circuit. If the system clock is applied from a pin of the IC, this pin can be used for application of the test clock signal during test mode. An extra pin to apply this signal is then not necessary.

For the setin signals, the primary input signals can be used. The method of application of these signals depends on the configuration of the circuit.

The minimum size DcT transistors are turned off during normal operation of the circuit. Only a small extra capacitance, formed by the drain capacitance of these turned off transistors, will be added to the dynamic nodes of the circuit. The speed degradation is therefore expected to be minimal.

The test vector set can probably be reduced, since propagation of a test vector through previous gates is not necessary while using the clock switching method.

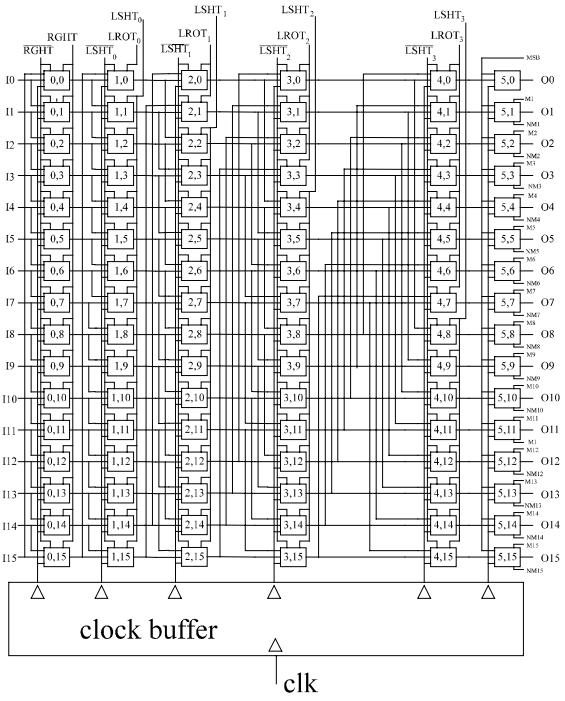
4. Clock switching applied to TSPC circuits

4.1. The basics

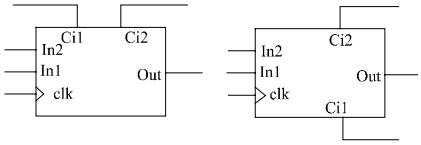
All dynamic logic gates consist of the same precharge logic units and differ only in the following stages (inverter, latch(es)) and in the clock signal used. Clock switching can thus be applied to all kinds of dynamic logic circuitry. Small adjustments must be made depending on the kind of circuit that has to be designed for test.

In this chapter the "*clock switching*" method will be applied to a True Single-Phase Clock (TSPC) circuit [13, 14] using the same approach as in the previous chapter. The shift and rotate array, which is part of the barrel shifter described in [15] is used as an example TSPC circuit. This shift and rotate array is shown in figure 4. A single cell of this array consists of a precharge logic unit followed by two latches and a split-P (an inverter, which input is "split" by a PMOS transistor). The array consists of 95 of these basic cells and 1 slightly adjusted cell. The signals I_0 to I_{15} form the input of the array. The signals on top of the array are control signals used to either shift or rotate data. On the right side of the array both the output signals, the signals O_0 until O_{15} and some signals used to mask invalid outputs are situated. Every cell contains four nodes that can be electrically isolated during one of the clock phases (named D1 to D4). The TSPC cell without

and with DcT circuitry is shown in figure 5.a and figure 5.b respectively. The DcT circuitry is indicated by the shaded areas in figure 5.b.



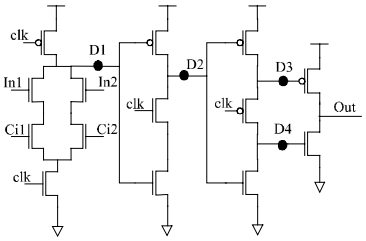
a) shift and rotate array



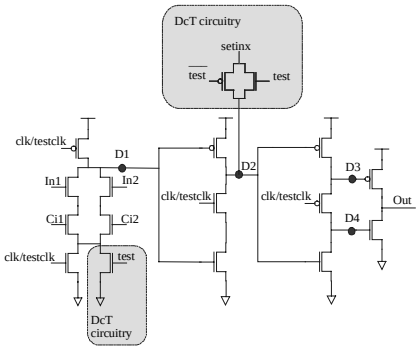
b) basic cells of the array

Figure 4. Shift and rotate array and cells

Similar to the application of the “clock switching” technique to Domino logic, a transmission gate, consisting of two minimum size transistors, is added to the circuit. If this transmission gate is applied to node D1, it is not possible to set the output to a desired value. The two latches with clocked transistors of different type (NMOS and PMOS respectively) prevent the signal from being propagated to the output. Therefore, the transmission gate is connected to node D2. This eliminates electrical isolation of nodes D2, D3 and D4.



a) TSPC cell without DcT circuitry

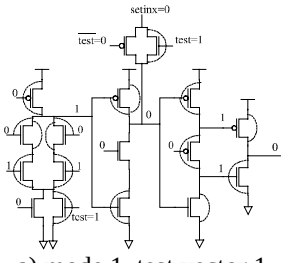


b) TSPC cell including DcT circuitry

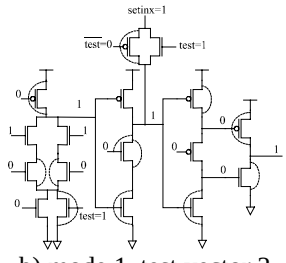
Figure 5. TSPC cell with and without DcT circuitry

The first test mode occurs when the testclk signal is a logic 0. Node D2 is electrically isolated from node D1 during this test mode, since the clocked NMOS transistor inside the latch is turned off. The output of each gate is now set by its setin signal. Propagation of the inserted value at node D2 to the output is possible, since the other latch is turned on. The extra transistor in parallel to the evaluation transistor is added to enable the dectection of bridges inside the logic tree during this test mode. Two test vectors are applied. The detection of bridges in this mode is schematically depicted in figure 6.a and figure 6.b.

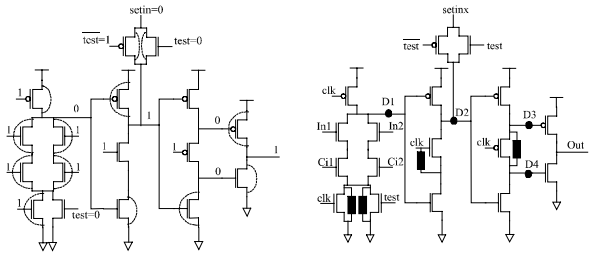
The second test mode occurs when the testclk signal is a logic 1. All inputs are now set to a logic 1. Some shorts that were undetected during the first test mode are now detected. This is shown schematically in figure 6.c. In figure 6.d the undetected bridges are shown.



a) mode 1, test vector 1



b) mode 1, test vector 2



c) mode 2 d) undetectable bridging faults

Figure 6. detection of bridges in the two test modes and undetectable bridges

4.2. Evaluation of the effects of the method

Area overhead

Three extra transistors are added per gate of 14 transistors. The exact area overhead depends on the size of the DcT transistors compared to the size of the other transistors in the circuit.

Three extra transistors in a gate of 14 transistors seems like a large area overhead. However, the DcT transistors can be of minimum size. The transistors present in the circuit are often much larger, since typical aspect ratios of transistors in dynamic logic circuits lay in the order of 20 [16].

Fault coverage

The fault coverage regarding source-drain, gate-source and gate-drain bridges in this cell is evaluated using CADEFSIM, a fault simulation tool build in CADENCE, developed at Lancaster University. The threshold current for detection of a fault was set at 1μA. Shorts with a relatively low resistance of 0.2Ω and shorts with a relatively high resistance of 100kΩ were inserted. In [17] the resistance for shorts between two metal layers was found to be between lower than 0.5Ω and 20kΩ. The range of inserted shorts was chosen even higher to assure all bridging defects are detected. For a single cell a fault coverage of 92% is found using three test vectors (using only I_{ddq} testing). All detected shorts resulted in a quiescent current higher than the threshold current for both values of the inserted resistance's. This means that detection occurs over the whole range of resistive values within these two values. Since all cells are tested in parallel, the complete shift and rotate array can be tested using only three test vectors. These simulations showed that the four faults that were already indicated in figure 6.d are undetectable. A bridging fault converage can now be calculated. Based on the original cell containing 14 transistors and therefore 52 possible intra-transistor bridges the fault coverage is found to be 92% using only I_{ddq} testing.

Speed degradation

The additional transistors will cause a speed degradation during normal mode of operation of the circuit. This speed degradation will be minimal, since all added transistors are turned off during normal mode. A small extra capacitance consisting of the drain capacitance's of the minimum size DcT transistors will be added to two points of the circuit. The largest speed degradation occurs on both the rise and the fall time of node D2. Both transition times are incremented by about 50 ps, which is small compared to the nominal times of 1.5 ns and 0.73 ns respectively.

Test vector set

Only three test vectors are used to test the entire circuit. This test vector set is small, since both propagation of a test vector from a primary input to a fault and propagation of a fault to the output do not have to occur. Propagation of a test vector from a primary input to a fault is avoided by the insertion of the vector at the preceding gates. Propagation of the vector to the output does not have to occur when I_{ddq} testing is used.

5. Conclusion

A DcT method, called clock switching, that can be applied to different kinds of dynamic circuits has been developed. Usage of this method avoids the charge leakage related problems that cause problems with the I_{ddq} technique.

Using this method, an I_{ddq} test can be performed using only a small number of test vectors. For a TSPC example circuit only three test vectors are needed for the entire circuit.

The speed degradation estimated through HSPICE simulations on the TSPC example circuit was found to be only 50 ps during both the evaluation period and the precharge period.

The fault coverage estimate depends on the CUT but is found to be high for the example circuits in this paper. A 92 % estimated fault coverage for shorts between the nodes of the transistors resulted when applying only I_{ddq} testing on the example TSPC circuit.

Some design effort has to be spent to apply the method to a dynamic logic circuit. However, with some small modifications the same steps can be used as were described for the application to Domino logic circuits and to the example TSPC circuit.

Finally it should be noted that as this is a theoretical study, firm estimates of silicon, power and performance overheads are not possible. In addition, as no layout was available, the fault coverage figures must be treated with respect as an accurate layout dependent fault list was not available. These issues represent future work that will also look at the optimal combination of tests on a real device where DcT has been applied.

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