IJTAG Compatible Delay-line based Voltage Embedded Instrument with One Clock-cycle Conversion Time

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***Abstract*—The monitoring of critical-paths in Systems-on-Chip to ensure dependable operation during the lifetime is becoming essential for safety-critical applications. Based on the timing information, different procedures like remaining lifetime prediction, voltage, and frequency scaling can be carried out to retain the desired functionality. To perform these operations, it is important to measure the run-time changing parameters like operating voltage and temperature, at the same moment of measuring slack-delay timing in critical paths. This will provide a better correlation, as compared to measuring the slack-delay timing alone, for instance, to determine the remaining lifetime. This paper presents a novel delay-line based voltage embedded instrument with a conversion time of just one clock cycle along with its integration to the IJTAG network. The proposed embedded instrument (EI) has been designed using the TSMC 40nm standard cell library. Simulation results of the proposed EI show a resolution of 10mV with a detection range from 0.95V to 1.20V, which is sufficient for most dependability applications.**

Keywords—Dependability, System Awareness, IJTAG, Embedded Instrument, Data fusion

I. INTRODUCTION

CMOS technology is rapidly advancing by reducing its minimum dimensions, and despite having many integration benefits in the same die, aging-related challenges like Negative Bias Temperature Instability (NBTI), hot carrier effect and electromigration (EM) are becoming major dependability concerns. This results in a shorter lifespan as compared to older technologies (90nm and above) [1-3]. These aging phenomena result in threshold voltage (V_{th}) degradation of a transistor that changes the propagation delays of logic gates, causing timing violations in the system.

For the safety-critical applications, like automotive, avionics and space industry, it is of crucial importance to determine the remaining lifetime of the system. However, knowing the changing characteristics of the propagation delay over time caused by the aging phenomena is not as straightforward as the data propagation in digital systems depends on several parameters. During the manufacturing of an integrated circuit, process variations can affect the delay characteristics of a fabricated circuit. These variations can be tackled at the design (simulation) phase of the circuit to ensure that it can perform the desired functionality by meeting the constraints at all the process corners. These variations usually occur from die-to-die and can be categorized as static variations. However, there are dynamic variations as well that affect digital systems during their operational phase, e.g. voltage-droop, temperature fluctuations, and aging. These parameters have different variation scales; e.g. temperature is a relatively slow changing parameter with a changing scale of 100µs to 1ms while voltage is a fast-changing parameter with a time-scale of around 2ns [4]. In the case of voltage-droop, some studies suggest a drop of 10% of the nominal voltage due to fast switching [5]. Aging on the other hand, is also a slow-changing physical phenomenon that depends on the operating voltages and temperature [6].

A lot of research has been carried out on developing embedded instruments that can be integrated on the same die with processor cores in Multi-Processor SoCs (MPSoC). These embedded instruments help to prolong the operational life by assisting in performing specific tasks like frequency scaling, voltage scaling and in a remaining-lifetime assessment. Among the embedded instruments, timing-slack embedded instruments are becoming an inevitable choice to monitor the propagation delay behaviour and to detect timing violations [7-9]. However, relying only on timing-slack EIs to conclude on delay degradation is not sufficient as discussed earlier; propagation delay depends on supply-voltage and die-temperature. To assist timing-delay measurements, temperature and voltage embedded instruments have been proposed [10-12] to assist in data fusion [13] and act more accurately on the EI's data. In this paper we extend the same research approach by proposing a delay-line based voltage embedded instrument that can measure the average voltage drop over one clock cycle, making it a perfect companion of the timing-slack EI to debug on timing data from critical paths.

Ring-oscillator (RO) based voltage monitoring techniques have been presented in the past [12]. These techniques determine the change in frequency as a function of the supply voltage. However, the application like remaining life-time prediction requires fast conversion time, and ring oscillators require some time to reach a stable oscillation state before one can calculate the frequency.

Our proposed design also measures the propagation delay with respect to the supply-voltage but rather than measuring the change in frequency; we opt to go for a direct timing measurement. With this approach, one obtains a conversion time of only one clock cycle that can help to provide a better correlation as compared to measuring the slack-delay timing alone, for instance, to determine the remaining lifetime. The circuit has been designed using the TSMC 40nm LP standard cell library; the key features of the design are:

1. The change in propagation delay as a function of voltage is determined in a conversion time of only one clock cycle.
2. Normally the relationship between propagation delay and voltage is non-linear. A technique to

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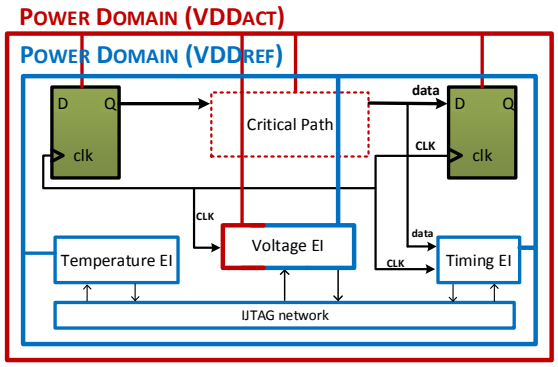

Figure 1: Overview of a health monitoring system

provide a linear response from the embedded instrument, in the presence of process and temperature variations has been used.

3. Incorporation of a controller to calibrate the design against process variations.
4. The embedded instrument is IJTAG-compatible.

The paper is organized as follows: in section II, a system level view is presented whereas, in section III, the design of the proposed voltage embedded instrument is shown. Section IV discusses the implementation details together with the simulation results while section V provides our conclusions.

II. Proposed Methodology

The top-level diagram of the proposed methodology is shown in Figure 1. The red line represents the power domain for functional cores, while the blue line indicates the power domain for embedded instruments. A timing EI, voltage EI, and temperature EI can be used to form a cluster of instruments. These three EIs can be configured together via the IJTAG network to start the operation and hence time-slack, voltage and temperature readings can be accessed at the same time. At the software level, these values can be fused to estimate aging and hence the remaining lifetime. The top-level design of the proposed voltage embedded instrument is shown in Figure 2. It consists of four blocks which are discussed in detail in section III of the paper.

The basic principle of the proposed voltage EI is shown in Figure 3. The CLK signal is used as a reference signal and it is delayed by τ_{ACT} using a delay-line which is powered by the functional supply line (VDD_{ACT}). Depending on the voltage variations on the VDD_{ACT}, τ_{ACT} can change for each clock cycle. This change in τ_{ACT} can be determined by the measuring the time between the positive edge of delayed clock signal DEL_CLK and the positive edge of the original clock signal CLK. This is highlighted as $\Delta\tau$ under signal Output in Figure 3. For further processing, the signal Output is converted to its digital equivalent by using a Time-to-Digital-Converter (TDC).

A. The Timing Embedded Instrument

An IJTAG compatible timing-slack monitor has been presented in [13]. It has three modes of operation, i.e. off-mode, infield calibration mode, and monitoring mode. In the calibration mode, the EI can calibrate for process and aging

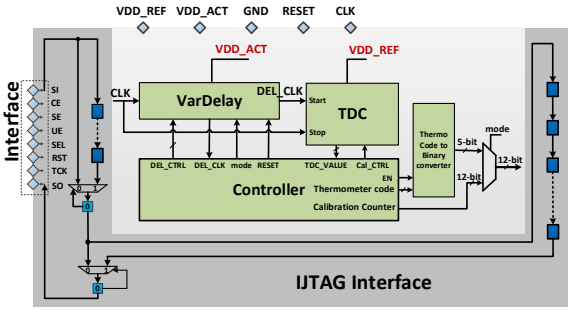

Figure 2: Top level design of the proposed wrapped voltage embedded instrument

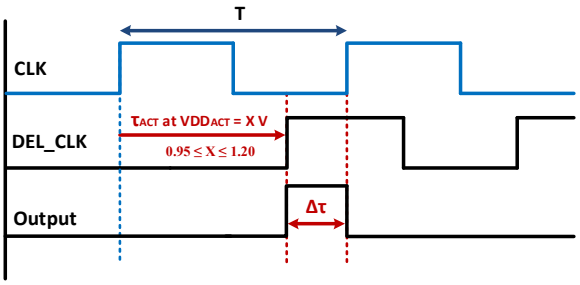

Figure 3: Overview of the basic operation of the proposed voltage embedded instrument

variations. While in monitoring mode, it samples the 'data' signal with respect to the CLK signal and sends a 5-bit binary code to the embedded processor via the IJTAG interface.

B. The Temperature Embedded Instrument

The choice of using temperature embedded instruments is inevitable when it comes to dependable VLSI systems. In order to measure the local temperature changes inside the processor cores, an IJTAG compatible temperature embedded instrument based on the bandgap principle has been presented in [10]. The sensing part of the temperature sensor occupies an area of $0.0012mm^2$ in 40nm CMOS technology. The proposed voltage monitoring method make use of this already available temperature EI to compensate for temperature variations.

C. The IJTAG Network

The IEEE 1687 standard (IJTAG) optimizes the access methods to embedded instruments [14]. IJTAG uses a test access port (TAP) to access scan flip-flops similar to JTAG. There are two main parts of the IJTAG standard; one defines the hardware architecture while the other defines the software part. In order to use IJTAG compliant instruments, two different languages are being introduced by the IJTAG standard referred to as the instrument connectivity language (ICL) and procedure description language (PDL). ICL is a hardware description language (HDL) for describing instrument interfaces, instrument test data registers (TDR) organization and the instrument network architecture. PDL is based on the tool command language (TCL) that defines the procedures required to operate an embedded instrument. The adoption of IJTAG is becoming popular due to the balance that it offers between hardware cost and the instrument's access time.

The IJTAG interface is serial which means that it takes several clock cycles during shift operation to configure or read an embedded instrument. However, applications like remaining lifetime assessment require mainly fast capturing of the physical data by the embedded instruments (EIs). Once the data is captured at the right moment by the EIs, despite the slow interface of IJTAG, it does not affect the overall outcome as these applications do not require data on every clock cycle and they are executed only once in a while. Functionally, the proposed voltage embedded instrument has two main parts;

(1) Circuit that measures the voltage droops in the power supply (VDD_{ACT}) due to switching because of the functional workload.

(2) Algorithm at the PDL level that fuses the data of voltage embedded instrument together with temperature EI to compensate the output of the voltage EI for environmental and process variations.

By following the proposed approach in terms of splitting the tasks at circuit and PDL level, one can save the die area by designing relatively simple circuits and can have more control over the calibration process with regard to environmental and process variations.

III. The Proposed Voltage Embedded Instrument

The scheme of our proposed IJTAG-compatible voltage monitor EI is shown in Figure 2. On top, the primary inputs to the voltage EI are shown. VDD_{REF} is the supply voltage for the EI, VDD_{ACT} is the voltage to be monitored, GND is the common ground, RESET is the monitor reset, and CLK is the clock signal drawn from the end of the critical path. On the left side, the IJTAG interface is shown while on the right side TDR registers are shown that capture the stable output from the embedded instrument.

The scheme in Figure 2 consists of four main parts, i.e. the Variable Delay-line (VarDelay), Time-to-Digital converter (TDC), Controller and a thermometric-code-to-binary converter. The design can detect voltage variations between 0.95V up to 1.20V. To measure the variation in the local supply voltage, VDD_{ACT} is connected to the functional power ring, of which the chosen critical path is being monitored. In this paper, it is assumed that since the VarDelay and TDC modules will be placed close to each other, the interprocess variations are negligible. This means that the Variable Delay line is fabricated for the typical case, TDC is also at the typical case and similarly for slow and fast processes. The details on each block are presented below.

A. Variable Delay-line (VarDelay)

The design for the Variable Delay-line (VarDelay) is shown in Figure 4; as the name suggests it is a configurable delay line. As discussed in the previous section, the first step is to delay the clock signal. For example, for the operational frequency of 200MHz, the required propagation delay is 5ns at 0.95V. However, due to the process variations, it can change so we opt for a variable delay-line that can be calibrated before starting to measure the voltage.

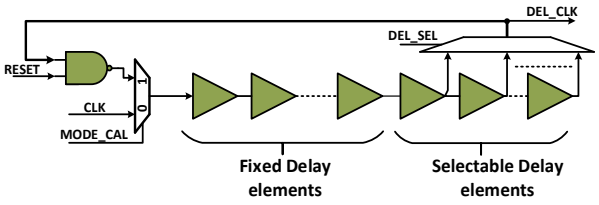

Figure 4: Design of the VarDelay block

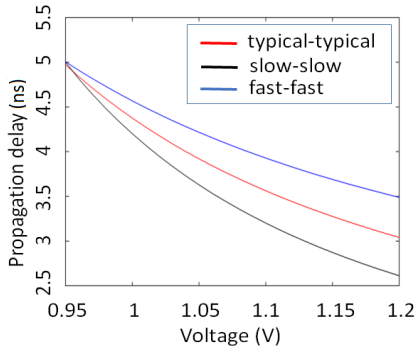

Figure 5: Propagation delay behavior of VarDelay block across different process corners after the calibration phase

The VarDelay block is powered by the functional power supply (VDD_{ACT}) that is intended to be monitored.

The VarDelay block can be configured into two different modes of operation, i.e. Calibration mode and Monitoring mode. During the calibration phase, the VarDelay module is converted into a ring oscillator, as shown in Figure 4. From its oscillation frequency, one can determine the propagation delay. By changing the DEL_SEL signal (which is a 5-bit signal, in the current implementation), the correct length of the delay-line can be chosen to match the time period T of the operational frequency. To build the Variable Delay-line, two types of delay elements are used, i.e. fixed and selectable. This helps in reducing the MUX size.

The propagation delay (τ_{ACT}) of the delay-line can be expressed using Equation (1), that uses a simple transistor model of an inverter in CMOS technology. Parameter N is the number of inverters, VDD_{ACT} is the voltage supply it is connected to, L_G is the gate length, W_G the gate width, C_L the load capacitor, C_{OX} is the gate oxide capacitance. The electron mobility is μ (considering $\mu = \mu_n = \mu_p$ for nMOS and pMOS) and V_{th} is the threshold voltage (considering V_{th}=V_{thn}=V_{thp} for nMOS and pMOS). Parameter α is the temperature-dependency of the threshold voltage, ΔT is the temperature variation and τ_{wire} denotes the wire delay.

$$\tau_{ACT} = \frac{2N \cdot 2L_G \cdot C_L \cdot VDD_{ACT}}{C_{OX} \cdot \mu \cdot W_G \cdot [VDD_{ACT} - V_{th}(1-\alpha \cdot \Delta T)]} + \tau_{wire} \quad (1)$$

From the equation, it can be noticed that the propagation delay depends on the process variables, operational voltage and temperature, and the dependence on these parameters is non-linear.

Once by selecting the "Selectable Delay elements" as shown in Figure 4, the propagation delay of VarDelay is adjusted to 5ns at VDD_{ACT} = 0.95V at temperature 25°C, to meet the target frequency of 200MHz. The VarDelay module is ready to be used in the monitoring mode, where it can be used to measure the operating voltage. Figure 5 shows the Spice simulation result (using TSMC 40nm

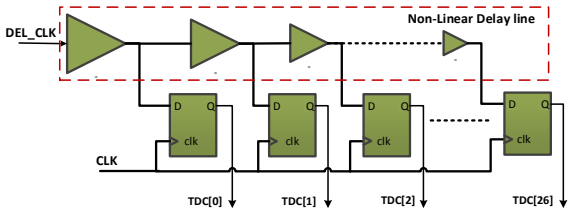

Figure 6: Design of a TDC with a non-linear delay-line

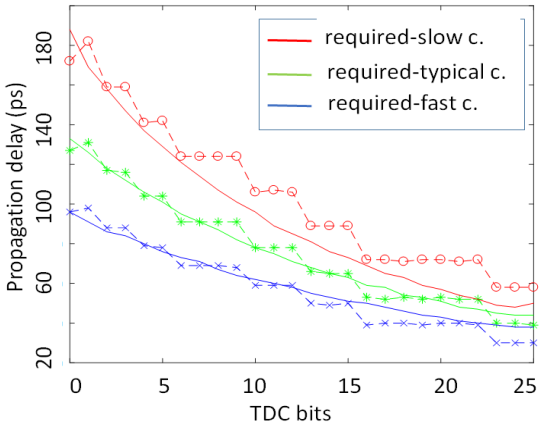

Figure 7: Resolution of TDC bits for required and actual

technology) which shows the behaviour of the propagation delay of VarDelay module for different operational voltages at different process corners after the calibration.

B. *The Time-to-Digital-Converter (TDC)*

The design of the TDC is presented in Figure 6. It consists of a nonlinear delay-line and flip-flops. This block is powered by a separate power line VDD_{REF} and fixed to a nominal voltage of 1.1V. This supply voltage is constant, and it is supposed that it will not experience the voltage drops like VDD_{ACT} due to the actual workload. It is worth mentioning here that since these two blocks (VarDelay and TDC) are supposed to be placed near to each other, inter-process variations can be neglected.

The basic operation of the TDC circuitry is to sample the delayed clock signal 'DEL_CLK' (output of VarDelay block) in time with respect to the positive clock edge and provides a 25-bit thermometric code that changes from all zeros (at $VDD_{ACT} = 0.95V$) to all ones (at $VDD_{ACT} = 1.20V$). To linearly measure the propagation delay changes in VarDelay as a function of VDD_{ACT}, the delay-line in the TDC block has been designed to match the propagation delay behaviour of the VarDelay block (at the typical case). Figure 6 shows the delay of each stage in TDC, where the buffer size represents its propagation delay.

To decide on the propagation delay of each buffer in the TDC circuitry, the behaviour of VarDelay at the typical corner and at 25°C is used as a baseline (also shown in Figure 5). The smallest sized buffers from the standard cell library were used to build the delay elements for each TDC stage.

Figure 7 shows the Spice simulation results based on the TSMC 40nm technology; the green solid line depicts the

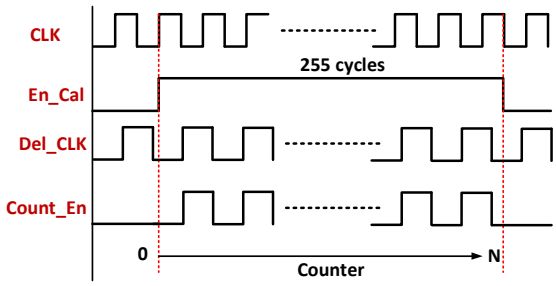

Figure 8: Calibration mechanism for VarDelay block

desired propagation delay for each TDC stage required to have a linear response for VarDelay. However, it is difficult to precisely follow the green line (typical case) by only using the digital cells which are at a fixed nominal voltage of 1.1V (unlike the power line of VarDelay where voltage can vary from 0.95V to 1.2V due to the functional switching). Red and blue solid lines in Figure 7 show the desired propagation delay of TDC stages for slow and fast corners respectively, while dotted lines show the resolution of the actually implemented TDC at different process corners. It can be seen that the resolution of implemented TDC deviates more from the desired resolution at the slow corner as compared to typical and fast corners.

C. *The Controller*

The voltage monitor can be configured into three different modes of operation i.e. monitoring-mode, off-mode and calibration-mode. In the monitoring mode, the controller module reads the flip-flop values from the TDC at every clock cycle; however, it waits for a signal from the timing monitor. If reading is required, it can lock the TDC data to another internal flip-flop stage to be sent over the IJTAG interface for higher-level analysis.

In the off-mode, the monitor is switched off by shutting down its power VDD_{REF}. This will reduce the aging-related degradation effects on the voltage EI itself.

In the calibration-mode (Figure 8), it calibrates the VarDelay block as discussed earlier for a maximum delay of one clock cycle at a VDD_{ACT} of 0.95V and a temperature of 25°C. The calibration process is required only once after the fabrication. To calibrate the VarDelay against process variations, it is converted into a ring counter. A 12-bit counter is used to determine the oscillation frequency within a reference interval EN_CAL, generated by the controller (Figure 8). It is important to note here that to have a propagation delay of 5ns, the oscillation frequency of the DEL_CLK signal should be half the clock signal. Therefore the current implementation requires the output of the. counter to be sent to the software level, where this value is compared to the reference value of 127 (which is approximately half of 255). Based on the value, a decision can be made either to increase or decrease the DEL_CTRL (Figure 2) value that will configure the VarDelay block for different delay lengths.

Once the calibration is complete, the value to configure VarDelay is stored with the instrument ID at the software level, and whenever the instrument is turned on, this value is sent to the controller via IJTAG interface where it can lock this value for monitoring mode until the instrument is turned off. This configuration value can also be used to estimate on the process corner information, e.g. to know if

the circuit implementation is on slow, typical or fast corners. This information can be used together with the temperature information to develop more precise fusion algorithm to compensate for environmental and aging variations. It is important to note that during this calibration procedure, the TDC circuitry is not calibrated, as calibrating VarDelay automatically defines the correct operation of the embedded instrument.

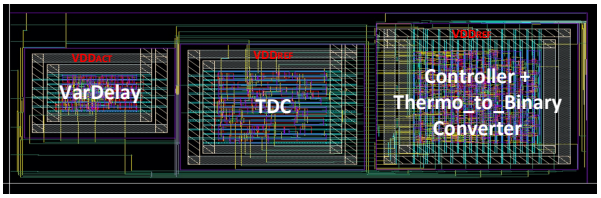

Figure 9: Layout of proposed voltage Embedded Instrument using the TSMC 40nm LP Standard Cell Library

Table 1: Area of each block of the voltage EI

Module	Area
Controller	37.7µm x 33.5µm
TDC	29µm x 26.2µm
VarDelay	13.65µm x 21.88µm

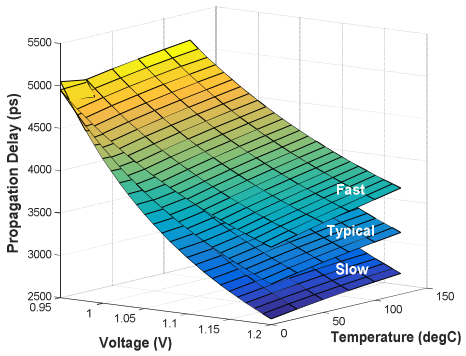

Figure 10: Propagation delay of the VarDelay block at the slow, typical and fast process corners

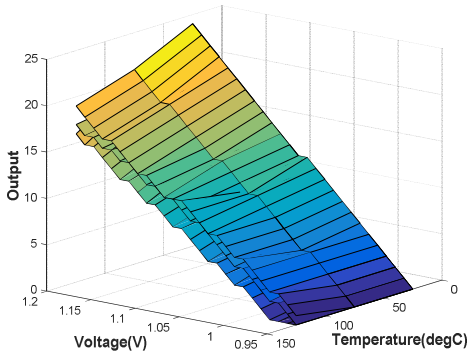

Figure 11: Response of voltage Embedded Instrument at the typical, slow and fast process corners

IV. Results and Discussions

The proposed design has been implemented using the TSMC 40nm LP standard cell library. The complete layout is presented in Figure 9 while the silicon area of each design block is given in Table 1. Figure 10 shows the simulation results for the change in propagation time of the VarDelay circuitry for different temperatures and for different process corners after its length is adjusted to 5ns (to meet the 200MHz target clock frequency).

Figure 11 shows the output of the proposed voltage embedded instrument without any compensation. On the horizontal axis, VDD_{ACT} is changed from 0.955V to 1.205V with a step of 10mV; also the temperature is changed from 25ºC to 125ºC with a step of 50ºC. This voltage sweep was chosen to determine the maximum output error. On the vertical axis, the output of the voltage monitor is shown. The output of the voltage monitor is a 5-bit binary code, which is shown in decimals for visual clarity. It is noticeable that for the typical case, the response is nearly linear with a 1-bit error (typical case, 25ºC). However at higher temperatures (above 75ºC), and a voltage (VDD_{ACT}) above 1.15V, the maximum deviation (at slow corner) from the standard response is about five bits. This translates into 50mV which is significant.

To compensate for this temperature offset, one can make use of temperature embedded instrument. A simple algorithm that makes use of the temperature information can be used to auto-correct the response. The response of a simple algorithm (at the PDL level) is shown in Figure 12. it can perform a simple fusion of temperature and voltage data to reduce the maximum error. Figure 13 shows a temperature compensated output of the voltage EI. It can be seen that the error is significantly reduced to a maximum error of three bits across all process corners. This error can be further reduced by incorporating the process corner information together with the temperature information. The response of a updated algorithm (at the PDL level) is shown in Figure 14, where process corner information (from the calibration phase, discussed in the previous section of the

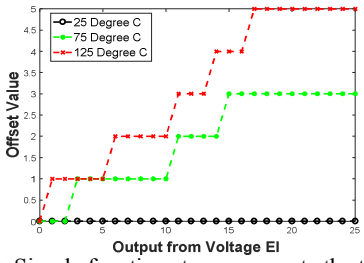

Figure 12: Simple functions to compensate the temperature changes in the voltage Embedded Instrument

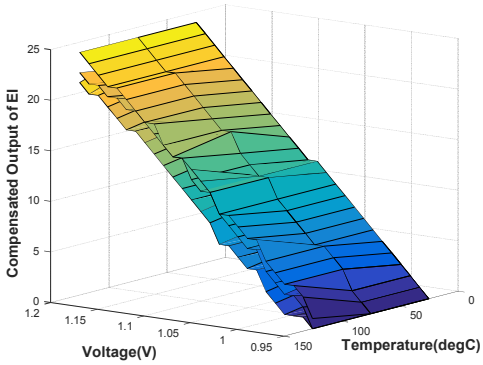

Figure 13: Temperature compensated output of the proposed voltage EI at the typical, slow and fast process corners

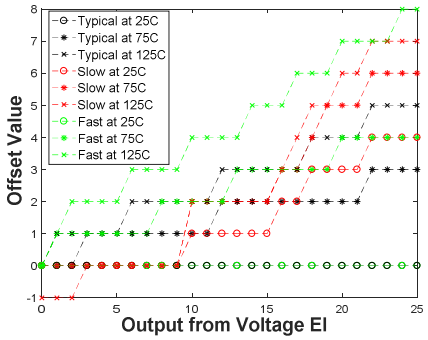

Figure 14: Offset functions to compensate the temperature changes together with process corners in the voltage Embedded Instrument

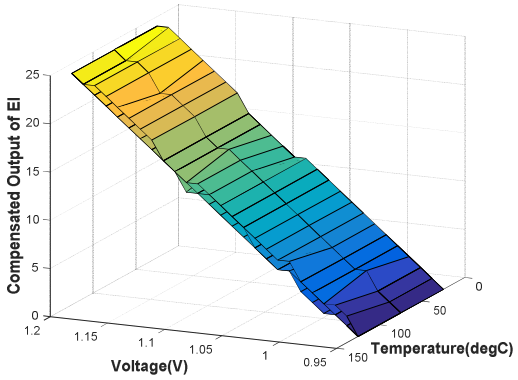

Figure 15: Improved compensated-output of the proposed voltage EI at the typical, slow and fast process corners

Table 2: Comparison table

Parameter	Ref [12]	Proposed Design
Test time	100µs	5ns @ 200MHz clock
Voltage range	0.91V – 1.09V	0.95V – 1.20V
Maximum error	7.71 mV	10mV
Technology	45nm	40nm
Interface	-	IJTAG

paper) is used together with the temperature information to further reduce the maximum error. Figure 15 shows the improved compensated output of the voltage EI. The maximum output error is further reduced to one bit (i.e. 10mV).

Table 2 shows the key differences of the proposed design with state-of-the-art. The key benefit is its area and one clock cycle conversion time. The proposed design is based on a standard-cell library that reduces the design effort for layout and system integration. The resolution of the proposed design is 10mV with a maximum error of 10mV when all the process corners are taken into account.

V. Conclusions

In this paper, a novel voltage embedded instrument has been presented along with its implementation using the TSMC 40nm LP standard cell library. The area of each block shows that the proposed design will not incur large area overhead. Simulation results show the potential of the proposed design to be used together with the slack-delay monitor to debug delay measurements. To compensate for variations because of temperature and process, a simple algorithm can improve the linearity of the proposed design.

Acknowledgements

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